101

一、**Single Choice.** (2 points per question)

1. The dual type of logic equation $A(B+C)=AB+AC$ is ( ).

A. $A+BC=(A+B)(A+C)$ B. $\overline{A}+\overline{BC}=(\overline{A}+\overline{B})(\overline{A}+\overline{C})$

C. $\overline{A}+\overline{BC}=(\overline{A}+\overline{B})(\overline{A}+\overline{C})$ D. $AB+AC=A(B+C)$

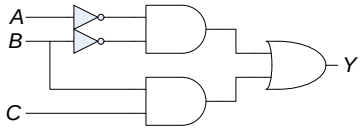
2. The number of Address Inputs (Selection Control Inputs) of an 8:1 Multiplexer is ( ).

A. 2 B. 3 C. 4 D. 8

3. The input of a 7-Segment Display Decoder is encoded by 8421BCD code, when the output of this decoder is abcdefg = 0011111, the input is ( ).

A. 0011 B. 0100 C. 0101 D. 0110

4. Which of the following condition can glitch occur for the circuit? ( )



A. The signal A changes from 0 to 1. B. The signal B changes from 0 to 1.

C. The signal C changes from 0 to 1. D. This circuit never occurs glitch.

5. A Finite State Machine (FSM) has 5 states. If you encode the states using binary encoding, the number of 1-bit D Flip-flops you need is ( ), and if you encode the states using one-hot encoding, the number of 1-bit D Flip-flops you need is ( ).

A. 2, 5 B. 5, 3 C. 3, 5 D. 5, 2

二、**Fill in the blanks.** (1 point per blank)

1. The decimal number of hexadecimal number $(1C4)_{16}$ is (_____)$_{10}$; the hexadecimal number of binary number $(0011101010110100)_2$ is (_____)$_{16}$; the binary number of decimal number $(342)_{10}$ is (_____)$_2$.

2. The TTL logic family has the following logic level characteristics: V_{DD}=5V, V_{IL}=0.8V, V_{IH}=2.0V, V_{OL}=0.4V, V_{OH}=2.4V. The Noise Margins of TTL logic family are NM_L = (_____)V and NM_H = (_____)V.

3. The outputs of sequential logic circuits are determined by (_____) and (_____) values of inputs.

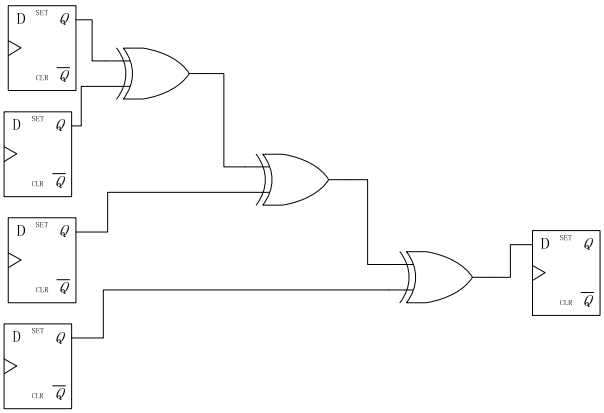
三、**Answer the Questions.** (6 points per question)

1. Convert the following decimal numbers to 8-bit two's complement binary numbers and add them. Indicate whether or not the sum overflows a 8-bit result.

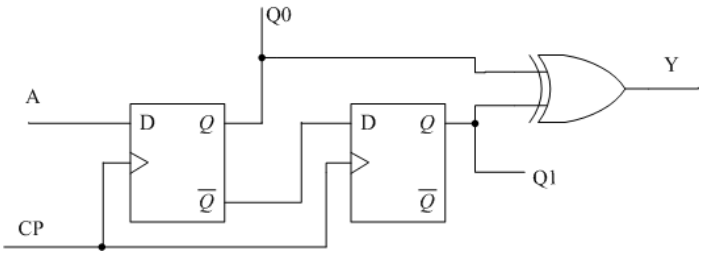
(a) $27_{10} + 31_{10}$

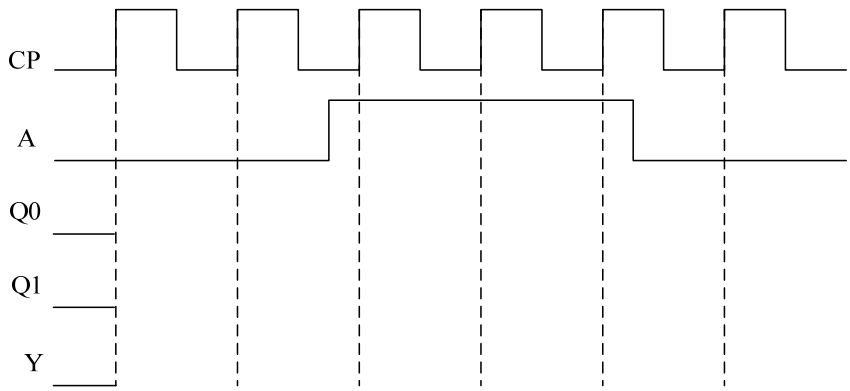
(b) $-76_{10} + -62_{10}$

2. In the following circuit, each XOR gate has a propagation delay of 100ps, each D flip-flop has a setup time of 60ps and a clock-to-Q propagation delay of 70ps. Please calculate the maximum clock frequency of this circuit.



3. The circuit schematic and waveforms of clock signal (*CP*) and input signal (*A*) are shown in the following figures. The D Flip-flops of this circuit are positive-edge triggered, and initial states are 0. Please sketch the waveforms of *Q0*, *Q1*, and output *Y*.





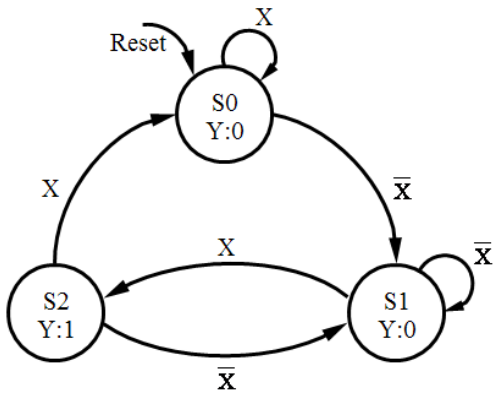
四、Combinational Logic Design (10 points)

A device which receives 3-bit binary number has three inputs: *A*, *B*, and *C*. The output *F* of this device is True when its binary number input can be divided by decimal number 3 or 6; otherwise, its output is False.

1. Write the Truth Table and the Boolean Equation with Sum-of-Products (SOP) form of the device. (4 Points)
2. Only use NAND gates and NOT gates to sketch the circuit schematic of the device. (6 Points)

五、Sequential Logic Design (20 points)

A Moore Finite State Machine (Moore FSM) has an input signal *X*, an output signal *Y*, and three states *S*0, *S*1, *S*2. The state transition diagram of this FSM is shown as following figure.



1. Write state transition table and output table using binary state encoding. (3 points)
2. Write Boolean equations for the next state and output logic. (4 points)
3. Sketch the circuit schematic of this FSM. (3 points)
4. Write Verilog HDL program to describe the FSM. (10 points)