Laboratory Report

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Laboratory Exercise Title:	FET Biasing		
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Part I

Field-effect transistors (FETs) are semiconductor devices that include a channel constructed of a semiconductor material and two electrodes connected at either end, known as the drain and source. They also include a third electrode, the gate, which is located near to the channel and controls the flow of current between the source and drain terminals. When a voltage is applied to the gate electrode, it creates an electric field across the insulating layer, resulting in a depletion region within the channel. This depletion zone reduces the quantity of free charge carriers, lowering the channel's conductivity. This phenomenon, called the field effect, is critical to FET operation. Figure 1.1 shows a typical transistor.

Biasing establishes a stable operating point, allowing for consistent amplification and switching behavior. Various biasing methods are employed depending on the application and desired characteristics of the circuit. FET Biasing configurations include fixed-bias, self-bias, voltage-divider, common-gate, and a special case where V_{GS} = 0 V.

Figure 1.1: 2N5458 Transistor

Fixed-bias configuration is a simple method in which a resistor connects the gate to a fixed voltage source. While simple to set up, this arrangement is unstable in the face of temperature fluctuations and device parameter changes.

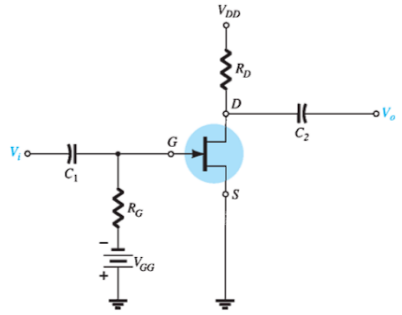


Figure 1.2: Fixed-Bias Configuration

Self-bias configuration includes a resistor in the source lead, creating a feedback mechanism that improves stability. The gate remains grounded via a high-value resistor, resulting in superior performance than fixed-bias approaches.

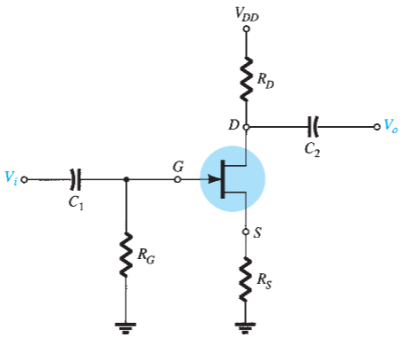


Figure 1.3: Self-Bias Configuration

Voltage-divider biasing utilizes a voltage divider network to establish the gate voltage. This configuration offers improved stability and reliability, making it suitable for a wide range of applications.

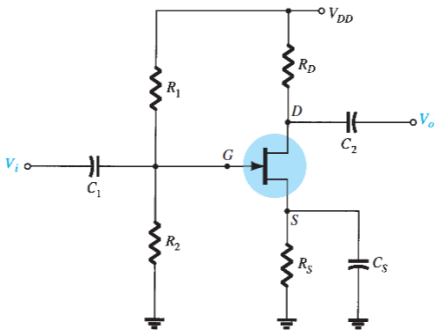


Figure 1.4: Voltage-Divider Bias Configuration

Common-gate configuration involves grounding or connecting the gate to a bias voltage while applying the input to the source. This setup is commonly used in high-frequency applications due to its low input impedance.

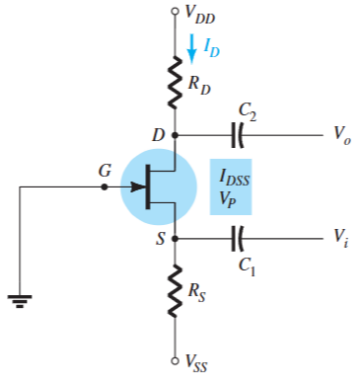


Figure 1.5: Common-Gate Bias Configuration

The zero-bias configuration is generally employed with depletion-mode MOSFETs. In this particular situation, the gate is directly connected to the source, resulting in a gate-to-source voltage of 0. The drain current remains at its maximum, resulting in a straightforward but limited approach. Each biasing setup has unique advantages and disadvantages in terms of stability, complexity, and applicability to specific applications.

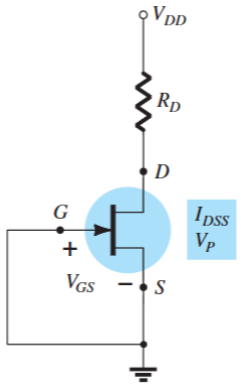


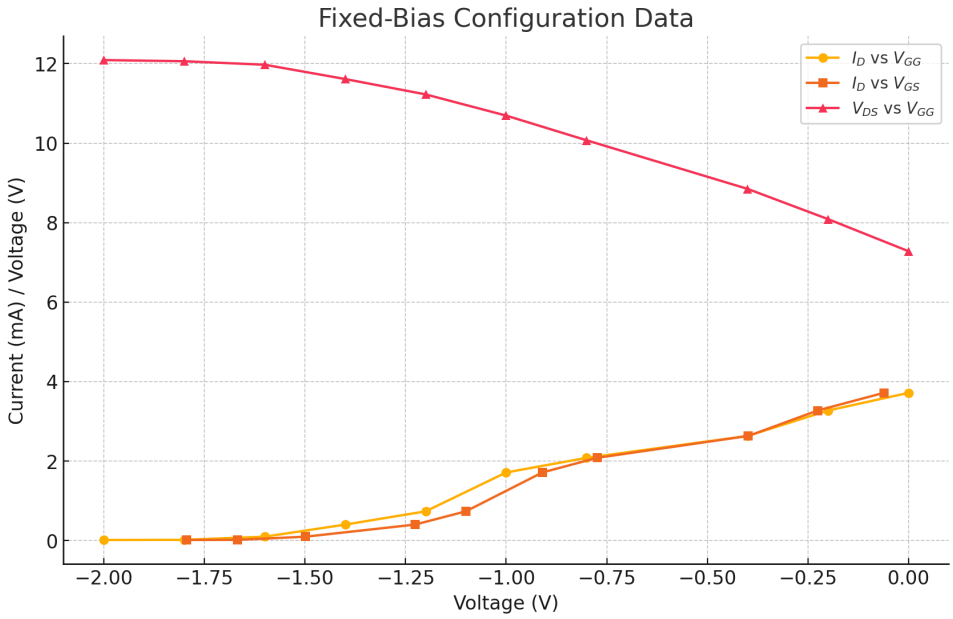
Figure 1.6: V_{GS} = 0 V Configuration

Part IIa: Fixed-Bias Configuration

Table 1 - Data for Fixed-Bias Configuration

V_{GG}	V_{GS} (V)	I_D (mA)	V_{DS} (V)
0 V	-0.0614	3.717	7.28
-0.2 V	-0.2262	3.2719	8.088
-0.4 V	-0.3982	2.632	8.849
-0.8 V	-0.774	2.081	10.072
-1.0 V	-0.910	1.713	10.694
-1.2 V	-1.1002	0.735	11.227
-1.4 V	-1.2267	0.401	11.614
-1.6 V	-1.4984	0.097	11.974
-1.8 V	-1.6677	0.017	12.062
-2.0 V	- 1.7940	0.014	12.091

Graph:

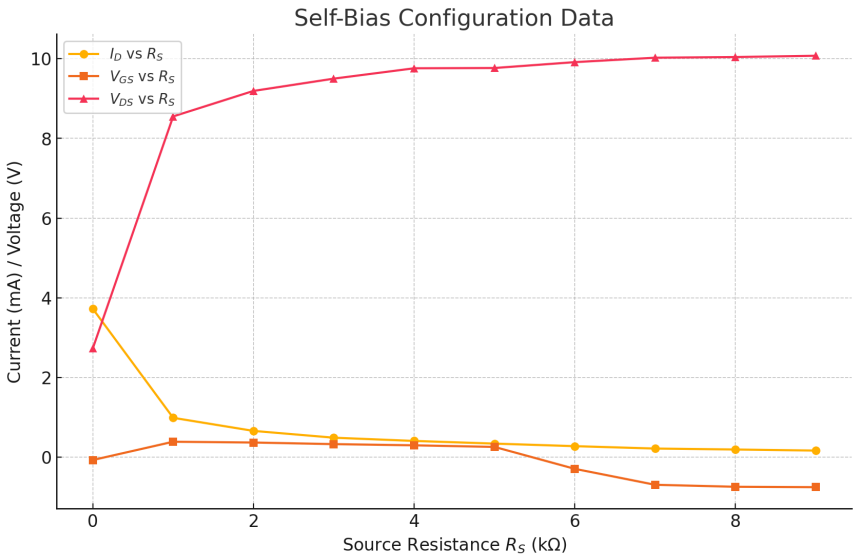


Part IIb: Self-Bias Configuration

Table 2 - Data for Self-Bias Configuration

R_S	V_{GS} (V)	I_D (mA)	V_{DS} (V)
0	-0.069	3.724	2.733
1k Ω	0.39	0.99	8.551
2k Ω	0.37	0.662	9.191
3k Ω	0.33	0.491	9.499
4k Ω	0.30	0.410	9.759
5k Ω	0.26	0.343	9.766
6k Ω	-0.29	0.279	9.913
7k Ω	-0.69	0.219	10.024
8k Ω	-0.74	0.195	10.041
9k Ω	-0.75	0.168	10.073

Graph:



Part IIc: Voltage-Divider Configuration

Table 3 - Data for Voltage-Divider Configuration

R_S	V_{GS} (V)	I_D (mA)	V_{DS} (V)
0	-0.4	11.3	0.71
1k Ω	-0.36	4.18	3.69
2k Ω	-0.53	2.17	5.51
3k Ω	-0.62	1.44	6.14
4k Ω	-0.69	1.13	6.4
5k Ω	-0.71	0.88	6.64
6k Ω	-0.76	0.72	6.72
7k Ω	-0.76	0.65	6.85
8k Ω	-0.77	0.58	6.88
9k Ω	-0.78	0.52	6.94

Part IId: Common-Gate Configuration

Table 4 - Data for Common-Gate Configuration

R_S	V_{GS} (V)	I_D (mA)	V_{DS} (V)
0	-	-	-
1k Ω	0.39	0.94	4.68
2k Ω	0.37	0.94	4.711
3k Ω	0.33	0.941	4.72
4k Ω	0.30	0.94	4.74
5k Ω	0.26	0.92	4.77
6k Ω	-0.29	0.9	5.4
7k Ω	-0.69	0.82	6.31

8k **Ω**	-0.74	0.72	7.61
9k **Ω**	-0.75	0.64	8.61

Part IIe: Special Case (V_{GS} = 0 V) Configuration

Table 5 - Data for Special Case (V_{GS} = 0 V) Configuration

R_S	I_D **(mA)**	V_{DS} **(V)**
0	6.49	0.54
1k **Ω**	0.76	9.98
2k **Ω**	0.37	10.4
3k **Ω**	0.28	10.6
4k **Ω**	0.21	10.7
5k **Ω**	0.17	10.8
6k **Ω**	0.14	10.8
7k **Ω**	0.13	10.9
8k **Ω**	0.11	10.9
9k **Ω**	0.1	10.91

Part III. Observations

1. **Observe the data (graph) in Table 1. What can you conclude on the data between V_{GG} and V_{GS} and its effect to I_D ?**
   - In a fixed-bias configuration, the gate-source voltage (V_{GS}) is directly set by the gate supply voltage (V_{GG}), such that $V_{GS} = -V_{GG}$. As V_{GG}becomes more negative, V_{GS} also becomes more negative, leading to a decrease in the drain current (I_D). This inverse relationship occurs because a more negative V_{GS} increases the depletion region within the FET channel, thereby reducing I_D.

2. **Observe the data (graph) in Table 2. What can you conclude on effect of R_S to V_{GS} and subsequently I_D ?**
   - In a self-bias configuration, the source resistor (R_S) introduces a voltage drop across itself, which increases with higher drain current (I_D). This increases the source voltage V_S, resulting in a more negative gate-source voltage (V_{GS}). As V_{GS} becomes more negative, the drain current is reduced, providing a stabilizing effect. This feedback mechanism ensures that I_D remains more stable compared to the fixed-bias configuration.

3. **From the data in Table 1 and Table 2, how I_D is controlled with fixed-bias and voltage divider configurations?**
   - The fixed-bias arrangement allows for direct control of I_D by altering V_{GG} . A negative V_{GG} results in a negative V_{GS}, which reduces I_D. However, this approach is unstable due to its sensitivity to temperature changes and device variances. In contrast, the voltage-divider arrangement sets the gate voltage through a resistive network. This arrangement improves stability by increasing the source voltage (V_S) and decreasing I_D, resulting in a self-correcting effect.

4. **How does I_D controlled by the other configurations?**
   - In the fixed-bias configuration, I_D is directly controlled by adjusting V_{GG}. A more negative V_{GG} leads to a more negative V_{GS}, thereby reducing I_D. However, this method is not very stable due to its sensitivity to temperature changes and device variations. In contrast, the voltage-divider configuration uses a resistive network to set the gate voltage. This setup offers better stability because any increase in I_D increases the source voltage V_S, making V_{GS} more negative and reducing I_D, creating a self-correcting effect.

References

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[2] T. Fiore, "12.3: DE-MOSFET Biasing," in *Semiconductor Devices - Theory and Application*, LibreTexts. [Online]. Available: https://eng.libretexts.org/Bookshelves/Electrical_Engineering/Electronics/Semiconductor_Devices_-_Theory_and_Application_(Fiore)/12%3A_Metal_Oxide_Semiconductor_FETs_(MOSFETs)/12.3%3A_DE-MOSFET_Biasing?. [Accessed: 22-Mar-2025].

[3] "DC Biasing of FETs (Part - 1)," EduRev. [Online]. Available: https://edurev.in/t/101000/DC-Biasing-of-FETs--Part-1--Analog-Electronics?. [Accessed: 22-Mar-2025].

