Modular Hardware System-Common Redundant Power Supply (M-CRPS) Base Specification

Part of the
Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

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Revision history

Date	Version	Description
April 15th 2022	0.70	Initial public release
June 24th 2022	0.75	Section 9 Control and Indicator Functions – Fixed typos Section 9.6.1 A0 Input addressing – Updated Table 9-7 A0 input signal characteristics: changed pull-up from 470kΩ to 47kΩ. Section 9.6.1 A0 Input Addressing – Updated Figure 9 6 Flow diagram to detect between logic and analog SMBus addressing: updated decision-making block Section 9.6.1 A0 Input Addressing – Updated Table 9-10: updated resistor values. Section 12.7.1 Physical Layer – Updated Figure 12-16 Section 12.7.1 Physical Layer – Updated Figure 12-17 Section 3 Thermal Requirements – Updated entire section Section 14 Regulatory & Ecology Requirements – Updated entire section Section 2.3 LED Marking and Identification – Updated Table 2-1 LED Characteristics and table notes. Section 5.3.2. Input Voltage Specification – Updated Table 5-12 -48VDC power supply Input voltage range. Section 7.1 Output Power/Currents – Added 54VDC output option in Table 7-1 Section 7.1 Peak Load Protection – Updated Table 7-2 Peak load protection testing conditions Section 7.1 Voltage Regulation – Added 54VDC output option in Table 7-3 Voltage regulation limits Section 7.5 Dynamic Loading – Added 54VDC output option in Table 7-4 Transient Load requirements. 7.6 Capacitive Loading – Added 54VDC output option in Table 7-6 Capacitive loading conditions 7.8 Closed Loop Stability – Updated paragraph Section 8.1.8 Under Voltage Protection - Added subsection Supplemental Material K. 185mm by 73.5mm -48VDC input M-CRPS mechanical drawing – Added drawing. Supplemental Material M, Reference Distorted Waveforms – Added section Section 4.1 Acoustics Requirements – Updated section. Section 4.2.9.1 Continuous Fan Speed Sweep – Updated Figure 4-6 Plot of mean peak vibration spectrum limit. Section 13.1 Component De-Rating – Deleted link.
August 23rd 2022	0.90	Section 2.3 LED Marking and Identification – Updated Table 2 1 LED Characteristics and added note 2. Supplemental Material O Luminosity Measurements – Added section. Section 3.3 Thermal Sensors – Change temperature sensor accuracy from ±1ºC to ±2ºC. Section 2.1.1.2 277VAC/380VDC Input - Updated Figure 2 4 185mm by 73.5mm form factor with 277VAC/380VDC inlet connector. Section 2.1.1.4 -48VDC Input (Telecom) – Updated Figure 2 6 185mm by 73.5mm form factor with -48VDC input connector. Section 2.1.2.2 277VAC/380VDC Input – Updated Figure 2 9 185mm by 60mm form factor with 277VAC/380VDC inlet connector. Section 2.1.2.4 -48VDC Input (Telecom) – Updated Figure 2 10 60mm form factor with -48VDC input connector. Supplemental Material P. Exhaust Temperature Measurement – Added section Section 3.1 Temperature and Altitude Conditions – Added note 3 in Table 3 1 Power supply thermal test conditions. Section 3.2 Power Supply Fan – Added L10 fan data. Section 9.5 Imon Signal (Output) – In Table 9 5 Imon signal characteristics: Updated signal delay from <100ns to <2us. Updated sensitivity, now two options configurable via config file. Added notes 2 and 3. Section 402.6.1 185mm by 73.5mm Form Factor – Updated Table 2 3 73.5mm in width PSU pinout definition to reflect 54V output option and added note 6. Section 5.2.2 Input Voltage Specification – Updated start up and power off voltages in Table 5 10 +54VDC input voltage specification. Section 5.2.4 Inrush Current - Updated paragraph. Section 5.2.8 Input Ripple Voltage - Updated paragraph. Section 5.3.1 Inlet Connector - Added reference to Figure 2 20 -48VDC inlet connector example (Telecom). Section 7.4 Voltage Regulation - Updated Table 7 4 Voltage regulation limits, added +54V output specifications, added more clarification to note 2 and added note 3. Section 7.5 Dynamic Loading - Updated Table 7 5 Transient load requirements. Section 7.6 Capacitive Loading - Updated Table 7 7 Capacitive loading conditions.

		Section 8.1.6 Over Voltage Protection (OVP) - Updated Table 8 4 Over Voltage Protection (OVP) Limits. Section 8.1.7 Under Voltage Protection (UVP) - Updated Table 8 5 Under Voltage Protection (OVP) Limits. Section 5.1.3 Input Voltage Specification - Added note 2 in Table 5 3 AC Input voltage ranges. Section 5.1.7 Inrush Current - Updated secondary inrush event current in paragraph. Section 5.3.7 Reversed Polarity Protection - Updated paragraph. Section 7.3 Auxiliary (Stand-by) Output - Added droop share characteristics and figure. Section 7.8 Closed Loop Stability - Updated Table 7 8 Phase and gain margin requirements and added note 2. Section 7.13.7 Concurrent Maintenance - Updated second paragraph. Section 7.13.9 Current Share Signal Characteristics - Updated Table 7 11 Current Share Signal Characteristics. Section 7.14 Ripple/Noise - Updated Table 7 12 Ripple and noise. Section 7.14 Ripple/Noise - Added note to Figure 7 5 Differential noise test setup. Section 7.15 Timing Requirements - Fixed typo in Table 7 13 Timing requirements (VINOK instead of VIONK). Section 8.1.7 Under Voltage Protection (UVP) - Fixed typo. Section 8.1.8 Over Temperature Warning (OTW) - Fixed typo in header. Section 9.1.1 Two-State Signal - Updated Table 9 1 Two-state PSON# signal characteristics (3.3VSB pullup). Section 9.2 PWOK Signal (Output) - Fixed typo in header (PWOK signal is active high not low). Section 9.2 PWOK Signal (Output) - Updated Table 9 2 PWOK signal characteristics (3.3VSB pullup). Section 9.3 SMBAlert# Signal (Output) - Updated Table 9 3 SMBAlert# signal characteristics (3.3VSB pullup). Section 9.4 VINOK Signal (Output) - Updated Table 9 4 VINOK Signal characteristics (3.3VSB pullup). Supplemental Material P. Exhaust Temperature Measurement – Added Figures O-3 and O-4 for temperature measurement in reversed airflow power supplies. Section 6.1.1.1 240VAC/240VDC and Wide Input Range - Updated efficiency at 100% loading condition from 91% to 92% in Table 6 1 Efficiency requirements for 240VAC/240VDC and wide input range power supplies. Section 277VAC/380VDC Input – Updated efficiency at 100% loading condition from 91% to 92% in Table 6 2 Efficiency requirements for 277VAC/380VDC power supplies. Section Data & Sideband Serialization Interface A(DSSI) – Updated Figure 12 32 Physical layer and connections for point-to-point communication between Host and Client, Host bias will be updated on a later version. Supplemental Material D. 73.5mm in width M-CRPS card edge mechanical drawing – Updated drawing added chamfer details. Supplemental Material E. 60mm in width M-CRPS card edge mechanical drawing – Updated drawing added chamfer details. Supplemental Material F. M-CRPS handle mechanical drawing – Updated drawing added handle material. Supplemental Material G. M-CRPS latch mechanical drawing – Updated drawing added radii detail. Supplemental Material H. M-CRPS latch plastic grip option 1 (snap-in version) – Updated drawing, added material and default color. Supplemental Material I. M-CRPS latch plastic grip option 2 (over molded version) – Updated drawing, added material and default color. Section 2.4.2 277VAC/380VDC Input - Added references for connector vendors and part numbers Section 2.4.4 -48VDC Input (Telecom) - Added references for connector vendors and part numbers Section 2.1.1.2 277VAC/380VDC Input - Added reference for connector vendors and part numbers Section 2.1.1.4 -48VDC Input (Telecom) - Added reference for connector vendors and part numbers Section 2.1.2.2 277VAC/380VDC Input - Added reference for connector vendors and part numbers Section 2.1.2.4 -48VDC Input (Telecom) - Added reference for connector vendors and part numbers Section 2.6.1 185mm by 73.5mm Form Factor - Updated Table 2 2 185mm/265mm by 73.5mm M-CRPS dimensions and receptacle connector; Added link to connectors information. Section 2.6.2 185mm by 60mm Form Factor – Updated Table 2 4 185mm by 60mm M-CRPS dimensions and receptacle connector; Added link to connectors information.

		Supplemental Material G. M-CRPS latch mechanical drawing - Added latch material. Section 9.7 Remote Sense And Return Sense / PSKILL – Added subsection Section 2.6.1 185mm by 73.5mm Form Factor - Added note 7 in Table 2 3 73.5mm in width PSU pinout definition, and updated typo in the title. Section 2.6.2 185mm by 60mm Form Factor - Added note 3 in Table 2 5 60mm in width PSU pinout definition, and updated typo in the title. Section 5.1.4 Line Isolation Requirements - Updated paragraph. Section 14.8.1 Dielectric Strength Testing - Updated paragraph. Section 5.1.9 Line Transient Specification – Updated note added test at full load
September 26th, 2022	1.00 RC2	Section 11 FRU Requirements – Updated Table 11 1 Minimum FRU contents and added Table 11 2 M-CRPS FRU MultiRecord definition. Section 12.1.56 Summary of PMBus commands – Added command MFR_SPECIFIC_COMMAND EXT (FEh) in Table 12 28 Summary of PMBus commands. Section 7.13.1 Current Share (Ishare) – Updated settling time in Table 7 9 Additional Requirements on current share behavior. Section 7.2 Peak Load Protection – Corrected typo in Table 7 2 Peak load protection testing conditions, peak load is Rated + 65% total. Section 2.6 Output Connector Interface – Updated Table 2 3 73.5mm in width PSU pinout definition and added note to reflect the notch in the +54V output M-CRPS. Section 2.6 Output Connector Interface – Updated Table 2 5 60mm in width PSU pinout definition and added note to reflect the notch in the +54V output M-CRPS. Supplemental Material D. 73.5mm in width M-CRPS card edge mechanical drawing – Added card edge's mechanical drawing with notch for +54V output M-CRPS and updated 12V output card edge. Supplemental Material E. 60mm in width M-CRPS card edge mechanical drawing - Added card edge's mechanical drawing with notch for +54V output M-CRPS and updated 12V output card edge. Supplemental Material Q. Additional Requirements on Input Line Transients – Added section. Section 7.3 Auxiliary (Stand-by) Output - Added Table 7 3 Output voltage droop characteristics and updated caption of Figure 7 2 Typical 12VSB droop share characteristics. Section 2.6 Output Connector Interface – Updated Figure 2 23 and its caption. Section 2.4.1 240VAC/240VDC Input – Updated Figure 2 16 IEC320-C20 Inlet connector example. Section 8.3 Short Circuit Protection – Added subsection Section 5.1.1 Power Factor and iTHD - Added option for less than 1400W PSUs iTHD Table 5 2 iTHD requirements. Section 5.1.8 Inrush Current High Voltage DC Input - Added subsection. Section 5.3 Low Voltage -48VDC Input Requirements (Telecom) - Added Section 5.3.5 Inrush Current. Section 5.3.3 Minimum Input Inductance - Removed last sentence since we already point to the supplemental material. Section 7.2 Peak Load Protection - Removed column voltage undershoot in Table 7 2 Peak load protection testing conditions. Section 7.4 Voltage Regulation - Updated note 1 of Table 7 4 Voltage regulation limits. Section 7.8 Closed Loop Stability - Updated paragraph and Note 2 in Table 7 8 Phase and gain margin requirements. Section 7.11 Zero Load Stability- Updated paragraphs. Section 7.16 PWOK Signal Timing Requirements – Updated note in Figure 7 9 Configurable PWOK warning time timing diagram for High voltage power supplies. Section 14.3 Safety Requirements and Standards - Removed duplicated paragraph i). Section 14.5 Telecommunications DC Mains Powered Power Supplies – Fixed typo in Note 1. Section 9.2 PWOK Signal (Output) - Corrected typo in the heading (removed input). Section 8.4 Input Over Current Protection – Added section. Section 9.1 PSON# Signal (Input) – Updated Figure 9 1 Required PSON# input signal circuit for two/three-state operation, for clarification. Section 9.2 PWOK Signal (Output) – Updated Figure 9 5 PWOK circuit implementation, for clarification. Section 9.1 PSON# Signal (Input) - Updated heading (removed duplicated "input" word). Section 9.3 SMBAlert# Signal (Output) - Updated heading (removed duplicated "output" word). Section 9.4 VINOK Signal (Output) - Updated heading (removed duplicated "output" word). Section 9.5 Imon Signal (Output) - Updated heading (removed duplicated "output" word). 185mm by 73.5mm M-CRPS mechanical drawing – Updated mechanical drawing to represent the different output voltage options (12V or 15V) and regular/reversed airflow Section 2.1.1.3 +54VDC Input (Rack Power Input) – Updated paragraph and Figure 2 5 185mm by 73.5mm form factor with bus bar connector input.

		Section 12.1.44 IIN_OC_WARN_LIMIT (5Dh) – Added section. Section 9.5 Imon Signal (Output) – Added note 4 in Table 9 5 Imon signal characteristics. Section 9.5 Imon Signal (Output) – Added Figure 9 6 Imon block diagram concept. Supplemental Material B 185mm by 60mm M-CRPS mechanical drawing - Added card edge's mechanical drawing with notch for +54V output M-CRPS and updated 12V output card edge. Supplemental Material C 265mm by 73.5mm M-CRPS mechanical drawing - Added card edge's mechanical drawing with notch for +54V output M-CRPS and updated 12V output card edge. Section 2.4.3 +54VDC Input (Rack Power Input) – Updated Figure 2 9 185mm by 60mm form factor with 277VAC/380VDC inlet connector. Section 9.5 Imon Signal (Output) – Updated Figure 9 6 Imon block diagram concept, added high frequency filter and added Note 2. Section 8.4 Input Over Current Protection - Table 8 6 Input OCW Averaging window and hysteresis moved from Section 8.4.1 to Section 8.4. Section 8.4.1 Input Over Current Warning – AC Input – Added cross reference to Section 12.1.44. Section 5.1.1 Power Factor and iTHD – Added notes 3, 4 & 5 in Table 5 2 iTHD requirements. Section 5.1.9 Line Transient Specification – Added cross-reference to Supplemental Material Q. Additional Requirements on Input Line Transients. Section 12.9 Security – Updated section. Section 7.16 PWOK Signal Timing Requirements – Updated cross-references and elaborated return to default value condition. Section 7.15 Timing Requirements - Updated maximum Tpwok_off in Table 7 13 Timing requirements and added Note 4. Section 5.1 High Voltage AC/DC Input Requirements - Table 5 1 Power factor requirements added Current iTHD (120VAC) requirements and added '<' symbols. Section 7.16 PWOK Signal Timing Requirements - Updated note in Figure 7 9 Configurable PWOK warning time timing diagram for High voltage power supplies, changed -5% to 11.40V. Section 7.13.1 Current Share (Ishare) - Updated Ishare signal to 8V = 100% load Section 9.5 Imon Signal (Output) - Table 9 5 Imon signal characteristics updated compliance voltage to 3.3V. Section 12.1.44 IIN_OC_WARN_LIMIT (5Dh) – Added Figure 12 10 Input OCW flowchart. Section 2.4.3 +54VDC Input (Rack Power Input) – Added Figure 2 19 +54V Input connector pinout. Section 2.4.4 -48VDC Input (Telecom) – Added Figure 2 21 -48V Inlet connector (Telecom) pinout. Section 12.7 Data & Sideband Serialization Interface A(DSSI) – Updated section to have compatibility with M-PESTI discovery command and virtual wires command and also a compatible physical layer. Supplemental Material J. 185mm by 73.5mm +54VDC input M-CRPS mechanical drawing – Updated mechanical drawing. Section 2.1.1.3 +54VDC Input (Rack Power Input) - Added note with cross reference to Supplemental Material J. Section 2.1.1.4 -48VDC Input (Telecom) - Added note with cross reference to Supplemental Material K. Section 12.9 Security – Updated. Section 12.1.56 Summary of PMBus commands – Added DAh MFR_SPDM command in Table 12 28 Summary of PMBus commands. Section 4.2.5 Accelerometer Positions – Updated cross reference to Section 4. Section 4.2.5 Accelerometer Positions – Updated Figure 4 3 Accelerometer's locations in the bottom of the 185mm by 73.5mm power supply. Section 4.2.5 Accelerometer Positions – Updated Figure 4 4 Accelerometer's locations in the bottom of the 185mm by 60mm power supply. Section 4.2.5 Accelerometer Positions – Updated Figure 4 5 Accelerometer's locations in the bottom of the 265mm by 73.5mm power supply. Section 4.2.9.1 185mm by 60mm Continuous Fan Speed Sweep – Added section. Section 4.2.9.2 185mm by 73.5mm Continuous Fan Speed Sweep Limit – Added section. Section 4.2.9.3 265mm by 73.5mm Continuous Fan Speed Sweep Limit – Added section. Section 2.1.1.3 +54VDC Input (Rack Power Input) – Updated Figure 2 5 185mm by 73.5mm form factor with bus bar connector input. Section 12.7 Data & Sideband Serialization Interface A(DSSI) – Updated section. Section 12.8.2 Configuration File Header - Updated polynomial in Note of Table 12 52 Header area. Section 12.8.3.1 LED Behavior Configuration Block - Updated Table 12 55 Power supply event table. Section 12.8.3.9 Black Box Save on Fault/Warning Condition Configuration Block - Removed

		Section 12.8.3.6 Fans Configuration Block - Added note 2 to Table 12 60 Power supply fans thresholds. Section 12.8.3.8 Latch on Fault Condition Configuration Block - Updated Table 12-53 Power supply latch on fault condition configuration block. Section 12.8.3 Configuration Area Definition - Updated Table 12 53 Configuration block types. Section 12.8 Configuration File - Added note to Figure 12 43 Main areas of the configuration file. Section 12.8.3.10 Miscellaneous Configuration Block - Updated section Section 12.8.3.5 Input Configuration Block - Updated note 2 in Table 12 59 Power supply input thresholds. Section 12.8.5 Data Table Area Definition - Updated section. Section 12.5.1 FW Image Mapping - Added Figure 12 28 In-System FW Update Memory Mapping. Section 12.5.4 Power Supply Operating Mode During and After Firmware Update - Updated paragraph. Section 12.5.6 Firmware Update Process - Added Figure 12 30 PSU Boot flow during powering ON. Section 12.5.7 Power Supply Commands - Updated MFR_MODEL to 24 bytes Section 12.5.7 Power Supply Commands - Updated Table 12 38 PSU FW Image header and added notes. Section 12.1.56 Summary of PMBus commands - Added commands D1h, D2h and D3h in Table 12 28 Summary of PMBus commands. Section 2.3 LED Marking and Identification - Deleted note 1. Section 2.1.2.3 +54VDC Input (Rack Power Input) - Updated section Section 5.2.1 Inlet Connector - Updated paragraph Section 5.2.6 Susceptibility Requirements - Updated paragraph Section 7.13.1 Current Share (Ishare) - Added note 2 in Table 7 9 Additional Requirements on current share behavior. Section 12.1.44 IIN_OC_WARN_LIMIT (5Dh) - Updated Note 8.b and 9.a. Section 9.6.1 A0 Input Addressing - Added note 2 in Figure 9 7 Flow diagram to detect between logic and analog SMBus addressing. Section 12.5.7 Power Supply Commands - Updated length of MFR_FW_REVISION command to 5 bytes. Section 13.1 Component De-Rating - Removed ESD TBDs, added Transistor, GaAs, GaN, PHEMT (GaN) type in Table 13 1 Component de-rating guidelines. Supplemental Material J. 185mm by 73.5mm +54VDC input M-CRPS mechanical drawing – Updated mechanical drawing (latch). Supplemental Material K. 185mm by 73.5mm -48VDC input M-CRPS mechanical drawing – Updated mechanical drawings, added airflow direction options. Supplemental Material L. 185mm by 60mm -48VDC input M-CRPS mechanical drawing – Added mechanical drawing and shifting the rest of the Supplemental Material subsections. Section 12.1.56 Summary of PMBus commands – Added MFR_LINE_STATUS (E0h) and MFR_SYSTEM_LED_CNTL (E1h) commands to Table 12 28 Summary of PMBus commands. Section 12.8.3.1 LED Behavior Configuration Block – Updated Table 12 54 LED descriptor. Section 12.1.46 MFR_SYSTEM_LED_CNTL (E2h) – Added subsection. Section 12.1.44 IIN_OC_WARN_LIMIT (5Dh) - Updated Note 8.b and 9.a. Section 12.8.3.1 LED Behavior Configuration Block – Added mismatched event in Table 12 55 Power supply event table. Section 12.1.45 MFR_LINE_STATUS (E1h) – Added section. Section Acknowledgements – Updated section. Section III DC-MHS Family of Specifications – Added section. Section 7.3 Auxiliary (Stand-by) Output - Added notes 1 and 2. Formatted the entire document to have everything within the document margins.
September 27th, 2022	1.00 RC3	Removed Appendix A and B. Fixed typos
November 1st, 2022	1.00 RC4	Removed references to Appendix A and B in the table of contents. Section 8.1.4 Over Current Protection & Over Power Protection (OCP & OPP) - Updated Figure 8 6 PSU Output Current vs. Time. Section 8.1.3.3 Over Current Warning Level 3 (OCWPL3) - Updated Table 8 2 OCW Thresholds OCW3 column. Section 8.1.4 Over Current Protection & Over Power Protection (OCP & OPP)- Updated Table 8 3 PSU vs. Load Behaviors – Constant Current and Primary Power Limit, Initial Constant Current Setpoint. Section 8.1.3.3 Over Current Warning Level 3 (OCWPL3) - Updated Figure 8 5 SMBAlert# flow.

		Section 9.5 Imon Signal (Output) - Updated Figure 9 6 Imon block diagram concept and updated notes. Section 12.8.3.10 Miscellaneous Configuration Block - Added bit Imon/presence in Table 12 63 Miscellaneous configuration block. Section 2.6.2 185mm by 60mm Form Factor - Fixed typos in Table 2 5 60mm in width PSU pinout definition (swapped S1 thru S7 with S8 thru S14). Section 4.1 - Changed from Acoustic requirements to Overview. Section 4.1.9 Acoustical Requirements - Inserted page breaks to have 1 page per table. Section 4.1.9 Acoustical Requirements - Updated prominence ratio in Table 4 3 Home & Office PSU Acoustical Requirements, Table 4 4 General Data Center & Storage PSU Acoustical Requirements and Table 4 5 High Performance Computing PSU Acoustical Requirements. Section 12.4.7 Cold Redundancy Bus (CR_BUS) - Updated resistor's values in Figure 12 26 CR_BUS signal circuit. Section 12.8.5 Data Table Area Definition - Updated paragraph. Section 7.13 Forced Load Sharing - fixed typos in second paragraph: 8V at full load.
June 27th, 2023	1.01 RC1	Integrated Errata: - Section 9.5 Imon Signal (Output) – Added definition for MCU's GPO1 & GPO2 in Figure 9 6 Imon block diagram concept. - Section 9.1 PSON# Signal (Input) – Fixed notes 1 and 2 in Figure 9 1. - Section 9.4 VINOK Signal (Output) - Fixed typo in Table 9 4 VINOK Signal characteristics, should say VINOK instead of PWOK. - Section 2.6.2 185mm by 60mm Form Factor– Fixed typo in Figure 2 25 pins S7 & S14 were swapped. - Section 12.8.3.1 LED Behavior Configuration Block – Fixed typo in Offset column on Table 12 55 Power supply event table. - Section 12.8.3.8 Latch on Fault Condition Configuration Block - Fixed typo in Offset column on Table 12 62 Power supply latch on fault condition configuration block. - Section 12.1.56 Summary of PMBus commands - Fixed typos in Table 12 22 MFR_SYSTEM_LED_CNTL (E2h) command bitfield definition for commands DFh, E0h, E1h & E2h. Section 9.8 Pin Capacitance - Added new section Section 7.1 Output Power/Currents - Updated Table 7 1 Load requirements. Section 7.1 Output Power/Currents - Updated notes 2, 3 and added note 7 in Table 7 1 Load requirements. Section 8.1.3.3 Over Current Warning Level 3 (OCWPL3) - Updated Table 8 2 OCW Thresholds. Section 3.1 Temperature and Altitude Conditions – Updated Table 3 1 Power supply thermal test conditions. Section 12.1.47 MFR_READ_CONFIG_FILE_SIZE (D1h) - New section Section 12.1.48 MFR_READ_CONFIG_BLOCK_SIZE (D2h) - New section Section 12.1.49 MFR_READ_CONFIG_FILE (D3h) - New section Section 12.1.50 MFR_EFFICIENCY_DATA (B3h) - New section Section 12.1.51 MFR_PEAK_CURRENT_RECORD (E9h) - New section Section 12.1.56 Summary of PMBus commands - Updated Table 12 28 Summary of PMBus commands. Section 12.9 Security - Updated entire section Section 12.8.1 Overview - Updated Figure 12 43 Main areas of the configuration file., showing the file transfer header and added note. Section 12.7.8.2 Analog IO Expander Profile - Corrected typo in paragraph, single-channel instead of single-byte and multi-channel instead of multi-byte. Section 12.7.8.2 Analog IO Expander Profile - Updated Figure 12 40 Single-channel analog channels exchange, and deleted note 1. Section 12.7.8.2 Analog IO Expander Profile - Updated Figure 12 41 Multi-channel analog channels exchange, and updated note 1. Section 7.4 Voltage Regulation - Updated Table 7 4 Voltage regulation limits to reflect Figure 7 2 Typical 12VSB droop share characteristics Section 5.1.3 Input Voltage Specification - Updated 277VAC input version on Table 5 3 AC Input voltage ranges and updated note 1. Section R.2 Over Current Warning 2 (OCW2) – Updated Figure R-11. SMBAlert# assertion OCW2 Timing (Default Setting) with PWOK de-assertion. Section 7.16 PWOK Signal Timing Requirements – Updated Figure 7 9 Configurable PWOK warning time timing diagram for High voltage power supplies Section 7.16 PWOK Signal Timing Requirements – Updated note in Figure 7 8 Toff_latch flow diagram, slope decay from 1 to 10ms. Section 7.15 Timing Requirements – Updated Table 7 13 Timing requirements, added specification for -48VDC and +54VDC input power supplies for Tvout_holdup, & Tpwok_holdup.

		Section 12.8.3.1 LED Behavior Configuration Block - Added UVPmain, OVWmain, FanWarning and FanFault to Table 12 54 LED descriptor. Section 9.5 Imon Signal (Output) - Updated Imon total tolerance requirement. Section 11.2.1 Data Format – Corrected numeral in Note of Table 11 1 Minimum FRU contents. Section 12.1.43 MFR_MAX_IOUT_CAPABILITY (F1h) - Added notes about the data format of this command Section 11 FRU Requirements - Added paragraph allowing the use of a non-volatile memory area in the MCU. Section 12.1.2 Addressing - Update paragraph allowing the use of a non-volatile memory area in the MCU. Section 7.14 Ripple/Noise - Added 2,200uF Electrolytic capacitor as requirement for ripple and noise measurement. Section 7.14 Ripple/Noise - Updated Figure 7 5 Differential noise test setup to make it more representative. Section 7.14 Ripple/Noise - Updated note 1 in Figure 7 5 Differential noise test setup, the measurement needs to be done at the PSU connector. Section 7.14 Ripple/Noise - Updated note 2 in Figure 7 5 Differential noise test setup, to specify time/div in the measurement. Section 7.4 Voltage Regulation - Updated note 1 in Table 7 4 Voltage regulation limits, changed to 0% and 100% loading conditions. Section 7.5 Dynamic Loading - Updated note 2 in Table 7 5 Transient load requirements, from 5 Amps minimum to 5% of rated current. Section 5.1.1 Power Factor and iTHD - Added 277VAC input requirements in Table 5 1 Power factor requirements. Section 5.1.1 Power Factor and iTHD - Added 277VAC input requirements in Table 5 2 iTHD requirements. Section 7.5 Dynamic Loading - Updated Table 7 5 Transient load requirements to include voltage ranges. Section 2.6.1 185mm by 73.5mm Form Factor - Updated notes 1 and 2 Section 2.6.1 185mm by 73.5mm Form Factor - Updated Table 2 2 185mm/265mm by 73.5mm M-CRPS dimensions and receptacle connector. Section 2.6.2 185mm by 60mm Form Factor - Added note 7 Section 2.6.2 185mm by 60mm Form Factor - Updated Table 2 4 185mm by 60mm M-CRPS dimensions and receptacle connector. Section 2.3 LED Marking and Identification - Updated note in Figure 2 14 Flex PCB 3D representation showing the location of the LEDs. Section 2.2 Handle and Retention Latch - Updated Figure 2 12 M-CRPS illuminated handle Section 12.8.3.10 Miscellaneous Configuration Block - Updated Table 12 63 Miscellaneous configuration block added Cold Redundancy registers for up to 6 PSUs Section 6.1.1.1 240VAC/240VDC and Wide Input Range - Updated Table 6 1 Efficiency requirements for 240VAC/240VDC and wide input range power supplies Section 6.1.1.2 277VAC/380VDC Input - Updated Table 6 2 Efficiency requirements for 277VAC/380VDC power supplies Section 7.4 Voltage Regulation - Updated Note 1 in Table 7 4 Voltage regulation limits. Section 7.5 Dynamic Loading - Updated Note 5 in Table 7 5 Transient load requirements. Section 7.8 Closed Loop Stability - Updated note 2 in Table 7 8 Phase and gain margin requirements. Section 7.12 Hot Swap - Updated note to clarify output hot swap capability. Section 13.1 Component De-Rating – Added -48Vdc – -60Vdc; 277Vac; 336Vdc; +54Vdc as test condition for input voltage Section 8.1.3.3 Over Current Warning Level 3 (OCWPL3) - Updated Table 8 2 OCW Thresholds and added Note 1. Section 8.1.3 Over Current Warning (OCW) - Updated Figure 8 5 SMBAlert# flow. Section 9.7 Remote Sense And Return Sense / PSKILL - Added Maximum voltage droop compensation in Table 9 11 Remote Sense +/- And PSKILL signal parameters. Section 12.5.5 Firmware Image Header - Added option for multi-image package in Table 12 38 PSU FW Image header and added Note 4. Section 8.1.1 Current sense - Updated Note 1 on Figure 8 1 Main output current sense block diagram, current sense element on either rail. Section 5.1.14 Surge Immunity - Added Note 2 in Table 5 8 Surge immunity requirements, use 2Ω for testing. Section 7.15 Timing Requirements - Added Note 2 in Figure 7 7 VINOK assertion logic, 5th cycle after 12Vstby is within regulation. Section 12.1.23 Resetting to Default Limits - Added Note 1. Section 7.15 Timing Requirements - Updated Table 7 13 Timing requirements, Tvinok_on, Tvinok_off and Tpwok_holdup.

		Section 7.15 Timing Requirements - Updated Figure 7 6 Turn ON/OFF Timing (Power Supply Signals). Section 7.15 Timing Requirements - Updated Figure 7 7 VINOK assertion logic and added Note 3. Section 8.1.3 Over Current Warning (OCW) - Updated Figure 8 6 PSU Output Current vs. Time. Section 12.1.56 Summary of PMBus commands - Added new command MFR_COMPONENT_ID (EBh) in Table 12 28 Summary of PMBus commands. Section 12.1.56 Summary of PMBus commands - Updated Table 12 28 Summary of PMBus commands, fixed typos and added SMBus transaction types. Supplemental Material R. Over Current Warning Behavioral Timing Diagrams Examples - created new section. Section 8.1.4 Over Current Warning Behavioral Timing Diagrams - Moved to Supplemental Material R. Section 12.1.42 Conceptual View of How Status Bits and SMBAlert# Work - Updated Figure 12 7 Conceptual Schematic of STATUS bits and SMBAlert# for commands that support PAGE_PLUS_ logic gate generating SMBAlert# signal shall be a NOR gate. Section 12.1.42 Conceptual View of How Status Bits and SMBAlert# Work - Updated Figure 12 8 Conceptual schematic of STATUS bits and SMBAlert# without PAGE_PLUS_ logic gate generating SMBAlert# signal shall be a NOR gate and added Note 1. Section 7.3 Auxiliary (Stand-by) Output - Added Note 3 in Figure 7 2 Typical 12VSB droop share characteristics. Section 7.17 12V Internal Transfer Switch - New section. Section 12.5.2 Summary of Commands & Capabilities Supported in Bootloader Mode - Updated paragraph adding support for DSSI while in FW Update mode. Section 12.7.1 Physical Layer - Updated Figure 12 32 Physical layer and connections for point-to-point communication between Host and Client changed pullup in Host side to 100 KΩ. Section 14.4.1 Safeguard Robustness – Added paragraph and figure for hot surface label. Section 14.3 Safety Requirements and Standards – Fixed broken reference. Section 12.8.4.1 Executable Code Block Definition – Fixed offset in Table 12 65 Power supply event table. Supplemental Material A 185mm by 73.5mm M-CRPS mechanical drawing – Updated section. Supplemental Material B 185mm by 60mm M-CRPS mechanical drawing – Updated section. Supplemental Material C 265mm by 73.5mm M-CRPS mechanical drawing – Updated section. Supplemental Material D 73.5mm in width M-CRPS card edge mechanical drawing – Updated section. Supplemental Material E 60mm in width M-CRPS card edge mechanical drawing – Updated section. Supplemental Material F M-CRPS handle mechanical drawing – Updated section. Supplemental Material J 185mm by 73.5mm +54VDC input M-CRPS mechanical drawing – Updated section. Supplemental Material K 185mm by 73.5mm -48VDC input M-CRPS mechanical drawing – Updated section. Supplemental Material L 185mm by 60mm -48VDC input M-CRPS mechanical drawing – Updated section. Supplemental Material P. Exhaust Temperature Measurement – Updated Figure O-3. Thermocouple locations for the 185mm by 73.5mm and 265mm by 73.5mm form factors with reversed airflow. Supplemental Material P. Exhaust Temperature Measurement – Figure O-4. Thermocouple locations for the 185mm by 60mm form factor with reversed airflow. Section 12.5.7 Power Supply Commands - Updated description of bit 5 in Table 12 43 MFR_FWUPLOAD_STATUS command format. Section 12.1.51 MFR_PEAK_CURRENT_RECORD (E9h) – Updated note, only MFR_CLEAR_BLACKBOX (E0h) can reset historical peak current. Section 2.6.1 185mm by 73.5mm Form Factor – Added reference to output receptacle's outline in Table 2 2 185mm/265mm by 73.5mm M-CRPS dimensions and receptacle connector. Section 2.6.2 185mm by 60mm Form Factor - Added reference to output receptacle's outline in Table 2 4 185mm by 60mm M-CRPS dimensions and receptacle connector. Section IV Specification Compliance Table (For System Designers Only) - New section
July 20th, 2023	1.01 RC2	Section 5.2.7.2 Auxiliary (Stand-by) Output - Added support for 12VSB Auxiliary output in +54V input M-CRPS Section 6.1.1.1 240VAC/240VDC and Wide Input Range - Updated Table 6 1 Efficiency requirements for 240VAC/240VDC and wide input range power supplies, and added Note. Section 6.1.1.2 277VAC/380VDC Input - Updated Table 6 2 Efficiency requirements for 277VAC/380VDC power supplies, and added Note 2 and 3. Section 14.3 Safety Requirements and Standards – Added item J to the list and Figure 14 1 Multiple input sources IEC 60417-6172 symbol.

		Section 14.5.1 Output Grounding Requirements – Added new sub section. Section 14.16 Compliance Certifications – Updated China's CQC as a requirement in Table 14 8 Country approval and marking requirements. Section 7.17 12V Internal Transfer Switch – Fixed typo in Figure 7 10 12Vmain to 12VSB transfer switch. Section 4.2.2 Test Environment – Fixed reference. Section 4.2.4 Installation and Operation of the Power Supply – Fixed reference. Section 11.2 Device Protocol – Updated paragraph added Page Write and Random Read protocol. Section 12.1.5 Pull Ups – Change weak pull-up resistors for SDA and SCL to 100KΩ. Section 12.1.50 MFR_EFFICIENCY_DATA (B3h) – Updated Table 12 24 Efficiency data definition, added definition for high line and low line efficiency. Section 12.1.52 MFR_COMPONENT_ID (Ebh)– New section. Section 12.1.53 MFR_TOT_POUT_MAX (Ech) – New section. Section 12.1.56 Summary of PMBus commands – Updated table: - Added spaces between commands. - Added bit field definition for STATUS_CML. - Added bit 4 definition of STATUS_MFR_SPECIFIC. - Added new command MFR_TOT_POUT_MAX. - Added Note 1 at the end of the table. - Added new command MFR_VOUT_MARGINING. - Added new command MFR_OCWPL1_SETTING Section 13.1 Component De-Rating – Updated Table 13 1 Component de-rating guidelines, relaxed maximum voltage requirement for high voltage bulk storage aluminum hybrid capacitors requirement from ≥200V to ≥100V. Section 2.2 Handle and Retention Latch – Updated Figure 2 12 M-CRPS illuminated handle. Section 8.1.3.3 Over Current Warning Level 3 (OCWPL3) – Updated Table 8 2 OCW Thresholds, deleted OCWPL2 column and changed OCWPL3 Default set point threshold to 116%. Section 12.1.54 MFR_VOUT_MARGINING (EDh) – Added new subsection. Section 12.8.3.10 Miscellaneous Configuration Block – Added bits to VoutMarginingUnlock and OCWPL1SettingUnlock Table 12 63 Miscellaneous configuration block. Updated mechanical drawings in supplemental material section.
August 22nd, 2023	1.02 RC1	Moved the contents of section 5.3.5 to section 5.1.8 Moved the contents of section 5.3.12 to section 5.3.5 Deleted section 5.3.12. Section 12.7.7 Command Set – Added DSSI ping command in Table 12 50 Configuration commands set. Section 12.8.3.10 Miscellaneous Configuration Block – Added SetA1AsPresenceDetect option in Table 12 63 Miscellaneous configuration block and reformatted the table. Section 12.7 Data & Sideband Serialization Interface A(DSSI) – Added note: simple present not supported by default. Section 12.5.7 Power Supply Commands – Added bit 6 in Table 12 43 MFR_FWUPLOAD_STATUS command format, to indicate a wrong value in the configuration file that was just transferred. Section 12.8.3.2 Temperature Configuration Block – Updated note in Table 12 56 Power supply temperature thresholds. Section 12.8.3.3 Main Output Configuration Block – Updated note 1 in Table 12 57 Power supply main output's thresholds. Section 12.8.3.4 Standby Output Configuration Block – Updated note 1 in Table 12 58 Power supply standby output's thresholds. Section 12.8.3.5 Input Configuration Block – Updated note 1 in Table 12 59 Power supply input thresholds. Section 12.8.3.6 Fans Configuration Block – Updated note 1 in Table 12 60 Power supply fans thresholds. Section 12.8.3.7 Timing Configuration Block – Updated note 1 in Table 12 61 Power supply timing configuration. Section 12.8.3.8 Latch on Fault Condition Configuration Block – Fixed offset column in Table 12 62 Power supply latch on fault condition configuration block. Section 12.8.3.10 Miscellaneous Configuration Block– Added Use1BitPMBusAddressing & DisableRemoteSense option in Table 12 63 Miscellaneous configuration block and fixed offset column. Section 9.5 Imon Signal (Output) – Added range from 0 to 200% for sensitivity of 10uA/A also in Table 9 5 Imon signal characteristics. Section 4.1.7.3 Continuous Fan Speed Sweep – Changed altitude from 900m to 950m in Table 4 1 Definition of operating modes for constant fan speed testing for Home & Office PSU's.

		Section 4.1.7.3 Constant Fan Speed – Changed altitude from 900m to 950m and inlet temperature from 60degC to 55degC in Table 4 2 Definition of operating modes for constant fan speed testing for General Purpose & Storage PSU's and High-Performance Computing PSU's. Section 4.1.9 Acoustical Requirements – Changed altitude from 900m to 950m in Table 4 3 Home & Office PSU Acoustical Requirements. Section 4.1.9 Acoustical Requirements – Changed altitude from 900m to 950m and inlet temperature from 60degC to 55degC in Table 4 4 General Data Center & Storage PSU Acoustical Requirements. Section 4.1.9 Acoustical Requirements – Changed altitude from 900m to 950m in Table 4 5 High Performance Computing PSU Acoustical Requirements. Section 7.3 Auxiliary (Stand-by) Output – Added note 4 in Figure 7 2 Typical 12VSB droop share characteristics. Section 7.17 12V Internal Transfer Switch – Added note in Figure 7 10 12Vmain to 12VSB transfer switch. Section 7.4 Voltage Regulation – Added +-30mV to the 12.2V setpoint in note 1 of Table 7 4 Voltage regulation limits. Section 7.5 Dynamic Loading – Updated condition E in Table 7 6 Additional transient load requirements. Section 7.13.2 Main Output Voltage Regulation Droop – Updated output voltage factory setting to 12.2V +- 30mV. Section 7.15 Timing Requirements – Updated Tpwok_on in Table 7 13 Timing requirements. Section 8.1.3.1 Over Current Warning Level 1 (OCWPL1) – Updated section title and updated references of OCW1 to OCWPL1. Section 8.1.3.2 Over Current Warning Level 2 (OCWPL2) - Updated section title, updated references of OCW2 to OCWPL2 and updated the averaging window from 50ms to 10ms. Section 8.1.3.3 Over Current Warning Level 3 (OCWPL3) - Updated section title and updated references of OCW3 to OCWPL3. Section 8.1.3.3 Over Current Warning Level 3 (OCWPL3) – Updated threshold for OCWPL4 and averaging window range for OCWPL1 in Table 8 2 OCW Thresholds. Section 9.5 Imon Signal (Output) – Fixed typo in % Base Tolerance and % Read Tolerance Section 12.1.45 MFR_LINE_STATUS (E1h) – Renamed to fix the command number, before was E0h. Section 12.1.46 MFR_SYSTEM_LED_CNTL (E2h) – Renamed to fix the command number, before was E1h. Section 12.1.45.1.2 Pre-Set – Updated MFR_LINE_STAUS command number from E0h to E1h and fixed typo in the name of the command. Section 12.1.45.4 Flow Charts – Updated Figure 12 15 MFR_LINE_STATUS Main page flow diagram and Figure 12 18 MFR_LINE_STATUS Notify task flow diagram. Section 12.1.56 Summary of PMBus commands – Fixed duplicated command numbers in Table 12 28 Summary of PMBus commands. Section 12.4.2 Cold Standby Power Supply Operating State – Removed voltage setting of the output capacitor. Section 12.7.1 Physical Layer – Added note 4 in Figure 12 32 Physical layer and connections for point-to-point communication between Host and Client and fixed typos in notes 1, 2 & 3. Section 13.1 Component De-Rating – Updated life expectancy of E-Caps in Table 13 1 Component de-rating guidelines. Section 13.2 Life Requirement – Updated life requirements. Section R.3 Over Current Warning 3 (OCW3) – Updated Figure R-12. OCW3 Timing (Default Setting). Section 12.8.6 Configuration File Creation – Added Figure 12 47 MCU memory map example. Supplemental Material A – Updated drawing. Supplemental Material B – Updated drawing. Supplemental Material C – Updated drawing. Supplemental Material D – Updated drawing. Supplemental Material E – Updated drawing. Supplemental Material F – Updated drawing. Supplemental Material G – Updated drawing. Supplemental Material J – Updated drawing. Supplemental Material K – Updated drawing. Supplemental Material L – Updated drawing. Supplemental Material S – New section with the C22 connector mechanical drawing.
August 28th, 2023	1.02 RC2	Section 7.1 Output Power/Currents – Added clarification in the note 3 about the duration of the burst on Table 7 1 Load requirements. Section 7.5 Dynamic Loading – Added note 2 in Table 7 6 Additional transient load requirements.

		Section 7.5 Dynamic Loading – Changed from 3,300uF to 4,400uF test capacitive load for 70% step load size in Table 7 5 Transient load requirements. Supplemental Material P – Removed one thermal sensor in Figure O-2. Thermocouple locations for the 185mm by 60mm form factor.
December 15th, 2023	1.03 RC2	*Section 12.1.46 MFR_SYSTEM_LED_CNTL (E2h)* – Fixed typo, MFR_SYSTEM_LED_CNTL is command number E2h in *Table 12-22*. *Section 12.1.45.1.2 Pre-Set* – Fixed typos. *Section 12.1.45.1.1 Initial Line* – Fixed typo command E1h instead of E0h. *Section 12.1.45.3 12.1.45.3* – Added bit 6 PSU mismatch in *Table 12-19 MFR_LINE_STATUS* definition. *Section 12.1.59 Summary of PMBus commands* – Updated *Table 12-38 Summary of PMBus commands*: - Added the word Exhaust to command 8Fh READ_TEMPERATURE_3. - Added bit 2 High line power derated in command 80h STATUS_MFR_SPECIFIC. - Added "see note 1" legend to commands 5Dh IIN_OC_WARN_LIMIT, 46h IOUT_OC_FAULT_LIMIT, 4Ah IOUT_OC_WARN_LIMIT, . - Removed commands 11h, 12h, 15h, 16h, 20h through 2Ah, 38h, 39h, - Added bits VOUT_OV_WARNING and VOUT_UV_WARNING in STATUS_VOUT command. - Added bits VIN_OV_FAULT & VIN_OV_WARNING in STATUS_VIN command. *Section 2.3 LED Marking and Identification* – Rewritten paragraph that specifies the number of LEDs in the illuminated handle. *Section 3.1 Temperature and Altitude Conditions* – Updated in *Table 3-1 Power supply thermal test conditions*: - Added Note 1 to Tier level 1. - Added Note 1 to Tier level 2. *Section 3.4 Fan Speed Control* – Added note, 20% fan speed maximum when main rail is OFF. *Section 5.1.3 Input Voltage Specification* – Updates to Table 5-3 AC Input voltage ranges: - Updated start up voltage for wide range voltage from 89VAC to 90VAC. - Updated note 2 added 5Vrms hysteresis. *Section 6.1.1.1 240VAC/240VDC and Wide Input Range* – Updated Note 1 in *Table 6-1*, added including and excluding fan power. *Section 6.1.1.2 277VAC/380VDC Input* – Updated Note 3 – *Table 6-2*, added Including and excluding fan power. *Section 6.1.2.2 -48VDC Input (Telecom)* – Updated *Table 6-4 Efficiency requirements for -48VDC (Telecom) input power supplies* and added note 3. *Section 7.10 Soft Starting* – Added statement about all capacitive loading conditions for monotonic rise. *Section 7.13.8 Maximum Power Rating with Parallel PSUs* – Fixed typo from Table to Figure in *Table 7-10*. *Section 9.5* Imon Signal (Output) – Added Note 6 in *Figure 9-7 Imon block diagram concept*. *Section 9.8* Pin Ripple/Noise and Capacitance – Added Note 2 to Table 9-13 Pin capacitance summary. *Section 5.1.1* Power Factor and iTHD – Updated Table 5-2 iTHD requirements, added Note 6, and added a plot based on *Table 5-2*. *Section 12.5.7* Power Supply Commands – Updated bit 5 description in Table 12-55 MFR_FWUPLOAD_STATUS command format. *Section 12.5.7* Power Supply Commands – Added byte 5 Bootloader revision in Table 12-56 MFR_FW_REVISION command format. *Section 12.8.3.1 LED Behavior Configuration Block* – Added OVPsb and UVPsb events in*Table 12-67 Power supply event table*. *Section Supplemental Material Q. Additional Requirements on Input Line Transients* – Added Tpwok_holdup in all T6 references and added *missing Figure P-6. Input current averaging windows and timers* with its notes. T1 changed from 200ms to 1000ms *Section 8.1.4.1 Constant Current During Start Up into Overcurrent Condition* – Updated references of OCW1, OCW2 and OCW3 to OCWPL1, OCWPL2 and OCWPL3. *Section 7.3 Auxiliary (Stand-by) Output* - Added note 6 to *Figure 7-2 Typical 12VSB droop share characteristics*. *Section 7.15 Timing Requirements* – Updated *Table 7-13 Timing requirements*: - Maximum Tpwok_holdup. - Tvinok_off for AC/DC input power supplies min. 1000us to max. 4000us. - Added note 5 *Section 11.2.1 Data Format* – Added efficiency level in *Table 11-2 M-CRPS FRU MultiRecord definition*.

		Section *12.1.45.4 Flow Charts* – Updated: - *Figure 12-16 MFR_LINE_STATUS Initial line flow diagram*. - *Figure 12-18 MFR_LINE_STATUS Notify task flow diagram*. Section *12.7.8.3 GPIO + Analog IO Expander Profile* – Updated *Figure 12-49 Virtual wires plus analog channels exchange*. *Section 12.7.7 Command Set* – Added DSSI commands with checksum in *Table 12-62 Configuration commands set*: 81h, 90h, 91h, A0h. *Section 12.7.7 Command Set* – Added DSSI version fiends to *Table 12-63 M-CRPS Payload format*. Updated mechanical drawings: - *Supplemental Material F M-CRPS handle mechanical drawing*. - *Supplemental Material G M-CRPS latch mechanical drawing*. - *Supplemental Material B 185mm by 60mm M-CRPS mechanical drawing*. - *Supplemental Material L 185mm by 60mm -48VDC input M-CRPS mechanical drawing*. - *Supplemental Material R 185mm by 73.5mm M-CRPS Mechanical Drawing with C22 connector*. - *Supplemental Material J 185mm by 73.5mm +54VDC input M-CRPS mechanical drawing*. - *Supplemental Material K 185mm by 73.5mm -48VDC input M-CRPS mechanical drawing*. - Added thermal sleeves for: - 73.5mm by 185mm form factor - 73.5mm by 265mm form factor - 60mm by 185mm form factor - Plate for 73.5mm width - Plate for 60mm width *Section Supplemental Material S -48VDC Earth ground ring terminal* – New Section. *Section Supplemental Material T -48VDC Earth ground screw* – New Section. *Section 7.16 PWOK Signal Timing Requirements* – Updated note in *Figure 7-9 Configurable PWOK warning time timing diagram for High voltage power supplies*. Section 3.5 Additional Thermal and Airflow Characterization: - Updated *Table 3-2 Airflow requirement for thermal compliance for inlet temperature at different PSU load conditions*, added 65degC and 70degC test conditions and added Note 1. - Added note at the beginning of the subsection to have a thermal sleeve as requirement for all tests. *Section 3.1 Temperature and Altitude Conditions*: - Removed Note 1 from Max. exhaust temperature except for 90degC in *Table 3-1 Power supply thermal test conditions*. - Updated note 1 in *Table 3-1*. - Added note 4 in *Table 3-1*. - Added note 5 in *Table 3-1*. - Added note 6 in *Table 3-1*. *Section 8.1.4 Over Current Protection & Over Power Protection (OCP & OPP)* – Updated Figure 8-6 PSU Output Current vs. Time. *Section 8.1.4.1 Constant Current During Start Up into Overcurrent Condition* – Updated Figure 8-7 PSU Start up into Over Current Condition. *Section 7.15 Timing Requirements* – In *Table 7-13 Timing requirements*: - Updated note 1, default values for Tpwok_holdup and Tpwok_off. - Updated note 5. *Section 12.8.3 Configuration Area Definition* - Added Tvinok_off parameter to *Table 12-73 Power supply timing configuration*. *Section 9.1* PSON# Signal (Input) – Updated title of Figure 9-1. *Section 9.1* PSON# Signal (Input) – Updated *Figure 9-1 Required PSON# input signal circuit for two/multi-state operation*, and updated Note 1. *Section 9.1.2 Three-state Signal* – Section renamed to *9.1.2 Multi-State Signal*. *Section renamed to 9.1.2* Multi-State Signal – Updated title. *Section 9.5* Imon Signal (Output) – Updated Note 5 in Figure 9-7, logic states low and high were swapped for GPO2. *Section 12.4.5* Cold Redundancy SMBus Commands – Updated *Table 12-45 COLD_REDUNDANCY_CONFIG (D0h) values*. *Section 12.4.7* Cold Redundancy Bus (CR_BUS) – Updated Table 12-46 CR_BUS state table.

		Section 12.4.9 Power Supply Turn ON Function – Added Note 1 to *Figure 12-29 Power ON/OFF example of power supplies in Cold Redundant mode (4x750W PSUs)*. *Section 12.8.3.10 Miscellaneous Configuration Block* – In *Table 12-75 Miscellaneous configuration block*: - Fixed typo in Use1BitPMBusAddressing bit. - Added Enable/Disable thresholds for up to 15 Cold Redundant M-CRPS. - Renamed bit 2 from register 001Ah as SetA1BehaviorForDSSIActive, to select when to bias the DSSI bus in pin A1. - Updated name of bit 1 on register 0004h to Multi-StatePSON. *Section 12.5.5 Firmware Image Header* – Added Test FW revision field to *Table 12-50 PSU FW Image header*. *Section 12.5.7 Power Supply Commands* – Added Test FW revision to *Table 12-56 MFR_FW_REVISION command format*. *Section 12.8.3.1 LED Behavior Configuration Block* – Added the following events to *Table 12-67 Power supply event table*: - MainOutputONStbyON - MainOutputOFFStbyON - MainOutputOFFStbyOFF - ColdRedundantEnabled - AlwaysColdRedundantEnabled *Section Supplemental Material P Exhaust Temperature Measurement* – Added note about thermal sleeve requirement for all measurements. *Section 7.1* Output Power/Currents – In Table 7-1 Load requirements: - Updated Note 2 added: PL2 level support shall be 115% of the maximum output rating at any given input voltage and change dynamically based on the declared input voltage ranges. - Updated Note 3 added: PL3 level support shall be 155% of the maximum rating using the highest voltage of low and high line as reference. - Updated Note 7 added: PL4 level support shall be 165% of the maximum rating using the highest voltage of low and high line as reference. *Section 7.16* PWOK Signal Timing Requirements – Updated Note 1 in *Figure 7-9 Configurable PWOK warning time timing diagram for High voltage power supplies*. *Section 7.3 Auxiliary (Stand-by) Output* – Added Note 7 in *Figure 7-2 Typical 12VSB droop share characteristics*. *Section 8.1.1 Current sense* – Updated *Figure 8-1 Main output current sense block diagram* and Note 1: changed 12V Main Output to Main Output. *Section 8.1.2 Averaging Mechanism* – Updated: - *Figure 8-2* and title. - *Figure 8-3* and title and updated Notes 1& 2. *Section 12.1.60 Summary of PMBus Telemetry Accuracies* – New section. *Section 12.7.5 Interface Initialization* – Updated: - Step by step configuration flow. - *Figure 12-38 DSSI Flow diagram*. - *Added Figure 12-39 Default DSS transition to active sequence (SetA1BehaviorForDSSIActive = 0)*. - *Added Figure 12-40 Alternative DSSI transition to active sequence (SetA1BehaviorForDSSIActive = 1)*. *Section 9.6.1 A0 Input Addressing* – Added Note 3 in *Figure 9-10 Flow diagram to detect between logic and analog SMBus addressing*. *Section 9.1.2 Multi-State Signal* – Updated *Figure 9-3* and changed name. *Section 9.1.2 Multi-State Signal* – Added *Table 9-2 Multi-state PSON# voltage ranges definition*. *Section 6.1.1.1 240VAC/240VDC and Wide Input Range* – Added Note 2 in *Table 6-1 Efficiency requirements for 240VAC/240VDC and wide input range power supplies*. *Section 6.1.1.2 277VAC/380VDC Input* – Added Note 4 in *Table 6-2 Efficiency requirements for 277VAC/380VDC power supplies*. *Section 6.1.2.1 +54VDC Input*– Added note 3 in *Table 6-3 Efficiency requirements for +54VDC input power supplies*. *Section 6.1.2.2 -48VDC Input (Telecom)* – Added *Note 4 in Table 6-4 Efficiency requirements for -48VDC (Telecom) input power supplies*.

February 2nd, 2024	1.04 RC1	*Section 9.1 PSON# Signal (Input)* - Updates:
		- In *Table 9-2 Multi-state PSON# voltage ranges definition*:
		  o Added '<' sign to column Max of detect PSON# voltage.
		  o Divided M-CRPS Main output column in Main and 12VSB for 12V & 54V M-CRPS.

		○ Swapped the rows to have the voltages from high (top) to low (bottom). ○ Fixed reference in both Main output columns. ○ Added note 1. *Section 9.1.2 Multi-State Signal* - Updated paragraph to include description for Multi-State PSON# signal. *Section 9.1.2.1 Full Power Cycle* - Added new section. Section 12.1.56 MFR_FPC_MAIN_MIN_OFF_TIME - Added new section. *Section 12.1.57 MFR_FPC_12VSB_MIN_OFF_TIME* - Added new section. *section 12.1.59 Summary of PMBus commands* – Updates: - Added commands MFR_FPC_MAIN_MIN_OFF_TIME and MFR_FPC_12VSB_MIN_OFF_TIME. - Updated command 51h to Read/Write. - Updated command 5Dh to Read/Write. - Updated description of bit 2 in command 80h. - Updated command D9h length to 7 bytes. *Section 12.8.3.10 Miscellaneous Configuration Block* - Added VMainDischargeMax, VsbDischargeMax, FPCMainMinOFFTime, FPCVsbMinOFFTime registers in *Table 12-75 Miscellaneous configuration block* and corrected duplicated fields ColdStandby5Enable and ColdStandby5Disable. *Section 12.7.7* Command Set - Updated Table 12-62 Configuration commands set, added responses: OK, Not supported, can't execute and Checksum error to commands 40h through 7Fh. updated description of command 7Eh. *Section 7.5* Dynamic Loading - Added note 2 to 70% of max load step size in Table 7-5 Transient load requirements. *Section 7.15* Timing Requirements - Added Note 6 and 7, and fixed typo in Note 1 on Table 7-13 Timing requirements, updated Tpson_pwok and divided in two Tpwok_off input lost driven and PSON# deassertion driven behaviors. *Section 12.7.5* Interface Initialization - Updated Figure 12-38 DSSI Flow diagram. *Section 12.1.45.4* Flow Charts - Replaced *Figure 12-17a MFR_LINE_STATUS Preset flow diagram (AC Low Line)* with Figures 12-17a, 12-17b, 12-17c and 12-17d. *Section 12.1.46* MFR_SYSTEM_LED_CNTL (E2h) - Corrected typo E2h instead of E1h in paragraph and added Note 2 in *Table 12-22 MFR_SYSTEM_LED_CNTL (E2h) command bitfield definition*. *Section 12.5.4 Power Supply Operating Mode During and After Firmware Update* - Made live FW update mandatory. *Section 12.5.2 Summary of Commands & Capabilities Supported in Bootloader Mode* – Corrected typo command D9h is now 7 bytes long. *Section 3.1* Temperature and Altitude Conditions - Updated notes and added note 7 in Table 3-1 Power supply thermal test conditions. *Section 5.1.1* Power Factor and iTHD - Updated Table 5-2 iTHD requirements and Table 5-1 Power factor requirements. *Section 5.1.7.1* Cold Start Inrush Current With PSON# asserted - Added Notes 1 and 2 in Figure 5-4 I vs T profile of the PSU input current. *Section 7.1* Output Power/Currents - Updated input voltage range for wide input type in Table 7-1 Load requirements. *Section 7.4 Voltage Regulation* - Added Notes 4, 5 and 6 to Table 7-4 Voltage regulation limits, and updated 12V main output voltage regulation limits. *Section 7.3* Auxiliary (Stand-by) Output - Updated Note 7 in Table 7-2 Peak load protection testing conditions. *Section 7.5* Dynamic Loading - Updated upper regulation limit for 12V output at 70% of max. load step and added note 3 to profile D in Table 7-6 Additional transient load requirements. *Section 7.13.2* Main Output Voltage Regulation Droop - Updated voltage droop from 1.111mV/1% load to 2.222mV/1% load. *Section 7.13.3* Current Sharing Load Step Response - Updated timing from 5ms to 10ms. *Section 7.16 PWOK Signal Timing Requirements* - Updated Note 1 in Figure 7-9 Configurable PWOK warning time timing diagram for High voltage power supplies. *Section 8.1.6* Over Voltage Protection (OVP) - Updated Table 8-4 Over Voltage Protection (OVP) Limits. *Section 8.1.2* Averaging Mechanism - Updated Figure 8-2 OCWPL1 average window logic. *Section 8.1.3.2* Over Current Warning Level 3 (OCWPL3) - updated section name and paragraph. *Section 8.1.3.3 Over Current Warning Level 4 (OCWPL4)* - updated section name and paragraph, and updated Table 8-1 OCWPL4 Timings name and labels. *Section 8.1.4.1 Constant Current During Start Up into Overcurrent Condition* - Updated paragraph.

		Section 8.1.4 Over Current Protection & Over Power Protection (OCP & OPP) - Updated *Figure 8-6 PSU Output Current vs. Time* arrow pointing to constant current threshold. *Section 9.1 PSON# Signal (Input)* - Updated *Figure 9-1 Required PSON# input signal circuit for two/multi-state operation*, changed 0ohm resistor to 100ohm. *Section 9.5 Imon Signal (Output)* - Added Note 5 in *Table 9-7 Imon signal characteristics*. *Section 9.8 Pin Ripple*/Noise and Capacitance - Added Imon signal and Notes 3 and 4 in *Table 9-13 Pin capacitance summary*. *Section 12.1.20 Status Commands* - Added bits VOUT_OV_WARNING, VOUT_UV_WARNING, VIN_OV_FAULT and VIN_OV_WARNING in *Table 12-12 PMBus STATUS commands summary*. *Section 12.1.45.3 Extended High Line AC/High Line DC Mixed-mode PSU* - Updated Note 2 bit-2 to bit-4 in *Table 12-19 MFR_LINE_STATUS definition*. *Supplemental Material T. -48VDC Earth ground screw* - Updated drawing. *Supplemental Material F. M-CRPS handle mechanical drawing* - Updated drawing. *Supplemental Material A. 185mm by 73.5mm M-CRPS mechanical drawing* - Updated drawing. *Supplemental Material B. 185mm by 60mm M-CRPS mechanical drawing* - Updated drawing. *Supplemental Material C. 265mm by 73.5mm M-CRPS mechanical drawing* - Updated drawing. *Supplemental Material J. 185mm by 73.5mm +54VDC input M-CRPS mechanical drawing* - Updated drawing. *Supplemental Material K. 185mm by 73.5mm -48VDC input M-CRPS mechanical drawing* - Updated drawing. *Supplemental Material L. 185mm by 60mm -48VDC input M-CRPS mechanical drawing* - Updated drawing. *Supplemental Material R. 185mm by 73.5mm M-CRPS Mechanical Drawing with C22 connector* - Updated drawing. Fixed typos in different sections.
February 14th 2024	1.04 RC2	*Section 12.1.45.3 Extended High Line AC/High Line DC Mixed-mode PSU* - Updated bit 6 from Read to Read/Write in *Table 12-19 MFR_LINE_STATUS definition*. *Section 13.1 Component De-Rating* - Updated ripple current de-rating for high voltage bulk capacitors in *Table 13-1 Component de-rating guidelines*. *Section 8.1.4 Over Current Protection & Over Power Protection (OCP & OPP)* - Updated *Figure 8-6 PSU Output Current vs. Time*. *Section 5.1.5.1 Main output* - Updated *Table 5-5 AC/DC, 240VDC and* HVDC holdup / dropout. *Section 7.1 Output Power/Currents* – Updated 12Vmain (wide input rage) in *Table 7-1 Load requirements*. *Section 7.1 Output Power/Currents* - Updated *Figure 7-1 PSU Peak power timing example*. *Section 7.4 Voltage Regulation* - Updated Note 1 in *Table 7-4 Voltage regulation limits*. *Section 7.5 Dynamic Loading* - Added Note 6 in *Table 7-5 Transient load requirements* and updated 70% loading condition regulation limits. *Section 7.13.2 Main Output Voltage Regulation Droop* - Updated from 100mV to 200mV voltage droop. *Section 7.13.3 Current Sharing Load Step Response* - Updated from 20% current deviation from the ideal value to 50%. *Section 7.15 Timing Requirements* - Updated Note 7 in *Table 7-13 Timing requirements*. *Section 7.16 PWOK Signal Timing Requirements* - Updated Note 1 in *Figure 7-9 Configurable PWOK warning time timing diagram for High voltage power supplies*. *Section 12.8.3.8 Latch on Fault Condition Configuration Block* - Added ClearFaultsWithPSONCycle in *Table 12-74 Power supply latch on fault condition configuration block*. *Section 8 Protection Circuits* - Updated paragraph to include the option for faults reset using PSON# cycle. *Section 8.1.2 Averaging Mechanism* - Updated Note 1 in *Figure 8-2 OCWPL1 average window logic*. *Section 8.1.3.3 Over Current Warning Level 4 (OCWPL4)* - Updated Note 1 in *Table 8-2 OCW Thresholds*. *Section 8.1.3.2 Over Current Warning Level 3 (OCWPL3)* - Corrected typo in the section name. *Section 8.1.3.3 Over Current Warning Level 4 (OCWPL4)* - Corrected typo in the section name. *Section 8.1.3.3 Over Current Warning Level 4 (OCWPL4)* - Updated last row of *Table 8-1 OCWPL4 Timings, and updated Figure 8-4 PSU Output Current – Slew Rate Measurement*. *Section 9.8 Pin Ripple*/Noise and Capacitance - Updated Imon maximum noise level in *Table 9-13 Pin capacitance summary*. *Section 14.3 Safety Requirements and Standards* - Added Note 2 to this section. *Supplemental Material B 185mm by 60mm M-CRPS mechanical drawing* - Updated drawing. *Supplemental Material L 185mm by 60mm -48VDC input M-CRPS mechanical drawing* - Updated drawing.

		Supplemental Material A 185mm by 73.5mm M-CRPS mechanical drawing - Updated drawing. *Supplemental Material R 185mm by 73.5mm M-CRPS Mechanical Drawing with C22 connector* - Updated drawing. *Supplemental Material J 185mm by 73.5mm +54VDC input M-CRPS mechanical drawing* - Updated drawing. *Supplemental Material K 185mm by 73.5mm -48VDC input M-CRPS mechanical drawing*- Updated drawing. *Supplemental Material C 265mm by 73.5mm M-CRPS mechanical drawing* - Updated drawing.
February 22nd 2024	1.04 RC3	Updated typo in a dimension in the following mechanical drawings. - *Supplemental Material B 185mm by 60mm M-CRPS mechanical drawing* - Updated drawing. - *Supplemental Material L 185mm by 60mm -48VDC input M-CRPS mechanical drawing* - Updated drawing. - *Supplemental Material A 185mm by 73.5mm M-CRPS mechanical drawing* - Updated drawing. - *Supplemental Material R 185mm by 73.5mm M-CRPS Mechanical Drawing with C22 connector* - Updated drawing. - *Supplemental Material J 185mm by 73.5mm +54VDC input M-CRPS mechanical drawing* - Updated drawing. - *Supplemental Material K 185mm by 73.5mm -48VDC input M-CRPS mechanical drawing* - Updated drawing. - *Supplemental Material C 265mm by 73.5mm M-CRPS mechanical drawing* - Updated drawing.
June 20th 2024	1.05 RC1	*Section 12.5.6 Firmware Update Process* - Updated *Figure 12-33 FW update process*, added Bulk erase time and signature verification. *Section 12.5.5 Firmware Image Header* - Updated *Table 12-50 PSU FW Image header*, added Bulk erase time byte. *Section 13.4 Reliability Demonstration Test* - Updated paragraph, sample size to 100, test duration to 64 days, added 277VAC and 336VDC input voltages and added accelerated factor equation. *Section 5.1.9 Line Transient Specification* - Updated *Figure 5-9 100VAC/200VAC input brown-out behavior* and added figures for: - 200VAC/277VAC input brown-out behavior - 277VAC input brown-out behavior - 240VDC (192VDC - 288VDC) China Telecom DC input range - 260VDC - 400VDC ETSI DC input range - Updated *Table 5-6 AC Line Surge Transient Performance* and added Note 2. *Section 12.1.51 MFR_PEAK_CURRENT_RECORD (E9h)* - changed "Only CLEAR_HISTORY can..." to "Only MFR_CLEAR_BLACKBOX can...". *Section 7.15 Timing Requirements* – Updated *Table 7-13 Timing requirements*: - Updated Tsb_on_delay to 3000ms. - Updated Tac_on_delay to 5000ms. - Updated note 6 from 2% load to 100% load. - Updated note 4. - Added Note 8. *Section 12.1.45.3 Extended High Line AC/High Line DC Mixed-mode PSU* - Added Note 5 to *Table 12-19 MFR_LINE_STATUS definition*. *Section 12.1.45.3 Extended High Line AC/High Line DC Mixed-mode PSU* – Corrected typo in *Table 12-20 Power input line type definition*, AC Input High Line AC 240VAC instead of 240VDC. *Section 12.1.50 MFR_EFFICIENCY_DATA (B3h)* – Added note 1 efficiency measured included fan power and deleted bytes 25 to 44 in *Table 12-24 Efficiency data definition*. *Section 12.1.55 MFR_OCWPL1_SETTING (EEh)* - Command updated from Block Write only to Block Read / Block Read. *Section 12.1.55 MFR_OCWPL1_SETTING (EEh)* - Updated Exponent from 0 to 6 in Average window length field of *Table 12-27 MFR_OCWPL1_SETTING command bit field definition*. *Section 12.1.56 MFR_FPC_MAIN_MIN_OFF_TIME* - Corrected typo in Table 12-28 MFR_FPC_MAIN_MIN_OFF_TIME command valid range. *Section 12.1.57 MFR_FPC_12VSB_MIN_OFF_TIME* - Corrected typo in Table 12-29 MFR_FPC_12VSB_MIN_OFF_TIME command valid range. *Section 12.1.59 Summary of PMBus commands* - Added response length in commands 99h, 9Ah, 9Bh, 9Ch, 9Dh and 9Eh in *Table 12-38 Summary of PMBus commands*. *Section 12.4.5 Cold Redundancy SMBus Commands*- Removed Cold Standby 6 through 15 fields in *Table 12-45 COLD_REDUNDANCY_CONFIG (D0h) values*. *Section 12.5.2 Summary of Commands & Capabilities Supported in Bootloader Mode* - Added Note 1 & 2 in Table *12-49 Supported commands during FW upload* mode.

		Section 12.5.5 Firmware Image Header - Added byte 62 Option in *Table 12-50 PSU FW Image header*. *Section 12.7.7 Command Set*- Updated commands 81h, 90h and 91 in *Table 12-62 Configuration commands set*. *Section 12.8.3.10 Miscellaneous Configuration Block* - Changed bit 4 of register 001Ah from DisableRemoteSense to DisablePSKILL in *Table 12-75 Miscellaneous configuration block*. Section 14.3 Safety Requirements and Standards - Updated Note 2 in Figure 14-1 Multiple input sources IEC 60417-6172 symbol. *Supplemental Material Q. Additional Requirements on Input Line Transients* - Updated Note 3 timing form 1000ms to 200ms in *Figure P-5. Repetitive line disturbance*. *Section 3.1 Temperature and Altitude Conditions* - Updated paragraph about air temperature rise to point to Table 3-1 Power supply thermal test conditions. *Section 4.1.7.3 Constant Fan Speed* - Added new table for General Purpose & Storage PSU's. *Section 4.1.9 Acoustical Requirements* - Updated *Table 4-5 General Data Center & Storage PSU Acoustical Requirements*. *Section 5.1.5.1 Main output* - Updated table name *Table 5-5 AC/DC, 240VDC and HVDC holdup / dropout*. *Section 7.1 Output Power/Currents* - Updated Note 3 in *Table 7-1 Load requirements*. *Section 7.4 Voltage Regulation* - Updated Note 1 in *Table 7-4 Voltage regulation limits*. *Section 7.13.3 Current Sharing Load Step Response* - Updated paragraph. *Section 8.1.2 Averaging Mechanism* - added Note 1 in *Figure 8-2 OCWPL1 average window logic* and removed Note 1 in *Figure 8-3 OCWPL3 average window logic*. *Section 8.1.3.2 Over Current Warning Level 3 (OCWPL3)* - Fixed typos 10ms to 15ms OCWPL2 to OCWPL3. *Section 8.1.3.3 Over Current Warning Level 4 (OCWPL4)* - Fixed typos in *Table 8-1 OCWPL4 Timings* and updated *Figure 8-4 PSU Output Current – Slew Rate Measurement* and updated *Figure 8-5 SMBAlert# flow*. *Section 9.8 Pin Ripple/Noise and Capacitance* – Updated *Table 9-13 Pin capacitance summary* and notes and updated section name. *Section 8.1.4.1 Constant Current During Start Up into Overcurrent Condition* - Updated *Figure 8-7 PSU Start up into Over Current Condition*. *Section 8.1.4 Over Current Protection & Over Power Protection (OCP & OPP)* – Updated *Figure 8-6 PSU Output Current vs. Time*. *Section 9.5 Imon Signal (Output)* – Updated *Table 9-7 Imon signal characteristics* and Note 2, added Note 7. *Section 9.5 Imon Signal (Output)* – Added *Figure 9-9 Imon signal delay step response*. *Section 7.5 Dynamic Loading* – Updated regulation limits for 12V output power supplies in *Table 7-5 Transient load requirements* and added Note 4. *Section 7.3 Auxiliary (Stand-by) Output* – Updated *Figure 7-2 Typical 12VSB droop share characteristics (center green line), and worst case (top orange and bottom yellow lines).* And added Note 7.
June 27th 2024	1.05 RC2	Removed Supplemental Material R and renamed the sections after this one. *Section 12.5.6 Firmware Update Process* – Added path for MCUs with dual images capability and for M-CRPS that need PSON# cycle to run the new image in *Figure 12-33 FW update process*. *Section 9.1.2 Multi-State Signal* – Updated logic low max voltage for PSON# detection and system setting in *Table 9-2 Multi-state PSON# voltage ranges definition*. *Section 9.1.2.1 Full Power Cycle* – Updated *Figure 9-4 Multi-State PSON# signal state diagram*, updated Note 1 and added Note 2. *Section 9.1.2.1 Full Power Cycle* – Updated $T_{debounce}$ = 5ms in Figure 9-5 Full Power Cycle timing diagram *Section 3.1 Temperature and Altitude Conditions* – Updated note 6 in *Table 3-1 Power supply thermal test conditions*. *Section 9.1 PSON# Signal (Input)* – Updated *Figure 9-1 Required PSON# input signal circuit for two/multi-state operation*. *Section 5.1.5.1 Main output* – Updated *Table 5-5 AC/DC, 240VDC and HVDC holdup / dropout.* *Section 11.1 FRU Data* – Split byte 15 to add a bit that indicates the M-CRPS output can be derated if the input voltage is insufficient to support full power in *Table 11-2 M-CRPS FRU MultiRecord definition*. *Section 12.1.43 MFR_MAX_IOUT_CAPABILITY (F1h)* – Added not 3 in *Table 12-17 MFR_MAX_IOUT_CAPABILITY ccommand*. *Section 7.1 Output Power/Currents* – Updated PL4 total peak time in *Table 7-1 Load requirements*. *Section 7.1 Output Power/Currents* – Updated PL4 in *Figure 7-1 PSU Peak power timing example*.

		Section 12.7.7 Command Set – Command 43h changed to reserved in *Table 12-62 Configuration commands set*. *Section 7.1 Output Power/Currents* – Updated Note 1 in *Table 7-1 Load requirements*, to be clearer. *Section 12.8.3.10 Miscellaneous Configuration Block* - Removed ColdStandby6Enable/Disable through ColdStandby15Enable/Disable in *Table 12-75 Miscellaneous configuration block*. *Section 7.2 Peak Load Protection* – Updated *Table 7-2 Peak load protection testing conditions*. *Section 8.1.3.3 Over Current Warning Level 4 (OCWPL4)* – Updated OCWPL4 SMBAlert# assertion time post window average termination to 1.9ms in *Table 8-2 OCW Thresholds*. *Section 7.6 Capacitive Loading* – Updated minimum capacitance for 12Vmain in Table 7-7 Capacitive loading conditions and updated Note 1. *Section 7.5 Dynamic Loading* – Added Note 7 to *Table 7-5 Transient load requirements*. *Section 12.5.2 Summary of Commands & Capabilities Supported in Bootloader Mode* - Added PMBus commands from 78h through 81h *in Table 12-49 Supported commands during FW upload mode*. *Section 5.1.14 Surge Immunity* – Updated Note 2 and added Note 3 *in Table 5-8 Surge immunity requirements*.
August 27th 2024	1.05 RC3	*Section 7.13.1 Current Share (Ishare)* - Updated Ripple in *Table 7-9 Additional Requirements on current share behavior*. Updated from EN55024 to EN55035 in the document. *Section 4.1.9 Acoustical Requirements* - Updated Constant fan speed requirements in *Table 4-5 General Data Center & Storage PSU Acoustical Requirements*. *Section 12.5.7 Power Supply Commands* – Updated *Table 12-55 MFR_FWUPLOAD_STATUS command format*. *Section 5.1.6 Line Fuse* - Added IEC 60127 standard for the input fuse. *Section 5.3.6 Fuse* - Added IEC 60127 standard for the input fuse. *Section 14.3 Safety Requirements and Standards* - *Figure 14-1 Multiple input sources IEC 60417-6172 symbol* removed SELV in Note 2. Removed all references to 60950 standard in the document. *Section 12.5.2 Summary of Commands & Capabilities Supported in Bootloader Mode* - Added command E3h in *Table 12-49 Supported commands during FW upload mode*, and formatted table. *Section 12.5.7 Power Supply Commands* - Added description for command E3h MFR_FWUPLOAD_BLOCK_SIZE. *Section 12.1.59 Summary of PMBus commands* – Added commands E3h and E4h. MFR_FWUPLOAD_BLOCK_SIZE in *Table 12-38 Summary of PMBus commands*. Added *Section 12.1.58 Status Simulation Commands*. *Section 12.1.16 READ_EIN (86h)* - Corrected typo in *Table 12-8 READ_EIN requirements summary*. *Section 12.5.7 Power Supply Commands* – Added: - *Figure 12-35 MFR_FW_UPLOAD_STATUS PEC Error bit 7 assertion flow diagram*. - Bit 10 and 11 in Table 12-55 MFR_FWUPLOAD_STATUS command format. *Section 7.4 Voltage Regulation* – Corrected typo in Note 6 of *Table 7-4 Voltage regulation limits*. *Section 7.5 Dynamic Loading* – Updated 5th from top to bottom condition voltage limit in *Table 7-5 Transient load requirements*. *Section 12.7.7 Command Set* - Fixed typo in reply of command 45h in *Table 12-62 Configuration commands set*. *Section 12.7.5 Interface Initialization* – Added note *Figure 12-41 DSSI configuration flow diagram example*. *Section 12.7.6 Protocol* – Added calculation for communication refresh rate. *Section 12.7.6 Protocol* – Updated *Figure 12-42 Timing diagram for bi-directional DSSI protocol*. *Section 9.8 Pin Ripple/Noise and Capacitance* – in *Table 9-13 Pin capacitance summary*: - Added superscript 3 to Imon signal. - Added condition for Imon 0-2mA = 0-200% loading condition. *Section 12.5.5 Firmware Image Header* – Removed duplicated FW image verification block in *Figure 12-33 FW update process*. *Section 5.1.1 Power Factor and iTHD* – Corrected typo from 230VAC to 208VDC in 3rd row of *Table 5-2 iTHD requirements*. *Section 7.1 Output Power/Currents* - Updated PL4 peal ride through peak response ride through in *Table 7-1 Load requirements*. *Section 7.2 Peak Load Protection* - Change from <100us to <2ms. *Section 7.3 Auxiliary (Stand-by) Output*- Corrected reference to *Table 7-3 Output voltage droop characteristics* and updated Note 1 of *Figure 7-2 Typical 12VSB droop share characteristics (center green line), and worst case (top orange and bottom yellow lines)*.

		Section 7.4 Voltage Regulation - Updated 12VSB min/max in *Table 7-4 Voltage regulation limits*, and updated Note 1. *Section 7.5 Dynamic Loading* - Updated rows 4 and 5 of column Regulation limits and Note 2 5% minimum load per PSU in parallel in *Table 7-5 Transient load requirements*. *Section 7.13.1 Current Share (Ishare)* - Updated scale of Iout to Vimoni and Iout to Visharei. *Section 7.15 Timing Requirements* - Updated Tpwok_off note references of input lost condition and updating the maximum time of PSON# de-assertion based condition. *Section 7.16 PWOK Signal Timing Requirements* - Updated Note 1 of *Figure 7-9 Configurable PWOK warning time timing diagram for High voltage power supplies*. *Section 8.1.3.3 Over Current Warning Level 4 (OCWPL4)* - Updated Max. time for OCWPL4 total detect + report time in *Table 8-1 OCWPL4 Timings*. *Section 8.1.4 Over Current Protection & Over Power Protection (OCP & OPP)* - Updated *Figure 8-6 PSU Output Current vs. Time*. *Section 8.1.6 Over Voltage Protection (OVP)* - Updated 12VSB and +54V output ranges in *Table 8-4 Over Voltage Protection (OVP) Limits*. *Section 8.1.7 Under Voltage Protection (UVP)* - Fixed typo in *Table 8-5 Under Voltage Protection (UVP) Limits*. *Section 12.1.36 PSU Commands Supported For Testing Purposes* - Added reference to Section 12.1.58 Status simulation commands. *Section 12.4.7 Cold Redundancy Bus (CR_BUS)* - Updated pull-down resistor value in *Figure 12-28 CR_BUS signal circuit*. *Section 12.7.1 Physical Layer* - Updated Note 1 in *Figure 12-37 Physical layer and connections for point-to-point communication between Host and Client*. *Section 7.3 Auxiliary (Stand-by) Output* - Updated *Figure 7-2 Typical 12VSB droop share characteristics (center green line), and worst case (top orange and bottom yellow lines)*. *Section 13.7 Worst Case Electrical Parts Tolerance Analysis* - Updated last paragraph of this subsection. *Section 5.3.12 Isolation Requirements* - New section. *Section 7.13.1 Current Share (Ishare)* - Included reference about how to measure the delay between Iout to Vimoni and Iout to Visharei signals and clarified Vishare output accuracy at 16V = 200% loading condition. *Section 5.1.1 Power Factor and iTHD* – Updated iTHD at 0% loading condition in *Table 5-2 iTHD requirements* and updated *Figure 5-1 iTHD requirements* accordingly. *Section 1 Overview* – Added paragraph with the description of the M-CRPS being backwards compatible with the Legacy CRPS. *Section 2.4.2 277VAC/380VDC Input* – Added *Figure 2-18 277VAC/380VDC inlet connector from Anderson Power*. *Section 12.5.7 Power Supply Commands* - Command D8h MFR_FWUPLOAD_STATUS changed to Read Word / Write Word and added column in the bitfield table to highlight which bits can be cleared by the BMC/Host *Section 9.1.2.1 Full Power Cycle* – Updated *Figure 9-4 Multi-State PSON# signal state diagram*.
September 20th, 2024	1.05.00 RC4	*Section Supplemental Material P Exhaust Temperature Measurement* – Updated *Figure P-2 Thermocouple locations for the 185mm by 60mm form factor*. *Section Supplemental Material P Exhaust Temperature Measurement* – Added Note in the section. *Section 12.1.45.3 Extended High Line AC/High Line DC Mixed-mode PSU* - Corrected typo in the command number on *Table 12-19 MFR_LINE_STATUS definition*. *Section 12.1.59 Summary of PMBus commands* – Added bit 2 TON_MAX_FAULT to command 7Ah STATUS_VOUT in *Table 12-38 Summary of PMBus commands*. *Section 5.3.12 Isolation Requirements* – Isolation requirement between primary and secondary winding updated to 2121VDC. *Section 7.15 Timing Requirements* – Added Tsb_on_delay_active and Tac_on_delay_active in *Table 7-13 Timing requirements*. *Section 7.13.1 Current Share (Ishare)* – Updated signal delay Iout to Visharei to 1ms ±5% *Section 12.5.1 FW Image Mapping* – Added *Figure 12-31 Firmware image creation process flow* and *Figure 12-32 MFR_FWUPLOAD D7h command with PEC* with related text. *Supplemental Material B 185mm by 60mm M-CRPS mechanical drawing* – Updated drawings. *Supplemental Material L 185mm by 60mm -48VDC input M-CRPS mechanical drawing* – Updated drawings. *Supplemental Material A 185mm by 73.5mm M-CRPS mechanical drawing* - Updated drawings. *Supplemental Material R 185mm by 73.5mm M-CRPS Mechanical Drawing with C22 connector* – Updated drawings. *Supplemental Material J 185mm by 73.5mm +54VDC input M-CRPS mechanical drawing* – Updated drawings. *Supplemental Material K 185mm by 73.5mm -48VDC input M-CRPS mechanical drawing* – Updated drawings.

		Supplemental Material C 265mm by 73.5mm M-CRPS mechanical drawing – Updated drawings. *Supplemental Material T -48VDC Earth ground screw* – Updated drawing. *Supplemental Material Z 185mm by 73.5mm M-CRPS 277VAC input mechanical drawing* – New section. *Supplemental Material AA 185mm by 60mm M-CRPS 277VAC input mechanical drawing* – New section. *Section 12.8.3.10 Miscellaneous Configuration Block* – Added bit EnableStatusSimulationCmd in *Table 12-75 Miscellaneous configuration block*. *Section 12.1.58 Status Simulation Commands* – Added cross reference to Miscellaneous configuration block to enable the status simulation command. *Section 12.1.59 Summary of PMBus commands* - *Table 12-38 Summary of PMBus commands*: - IOUT_OC_FAULT_LIMIT (46h) command changed to read only. - MFR_FWUPLOAD_STATUS (D8h) command changed to read/write. *Section 5.1.2 Inlet Connector* – Added reference to DC-MHS connector list for 277VAC/380VDC input connector. *Section 12.7.7 Command Set* – Added command 43h Communication refresh rate and command 48h Command 44h execution delay in *Table 12-62 Configuration commands set*. *Supplemental Material P Exhaust Temperature Measurement* – Added *Figure P-4. Thermocouple locations to measure the surface temperature* and related text to measure the surface temperature. *Section 5.1.9 Line Transient Specification* – Added Note 3 in *Table 5-6 AC Line Surge Transient Performance*. *Section 12.5.7 Power Supply Commands* – Updated *Figure 12-35 MFR_FW_UPLOAD_STATUS PEC Error bit 7 assertion flow diagram* *Section 12.8.3.10 Miscellaneous Configuration Block* – Added SMBAlertPL4Behavior bit to register 001Ah in *Table 12-75 Miscellaneous configuration block*. *Section 7.1 Output Power/Currents* – Added note in *Figure 7-1 PSU Peak power timing example*. *Section 12.1.27 SMBAlert# Signal* – Updated TOC_Warning_latch and added Note 3 in *Table 12-14 PSU SMBAlert# timing requirements*. *Section 4.1.7 Operating Modes* – Updated *Table 4-3* name. *Section 12.5.5 Firmware Image Header* – added bitfield [7:4] of byte 62 in *Table 12-50 PSU FW Image header* and added Note 5.
September 25th 2024	1.05.00 RC5	*Section 12.5.7 Power Supply Commands* – Added bit 3 PSU supports MFR_FWUPLOAD_BLOCK_SIZE command in *Table 12-52 MFR_FWUPLOAD_CAPABILITY command format.* Fixed numeral sequence of the notes in the document.

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Acknowledgements

With the hope of making this specification useful for the entire OCP community, we acknowledge and appreciate the contributions, review, and feedback from various individuals and companies that participated in DC-MHS.

II. Scope

The present specification defines all the requirements for an M-CRPS internal redundant power supply used in Open Compute Project that could be used in different environments like home/office, datacenter, and high-performance computing, hence harmonizing the server power supply requirements used in the industry with the purpose of creating a standard specification that the customers and vendors of Enterprise and Hyperscale can use for their products.

Any supplier seeking OCP recognition for a hardware product based on this specification must be 100% compliant with any and all features or requirements described in this specification.

III. DC-MHS Family of Specifications

The **D**ata **C**enter – **M**odular **H**ardware **S**ystem (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-FLW** (**M**odular Hardware System **F**ul**L** **W**idth Specification) – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310-D Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-DNO** (**M**odular Hardware System Partial Width **D**e**n**sity **O**ptimized Specification) – Host Processor Module (HPM) specification targeted to partial width (i.e. ½ width or ¾ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310-D Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-CRPS** (**M**odular Hardware System **C**ommon **R**edundant **P**ower **S**upply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-PIC** (**M**odular Hardware System **P**latform **I**nfrastructure **C**onnectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-XIO** (**M**odular Hardware System E**x**tensible **I/O**) – Specifies the high-speed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as

PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.

- **M-PESTI** (**M**odular Hardware System **P**eripheral **S**ideband **T**unneling **I**nterface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (e.g., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.

Current Connector List – Vendor and part number information for all connectors referenced by DC-MHS specifications, updated as needed. Full URL:
https://docs.google.com/spreadsheets/d/1Vq_JxzZ43ysxBNHJ928vnzIcshA95GYGocaKmJCBC80/

To access additional DC-MHS specifications please visit the OCP Server Project Wiki – Working

IV. Specification Compliance Table (For System Designers Only)

The following compliance table is intended for system designers only to have compatibility with an M-CRPS power supply.

#	Technical Specification	Reference Section
1	Supported form factor outline.	*2.1 Form Factor Outline*
2	Compatible card edge receptacle connector with the proper pinout.	*2.6 Output Connector Interface*
3	Supported environment and thermal conditions.	*3 Thermal Requirements*
4	Capacitance loading within the specified range.	*7.6 Capacitive Loading*
5	Remote sensing connection at system side.	*9.7 Remote Sense And Return Sense / PSKILL*
6	Electrical interface connections and requirements needed at the system side.	*9 Control and Indicator Functions*
7	Signal connections between power supplies.	*12.4.1 Overview, Figure 12-27 Cold Redundancy 2+2 & 3+1 functional block diagram.*
8	An agent (for example BMC) with support for the specified firmware features: FRU, PMBus, FW update, Blackbox, Cold Redundancy, DSSI and Security.	*11 FRU Requirements* *12 Firmware Requirements*

1 Overview

The Modular Hardware System Common Redundant Power Supply (M-CRPS) Base Specification addresses multiple form factors that includes 185mm by 73.5mm (Length x width), 185mm by 60mm, and 265mm by 73.5mm all of them in 1U height and having different input connector types and voltage ranges like 240VAC/240VDC, 277VAC/380VDC, +54VDC for rack input power using a bus bar connector, and a -48VDC input for the Telecom industry. All the variations of the M-CRPS share the same electrical output interface.

Given the necessity of having some differentiation in the industry, the M-CRPS Base Specification can accommodate the preferences of different OEMs by choosing details like:

- LED blinking pattern
- latch finger grip color and design.
- Label artwork
- FRU content
- Packaging options

Along with the aforementioned customizations the M-CRPS introduces a new concept of Configuration File described in *Section 12.8*, with this feature the OEM can change the default configuration of most of the thresholds in the power supply and some of its signal timings as well as a new serial interface called Data & Sideband Serialization Interface (DSSI) described in *Section 12.8.3.10* with the purpose of be utilized as an I/O expander providing flexibility for the side-band signals of the M-CRPS, thus avoiding the need of changing the output connector in the future.

The M-CRPS as part of the DC-MHS project addresses the standardization of the server internal redundant power supply specification using the Intel Legacy CRPS as a starting point and creating an evolution with new features that will be useful for all the customers, the M-CRPS has been specified to be backwards compatible with systems using Legacy CRPS, the OxM or user of the M-CRPS is responsible for verifying such compatibility in their systems if they plan to use a M-CRPS in a system that uses Legacy CRPS.

2 Mechanical Overview

The physical sizes of the power supply enclosures are defined below. The power supply shall contain a fan for self-cooling. The power supply has a card edge output that interfaces with a high-power card edge connector in the system. The AC/DC plugs directly into the external face of the power supply. Refer to the following subsections for details.

2.1 Form Factor Outline

There are three main form factors addressed by this specification, they differ in width both sharing the same length and height: 185x73.5x40mm (LxWxH) and 185x60x40mm (LxWxH), and a third one having the following dimensions 265x73.5x40mm (LxWxH). *Figure 2-1* shows the 3D models of the three main form factors.

Figure 2-1 Form factors side by side (Front view), from left to right: 185mm by 73.5mm, 185mm by 60mm and 265mm by 73.5mm.

2.1.1 185mm by 73.5mm Form Factor

Figure 2-2 shows the outline for the 185mm by 73.5mm M-CRPS form factor, the power supply can support single or dual rotor fan depending on the application; single rotor fan is shown in the figure.

Figure 2-2 185mm by 73.5mm in width form factor outline

Note: Height of the power supply is 40mm in the fan area and 39mm on the rest of the case, for more details see *Supplemental Material A*

2.1.1.1 240VAC/240VDC Input

Figure 2-3 shows a front/rear isometric view of the 185mm by 73.5mm form factor using the C14 inlet connector. Same representation applies for the 265mm by 73.5mm form factor.

Figure 2-3 185mm by 73.5mm form factor with IEC320-C14 inlet connector as example

2.1.1.2 277VAC/380VDC Input

Figure 2-4 shows a front/rear isometric view of the 185mm by 73.5mm form factor using the 277VAC/380VDC inlet connector (refer to *Section 2.4.2 277VAC/380VDC Input* for more information). Same representation applies for the 265mm by 73.5mm form factor.

Figure 2-4 185mm by 73.5mm form factor with 277VAC/380VDC inlet connector

2.1.1.3 +54VDC Input (Rack Power Input)

Figure 2-5 shows a front/rear isometric view of the 185mm by 73.5mm form factor using the +54VDC Input Receptacle Connector for +54V input applications. Same representation applies for the 265mm by 73.5mm form factor.

Figure 2-5 185mm by 73.5mm form factor with bus bar connector input

Note: Refer to *Supplemental Material J* for detailed mechanical drawing.

2.1.1.4 -48VDC Input (Telecom)

Figure 2-6 shows a front/rear isometric view of the 185mm by 73.5mm form factor using the -48VDC Input Receptacle Connector (refer to *Section 2.4.4 -48VDC Input (Telecom)* for more information). Same representation applies for the 265mm by 73.5mm form factor.

Figure 2-6 185mm by 73.5mm form factor with -48VDC input connector

Note: Refer to *Supplemental Material* K for detailed mechanical drawing.

2.1.2 185mm by 60mm Form Factor

Figure 2-7 shows the outline for the 185mm by 60mm M-CRPS form factor, the power supply shall support single rotor fan.

Figure 2-7 60mm in Width form factor outline

Note: Height of the power supply is 40mm in the fan area and 39mm on the rest of the case, for more details see *Supplemental Material B*

2.1.2.1 240VAC/240VDC Input

Figure 2-8 shows a front/rear isometric view of the 185mm by 60mm form factor using the C14 inlet connector.

Figure 2-8 185mm by 60mm form factor with IEC320-C14 inlet connector as example

2.1.2.2 277VAC/380VDC Input

Figure 2-9 shows a front/rear isometric view of the 185mm by 60mm form factor using the 277VAC/380VDC inlet connector (refer to *Section 2.4.2 277VAC/380VDC Input* for more information).

Figure 2-9 185mm by 60mm form factor with 277VAC/380VDC inlet connector

2.1.2.3 +54VDC Input (Rack Power Input)

There is currently no +54V Input (Rack Power Input) type M-CRPS using the 185mm by 60mm form factor.

2.1.2.4 -48VDC Input (Telecom)

Figure 2-10 shows a front/rear isometric view of the 185mm by 60mm form factor using the -48VDC Input Receptacle Connector (refer to *Section 2.4.4 -48VDC Input (Telecom)* for more information).

Figure 2-10 60mm form factor with -48VDC input connector

2.2 Handle and Retention Latch

The power supply shall have a fixed water-clear polycarbonate illuminated handle to assist insertion and extraction, *Figure 2-12* shows the 3D representation of the handle. The operator shall be able to insert

and extract the power supply without the assistance of tools. The power supply shall have a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC/DC power cord is inserted into the power supply. The handle shall protect the operator from any burn hazard. The finger grip color and shape can be customized.

Figure 2-11 Retention latch example

Note: For details about the dimensions of the latch and finger grip options see *Supplemental Material G, Supplemental Material H,* and *Supplemental Material I*.

Figure 2-12 M-CRPS illuminated handle

Note: For details about the dimensions please see *Supplemental Material F.*

2.3 LED Marking and Identification

The power supply shall use a bicolor LED, Green & Amber. Below table shows the LED states for each power supply operating state and the LED's wavelength characteristics.

Table 2-1 LED Characteristics

	Nominal λd Wavelength	Luminosity (cd/m²)
Green	525 nm	500 ±100
Amber	590 nm	500 ±100

Notes:

1. For luminosity measurements please refer to *Supplemental Material N Luminosity Measurements*.

The handle shall be illuminated by LEDs mounted on a flex PCB in the rear that terminates to the control board in the front of the power supply as shown in *Figure 2-13* below.

Figure 2-13 Flex PCB with LEDs installed in a 185mm by 73.5mm form factor as example

LEDs shall be located at the end of the flex PCB as shown in *Figure 2-14* below; ither one bi color LED or two single color (green and amber) at the top bifurcation and either one bi color LED or two single color (green and amber) at the bottom bifurcation.

Figure 2-14 Flex PCB 3D representation showing the location of the LEDs

Note: The same flex PCB could be leveraged for the fan power and signals connection to have a cleaner solution. A flex PCB is shown in the figure as suggestion only, flex/flat wire can also be used instead, the implementer can decide what solution to use depending on its design.

The LEDs shall be controlled by Firmware to easily change blink rates and colors for the different states using update to the PSU secondary side Firmware's configuration file as defined in *Section 12.8.3.1 LED*

Behavior Configuration Block. This allow the M-CRPS to be reprogrammed to match different customer's LED state requirements.

2.4 Inlet Connector

The power supply can have different inlet connectors depending on the input voltages, current rating and type of connection that could be directly interfacing with a bus bar in a rack or through a power cord.

2.4.1 240VAC/240VDC Input

To comply with international regulations IEC320-C14 inlet connector shall be used when a maximum of 10 Amperes is required by the power supply. IEC320-C16 can be used to support higher exhaust temperatures in the power supply at 10 Amperes. A picture of the IEC320-C14 inlet connector is shown in the figure below.

Figure 2-15 IEC320 C14 Inlet connector example

To comply with international regulations IEC320-C20 inlet connector shall be used when a maximum of 16 Amperes is required by the power. Additionally, IEC320-C22 can be used to support higher exhaust temperatures in the power supply at 16 Amperes.

Figure 2-16 IEC320-C20 Inlet connector example

2.4.2 277VAC/380VDC Input

The 277VAC/380VDC inlet connector is shown in below figure, for more information about vendors and part numbers refer to: documentation of connector vendors and part numbers located at [DC-MHS Connector Information.]

Figure 2-17 277VAC/380VDC inlet connector

Figure 2-18 277VAC/380VDC inlet connector from Anderson Power

2.4.3 +54VDC Input (Rack Power Input)

A bus bar type connector shall be used when using a direct bus bar connection for the input of the power supply to interface with +54VDC rack power delivery, the connector shall be properly sized for the required input current of the power supply. An example of this type of connector is shown in the following figure.

Figure 2-19 +54V Input connector example (M-CRPS side)

Figure 2-20 +54V Input connector pinout (M-CRPS side)

for more information about vendors and part numbers refer to: documentation of connector vendors and part numbers located at DC-MHS Connector Information.

2.4.4 -48VDC Input (Telecom)

The -48VDC Input Receptacle Connector is shown in below figure, for more information about vendors and part numbers refer to: documentation of connector vendors and part numbers located at DC-MHS Connector Information.

Figure 2-21 -48VDC inlet connector example (Telecom)

Note: This connector requires the mating -48VDC Power plug for the power cord, refer to DC-MHS Connector Information for information about vendors and part numbers.

Figure 2-22 -48V Inlet connector (Telecom) pinout

2.5 Label Outline and Artwork

All the supported power supply form factors shall have a space of 115x52mm for the label, an example of the label artwork is shown in the figure below. Refer to specific OEM artwork and drawing for more details about the required information like company name, addresses, etc.

Figure 2-23 PSU Label artwork example

2.6 Output Connector Interface

The output connector interface for the form 185mm by 73.5 and the 185mm by 60mm factors include the same amount of signal and power connections, the difference in the 185mm by 60mm form factor is the reduced contact area of the Ground and Power connections. *Figure 2-24* shows 3D representations of the

two different card edge interfaces, mechanical details are shown in *Supplemental Material D* for the 185mm by 73.5mm form factor and *Supplemental Material E* for the 185mm by 60mm form factor.

Figure 2-24 a) 185mm by 60mm card edge for 12V output power supplies, b) 185mm/265mm by 73.5mm card edge for 12V output power supplies, c) 185mm by 60mm card edge for 54V output power supplies, d) 185mm/265mm by 73.5mm card edge for 54V output power supplies.

2.6.1 185mm by 73.5mm Form Factor

Table 2-2 185mm/265mm by 73.5mm M-CRPS dimensions and receptacle connector

Dimensions	M-CRPS-185-73.5: 40mm x 73.5mm x 185mm (H x W x L)
Output connector	These form factors use the 73.5mm Output Receptacle for the different options refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information. For guidance about how to check and existing connector or create a new connector for the M-CRPS compatible with dimensions, datums, and footprint for DC-MHS please refer to *Supplemental Material D.*

Power supply front view

Figure 2-25 185mm/265mm by 73.5mm Power supply's output pin numbering

Note: Pin numbering is shown based on listed connectors in *Table 2-2*.

The power supply card edge pinout for the 73.5mm in width PSU form factor is defined in the below table.

Table 2-3 73.5mm in width PSU pinout definition

Name	High pwr conn[2]	Regular conn[1]	Regular conn[1]	High pwr conn[2]	Name
GND	P1	A1	B1	P7	GND
GND		A2	B2		GND
GND		A3	B3		GND
GND	P2	A4	B4	P8	GND
GND		A5	B5		GND

GND			A6	B6		GND	
GND		P3	A7	B7	P9	GND	
GND			A8	B8		GND	
GND			A9	B9		GND	
+12V	Empty (N.C.) [8]	P4[6]	A10	B10	P10[6]	Empty (N.C.) [8]	+12V
+12V	Empty (N.C.) [8]		A11	B11		Empty (N.C.) [8]	+12V
+12V	Empty (N.C.) [8]		A12	B12		Empty (N.C.) [8]	+12V
+12V	+54V	P5[6]	A13	B13	P11[6]	+54V	+12V
+12V	+54V		A14	B14		+54V	+12V
+12V	+54V		A15	B15		+54V	+12V
+12V	+54V	P6[6]	A16	B16	P12[6]	+54V	+12V
+12V	+54V		A17	B17		+54V	+12V
+12V	+54V		A18	B18		+54V	+12V
PMBus SDA		S1	A19	B19	S8	A0 (SMBus address)[5]	
PMBus SCL		S2	A20	B20	S9	A1 (SMBus address)[4]	
PSON#		S3	A21	B21	S10	+12VSB	
SMBAlert#		S4	A22	B22	S11	Cold Redundancy Bus	
Return Sense / PS_KILL[7]		S5	A23	B23	S12	12V load share bus	
+12V/+54V Remote sense		S6	A24	B24	S13	Imon[3]	
PWOK		S7	A25	B25	S14	VINOK	

Notes:

1. Regular 50-pin card edge connector *Table 2-2*. The description is based on the receptacle connector's perspective.
2. High power connector listed in *Table 2-2.* The description is based on the receptacle connector's perspective.
3. *Imon* output signal current information based on 12V main output's loading condition, please see details in *Section 9.5 Imon Signal (Output)*.
4. A1 pin shall support bi-directional serialization mechanism described in *Section 12.7 Data & Sideband Serialization Interface (DSSI)*.
5. A0 pin shall be connected to an ADC input in the secondary side MCU to support up to 6 SMBus addresses, levels are described in *Section 9.6.1 A0 Input Addressing*.
6. These power contacts can be +12V or +54V depending on the output voltage of the power supply.
7. This pin is dual purpose, for more information refer to *Section 9.7 Remote Sense And Return Sense / PSKILL.*
8. +54V output M-CRPS card edge has a notch in this location, refer to *Supplemental Material D. 73.5mm in width M-CRPS card edge mechanical drawing*.

2.6.2 185mm by 60mm Form Factor

Table 2-4 185mm by 60mm M-CRPS dimensions and receptacle connector

Dimensions	M-CRPS-185-60: 40mm x 60mm x 185mm (H x W x L)
Output connector	This form factors use the 73.5mm Output Receptacle for the different options refer to documentation of connector vendors and part numbers located at: DC-MHS Connector Information.

	For guidance about how to check and existing connector or create a new connector for the M-CRPS compatible with dimensions, datums, and footprint for DC-MHS please refer to *Supplemental Material D.*

Power supply front view

Figure 2-26 185mm by 60mm Power supply's output pin numbering

Note: Pin numbering is shown based on listed connectors in *Table 2-4***.**

The power supply card edge pinout for the 60mm in width PSU form factor is defined in the below table.

Table 2-5 60mm in width PSU pinout definition

Name		Conn. Pin[7]	Conn. Pin[7]	Name	
GND		PT1	PB1	GND	
GND				GND	
GND				GND	
GND		PT2	PB2	GND	
GND				GND	
GND				GND	
Empty (no connection)[6]		PT3	PB3	Empty (no connection)[6]	
Empty (no connection)[6]				Empty (no connection)[6]	
Empty (no connection)[6]				Empty (no connection)[6]	
+12V	+54V	PT4[5]	PB4[5]	+54V	+12V
+12V	+54V			+54V	+12V
+12V	+54V			+54V	+12V
+12V	+54V	PT5[5]	PB5[5]	+54V	+12V
+12V	+54V			+54V	+12V
+12V	+54V			+54V	+12V
PMBus SDA		S1	S8	A0 (SMBus address)[3]	
PMBus SCL		S2	S9	A1 (SMBus address)[2]	
PSON#		S3	S10	+12VSB	
SMBAlert#		S4	S11	Cold Redundancy Bus	
Return Sense / PS_KILL		S5	S12	12V load share bus	
+12V Remote sense[4]		S6	S13	Imon[1]	
PWOK		S7	S14	VINOK	

Notes:

1. *Imon* output signal current information based on 12V main output's loading condition, please see details in *Section 9.5 Imon Signal (Output)*.
2. A1 pin shall support bi-directional serialization mechanism described in *Section 12.7 Data & Sideband Serialization Interface (DSSI)*.
3. A0 pin shall be connected to an ADC input in the secondary side MCU to support up to 6 SMBus addresses, levels are described in *Section 9.6.1 A0 Input Addressing*.
4. This pin is dual purpose, for more information refer to *Section 9.7 Remote Sense And Return Sense / PSKILL.*
5. These power contacts can be +12V or +54V depending on the output voltage of the power supply.
6. +54V output M-CRPS card edge has a notch in this location, refer to *Supplemental Material E. 60mm in width M-CRPS card edge mechanical drawing*.
7. The description is based on the receptacle connector's perspective.

3 Thermal Requirements

The following subsections describe the power supply thermal test conditions. The power supply is intended to be installed in a system in which the power supply will support limited operation up to an inlet temperature of 70°C during loss of redundancy conditions, however the typical maximum operating ambient power supply's inlet temperature is 55°C.

3.1 Temperature and Altitude Conditions

All internal components in the power supply shall meet their respective temperature specifications and lifetime requirements for each condition in *Table 3-1 Power supply thermal test conditions*.

All airflow shall pass through the internal volume of the power supply and not over the exterior surfaces of the power supply.

Table 3-1 Power supply thermal test conditions

Tier Level	Load on a power supply	Max. Inlet Temperature	Max. Exhaust Temperature[3]	Max. Touch Surface Temperature	Altitude	Application
1[7]	100%	55°C	70°C	70°C	950m	Home / Office / Small Business
2[7]	100%	55°C	75°C	75°C[6]	950m	General Data Center & Storage
3[4,7]	100%	55°C	75°C	75°C[6]	2286m	High Performance Computing, High End Storage
		70°C[1]	90°C[1]	90°C[1,6]		

Notes:

1. This condition shall be supported only once in the life of the power supply for 24 hours straight.
2. A maximum of 3000m might be required for some models of power supplies, this requirement shall be stated in the design specification of a given model.
3. Texit (Exhaust temperature) shall be measured using the procedure described in *Supplemental Material P Exhaust Temperature Measurement.*
4. Tier 3 power supply shall limit the back pressure to +0.5".
5. A thermal sleeve shall be used for all the tests, refer to supplemental material section for the mechanical drawings.

6. PSU will need to have a mylar coating in all the metal parts in the rear part of the chassis when the temperature exceeds 70°C and up to 90°C.
7. The temperature limit for the components will be based on their maximum Tj -10°C for components like Power semiconductors, magnetics, bulk capacitor, aluminum polymer capacitors at the output of the power supply and PCB.

All conditions in the table above shall be supported assuming free delivery which corresponds to 0 inches H2O of back pressure. For PCBs with SMD power components, the maximum operating temperature shall be kept below Tg -10°C, for example an FR4 material with a Tg = 130°C shall be kept below 120°C. Air temperature rise is allowed for 100% load from the inlet to the exhaust of the power supply as stated in *Table 3-1 Power supply thermal test conditions,* and 15C air temperature rise is allowed for 70% load. SMBAlert# shall not assert under any of the operating conditions stated in the above table unless configured in the configuration file. The max load on the power supply may vary based on input voltage. The rated load stated in *Section 7.1 Output Power/Currents* shall be used when testing at lower input voltages.

The power supply must always meet UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side must be classified as "Handle, knobs, grips, etc. held for short periods of time only".

3.2 Power Supply Fan

The fan shall use either a Hall IC (in addition to hall sensor) OR should have an internal circuit & / or FW for noise immunity. Additionally, the fan shall be certified by any accredited lab for IEC61000-4-3 (radiated Magnetic Immunity) & IEC61000-4-8 (Power Frequency Magnetic Field Immunity).

L10 data at 70°C and 90°C shall be provided for reliability purposes.

3.3 Thermal Sensors

The PSU shall at a minimum have thermal sensors (with an accuracy within +/-2°C) to measure inlet temperature, exhaust temperature, and two hot spot component temperatures. These shall be used for fan speed control as well as asserting over temperature warning conditions (OTW), over temperature protection/shutdown (OTP), reporting temperatures via PMBus.

Inlet ambient temperature sensors OTW and OTP levels are defined in *Section 8.1.8 Over Temperature Warning (OTW)*.

Both the hotspot thermal sensor(s) and the ambient inlet thermal sensor shall have both OTW level and OTP level associated with them. The OTW level must be set at least 4°C lower than the OTP level to guarantee a warning condition is reported to the system before a shutdown condition.

3.4 Fan Speed Control

The power supply shall incorporate a fan for cooling the power supply. The fan speed controller shall protect the power supply from overheating under any validated loading condition including high ambient temperatures, loading, voltage input, and airflow impedance. The normal airflow direction shall be from

the DC output connector side to the AC/DC inlet side of the power supply. However, there are also reverse airflow power supplies with airflow from the AC/DC inlet side to the DC output connector side.

> ***Note:*** The fan may run at 20% speed when Standby current >1.5A and the ambient temperature is higher than 35C if the main rail of the power supply is off and standby rail is available, as not to exceed 12VSB load.

3.4.1 Fan Speed Control Algorithm

The fan speed control shall implement a PID (Proportional, Integral, Derivative) type closed loop feedback algorithm with hysteresis using at least the four minimum required thermal sensors (inlet air temperature, both the critical component temperature and exit air temperature as defined in *Section 3.3 Thermal Sensors*). It is suggested to calculate a single aggregate thermal margin from the temperature sensors as the input to the algorithm. It is also required that the gain coefficients and thermal sensor targets are Firmware programmable.

After the new load and/or cooling condition steady state is established, transition to the steady state fan speed shall take less than 60 seconds.

The power supply fan speeds shall not oscillate under any steady state operating condition (steady state power output level and steady state inlet air temperature). Fan oscillation shall be controlled such that associated sound power level variation falls within a band of 2.0 dBA. This condition may be treated as steady state fan speed condition.

The fan is allowed to run in Standby mode as necessary to cool the PSU when the ambient temperature exceeds 35C. In Standby mode, the power supply shall support the PMBus command to override PSU fan speed.

3.4.2 Fan Fault

The PSU shall detect a warning or fault of the PSU fan and report the fault over the PMBus. A fan fault is defined as when the actual fan speed is lower than the FSC setpoint by a configurable amount and is measured in RPM. If the difference is greater than a configurable value in RPM over 5 seconds, the “Fan X Warning” should be asserted. If the difference greater than a configurable value in RPM within 15 seconds, the “Fan X fault” should be asserted immediately. If the “Fan X Fault’ is asserted, then the PSU main rail (+12V) shall also shut down when in Normal operation. The fan fault shutdown mechanism shall be activated no more than 15 seconds after the power supply outputs are first turned-on to allow sufficient time for the fan to come up to speed and the fan detect circuitry to stabilize. If the Fan Fault is removed when PSU is still in STANDBY mode, then the fan shall be able to recover depending on the selected configuration. Optionally the PSU can be configured to try to restart the fan to see if fault is cleared, and if the fault is cleared, STANDBY becomes operational (subject to input being within operational range and there is no other fault in the PSU which could cause STANDBY to shutdown).
When there is a fan fault, no safety issue should occur due to the lack of airflow.

3.4.3 System Fan Speed Override

In some system applications, if the system is creating a low pressure at the inlet to the power supply, there is a possibility that the airflow through the PSU could reverse direction and flow backwards through the PSU drawing flow from the 'hot isle' and may lead to components exceeding their thermal limits. To prevent this reverse airflow condition, the PSU must support PMBus commands from the system to override and increase the PSU fan speed if or as needed. This feature will not allow the system to reduce the PSU fan speeds below the PSU internal FSC settings but can increase the fan speed. System will communicate the minimal fan speed to the PSU via the FAN_COMMAND_1 (3Bh) PMBus command. This sets the PSU minimum fan speed to guarantee positive airflow direction through the PSU.

The power supply shall be able to accept and execute the FAN_COMMAND_1 (3Bh) while in standby or when the input voltage is not present, for this mode of operation the PSU shall bias its internal fan from the main output when it is available or from the standby rail when the power supply is in standby mode. Writing 0000h to the FAN_COMMAND_1 (3Bh) shall stop the fan operation in standby operation as well as ON state. The connection between fan VCC and +12Vmain output of the power supply shall include necessary isolation and protection circuit as shown in the figure below.

Figure 3-1 Fan power isolation circuit example

3.5 Additional Thermal and Airflow Characterization

System designers need to understand how the system may impact power supply airflow and how to correctly integrate the power supply into the overall system thermal solution. It is possible that the system configuration could either impede the PSU airflow or could support the PSU airflow. This section describes the power supply characterization needed by the system thermal designer to ensure a sufficient cooled system.

> ***Note:*** All tests shall be conducted using a thermal sleeve, refer to supplemental material for the mechanical drawings.

The most critical data is the airflow required for various load and inlet air temperature conditions. An example of the resulting characterization is shown in *Figure 3-2 Airflow requirement for thermal compliance for inlet temperature for different PSU loads*. The power supply shall be instrumented with thermocouples on at least the top 10 key components and the required airflow shall be based on satisfying the internal component temperatures as well as the max exit air temperature requirement.

Figure 3-2 Airflow requirement for thermal compliance for inlet temperature for different PSU loads

Power supply vendors shall perform testing to complete the table shown in *Table 3-2* below. Tests shall be performed at the specified operating ambient.

Table 3-2 Airflow requirement for thermal compliance for inlet temperature at different PSU load conditions

PSU Load	20%		30%		40%		50%		60%		70%		80%		90%		100%	
PSU Tla	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM
70 °C																		
65 °C																		
60 °C																		
55 °C																		
50 °C																		
45 °C																		
40 °C																		
35 °C																		
30 °C																		
25 °C																		
20 °C																		
15 °C																		
10 °C																		
5 °C																		

Note:

1. The power supply shall be characterized at sea level and in a free delivery condition, meaning zero back pressure and also at 950m, 2286m and 3000m.

The airflow from *Table 3-2* does not include the influence from the system design. The influence from the system could be either a source or an impedance. A source, typically caused by system fans pressurizing

the inlet of the power supply will often increase airflow through PSU. However, an impedance, typically caused by the system fans operating in parallel to the power supply resulting in a low pressure at the inlet of the power supply will typically reduce power supply airflow.

In order for the system designer to understand and account for the system influence on the power supply, three power supply airflow characterization tests are required. The first is the full power supply performance curve measured as airflow versus pressure. The second is the power supply impedance curve measured without the fan installed. The third is the power supply fan curve measured as a stand-alone fan. This data will also allow the system designer to accurately model the PSU airflow in CFD analysis.

Examples of these performance curves are shown in *Figure 3-3 Power supply airflow impedance, fan curve and equivalent performance curve (Example from a real test)*. Tests shall be performed at sea level conditions (test facilities at elevated environment shall perform altitude correction projections).

Figure 3-3 Power supply airflow impedance, fan curve and equivalent performance curve (Example from a real test)

Power supply vendors shall perform testing to complete the *Table 3-3* below.

Table 3-3 Power supply airflow impedance, fan curve and equivalent performance curve

	PSU without fan	Stand-alone fan	PSU with fan
Airflow (CFM)	Pressure (in H_2O)	Pressure (in H_2O)	Pressure (in H_2O)
0			
2			
4			
6			
8			
10			
12			
14			
16			
18			
20			

Notes:

1. Maximum CFMs in the previous table is an example and actual maximum shall be based on the maximum airflow for the stand-alone fan specification.

Lastly, the power supply's fan shall be characterized to create the *Figure 3-4 Power supply fan PWM characterization (example only)* below and complete *Table 3-4*. The airflow in the table is the total power supply free delivery airflow measured at sea level.

Figure 3-4 Power supply fan PWM characterization (example only)

Table 3-4 Power supply fan PWM characterization

PWM Duty cycle (%)[1]	PSU Free Delivery Airflow (CFM)
10%	
20%	
30%	
40%	
50%	
60%	
70%	
80%	
90%	
100%	

Notes:

1. Minimum PWM duty cycle shall be taken from the specific fan being used in the power supply (either 10% or 20% PWM duty cycle).

4 Acoustics and Vibration Requirements

4.1 Overview

Each PSU offering shall meet a set of acoustical limits and reporting requirements to be compliant with this specification. Information about the acoustical noise of power supplies is useful to manufacturers of data center equipment for the purposes of product design and to compare power supplies developed under this standard. Three acoustical categories have been defined in this section to represent different acoustical limits by the anticipated product application space: Home and Office, General Purpose and Storage, and High-Performance Computing. Individual power supply design specifications shall indicate which acoustical category the power supply shall be qualified against.

In general, this specification seeks to leverage ECMA-74 as the modern standard for performing sound power and sound pressure measurements; however, this standard defines a set of unique bystander microphone locations and defines several specific operating conditions not included in ECMA-74.

The limits developed in this standard are agreed upon by the participating members of the M-CRPS working ground within OCP. Data center IT equipment has a wide breadth of application spaces and environments; this specification seeks to define a subset of physical deployment environments to set limits on sound power and sound quality of a given PSU.

This standard includes specific sound power reporting requirements that shall be published as a part of compliance to this standard. In addition to a limited set of published data, this standard includes a set of data that shall be made available to individual product manufacturers for the purposes of system design and implementation.

4.1.1 General, Laboratory, and Sampling Requirements

Acoustical measurements shall be performed in a NVLAP, or equivalent, certified laboratory qualified to measure and report in accordance with ECMA-74. The test environment should provide an essentially free field over a reflecting plane. Per EMCA 74 clause 7.3.1.1, criteria for suitable test environments are defined in ISO 3744 and ISO 3745.

Samples to be evaluated for acoustical compliance with this specification shall be randomly selected from a larger batch manufactured for qualification. At least three power supply samples for each qualified fan make and model qualified in the design shall be tested to comply with this specification. For example, if two fan models are to be qualified for use, 6 total power supplies shall be sampled from a qualification batch, three for each of the fan models.

4.1.2 Test Environment

The test environment and meteorological conditions shall meet the requirements of ECMA-74 clause 7.

4.1.3 Instrumentation

Microphones shall meet the instrumentation requirements of ECMA-74 clause 7 for sound power measurements and ECMA-74 Clause 8 for sound pressure and sound quality measurements.

A sound power array meeting the qualifications of ISO 3744 or ISO 3745 shall be used for measuring sound power. Two additional microphones shall be used to measure sound pressure and for the purposes of evaluating sound quality. The location of these microphones is documented in *Section 4.1.5 Microphone Positions.*

In addition to microphones for measuring acoustical data, fan speed should also be measured and recorded simultaneously. For simplicity across acoustical and vibration testing, recording the fan tachometer signal directly is recommended to record fan speed. An optical tachometer may be used for acoustical testing; however, optical tape may negatively impact fan vibration measurements, and thus should be removed for vibration tests. NOTE: fan speed measurement is still required for vibration testing.

The optical tachometer shall not be positioned to interfere with acoustic transmission between the fan and the bystander microphone.

For some constant fan speed tests, described in *Section 4.1.5 Microphone Positions*, a resistive load is required to be applied to an energized PSU to evaluate electronic noise. The load shall not be a DC electronic load or any load that itself produces noise.

4.1.4 Installation and Operation of the Power Supply

PSU should be installed in the test environment in accordance with sub-assembly requirements per ECMA-74 clause 5.1.7. The PSU shall be supported 0.25 m ± 0.03 m above the reflecting plane by a vibration isolating stand or fixture, or by appropriate vibration-isolating elements. The method of supporting the sub-assembly shall not interfere with the propagation of airborne sound from the sub-assembly or generate any additional sound radiation. Vibration isolation elements should be placed on the bottom of the PSU at each of the four corners of the device; rubber isolators approximately 20mm in diameter and 12mm in height are recommended.

For tests which specify operation of the fan, the fan shall be manually controlled through the PSU firmware or directly with wires to a power supply and function generator. In these cases, the fan should not be controlled with a closed loop fan control algorithm.

4.1.5 Microphone Positions

For sound power measurement, the measurement surface and microphone positions shall follow ECMA-74 clause 7.6.

For sound pressure measurement, two microphones, defined as front and rear operator microphones shall be installed. The operator positions shall be at a horizontal distance of 0.5 m ± 0.03 m from the front and rear sides of the reference box, as defined in ECMA-74 clause 7.6.1, at a vertical height of 0.25 m ± 0.03 m. For the purposes of this acoustical measurement, the front and rear of the PSU are defined in *Figure 4-1 Front and rear surface definition for PSU bystander microphone position*. PSU setup with operator microphone positions are shown in *Figure 4-2 PSU installation and operator microphone position locations [side view]* in accordance with ECMA-74 Clause 5.1.7.Operator microphones located downstream of the fan shall have a windscreen placed on the microphone to prevent wind noise.

Microphone orientation shall follow requirements in ECMA-74 clause 8.6.4.

Figure 4-1 Front and rear surface definition for PSU bystander microphone position.

Figure 4-2 PSU installation and operator microphone position locations [side view] in accordance with ECMA-74 Clause 5.1.7.

4.1.6 Measurement of Acoustical Data

The following data shall be recorded simultaneously for each operating mode defined in *Section 4.1.7 Operating Modes:*

- Raw waveform (pressure time history) and associated calibration information
- Rotation speed of the fan.

These signals are then used to calculate the acoustic metrics.
The duration of the recording is outlined by operating mode in *Section 4.1.7 Operating Modes*.

4.1.7 Operating Modes

Acoustical requirements are provided for five primary operating modes:

1. Continuous Fan Speed Sweep
2. Discrete Fan Speed Sweep
3. Constant Fan Speed
4. Transient Event

5. Retaining Latch

Fan sweep requirements provide overall limitations on the fan performance and give integrator designers data to use for engineering products. Constant speed fan operation modes reflect the efficiency of the design by reporting and limiting response at simulated operating points at a given PSU inlet temperature, load as a percentage of maximum PSU outlet wattage, inlet pressure, and altitude. Limits on transient fan control response are designed to prevent annoying oscillation during steady state operation, overshoot when the PSU changes load or inlet temperature states, and perceptions of poor product quality during PSU startup and shutdown. Lastly, limits are set on the mechanical latch noise to prevent annoyance or perceptions of poor product quality during physical install or removal of the PSU.
The 5 operating modes are now outlined in more detail:

4.1.7.1 Continuous Fan Speed Sweep

Fan speed shall be continuously ramped from 10% of the maximum fan speed to 100% of the maximum fan speed over a period of at least 120 seconds. Recordings should contain at least 5 seconds at the minimum and maximum fan speeds to ensure that all fan speeds are contained in the analysis sweep.

4.1.7.2 Discrete Fan Speed Sweep

The fan speed shall be operated at 10 discrete fan speeds from 10% of the maximum fan speed to 100% of the maximum fan speed. The fan speed shall be incremented by 10% of the maximum fan speed. Recordings at each discrete fan speed sweep should have an equal measurement duration of at least 10 seconds.

4.1.7.3 Constant Fan Speed

For the duration of the recording, the fan will be manually controlled at a fixed fan speed. The fan should be operating at the prescribed fan speed for at least 30 seconds prior to beginning a recording to ensure no transient fan speed fluctuations are captured. Constant fan speed recordings shall be at least 10 seconds in duration.

This standard specifies a set of operating modes that nominally correlate to potential end-user states of operation. These operating modes are defined by inlet air temperature to the PSU, an operating load defined as a percentage of the maximum PSU design load, inlet air pressure differential, and altitude. For acoustical testing, these load conditions shall be simulated by manually setting the fan speed to the measured performance of the PSU under the default fan speed control algorithm in a thermal test chamber as performed to satisfy the requirements of *Section 3 Thermal Requirements* in this document.

For several acoustical metrics defined in this section, a maximum fan speed is used to calculate a percentage of potential fan speed. For acoustical and vibration testing, maximum fan speed is the maximum fan speed required to cool the PSU at 60°C inlet and 100% of maximum design power as measured for *Section 3 Thermal Requirements*.

For some test constant fan speed testing, a load is required to be applied during testing to measure potential electronic noise. For load testing, a resistive load shall be used and installed such that the components applying the load do not interfere with the transmission of noise between the PSU fan inlet

or outlet and the bystander microphone positions. The resistive load shall not be a DC electronic load or any load that is itself a source of noise. Equipment used to apply a load should be removed for all testing that does not require a resistive load.

Nominal operating states are defined in *Table 4-1* for PSU's designed for office applications and *Table 4-2* for general purpose and high-performance computing applications.

Table 4-1 Definition of operating modes for constant fan speed testing for Home & Office PSU's.

Constant Fan Speed Operating Modes					
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum, Non-Redundant
Applied/Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply Inlet Temperature	25° C	25° C	35° C	35° C	35° C
Altitude, m	950	950	950	950	950

Table 4-2 Definition of operating modes for constant fan speed testing for General Purpose & Storage PSU's.

Constant Fan Speed Operating Modes					
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum, Non-Redundant
Applied/Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply Inlet Temperature	25° C	50° C	50° C	50° C	55° C
Altitude, m	950	950	950	950	950

Table 4-3 Definition of operating modes for constant fan speed testing for High-Performance Computing PSU's.

Constant Fan Speed Operating Modes					
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum, Non-Redundant
Applied/Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No

Simulated Power Supply Inlet Temperature	25° C	50° C	55° C	55° C	55° C
Altitude, m	950	950	950	950	950

4.1.7.4 Transient Event

For transient mode evaluation, a fully operational PSU shall be used. The fan shall be controlled by the default fan control algorithm.

The operator applying power should minimize acoustical impact on the measurement by remaining as still as possible and standing out of the direct acoustical path between the device and the measurement microphones.

Two primary operating transient operating modes shall be evaluated:

a) Apply power by inserting the external power plug into the device.
b) Remove power by unplugging the external power plug from the device.

Transient event recordings shall be at least 10 seconds. At least 1 second shall be recorded prior to the application or removal of the power plug.

4.1.7.5 Retaining Latch

For retaining latch evaluation, a fully operational PSU shall be used. For this operating a mode the PSU shall have no inlet plug installed.

To perform a latch event, the operator shall place a hand on the PSU to prevent it from moving and with the thumb of the opposite hand, push the latch open so that it would be fully disengaged when installed in a system; for most products the latch element should be touching the PSU housing in this mode. To initiate the latch event, the operator should suddenly release the latch to capture the closure sound of the retaining latch.

At least three latch events shall be performed in each recording. At least 10 seconds shall pass between latch events. At least 10 seconds shall be recorded prior to the first latch event. Each recording shall be at least 40 seconds.

4.1.8 Calculation of Acoustical Values by Operating Mode

4.1.8.1 Continuous Fan Speed Sweep

For continuous fan speed sweeps, analysis should focus on the ramped fan speed region of the recording and thus recordings should be edited to include less than 500ms of starting and ending fan speeds.

For continuous fan speed sweep recordings, the following acoustical values shall be calculated:

- ISO 532-1 Loudness vs. % Maximum Fan Speed. In this calculation the recording shall be divided into RPM bins no smaller than 50 RPM's and no larger than 150 RPM's. In each of these RPM bins,

an average ISO 532-1 loudness shall be calculated. The RPM bins should then be scaled to the maximum thermal fan speed defined in Section 4.1. For ISO 532-1, assume a free sound field for the purposes of this calculation. A single curve should be calculated for each fan sample tested.

- Maximum Specific Prominence Ratio vs. % of Maximum Fan Speed. In this calculation the recording shall be divided into RPM bins no smaller than 50 RPM's and no larger than 150 RPM's. In each of these RPM bins, prominence ratio shall be calculated with an average FFT in accordance with ECMA 418-1 Clause 12. Next, the maximum measured prominence ratio across all frequencies per RPM bin shall be calculated. The RPM bins should then be scaled to the maximum thermal fan speed defined in Section 4.1. A single curve should be reported for each fan sample tested.
- Sound Pressure Level vs. % of Maximum Fan Speed. In this calculation the recording shall be divided into RPM bins no smaller than 50 RPM's and no larger than 150 RPM's. In each of these RPM bins, unweighted sound pressure level and A-weighted sound pressure level shall be calculated. Fast time weighting shall be used for the time integral duration. The RPM bins shall then be scaled to the maximum thermal fan speed defined in Section 4.1. One plot for each operator position and fan vendor shall be generated. Both A-weighted and unweighted sound pressure level shall be included on the plot. All samples tested with the same vendor shall be on the plot.

4.1.8.2 Discrete Fan Speed Sweep

For discrete fan speed sweep recordings, the following acoustical values shall be calculated:

- Mean A-weighted Sound Power Level vs. % Maximum Fan Speed. For each discrete fan speed sweep recording, A-weighted sound power level shall be calculated in accordance with ECMA-74 clause 7. For multiple samples of the same fan model the linear mean of n, samples shall be calculated for reporting. One curve of mean A-weighted Sound Power Level vs. % of maximum fan speed shall be calculated for each fan model.

4.1.8.3 Constant Fan Speed

For constant fan speed recordings, the following acoustical values shall be calculated:

- Mean A-weighted Sound Power Level. For each recording, A-weighted Sound Power Level shall be calculated in accordance with ECMA-74 clause 7. For each operating mode, the mean A-weighted Sound Power Level shall be calculated for each fan model. One mean A-weighted Sound Power Level shall be calculated for each operating mode and fan model.
- Maximum Specific Prominence Ratio. For each recording, specific prominence ratio shall be calculated at frequency resolution smaller than 7Hz using the prominence ratio methods of ECMA 418-1. The maximum measured specific prominence ratio across all frequencies shall be calculated for each recording. For each operating mode and fan model, one maximum shall be calculated as the maximum of the individual maximum values measured.

4.1.8.4 Transient Modes

For transient mode recordings, the following acoustical values shall be calculated:

- Maximum of ISO 532-1 Loudness vs. Time. For each recording, loudness should be calculated in accordance with ISO 532-1 vs. time. Next take the maximum value from the recording to calculate

the maximum loudness for each recording. Finally, the maximum for all transient tests should be obtained.

- Maximum specific prominence ratio. For each recording, specific prominence ratio shall be calculated at frequency resolution smaller than 7Hz using the prominence ratio methods of ECMA 418-1. Next, the maximum value across all frequencies and time shall be calculated. Finally, the maximum value across all samples tested shall be calculated.

4.1.9 Acoustical Requirements

Acoustical requirements include specific limits on sound power, sound pressure, and sound quality metrics. Acoustical requirements also include some report-only values for the purposes of designing systems with these PSUs as components. PSU limits may differ based on the intended PSU application space:

- Home & Office use PSU's are designed for use in lightly configured rack and tower servers that may be physically located in home or office environments around bystanders. PSU's that support low-line AC voltage input and that are designed for maximum output of approximately 1400W (including low-line AC derated power) will likely be required to meet this level of acoustical output. A PSU vibration limit is also applicable to rotational storage media, see *Section 4.2 Vibration Requirements*.
- General data center & storage PSU's are designed for general purpose server applications and specifically for servers that utilize rotational media for storage. Rotational storage media has a demonstrated sensitivity to excessive noise and vibration levels, the maximum acoustical output of these PSU's is limited to prevent excessive impact to storage performance. A PSU vibration limit is also applicable to rotational storage media, see *Section 4.2 Vibration Requirements*.
- High performance computing PSU's are designed for high power sever computing applications in unattended data center environments and other areas where power density is prioritized over sound quality. PSU's designed to meet this acoustical output category may degrade the performance of rotational storage devices in some server and storage applications.

Limits are defined according to operating mode for each PSU classification.

In addition to quantifiable acoustical metric limits, three additional sound quality requirements must be evaluated by the PSU vendor:

- The default fan control algorithm should not induce fan oscillation during steady state load and inlet temperature conditions. Operator position noise levels should not fluctuate more than ±2 dBA over a 10-minute period. A statement indicating compliance to this specification is required.
- The default fan control algorithm should not induce overshoot over 3dB during fan speed transients of PSU load change. A statement indicating compliance to this specification is required.
- The PSU should not produce any buzzes, squeaks, or rattles during operation. A statement indicating no buzzes, squeaks, or rattles shall be included in the report for compliance to this specification.

Table 4-4 Home & Office PSU Acoustical Requirements

Home & Office PSU Acoustical Requirements					
Continuous Fan Speed Sweep Requirements					
Metric	**Limit**				
SPL vs. % of Max RPM	Report				
Loudness vs. % of Max RPM	Report				
Maximum Prominence Ratio vs. % of Max RPM	For fan speeds between 10% and Operating Redundant ≤ 15dB For fan speeds more than Operating Redundant ≤ 20dB				
Discrete Fan Speed Sweep Requirements					
Mean A-weighted Sound Power Level vs. % of Max Fan Speed	Report				
Constant Fan Speed Requirements					
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum Non-Redundant
Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply inlet Temperature	25° C	25° C	35° C	35° C	35° C
Simulated Altitude, m	950	950	950	950	950
Fan Speed (% of Max Fan Speed)	Report	Report	Report	Report	Report
LwA,m, Bels, limit	3.9	4.4	4.7	6.2	7.1
Maximum Prominence Ratio limit	10	11	13	20	25
Transient Mode Requirements					
Maximum of Loudness vs. Time	1.0 sone				
Maximum Prominence Ratio	9dB				
Retaining Latch Noise Requirements					
Maximum of Loudness vs. Time	1.0 sone				
Maximum Prominence Ratio	9dB, no prominent tones				
General Thermal Control Requirements					
Operating Thermal Response	No Oscillation: < 2 dB over 10-min. Report compliance. No Overshoot: <3dB. Report compliance.				
All Operating Modes	No buzzes, squeaks, or rattles. Report compliance.				

Table 4-5 General Data Center & Storage PSU Acoustical Requirements

General Data Center & Storage PSU Acoustical Requirements					
Continuous Fan Speed Sweep Requirements					
Metric	**Limit**				
SPL vs. % of Max RPM	Report				
Loudness vs. % of Max RPM	Report				
Maximum Prominence Ratio vs. % of Max RPM	For fan speed between 10% and Operating Redundant, ≤ 20dB For fan speed more than Operating Redundant, ≤ 25				
Discrete Fan Speed Sweep Requirements					
Mean A-weighted Sound Power Level vs. % of Max Fan Speed	Report				
Constant Fan Speed Requirements					
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum Non-Redundant
Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply inlet Temperature	25° C	45° C	50° C	50° C	55° C
Simulated Altitude, m	950	950	950	950	950
Fan Speed (% of Max Fan Speed)	Report	Report	Report	Report	Report
LwA,m, Bels, limit	4.8	5.0	5.4	7.0	9.0
Maximum Prominence Ratio limit	10	18	18	25	Report
Transient Mode Requirements					
Maximum of Loudness vs. Time	1.0 sone				
Maximum Prominence Ratio	9dB				
Retaining Latch Noise Requirements					
Maximum of Loudness vs. Time	1.0 sone				
Maximum Prominence Ratio	9dB, no prominent tones				
General Thermal Control Requirements					
Operating Thermal Response	No Oscillation: < 2 dB over 10-min. Report compliance. No Overshoot: <3dB. Report compliance.				
All Operating Modes	No buzzes, squeaks, or rattles. Report compliance.				

Table 4-6 High Performance Computing PSU Acoustical Requirements

High Performance Computing PSU Acoustical Requirements					
Continuous Fan Speed Sweep Requirements					
Metric	**Limit**				
SPL vs. % of Max RPM	Report				
Loudness vs. % of Max RPM	Report				
Maximum Prominence Ratio vs. % of Max RPM	≤ 25dB				
Discrete Fan Speed Sweep Requirements					
Mean A-weighted Sound Power Level vs. % of Max Fan Speed	Report				
Constant Fan Speed Requirements					
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum Non-Redundant
Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply inlet Temperature	25° C	50° C	55° C	55° C	60° C
Simulated Altitude, m	950	950	950	950	950
Fan Speed (% of Max Fan Speed)	Report	Report	Report	Report	Report
LwA,m, Bels, limit	4.6	6.9	7.1	8.6	Report
Maximum Prominence Ratio limit	12	18	20	25	Report
Transient Mode Requirements					
Maximum of Loudness vs. Time	1.0 sone				
Maximum Prominence Ratio	9dB				
Retaining Latch Noise Requirements					
Maximum of Loudness vs. Time	1.0 sone				
Maximum Prominence Ratio	9dB, no prominent tones				
General Thermal Control Requirements					
Operating Thermal Response	No Oscillation: < 2 dB over 10-min. Report compliance. No Overshoot: <3dB. Report compliance.				
All Operating Modes	No buzzes, squeaks, or rattles. Report compliance.				

4.1.10 Reporting Requirements

Reporting requirements are divided into two categories, mandatory and on-request. Mandatory reporting of some acoustical output values is typical for IT equipment that produces noise. The reported values are limited a specific set of sound power outputs at defined operating states *per Section 4.1.7.3* with a specific pointer to *Table 4-1* or *Table 4-2* identified in individual M-CRPS design specifications.

Mandatory reporting shall include the maximum of mean A-weighted sound power level calculated in accordance with *Section 4.1.8.3* for each fan model shipped on the platform. The recommended format for the reporting is shown in *Table 4-7*. Sound power level shall be reported in decibels to the nearest whole decibel.

Table 4-7 Template for declaration of sound power output

M-CRPS Sound Power Output					
PSU Make & Model	Report				
M-CRPS Form Factor	Report				
Maximum Rated Power	Report				
Operating Mode	**Standby**	**Idle**	**Operating**	**Operating**	**Maximum**
			Redundant	**Non-Redundant**	**Non-Redundant**
Declared Sound Power Output (dB)	Report	Report	Report	Report	Report
Sound power is measured and reported in accordance with the open compute M-CRPS standard utilizing the [Select One: Office/General Use/HPC] operating mode test conditions.					

On-request reporting shall be provided to system integrators for use in the development of data center equipment. In this case, the data represents critical design information for developing data center appliances that incorporate power supplies developed under this M-CRPS specification. The following is a list of items that shall be provided on-request by system integrators.

Vendors should provide detailed identifying information about the following items:

- PSU Make/Model/Serials tested
- Fan make, model, and PPID
- Laboratory information

For continuous fan sweep mode, the following items shall be reported:

- Plot of ISO 532-1 Loudness vs. % of Maximum Fan Speed for each operator position and fan vendor.
    1. One front operator position plot per fan vendor
    2. One rear operator position plot per fan vendor
- Plot of Maximum Specific Prominence Ratio vs. % of Maximum Fan Speed for each operator position and fan vendor.
    1. One front operator position plot per fan vendor
    2. One rear operator position plot per fan vendor
- Plot of unweighted sound pressure level and A-weighted sound pressure level vs. % of Maximum Fan Speed for each operator position and fan vendor.
    1. One front operator position plot per fan vendor, include A-weighted and unweighted SPL
    2. One rear operator position plot per fan vendor, include A-weighted and unweighted SPL

For discrete fan sweep mode, the following items shall be reported:

- Plot of averaged sound power, $L_{wA,m}$ vs. % of maximum fan speed for each fan vendor. Report only.

For Constant Speed Fan testing, the following items shall be reported:

- Mean A-weighted Sound Power Level for each fan vendor and operating mode
- Maximum prominence ratio for each fan vendor and operating mode.

For Transient Mode testing, the following items shall be reported:

- Maximum loudness for all samples
- Maximum prominence ratio for all samples

For Retaining Latch Noise, the following items shall be reported:

- Maximum loudness for all samples
- Maximum prominence ratio and frequency for all samples

4.2 Vibration Requirements

Each PSU offering shall meet a set of vibration limits and reporting requirements to be compliant with this specification.

4.2.1 General, Laboratory, and Requirements

Vibration limits are designed to avoid performance degradation in electro-mechanical storage components in end-use PSU applications. This standard is written with the intent that acoustical and vibration measurements can be performed concurrently; however, vibration measurements may be conducted outside of an acoustical facility if background vibration noise can be controlled, and environmental conditions can be satisfied.

Vibration sampling requirements shall be the same as acoustical sampling requirements detailed in *Section 4.1.1 General, Laboratory, and Sampling Requirements.*

4.2.2 Test Environment

The test environment shall be a quiet room with a sufficiently low vibration noise floor to measure the performance of the PSU. The environmental requirements of section 4 are strongly recommended.

For environments that do not meet the requirements of *Section 4.1 Overview*, measurement of the background vibration levels should be performed to verify no elements of noise are within 15dB of the measured PSU vibration level at 50% of PSU fan speed in all individual channels.

4.2.3 Instrumentation

Four accelerometers shall be required for vibration testing. Accelerometer shall have a mass equal to or less than 1 gram and be capable of measuring vibration to an accuracy of ±5% over the frequency range from 10 Hz to 5000 Hz.

A method for measuring fan speed is required for vibration testing. Although optical tachometers may be used, direct measurement of the fan tachometer signal is strongly recommended. Optical tape applied to the fan may impact the vibration results.

4.2.4 Installation and Operation of the Power Supply

The PSU shall be installed on a support structure as described in *Section 4.1 Overview*, or at the center of a standard test table as described in ECMA-74 Annex A.1.

Vibration isolation elements should be placed on the bottom of the PSU at each of the four corners of the device; rubber isolators approximately 20mm in diameter and 12mm in height are recommended.

4.2.5 Accelerometer Positions

For the purposes of vibration testing, the front and rear of the PSU shall be defined as in *Section 4 Acoustics and Vibration Requirements.* The bottom of the PSU shall be designated as the exterior surface of the enclosure closest to and coplanar to the primary PCB of the PSU.

Four accelerometers shall be installed in the bottom side of the power supply when measuring vibration as shown in the figures below.

Figure 4-3 Accelerometer's locations in the bottom of the 185mm by 73.5mm power supply

Figure 4-4 Accelerometer's locations in the bottom of the 185mm by 60mm power supply

Figure 4-5 Accelerometer's locations in the bottom of the 265mm by 73.5mm power supply

4.2.6 Measurement of Acoustical Data

The following data shall be recorded simultaneously for all PSU vibration testing:

- Acceleration time history
- Fan speed time history

The duration of the recording is outlined by operating mode in *Section 4.2.7 Operating Modes.*

4.2.7 Operating Modes

4.2.7.1 Continuous Fan Speed Sweep

Fan speed shall be continuously ramped from 10% of the maximum fan speed to 100% of the maximum fan speed over a period of at least 120 seconds. Recordings should contain at least 5 seconds at the minimum and maximum fan speeds to ensure that all fan speeds are contained in the analysis sweep.

4.2.8 Calculation of Vibration Values to Report

4.2.8.1 Continuous Fan Speed Sweep

For continuous fan speed sweeps, analysis should focus on the ramped fan speed region of the recording and thus recordings should be edited to include less than 500ms of starting and ending fan speeds prior to calculation of vibration values.

For continuous fan speed sweep recordings, the following vibration values shall be calculated:

- Mean Peak-hold Spectrum. For each accelerometer channel, a spectrum vs. time shall be calculated using an FFT with the following properties:
    - Window size set to the first factor of two where the frequency resolution is equal to or less than 6Hz.
    - Hanning window
    - ≥75% overlap of FFT windows
    - RMS amplitude scaling

  Next the maximum value measured in each frequency bin shall define the peak-hold spectrum for a single accelerometer channel. Finally, the mean of peak-hold spectrums for four accelerometer channels shall be calculated as the mean peak-hold spectrum. One spectrum shall be calculated for each fan sample.

- Mean Acceleration Level vs. % Maximum Fan Speed. In this calculation the recording shall be divided into RPM bins no smaller than 50 RPM's and no larger than 150 RPM's. In each of these RPM bins, acceleration level for each accelerometer channel shall be calculated using rectangular (real-time) time weighting. The mean of all four accelerometer channels shall be calculated for each frequency bin to obtain the mean acceleration level. The RPM bins shall then be scaled to the maximum thermal fan speed defined in *Section 4.1.1 General, Laboratory, and Sampling Requirements*.

4.2.9 Vibration Requirements

4.2.9.1 185mm by 60mm Continuous Fan Speed Sweep

For power supplies using the 185mm x 60mm form factor, peak-hold spectrum response of the continuous fan speed sweep shall be less than a frequency-dependent limit curve defined by vertices listed in *Table 4-8 Mean peak vibration spectrum limit line vertices for 185mm by 60mm*. A plot of the limit line composed of these vertices is shown in *Figure 4-6 Plot of mean peak vibration spectrum limit for 185mm by 60mm form factor.*

Table 4-8 Mean peak vibration spectrum limit line vertices for 185mm by 60mm

Mean Peak Vibration Spectrum Limit	
Frequency (Hz)	**Vibration Level (g)**
0	0
800	0.7
1250	0.7
1900	0.4
2500	0.4

Figure 4-6 Plot of mean peak vibration spectrum limit for 185mm by 60mm form factor.

4.2.9.2 185mm by 73.5mm Continuous Fan Speed Sweep Limit

For power supplies using the 185mm x 73.5mm form factor, peak-hold spectrum response of the continuous fan speed sweep shall be less than a frequency-dependent limit curve defined by vertices listed in *Table 4-9 Mean peak vibration spectrum limit line vertices for 185mm by 73.5mm form factor*. A plot of the limit line composed of these vertices is shown in *Figure 4-7 Plot of mean peak vibration spectrum limit for 185mm by 73.5mm form factor.*

Table 4-9 Mean peak vibration spectrum limit line vertices for 185mm by 73.5mm form factor

Mean Peak Vibration Spectrum Limit	
Frequency (Hz)	**Vibration Level (g)**
0	0
800	0.7
1250	0.7
1900	0.4
2500	0.4

Figure 4-7 Plot of mean peak vibration spectrum limit for 185mm by 73.5mm form factor

4.2.9.3 265mm by 73.5mm Continuous Fan Speed Sweep Limit

Power supplies developed in the 265mm x 73.5mm PSU form factor are designed for modular infrastructure platforms and shall not be restricted to a vibration limit beyond the general requirements that the PSU induce no bumps, squeaks, or rattles and the fan shall meet the balance grade requirements of *Section 4.2.9.4 Fan Balance Requirements*. Continuous fan sweep vibration levels shall be made available to system integrators on request.

4.2.9.4 Fan Balance Requirements

In addition to PSU requirements, each fan shall meet ISO1940 Balance Grade G5.2 or better. This fan balance grade will help ensure that the PSU meets continuous fan sweep vibration and acoustical requirements.

4.2.10 Reporting Requirements

Fan and PSU identification reporting requirements shall be the same as *Section 4.1.10 Reporting Requirements.*

For continuous fan sweep mode, the following items shall be reported:

- Plot of Mean Peak-Hold Spectrum with overlay of Mean Peak Vibration Limit indicating compliance with the spec. Report one plot for each fan vendor model tested.
- Plot of Mean Acceleration Level vs. % of Maximum Fan Speed. One plot per fan model that includes each mean acceleration level curve.

5 Electrical Input Requirements

5.1 High Voltage AC/DC Input Requirements

5.1.1 Power Factor and iTHD

The power supply must meet the power factor and current iTHD requirements are stated below. These requirements are within the Energy Star® Program Requirements for Computer Servers.

Table 5-1 Power factor requirements

Output power	10% load	20% load	50% load	100% load
Power factor 249VAC to 305VAC 50/60Hz	> 0.92	> 0.96	> 0.98	> 0.99
Power factor 240VAC 50/60Hz				
Power factor 230VAC 50/60Hz				
Power factor 208VAC 50/60Hz				
Power factor 120VAC 60Hz				
Power Factor 100VAC 50Hz				

Table 5-2 iTHD requirements

% Input Current	0%	5%	10%	20%	50%	100%
iTHD (240VAC, 50Hz) for PSUs ≥ 1500W 240VAC	40.0%	25.0%	10.0%	7.5%	5.0%	4.0%
iTHD (230VAC, 50Hz) for PSUs ≥ 1500W 230VAC	40.0%	25.0%	10.0%	7.5%	5.0%	4.0%
iTHD (208VAC, 60Hz) for PSUs ≥ 1500W 208VAC	40.0%	25.0%	10.0%	7.5%	5.0%	4.0%
iTHD for PSUs < 1500W 240VAC 50Hz	40.0%	25.0%	8.5%	7.5%	5.0%	3.5%
iTHD for PSUs < 1500W 230VAC 50Hz	40.0%	25.0%	8.5%	7.5%	5.0%	3.5%
iTHD for PSUs < 1500W 208VAC 60Hz	40.0%	25.0%	8.5%	7.5%	5.0%	3.5%
For all PSU Capacities 120Vac 60Hz	40.0%	25.0%	10.0%	7.5%	5.0%	4.0%
For all PSU Capacities 277Vac 60Hz	40.0%	25.0%	20.0%	15.0%	8.0%	5.0%
For all PSU Capacities 305Vac 60Hz	40.0%	35.0%	30.0%	20.0%	10.0%	8.0%

Notes:

1. Tested according to Generalized Internal Power Supply Efficiency Testing Protocol. This is posted at http://www.plugloadsolutions.com/80pluspowersupplies.aspx

2. No single harmonic should exceed 80% of the total harmonic distortion and shall be guaranteed by design.
3. iTHD validation should be done by setting the load from No Load to 100% Load (or 100% to No Load) in steps of 5%. At each point iTHD and Input Current should be recorded in addition to Input Voltage, Power Factor, Output Load Current etc. Then a graph should be plotted for iTHD vs Input Current.
4. iTHD should also be validated at each design stage at 100Vac / 60 Hz and 200Vac / 50Hz.
5. Actual value of Input Current (RMS) should be calculated for each PSU based on it's rated currents at 120Vac / 60Hz, 240Vac / 50Hz, 277Vac / 50Hz, 305Vac / 50Hz

Figure 5-1 iTHD requirements

5.1.2 Inlet Connector

The AC input connector shall be an IEC 320 C-22, IEC 320 C-20 connector may be used upon request from the costumer for environment conditions where the exhaust temperature of the power supply will not exceed 70C. This inlet is rated for 16A/250VAC. Additionally an IEC 320 C-14 can be used for input currents up to 10A/250VAC. IEC320-C16 can be used to support higher exhaust temperatures in the power supply at 10 Amperes.

For 277VAC/380VDC connector vendors and part numbers refer to: documentation of connector vendors and part numbers located at DC-MHS Connector Information.

5.1.3 Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage ranges. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits.

Table 5-3 AC Input voltage ranges

PARAMETER	MIN	RATED	V_{MAX}	Startup VAC[2]	Power Off VAC
Voltage (240 V_{RMS})	180 V_{RMS}	200-240 V_{RMS}	264 V_{RMS}	174V_{RMS} – 180V_{RMS}	169V_{RMS}– 175V_{RMS}
Voltage (Wide range)	90 V_{RMS}	120/240 V_{RMS}	264 V_{RMS}	84V_{RMS} – 90V_{RMS}	79V_{RMS} – 85V_{RMS}
Voltage (277 V_{RMS})	249 V_{rms}[1]	277 V_{RMS}	305 V_{RMS}	243V_{RMS} – 249V_{RMS}	238V_{RMS} – 244V_{RMS}
Frequency	47 Hz	50/60	63 Hz		

Notes:

1. 277VAC input power supply's efficiency shall be tested at 277Vac, 50Hz.
2. Start up and Power Off voltage levels must always have a 5V_{RMS} hysteresis.
3. Maximum input currents are defined on individual design specifications per model.

Application of an input voltage below the power off threshold shall not cause damage to the power supply, including a blown fuse.

5.1.3.1 Crest Factor

The PSU shall be capable of starting and operating at Minimum Turn-On Voltage and Maximum Operating Voltage with Crest Factors (C.F.) between 1.1 and 1.5 (both inclusive) of the Input Waveform. In either case the PSU continues to operate but PSU performance may not meet the specification requirements such as but not limited to – iTHD, Power Factor, efficiency, output voltage regulation and ripple, dynamic load response. Crest factor (C.F.) is defined as the ratio of Peak Voltage to RMS Voltage of the Input Sinewave. CF Test should be done using both waveforms – Clipped Sinewave and AC Sinewave with Peak at the top. The input voltage shall be provided by a programmable source capable of providing a clipped AC waveform and an AC Sinewave with peak at the top shown in the figure below.

Figure 5-2 Crest factor examples

Note: More reference waveforms are described in *Supplemental Material M. Reference Distorted Waveforms*.

5.1.3.2 240VDC/380VDC

The power supply must be able to operate normally with 240VDC input.

- Operating range: 192VDC to 310VDC
- PMBus commands must function normally
- Power timing requirements met during power cycling
- Output power requirements support for same equivalent RMS AC input voltage
- LED functioning correctly
- In Always Standby mode in a 1+1 PSU configuration the active PSU will have >95% load, the Standby PSU will have <5% load
- In 1+1 PSU configuration and one PSU Active and the other in Always Standby mode; if the Active PSU fails the Standby PSU must support the load to maintain output voltage > 11.20V. Tested with 2,200uF 12V capacitance.
- For slow input voltage ramp.
- turn ON input voltage: 180VDC / 192VDC (MIN/MAX)
- turn OFF input voltage: 175VDC / 187VDC (MIN/MAX)

Table 5-4 DC input voltage ranges

PARAMETER	MIN	RATED	V_{MAX}	Startup VDC	Power Off VDC
Voltage (240 V_{DC})	192 V_{DC}	200-240 V_{DC}	310 V_{DC}	180V_{DC} – 192V_{DC}	175V_{DC} – 187V_{DC}
Voltage (380 V_{DC})	260 V_{DC}	336 V_{DC}	400 V_{DC}	254V_{DC} – 260V_{DC}	249V_{DC} – 255V_{DC}
Hysteresis				5 V	5 V

5.1.4 Line Isolation Requirements

The power supply shall meet all safety agency requirements for dielectric strength. Transformers' isolation for AC mains between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used. The insulation system must comply with reinforced insulation per safety standard IEC 62368-1. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 62368-1 spacing requirements.

Note: This test shall be done only during development.

5.1.5 Line Dropout/Holdup

5.1.5.1 Main output

An AC/DC line dropout is defined to be when the AC/DC input drops to 0$V_{AC/DC}$ at any phase of the AC/DC line for any length of time. During an AC/DC dropout the power supply must meet dynamic voltage regulation requirements. An AC/DC line dropout of any duration shall not cause tripping of control signals or protection circuits other than the SMBAlert# signal. If the AC/DC dropout lasts longer than the holdup

time the power supply should recover and meet all turn on requirements. The power supply shall meet the AC/DC dropout requirement overrated AC/DC voltages and frequencies. A dropout of the AC/DC line for any duration shall not cause damage to the power supply.

Table 5-5 AC/DC, 240VDC and HVDC holdup / dropout

Loading during AC/DC dropout / holdup	Holdup time / Dropout duration[1] (T_{pwok_holdup} + T_{pwok_off})
100% of rated load	11msec (10ms + 1ms)
45% of rated load	20ms (19ms + 1ms)
22.5% of rated load	40ms (39ms + 1ms)
11.3% of rated load	80ms (79ms + 1ms)

Notes:

1. This must be proven by calculation using the worst capacitance tolerance, variance with temperature and bus voltage. It shall be tested with a bulk capacitor having the minimum capacitance tolerance, at worst case loading and at worst case AC voltage conditions.

5.1.5.2 Auxiliary (Stand-by) Output

The 12VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of 70ms min (=12VSB holdup time) at 70% of max load and 150ms minimum at 1 Ampere of load whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

5.1.6 Line Fuse

The power supply shall have one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing shall be acceptable for all safety agency requirements including adequate breaking capacity. The input fuse shall be a High breaking capacity and fast blow type in accordance with IEC 60127 series. AC/DC inrush current shall not cause the AC/DC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC/DC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

Additionally, the power supply shall incorporate an input over current warning feature as described in *Section 8.4 Input Over Current Protection.*

5.1.7 Inrush Current

AC line inrush current shall not exceed 35A peak ignoring the initial 500us of the EMI filter charge, for up to one-half of the AC cycle, after which the power supply is allowed to have a secondary inrush event for up to PSU model label current rating Amperes and lasting for up to 2500ms, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).
The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (Top).

5.1.7.1 Cold Start Inrush Current With PSON# asserted

The PSU Input Current during a Cold Start event (with PSON# in asserted state) should follow the timing diagram below.

Figure 5-3 Inrush condition at cold start with PSON# asserted

At any point during this event input current should meet I vs t profile shown below (excluding the charging current of EMI Caps if the duration of the peak is ≤ 500µs)

Figure 5-4 I vs T profile of the PSU input current

Notes:

1. After power on, the peak current for 1st ½ cycle (Initial Inrush current) should meet the peak value requirement called out in individual M-CRPS Design Specification.
2. Secondary Inrush Current should meet the requirement called out for Maximum Rated RMS Current defined in the M-CRPS Design Specification. During the Secondary Inrush Event, the peak current can exceed the RMS Value as long as the peaks are less than 300% of Maximum Rated RMS Current defined in the M-CRPS Design Specification and are within the I vs T Profile of the PSU shown in *Figure 5-4*.

5.1.7.2 Cold Start Inrush Current With PSON# de-asserted

The PSU Input Current during a Cold Start event (with PSON# in De-Asserted state) should follow the timing diagram below.

Figure 5-5 Cold start inrush current with PSON# de-asserted

5.1.7.3 Re-rush Current

In addition to the Inrush Requirements, the Re-Rush current profile on the PSU should satisfy the following requirements when the Input Voltage is applied after an Input Brown out / Black Out event. The re-application of the Input Voltage can happen at the Peak of the Input Waveform at Maximum Specified Operating Voltage. The values defined below are true over the Operating Input Voltage, Frequency, Load Capacity and Temperature Range of the PSU. The re-rush condition shall meet the timing and duration of the figure below.

Figure 5-6 Re-rush current and timing

The RMS Value of the Re-Rush Current will not exceed 5 x Maximum PSU Rating over ½ Cycle of Input Frequency, 3.5 x Maximum PSU Rating over 1 Cycle of Input Frequency. In addition, the Input Current of the PSU should settle to a value less than or equal to 2 x Maximum PSU Rating of the PSU within 2 Cycles of the Input Frequency after the AC Input is applied.

The secondary Inrush Current Event if present should be over within 1000ms after the initial 3 cycles of re-application of Input. The RMS value of this Secondary Inrush Current should not exceed 2 x Maximum Rated Input Current of the PSU as measured during any 100ms interval within the 1000ms period. Maximum of 2 such intervals are permitted during this 1000ms period. After 1000ms the Input Current of the PSU should be less than or equal to the Maximum Rated Current Rating of the PSU.

At any point during this event, input current should fit under the profile shown in *Figure 5-4 I vs T profile of the PSU input current*.

5.1.8 Inrush Current High Voltage DC Input

For PSUs operating with HVDC Input Voltage, Initial Inrush, Secondary Inrush and Re-Rush Current is defined below:

Figure 5-7 I vs T Pulse Profile for DC Input

Note: For pulse duration T50 < 0.5 ms, the inrush and re-rush current is not considered due to too low "energy content" to trip a protective device (Per ETSI EN 300 132-3-1 Section 9.1).

Maximum inrush current characteristics for Telecommunications and Datacom (ICT) equipment at nominal voltage and maximum load:

Figure 5-8 I vs T profile for High Voltage DC input at nominal voltage

5.1.9 Line Transient Specification

AC line transient conditions shall be defined as "sag" and "surge" conditions. "Sag" conditions are also commonly referred to as "brownout", these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. "Surge" will be defined to refer to conditions when the AC line voltage rises above nominal voltage. The power supply shall meet the requirements under the following AC line sag and surge conditions.

Figure 5-9 100VAC/200VAC input brown-out behavior

Note: This test shall be done only during development at full load.

Figure 5-10 200VAC/277VAC input brown-out behavior

Note: This test shall be done only during development at full load.

Figure 5-11 277VAC input brown-out behavior

Note: This test shall be done only during development at full load.

Figure 5-12 240VDC (192VDC - 288VDC) China Telecom DC input range

Note: This test shall be done only during development at full load.

Figure 5-13 260VDC - 400VDC ETSI DC input range

Note: This test shall be done only during development at full load.

Table 5-6 AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0.5ms to ½ AC cycle[3]	35%	Maximum of nominal AC Voltages	50/60Hz	No loss of function or performance

Note:

1. During these tests, the load should be set to 50% of maximum load.
2. Value of input voltage is defined in design spec for 10% and 35% surge levels.
3. 25% surge 0.5ms to ½ AC cycle for 277VAC input M-CRPS.

Additional requirements are described in *Supplemental Material Q Additional Requirements on Input Line Transients*.

5.1.10 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 5-7 Performance criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

5.1.11 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55035:2017/A11:2020 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria A defined in Annex B of CISPR 24.

5.1.12 Fast Transient/Burst

The power supply shall comply with the limits defined in EN 55035:2017/A11:2020 using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria A defined in Annex B of CISPR 24.

5.1.13 Radiated Immunity

The power supply shall comply with the limits defined in EN 55035:2017/A11:2020 using the IEC 61000-4-3: Edition 2.1: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24.

5.1.14 Surge Immunity

The power supply shall be tested with the system for immunity to AC Unidirectional wave as shown in the table below per EN 55035:2017/A11:2020, IEC 61000-4-5:2014+A1:2017.
The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

Table 5-8 Surge immunity requirements

Condition	Surge immunity (for EN55035)	Surge immunity (GR-1089)[2,3]
Line to ground (tested for design margin)	2.5kV	2.5kV for AC input
Line to line (tested for design margin)	1.5kV	2.5kV for AC input

Notes:

1. Margin test shall be conducted only during development.
2. Tests shall be conducted using 2Ω impedance for generator for both AC and -48Vdc Input PSUs as defined in GR-1089.
3. AC/DC Input PSUs - for Phase to Neutral, Phase to Ground, Neutral to Ground per requirement of GR1089 Table 4.2 items 20 (AC Power ports with SPD), items 23 (DC power ports).

The power supply shall comply with the limits defined in EN 55035:2017/A11:2020 with 500V margin using the IEC 61000-4-5:2014+A1:2017 test standard and performance criteria A defined in Annex B of CISPR 35.

5.1.15 Voltage Interruptions

The power supply shall comply with the limits defined in EN 55035:2017/A11:2020 using the IEC 61000-4-11: Second Edition: 2004-03 test standard and performance criteria defined in Annex B of CISPR 35.

5.1.16 Power Recovery

The power supply shall recover automatically after an AC/DC power failure. AC/DC power failure is defined to be any loss of AC power that exceeds the dropout criteria stated in section *5.1.5 Line Dropout/Holdup*.

Although the power supply may power off under conditions described in this section, it must be capable of restarting, either automatically or under program control after the disturbance. In addition, the power supply should not be in a latched state such that any of the operator buttons/switches do not operate correctly after the disturbance. At no time should the AC/DC power cord have to be removed to clear an error condition.

Auto restart conditions are tested from –40% to –100% Input under voltage conditions for time intervals ranging from 25ms to 2 seconds.

These tests are performed at both the lowest and highest nominal operating voltages of the power supply.

Time intervals: 25ms, 40ms, 60ms, 90ms, 130ms, 200ms, 280ms, 400ms, 600ms, 900ms, 1.3s, and 2.0s

Under voltage deviation from nominal AC voltage: -40%, -50%, -60%, -70%, -80%, -90%, -100% In a temporary AC input power outage situation (dropout/brownout/blackout), the power supply will be able to automatically restart under any load, once the PSON# signal is asserted LOW. This is true even under a condition such as the PSON# signal de-asserts (HIGH) and then asserts (LOW) during the temporary power outage period. This toggling of the PSON# signal can happen at any interval and may repeat during the temporary power outage period.

5.1.17 Minimum Input Inductance

The power supply shall have a minimum input inductance (*Lin*) specified in table below when operating with a voltage range defined in *Table 5-4 DC input voltage ranges.*

Table 5-9 Minimum input inductance for High Voltage DC input power supplies

PARAMETER	MIN
Input inductance (*Lin*)	11mH/kW

Note: The recommended approach to determine the input inductance (*Lin*) of the power supply is shown below in *Supplemental Material O DC input impedance measurement procedure.*

5.2 Low Voltage +54VDC Input Requirements (Rack Power Input)

5.2.1 Inlet Connector

The power supply shall have a 100A power blade type connector defined in *Section 2.4.3 +54VDC Input (Rack Power Input)*.

5.2.2 Input Voltage Specification

The power supply must be able to operate normally with +54VDC input.

- Operating range: 40 VDC to 60 VDC
- PMBus commands must function normally
- Power timing requirements met during power cycling
- LED functioning correctly

- In Always Standby mode in a 1+1 PSU configuration the active PSU will have >95% load, the Standby PSU will have <5% load
- In 1+1 PSU configuration and one PSU Active and the other in Always Standby mode; if the Active PSU fails the Standby PSU must support the load to maintain output voltage > 11.20V. Tested with 2,200uF 12V capacitance.
- turn ON input voltage: 38 VDC / 40 VDC (MIN/MAX)
- turn OFF input voltage: 37 VDC / 39 VDC (MIN/MAX)

Table 5-10 +54VDC input voltage specification

PARAMETER	MIN	Typical	V_{MAX}	Startup VDC	Power Off V DC
Steady state voltage	40 V_{DC}	54 V_{DC}	60 V_{DC}	38 VDC – 40 VDC	37 VDC – 39 VDC
Transient state voltage	40 V_{DC}	54 V_{DC}	60 V_{DC}	NA	NA

5.2.3 Fuse

Input fusing shall be provided at the input of the PSU.

5.2.4 Inrush Current

Hot swap/inrush controller MOSFET shall be used to avoid arcing at insertion. Capacitors in front of the Hot Swap Controller shall be avoided. Sense +/- (short pins in the input connector) shall be used to turn ON/OFF the Hot Swap Controller (Inrush switch MOSFETs) to avoid arcing during the insertion and extraction operations.

5.2.5 Transients Requirements

Voltage transitions could take place when the power source transitions from/to the backup power. The input power circuitry must be fully functional during the input voltage transitions, i.e., the input capacitor should be sized properly, and the hot swap controller protection levels should be set correctly to avoid protection tripping during voltage transitions. The maximum voltage slew rate during the transitions is listed below:

Table 5-11 Maximum voltage slew rate during input transient events.

PARAMETER	Slew rate (V/ms)
Ramp up rate	30
Ramp down rate	10

5.2.6 Susceptibility Requirements

Not applicable to this type of power supply.

5.2.7 Input Dropout/Holdup

5.2.7.1 Main output

A DC input dropout is defined to be when the DC input drops to $0V_{DC}$ for any length of time. During an DC dropout the power supply must meet dynamic voltage regulation requirements. A DC input dropout of

any duration shall not cause tripping of control signals or protection circuits other than the SMBAlert# signal. If the DC dropout lasts longer than the specified holdup time in *Table 5-12 +54VDC input power supply holdup / dropout* below the power supply should recover and meet all turn ON requirements. The power supply shall meet the DC dropout requirement overrated DC voltages. A dropout of the DC input for any duration shall not cause damage to the power supply.

Table 5-12 +54VDC input power supply holdup / dropout

Loading during AC/DC dropout / holdup	Minimum Holdup time / Dropout duration[1]
0% to 100% of rated load	1 msec

Notes:

1. This must be proven by calculation using the worst capacitance tolerance, variance with temperature and bus voltage. It shall be tested with a bulk capacitor having the minimum capacitance tolerance, at worst case loading and at worst case DC voltage conditions.

5.2.7.2 Auxiliary (Stand-by) Output

The +54VDC input M-CRPS shall have an auxiliary (Stand-by) 12V output rail as described in *Section 7.3 Auxiliary (Stand-by) Output*, timing in *Section 7.15 Timing Requirements* and follow the requirements in *Section 8 Protection Circuits* for the Auxiliary output Over Current Protection.

5.2.8 Input Ripple Voltage

The maximum ripple voltage on the input bus (generated from the source & infrastructure) shall be 1Vpp (peak to peak) as measured at the PSU terminals measured at 20MHz bandwidth. The PSU should consider this ripple as normal operating range, if the ripple is outside this range the performance may be degraded. If the PSU continues to operate outside the range, it should operate safely.

5.2.9 Isolation Requirements

Isolation between input and output is not required in this type of power supply.

5.3 Low Voltage -48VDC Input Requirements (Telecom)

This type of power supply is intended to be in a Telecom environment, due to this, compliance with NEBS specification is required, please see *Section 14.5 Telecommunications DC Mains Powered Power Supplies*.

5.3.1 Inlet Connector

Please refer to *Figure 2-21 -48VDC inlet connector example (Telecom)*

5.3.2 Input Voltage Specification

Table 5-13 -48VDC power supply Input voltage range

PARAMETER	MIN	RATED	V_{MAX}	Startup VDC	Power Off VDC
Voltage (-48 V_{DC})	-40 V_{DC}	-48 V_{DC} – -60 V_{DC}	-72 V_{DC}	-38 V_{DC} – 40 V_{DC}	-37 V_{DC} – -39 V_{DC}
Hysteresis				1V	1V

5.3.3 Minimum Input Inductance

The power supply shall have a minimum input inductance (*Lin*) specified in table below when operating with a voltage range defined in *Table 5-13 -48VDC power supply Input voltage range.*

Table 5-14 Minimum input inductance for -48VDC input power supplies

PARAMETER	MIN
Input inductance (*Lin*)	11mH/kW

Note: The recommended approach to determine the input inductance (*Lin*) of the power supply is shown below in *Supplemental Material O DC input impedance measurement procedure.*

5.3.4 Input Impedance

The power supply vendor shall measure and characterize the input impedance of the power supply following the procedure described in *Supplemental Material O. DC input impedance measurement procedure.*

5.3.5 Inrush Current

For power supplies used in telecommunication applications (operating on -48VDC nominal), the Initial Inrush, secondary Inrush and Re-Rush current the ratio of the instantaneous inrush current It to maximum steady state current ***Im*** at interface "A", when the switch is closed within the normal service voltage range, shall not exceed the limits shown in *Figure 5-14 I vs T Profile for -48VDC Input power supply at nominal voltage and maximum load.*

The parameters are defined as follows:

- ***It*:** inrush current (magnitude of instantaneous value).
- ***Im*:** maximum steady state input current for a fully equipped equipment under test connected to interface "A", at nominal voltage.

The power generator for Inrush current test shall be in accordance with CENELEC EN 61000-4-29.
Performance criteria:

- Below 0.1 ms, the inrush current is not defined.
- Below 0.9 ms the ***It/Im*** ratio shall be lower than 48.
- Above 1 ms: the curve corresponds to the maximum tripping limit of the majority of existing protective devices.

Maximum inrush current characteristics for Telecommunications and Datacom (ICT) equipment at nominal voltage and maximum load:

Figure 5-14 I vs T Profile for -48VDC Input power supply at nominal voltage and maximum load

Note: Refer to ETSI EN 300 132-2 V2.5.1 (2016-10) for measurement set-up.

Re-rush Current (DC input) is defined as the input peak current (duration >0.5mS) due to Multiple Input Dropouts of intervals from 10ms up to 100ms and the input coming back at -48VDC with dv/dt = 10 V/us.

5.3.6 Fuse

The power supply must have internal primary overcurrent protection. A fuse type acceptable for all safety agencies' requirements and placed in the input circuit, including adequate breaking capacity in accordance with IEC 60127 series. The fuse is not to be considered replaceable for the purposes of determining power supply reliability and life as specified in *Section 13 Reliability.* The fuse shall not open in any transient condition but only in an internal failure of the power supply.

5.3.7 Reversed Polarity Protection

Reversed polarity protection is required for a -48VDC input Telecom power supply. No damage shall occur to the power supply however shutdown is acceptable. Restoring the correct input polarity shall restore full functionality of the power supply.

5.3.8 Input dv/dt

The PSU while operating on a DC input shall be able to sustain a dv/dt defined in *Table 5-15 Input dv/dt during* Turn-On and Turn-Off and during input line transients including input voltage sags and surges. The value of dv/dt should be guaranteed by design (by including data on dv/dt and di/dt of all components exposed to input dv/dt).

Table 5-15 Input dv/dt

Parameter	Max
Input dv/dt	10 V/us

5.3.9 Input Ripple Voltage

While operating on a DC input, the maximum ripple voltage on the input bus (generated from the source & infrastructure) shall be 1% peak-peak of the operating voltage as measured at the PSU terminals. The frequency of the input ripple voltage is 94 Hz – 126Hz. The PSU should consider this ripple as normal operating range, if the ripple is outside this range the performance may be degraded. If the PSU continues to operate outside the range, it should operate safely.

5.3.10 Input Reflected Ripple Current

While operating on DC Input, the pk-pk ripple current as seen on the PSU input from 10% load to 100% load shall be less than 10% of the maximum DC Input Current specified in the Design Specification for individual PSU, at loads below 10%, the value is 30% of the maximum DC Input Current specified in the Design Specification for individual PSU with input ripple voltage defined above.

The Input Current ripple will be measured with scope bandwidth limited to 1 MHz.

5.3.11 Surge Immunity

Compliance with NEBS specification is required. See *Section 14.5 Telecommunications DC Mains Powered Power Supplies* for more details.

Table 5-16 Surge immunity requirements

Condition	Surge immunity (GR-1089)[1,2]
Line to ground (tested for design margin)	1.5kV
Line to line (tested for design margin)	1.5kV

Notes:

1. Tests shall be conducted using 2Ω impedance for generator for both AC and -48Vdc Input PSUs as defined in GR-1089.
2. AC/DC Input PSUs - for Phase to Neutral, Phase to Ground, Neutral to Ground per requirement of GR1089 Table 4.2 items 20 (AC Power ports with SPD), items 23 (DC power ports).

5.3.12 Isolation Requirements

The power supply shall meet all safety agency requirements for dielectric strength. Transformers' isolation between primary and secondary windings must comply with the 2121VDC dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used. The insulation system must comply with reinforced insulation per safety standard IEC 62368-1. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 62368-1 spacing requirements.

Note: This test shall be done only during development.

6 Efficiency

6.1.1 High Voltage AC/DC Input Power Supplies

The power supply shall be tested for efficiency to meet efficiency levels of www.80plus.com for 230V Internal power supplies. There is a link to the testing protocol here; Generalized Test Protocol for Calculating the Energy Efficiency of Internal Ac-Dc and Dc-Dc Power Supplies revision 6.7. Output shall be loaded according to the proportional loading method defined by 80 Plus in Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.7. In these testing requirements the power supply is tested at 230VAC/60Hz input and does not include the losses of the PSU fan.

6.1.1.1 240VAC/240VDC and Wide Input Range

Table 6-1 Efficiency requirements for 240VAC/240VDC and wide input range power supplies

Loading[2]	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Titanium efficiency	Please refer to www.80plus.com, efficiency level specified in the Design specification for the specific M-CRPS model.			
Platinum efficiency				

Notes:

1. The M-CRPS efficiency shall be characterized using 230VAC, 115VAC and 60Hz using 1 Ampere step including and excluding the fan losses and using the 80PLUS setup and procedure.
2. Efficiency at 100% load and other input voltages with fan power included is defined in the PSU design specifications.

6.1.1.2 277VAC/380VDC Input

Table 6-2 Efficiency requirements for 277VAC/380VDC power supplies

Loading[4]	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Titanium efficiency	Please refer to www.80plus.com, efficiency level specified in the Design specification for the specific M-CRPS model.			
Platinum efficiency				

Notes:

1. Titanium efficiency certificate is required for 380VDC input power supplies.
2. Efficiency test in 80PLUS is required for 277VAC input power supplies and post the result in 80PLUS appropriated section.
3. The M-CRPS efficiency shall be characterized using 230VAC, 115VAC and 60Hz using 1 Ampere step including and excluding the fan losses and using the 80PLUS setup and procedure.
4. Efficiency at 100% load and other input voltages with fan power included is defined in the PSU design specifications.

6.1.2 Low Voltage DC Input Power Supplies

The subsections provide the required minimum efficiency levels at various loading conditions for power supplies with low input voltage. These are provided at different load levels; 100%, 50%, 20%, and 10%.

6.1.2.1 +54VDC Input

Table 6-3 Efficiency requirements for +54VDC input power supplies

100% of maximum	50% of maximum	20% of maximum	10% of maximum
95%	96%	94%	90%

Notes:

1. Tested at +51VDC and +54VDC.
2. Efficiency test shall be conducted excluding the losses of the PSU fan.
3. Efficiency with different input voltages with fan power included is defined in the PSU design specifications.

6.1.2.2 -48VDC Input (Telecom)

Table 6-4 Efficiency requirements for -48VDC (Telecom) input power supplies

100% of maximum[3]	50% of maximum	20% of maximum	10% of maximum
92%[2]	94%	90%	85%

Notes:

1. Tested at -48VDC.
2. Efficiency test shall be conducted excluding the losses of the PSU fan.
3. Efficiency at -40VDC input with 100% load shall be at least 91% including the fan losses.
4. Efficiency with different input voltages with fan power included is defined in the PSU design specifications.

7 Output Requirements

7.1 Output Power/Currents

The following tables define the minimum power and current ratings. The power supply must meet both static and dynamic voltage regulation requirements for all conditions.

Table 7-1 Load requirements

Output	Input voltage	Min. (A)	PL1 Max. Continuous[4] (A)	PL2[2] (%)	PL3[3] (%)	PL4 (%)[7]
12V main	200-240 VAC	0.0	PSU rating	115%	155%	165%
12V main (wide input range)	100-240 VAC	0.0	PSU rating	115%	155%	165%
54V main	200-240 VAC	0.0	PSU rating	115%	155%	165%
54V main[6]	54 VDC	0.0	PSU Rating	115%	155%	165%
12VSB [1]	100-240	0.0	3.0	113%	NA	NA
Peak Ride Through			NA	20 s	10 ms	1.9 ms
Peak Response Ride Through			NA	Dependent on OTW	5 ms	100 us
Total Peak Time			NA	>= 20 s	15 ms	2 ms
Duty Cycle			NA	Not defined	25%	
PMBus STATUS registers Trigger Method			Moving Average: PL2	OTW	Timer: PL3 Peak ride through (10 ms)	Timer: PL4 Peak ride through (1.9 ms)

			Peak ride through (20 s)			

Notes:

1. 12VSB must provide 6.0A when two power supplies are connected in parallel and are within the regulation limits, before this the load shall be kept at 3A maximum. The Fan may work when Standby current >1.5A and the ambient temperature is higher than 35C.
2. PL2 Peak load duration is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration shall be 20 seconds without asserting the SMBAlert# signal at maximum operating temperature. The power supply shall support 115% of its rating, however any load between 101% to 115% is considered PL2 level for definition purposes. PL2 level support shall be 115% of the maximum output rating at any given input voltage and change dynamically based on the declared input voltage ranges.
3. PL3 peak duty cycle test shall be 25%; 4msec at PL3 / 12msec at PL2 Peak and repeat for 1 second. Applying a PL3 peak load must not trip the SMBAlert# signal. The maximum length of time the PL3 peak must be supported is based on the SMBAlert# signal asserting. The PSU must support this peak load for 5msec after SMBAlert# asserts. The power supply shall support 155% of its rating, however any load between 116% to 155% is considered PL3 for timer start purposes. If this peak load pattern continues indefinitely the power supply shall protect itself by tripping its thermal sensor. PL3 level support shall be 155% of the maximum rating using the highest voltage of low and high line as reference.
4. When applying a repetitive or non-repetitive transient load profile, the effective Iavg load must never exceed the maximum current rating as stated on PL1.
5. Refer to *Section 8.1.2 Averaging Mechanism* for more details about the averaging algorithm, accuracy, and timing.
6. This power supply is intended for pass-through applications using a power shelf and bus bar in the rack, and a Hot Swap Controller inside the power supply module.
7. The power supply shall support 165% of its rating, however any load between 156% to 165% is considered PL4 for timer start purposes. PL4 level support shall be 165% of the maximum rating using the highest voltage of low and high line as reference.

Figure 7-1 PSU Peak power timing example

Notes:

1. After an SMBAlert# assertion caused by a PL4 event the default behavior is to assert (keep low) for 150ms then release the SMBAlert# signal.
2. Clear command shall be sent to the M-CRPS to de-assert SMBAlert# prior to a PL4 event to be able to send the notification to the system when PL4 event happens by asserting SMBAlert# back again when bit SMBAlertPL4Behavior of register 001Ah in *Table 12-75 Miscellaneous configuration block* is in 1.

7.2 Peak Load Protection

For peak loads above the PL3 peak load level the PSU may assert the SMBAlert# signal to shorten the duration of the peak load to < 2msec. For peak loads up to PL3 peak load level the PSU must not assert SMBAlert# if the peak load duration is <10msec. If the peak load last longer than 10msec the PSU may assert SMBAlert# to throttle the load within 15msec. Below are PSU requirements for peak load conditions.

Table 7-2 Peak load protection testing conditions

Peak Load	Peak current	System capacitance	SMBAlert# timing	Peak load duration
PL4	Rated+65% (165%)	3,300µF	1.9msec	2ms

7.3 Auxiliary (Stand-by) Output

The 12VSB output shall be present when an AC input greater than the power supply turn on voltage is applied. There should be load sharing in the standby rail using the specified output voltage droop in *Table*

7-3 Output voltage droop characteristics and shown in *Figure 7-2 Typical 12VSB droop share* characteristics.

Table 7-3 Output voltage droop characteristics

Parameter	Min.	Typical	Max.	Units
Output voltage droop	145	150	155	mV/A

Figure 7-2 Typical 12VSB droop share characteristics (center green line), and worst case (top orange and bottom yellow lines).

Notes:

1. Voltage calibration setpoint shall be 12.075V at 1.5Amps load.
2. Tolerance shall be ±40mV at 1.5Amps load.
3. It is recommended to have a transfer switch between the 12Vmain output and the 12VSB output as described in *Section 7.17 12V Internal Transfer Switch.*
4. The droop control shall be disabled when the transfer switch between the 12Vmain output and 12VSB output is ON.
5. For power supplies without transfer switch the droop control on the 12VSB output shall be disabled when the main output is enabled/ON.
6. For power supplies with transfer switch the 12VSB output shall be tested for static and dynamic regulation as well as OCP, Ripple & Noise, OCP, OVP, Short Circuit while keeping the PSON# de-asserted (Main output OFF), during transition of STBY load to Main bus voltage on STBY output shall not drop below 11.4V.
7. Worst case limits shall use WCEPTA guaranteed for 5 years, using -5°C to +55°C inlet temperature, for detailed data table to generate this plot please refer to the Design Specification.

7.4 Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state, for dynamic conditions see section *7.5 Dynamic Loading*. These limits include the peak-peak ripple/noise. These shall be measured at the output connectors.

Table 7-4 Voltage regulation limits

Parameter	Min.	Nom.	Max.	Units
+12V[1,4,6]	+12.06	+12.20	+12.34	V_{RMS}
+54V (High voltage input)[3,5,6]	+53.80	+54	+54.20	V_{RMS}
+54V (+54V input)[2,5,6]	+40.00	+54	+60.00	V_{RMS}
+12V SB[4,6]	+11.65	+12.00	+12.35	V_{RMS}

Notes:

1. Output voltage set point when the PSU is standalone shall be 12.2V ±40mV at 50% loading condition and vary from 12.06V at 100% loading condition to 12.34V at 0% loading condition measured at the mating connector. The droop bandwidth shall be equivalent to the +12Vmain voltage regulation loop.
2. This power supply is intended for pass-through applications using a power shelf and bus bar in the rack, and a Hot Swap Controller inside the power supply module. Minimum voltage is stated to handle the required current at maximum load and maximum voltage is stated for component voltage ratings.
3. Output voltage setpoint when the PSU is standalone shall be 54V ±140mV at 50% loading condition.
4. During turn ON the 12V M-CRPS Main output's overshoot shall not exceed 12.96V.
5. During turn ON the 54V M-CRPS Main output's overshoot shall not exceed 57.34V.
6. During turn OFF the 12V or 54V M-CRPS Main output's undershoot shall not exceed -0.3V.

7.5 Dynamic Loading

The output voltages shall remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the Peak load conditions.

Table 7-5 Transient load requirements

Output	Δ Step Load Size	Load Slew Rate	Test capacitive Load[3]	Regulation limits
+12V	100% of max load[1]	2.5 A/µsec	3,300µF	12V -8% / +8% (11.04V to 12.96V)
+12V	70% of max load[2]	2.5A/µsec	4,400µF	12V -6% / +6% (11.28V to 12.72V)
+12V	60% of max load[2]	2.5 A/µsec	1,000 µF	12V – 7% / +7% (11.16V to 12.84V)
+12V	60% of max load[2]	2.5 A/µsec	1x 2,200 µF	12V – 6% / +7% (11.28V to 12.84V)
+12V	60% of max load[2]	2.5 A/µsec	3x 2,200 µF	12V – 5% / +7% (11.40V to 12.84V)
+54V (High voltage input)	100% of max load[1]	1 A/µsec	1,000 µF	54V -8% / +8% (49.68V to 58.32V)
+54V (High voltage input)	50% of max load[5]	1 A/µsec	1,000 µF	54V – 5% / +5% (51.30V to 56.70V)
+54V (+54V input)[4]	Not applicant	Not applicant	Not applicant	Not applicant

+12VSB	1.0A	0.5 A/µsec	1,000 µF	12V -8% / +8% (11.04V to 12.96V)

Notes:

1. For 100% step dynamic condition it shall be tested from 5% to 105% loading.
2. For step loading condition +12V minimum loading is 5% of rated current and the step can be anywhere between 5% of rated current to max load. E.g., if the 100% load rated current of the power supply is 108 Amperes, then the minimum loading shall be 5.4 Amperes. If two power supplies are in parallel, then each power supply shall have 5% as minimum loading condition.
3. The capacitor type used for this test shall be Aluminum Electrolytic.
4. This power supply is intended for pass-through applications using a power shelf and bus bar in the rack, and a Hot Swap Controller inside the power supply module.
5. For step loading condition +54V minimum loading is 5% and can be anywhere between 5% to max load.
6. The voltage measurement shall be done at the output of the power supply.
7. Conditions in this table are for system designers to determine voltage limits under different external capacitance for various dynamic load steps.

Additionally, the power supply shall support the transient conditions stated in below table.

Table 7-6 Additional transient load requirements

Profile	Starting Load		End Load		Step Size %	Frequency Hz	Duty Cycle %	Load Slew Rate A/us
	%	Mode	%	Mode				
A[3]	70	CC	170	CC	100	100	20	2.5
B[3]	85	CR	170	CC	85	40	8	2.5
C	90	CC	140	CC	50	40	20	2.5
D[3]	77	CR	165	CC	88	28	40	2.5
E[4]	2	CC	52	CC	50	50	50	2.5
F	5	CC	105	CC	100	50	50	2.5
G[4]	0	CC	50	CC	50	50	50	2.5

Notes:

1. CC = Constant Current, CR = Constant Resistance.
2. For all test conditions the regulation limits are +-8% with 3,300uF.
3. The intent of this profile is to trigger the constant current mode of the M-CRPS.
4. Starting load below 5% is intended to cross the threshold current to turn ON the output synchronous rectifiers when the transient load is applied.

7.6 Capacitive Loading

The power supply shall be stable and meet all requirements with the following capacitive loading ranges.

Table 7-7 Capacitive loading conditions

Output	MIN	MAX	Units
+12VSB	270	4,700	µF
+12V	3,300[1]	70,000	µF
+54V (High voltage input)	100[1]	15,000	µF
+54V (+54VDC input)	100[1]	15,000	µF

Notes:

1. Minimum 2000uF capacitive load on this output is required to hold regulation during Cold Redundancy mode PSU failures and PSU hot swapping.

7.7 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC current.

7.8 Closed Loop Stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in *Section 7.6*. A minimum of 45 degrees phase margin and -10dB-gain margin over temperature is required using 0mF and 5mF of capacitance, in addition the test shall be performed with 70mF for exploratory purposes. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at 10%, 25%, 50% and 100% loading conditions. A gain of 20dB is desired at 100Hz and 120Hz for each one of the capacitances and loading conditions in AC to DC power supplies.

Table 7-8 Phase and gain margin requirements

Capacitance[1]	Load	Phase margin	Gain margin
0µF/5000µF	Min.[2] 10%, 25%, 50% and 100%	45°	-10dB
70,000µF	Min. [2] 10%, 25%, 50% and 100%	Characterization	Characterization

Notes:

1. The capacitor type used for this test shall be Aluminum Electrolytic.
2. Minimum load is 5% or the load at which PSU transitions from Burst Mode to Steady PWM If this is higher than 5%.

7.9 Residual Voltage Immunity in Standby Mode

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.
The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

7.10 Soft Starting

The Power Supply shall contain a control circuit which provides monotonic soft start for its outputs without overstress of the input line or any power supply components at any specified input line, output load conditions in combination with all capacitive loading conditions.

7.11 Zero Load Stability

When the power subsystem operates in a no-load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault. PSU should be unconditionally stable at No Load over Input Voltage and Temperature range and with zero and maximum external capacitance.

7.12 Hot Swap

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

> ***Note:*** +54VDC input power supplies do not have output hot swap capability due to the usage model.

7.13 Forced Load Sharing

The +12V output will have active load sharing using average plus droop control methods. The output shall share within <2% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to share load in parallel and operate in a hot swap / redundant 1+1, 2+1, 3+1 and 2+2 configurations. The 12VSB output is required to actively share current between power supplies (droop control). The 12VSB output of the power supplies are connected in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

The Ishare bus signal shall have a voltage setting of 8V at full load to accommodate a dynamic range of up to 16V for a 2x rated current measurement.

7.13.1 Current Share (Ishare)

The requirements for the Ishare signal are listed below.

- Vishare Output Accuracy: +/-0.5% of 16V @200% loading condition full scale plus +/-0.5% of reading.
- Vishare Output Bandwidth: 1 kHz +/-5%.
- Current Sharing method: Voltage Droop + Active Average.

- Current Sharing Accuracy: +/-2% individual PSU relative to total average (sample averaged over 20ms moving window for 500ms after change in load). The accuracy shall be based on the highest rating of the PSU (irrespective of at what input voltage range the PSU is operating).
- Output Voltage Adjusting Range/Clamping due to Current Sharing loop: +/-200 mV with +/-5% tolerance.
- Output Voltage Adjusting Resolution due to Current Sharing loop: <1mV, to cover low impedance Power Distribution Boards.

Table 7-9 Additional Requirements on current share behavior

Parameter	Value	Remarks
Gain at 1Hz	> 25dB	All parameters validated by Test at each stage during development using inter PSU board as 800µΩ (±10%). In addition, all parameters to be verified by calculation / simulation based in inter PSU impedance
Cross Over Frequency	100Hz (±5Hz)	
Gain Margin	-12dB	
Phase Margin	90 Degrees	
Output Clamp	+200mV (±10mV) / -200mV (±10mV)	
Vishare Ripple [Note 1]	100mV pk-pk	
Transient test for Load Step (Applicable load steps up to 100% for the defined profiles)	Settling Time (settling within +/-2% of final value) ≤ 10ms	
Response – Vishare_error (1V step) to 12Vmain	Settling Time (settling within +/-2% of final value) = 200ms ±50ms	

Notes:

1. Vishare ripple to be measured with BW limited to 10 kHz measured with a single PSU. This specification limit is not applicable when more than one PSU is sharing load.
2. Refer to *Calculator_Current Share Accuracy Capacity Interboard Impedance_12V.xlsx* and *Calculator_Current Share Accuracy Capacity Interboard Impedance_54V.xlsx* files placed here M-CRPS/Version 1p00/Electrical/ or guidance on how to calculate the current share accuracy in an unbalanced scenario

The following figure depicts the implementation of the average current share mechanism.

Figure 7-3 Digital control implementation of average current mode control

<u>Iout to Vimoni</u>

Scale: 8V @ 100% and 16V @200% of maximum rated capacity of Multi-Rated PSU.

DC Accuracy: ±1% of full scale plus ±1% of reading

Time Constant: 4us (40 kHz BW) ±5%

Signal Delay: <100ns ***Note:*** use the method shown in *Figure 9-9 Imon signal delay step response* to measure the delay

<u>Iout to Visharei</u>

Scale: 8V @ 100% and 16V @200% of maximum rated capacity of Multi-Rated PSU.

DC Accuracy: ±0.5% of full scale plus ±0.5% of reading

Time Constant: 160us (1 kHz BW) ±5%

Signal Delay: 1 ms ±5% ***Note:*** use the method shown in *Figure 9-9 Imon signal delay step response* to measure the delay

Implementation Considerations:

The voltage across R-Vishare should be detected by an analog differential amplifier. Feeding the two signals directly into an A/D converter, to process the signal digitally requires 8-10 bits resolution for the

Ishare error and would require 12-bit or more resolution for direct A/D measurements of Vishare external and internal.
Limiter should be implemented with an analog circuit, so the A/D converter will receive a delta signal of 200mV only, so an 8–10-bit converter can be used.
The converter voltage regulation loop must have the capability of adjusting the output voltage with a resolution better than 1mV for proper current sharing operation with low impedance between the PSUs. This would equate to minimum 14-bit resolution out of the 12.2V output. Depending on details of Voltage Regulation loop implementation this might require 12.2V out and 12.2V ref to be represented in the MCU calculation as 14–16-bit numbers.

Notes:

1. Time Constant is defined as the time it takes for the signal to reach 63.2% of the signal step.
2. In *Figure 7-3 Digital control implementation of average current mode control* above, at any point of this compensator, the value should not exceed +/- 200mV (anti-windup).

7.13.2 Main Output Voltage Regulation Droop

The main output voltage will have a droop characteristic. Droop is set at 200mV for 5%-95% of rated load (2.222mv / 1% load). A standalone PSU will have the output voltage factory set at 12.20V +/-30mV. A standalone PSU will have a voltage drop of 200mV with a load change from 5% to 95%, voltage measured on the PDB's mating power connector. Bandwidth for the droop shall be equivalent to the main rail voltage regulation loop. For load transients in an "N" parallel PSU system, the output voltage must stay within the Dynamic Regulation band.

7.13.3 Current Sharing Load Step Response

When using power supplies from the same vendor they shall have a maximum of 20% current deviation from the ideal value, recovering within 4% of the ideal value within 5ms, and when using power supplies from different vendors they shall have a maximum of 50% current deviation from the ideal value, recovering within 4% of the ideal within 10ms.

7.13.4 Current Share with Margining

PSU shall meet all Current Share requirements (including current sharing load step response) when Margin is enabled. For test purposes, Margin should be enabled before stating the load step. This requirement is applicable only when margin is enabled on all PSUs sharing the load. In case when margin on one or more PSUs operating in parallel is not enabled (PSUs are mis-matched in margin function), PSU/s shall not shutdown under any load profile (either steady state or transient load) defined in the specification and will support a load which within the defined boundary of PSU Load vs Timing Behavior. In such cases PSUs can operate in Constant Current mode to keep supporting the load.

When margin is enabled all pertinent output voltage parameters except OVP and UVP would shift with the same value as the margin.

The margin function is achieved via a PMBus command described in *Section 12.1.54 MFR_VOUT_MARGINING (EDh)* and should only be used on systems that require a level of voltage drop compensation, in place of a remote sense solution. This function is NOT intended for dynamically changing of the PSU output voltage and shall be set prior to enabling the main rail output voltage. The command when executed raises the +12.2V output to +12.4V of the main output.

When the command is issued prior to assertion of PSON# or after PSON# assertion but prior to PWOK assertion, +12Vmain output continues to rise at designed dv/dt and shall meet the rise time (Tvout_rise) as defined in section 7.15 of this document. Though NOT recommended, if the margin enable command is issued after PWOK assertion, +12Vmain output shall rise at a rate of 2mv/ms rate (±100uV/ms).
The execution of the command to be delayed by 2ms ((±100us).

Margin function will default to Low / Off after PWOK is de-asserted for any reason. Assertion of PWOK will default PSU to Margin Low / Off state until the system issues Margin enable command.

7.13.5 Current Share Activation

Average Current Sharing must be activated within 10ms from the PWOK signal being asserted. Current Sharing loop could be deactivated if the PSU output current is below 5% or if the current unbalance (PSU versus total load average) is below 1%

7.13.6 Ishare Disconnect Circuitry

Disconnect circuit ON resistance < 50 Ohm. The disconnect circuit should be configured with 2 Back-to-Back MOSFETs.

7.13.7 Concurrent Maintenance

This power supply will be designed to be “hot plugged/removed”. No faults will be generated in the functioning units, or the system, during removal or insertion of a power supply. Output voltages must remain within regulation limits on either insertion or extraction. No damage should occur to either the operating or non-operating power supply.

A fault (UVP, OTP and short-circuit except OVP) within one power supply while running (synch FET, output cap, etc.) shall not cause output voltage of the system/common bus voltage to go outside regulation limits. No faults will be generated in the functioning units, or the system. If the current sharing is disabled by shorting the current share bus to ground, the power system must continue to operate within regulation limits for loads less than or equal to one power supply.

When VINOK# has been de-asserted and the power supply is shutting down due to the loss of AC/DC input, the output’s OR’ing FETs must be turned OFF when the secondary main converter has turned OFF within 50us of POK de-assertion.

> ***Note:*** The requests above must be validated during the power supply development phase to ensure concurrent maintenance.

7.13.8 Maximum Power Rating with Parallel PSUs

The supplies must be able to current share with any combination from 1 to 6 PSUs in the system. Maximum Output Power for systems with "n" PSU of "W" power each, in parallel: 1*W +0.95*(n-1)*W.

Table 7-10 Number of power supplies in parallel vs. maximum system power rating

PSU SKUs	Number of Supplies	Maximum System Power Rating
1+0	1	100% of One PSU Rating
1+1	2	100% of One PSU Rating
2+0	2	100%+(95% x 1) x PSU Rating
2+1	3	100%+(95% x 1) x PSU Rating
2+2	4	100%+(95% x 1) x PSU Rating
3+0	3	100%+(95% x 2) x PSU Rating
3+1	4	100%+(95% x 2) x PSU Rating
3+2	5	100%+(95% x 2) x PSU Rating
3+3	6	100%+(95% x 2) x PSU Rating

7.13.9 Current Share Signal Characteristics

This current sharing section is a proposed method for achieving load sharing compatibility between different manufacturer's power supplies. This section may be updated based on information gathered during testing and other investigations to make it a reliable set of requirements. Descriptions of the voltage and current share loop stability are shown below.

Table 7-11 Current Share Signal Characteristics

Item	Description	Min	Nom	Max	Units
Ishare sink. Ishare =10V	Amount of current the load share bus of each power supply sinks.	-	-	1.5	mA
Ishare source. Ishare =10V	Amount of current the load share bus of each power supply sources.	-	-	1.5	mA
T_{SS}	Soft start of current sharing loop, count from output voltage is rising to its 90% voltage rating	-	50	100	msec
T_{Ishare}	Delay from PSU2 reaching 90% of its nominal voltage to PSU1 & PSU2 Currents settling within Current Share Specification.	-	-	150	msec

Figure 7-4 TSS and Tishare timing

7.14 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in *Table 7-12 Ripple and noise* below. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A

10µF in parallel with a 0.1µF ceramic capacitor is placed at the point of measurement. To help reduce switching ripple further, an additional 2,200µF low ESR electrolytic capacitor is required to be placed in parallel.

Table 7-12 Ripple and noise

+12V main	+54V main	+12VSB
120mVp-p	540mVp-p	120mVp-p

The test set-up shall be as shown below.

Figure 7-5 Differential noise test setup

Notes:

1. When performing this test, the probe clips and capacitors should be located close to the PSU connector.
2. Perform a load sweep from minimum load up to 100% in 10% load increments. Using a time/div of 10ms and 10us/div.

7.15 Timing Requirements

This section describes the timing requirements for the power supply operation. All outputs must rise monotonically. Table below shows the timing requirements for the power supply being turned ON and OFF in two different ways; 1) via the AC/DC input with PSON# signal held low; 2) via the PSON# signal with the AC/DC input applied.

Table 7-13 Timing requirements

Item	Description	MIN	MAX	Units
Tvout_rise	Output voltage rise time for 12V and 12VSB from 10% to within regulation limits.	10	70	ms
Toff_latch[2]	This is the time the PSU must stay off when being powered off with loss of input. Both outputs must meet this OFF time; 1) whenever PWOK is de-asserted for the 12Vmain output; 2) whenever the 12VSB output drops below regulation limits.	500	1000	ms
Tsb_on_delay	Delay from input being applied to 12VSB being within regulation.		3000	ms

Tsb_on_delay_active	Delay from input being applied to 12VSB being within regulation when the MCU/DSP is already ON and powered by remaining charge in the bulk capacitor or being externally powered by another M-CRPS in parallel.			1700	ms
Tac_on_delay	Delay from input being applied to all output voltages being within regulation.			5000	ms
Tac_on_delay_active	Delay from input being applied to all output voltages being within regulation when the MCU/DSP is already ON and powered by remaining charge in the bulk capacitor or being externally powered by another M-CRPS in parallel.			2000	ms
Tvout_holdup[8]	Time 12V output voltage stays within regulation after loss of input.	AC/DC input	11		ms
		-48VDC and +54VDC input	2		
Tpwok_holdup[1]	Delay from input loss to de-assertion of PWOK	AC/DC input	5	>=10	ms
		-48VDC and +54VDC input	1		
Tpson_off_delay	Delay from PSON# de-asserted to power supply turning off			5[6]	ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.		5	400	ms
Tpson_pwok	Delay from PSON# deactivate to PWOK being de-asserted.			3	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.		380	420	ms
Tpwok_off[1]	Delay from PWOK de-asserted to output voltages dropping out of regulation limits based on Input lost condition		1[6]	6[4,6]	ms
	Delay from PWOK de-asserted to output voltages dropping out of regulation limits based on PSON# de-asserted condition		1[6]	6[6]	ms
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using input or the PSON# signal.		100		ms
Tsb_vout	Delay from 12VSBbeing in regulation to O/Ps being in regulation at input turn on.		50	1000	ms
T12VSB_holdup	Time the 12VSB output voltage stays within regulation after loss of input.		70		ms
Tvinok_on[3]	Delay from 12VSB within regulation limits to assertion of VINOK		0	50	ms
Tvinok_off[3]	Time from loss of input to de-assertion of VINOK	AC/DC input	1000	4000[5]	us
		-48VDC and +54VDC input		100	

Notes:

1. The T_{pwok_holdup} = 10ms and T_{pwok_off} = 1ms, are the default values in the PSU when it's being energized, however the system now can configure the warning time established by T_{pwok_off} to have a different value please refer to section *7.16 PWOK Signal Timing Requirements*.
2. T_{off_latch} flow diagram is shown in *Figure 7-8 Toff_latch flow diagram.*
3. Additional logic dependencies are described *Figure 7-7 VINOK assertion logic* Below.
4. T_{pwok_off} can be configure from 1ms (default) to 6ms, refer to *Section 7.16 PWOK Signal Timing Requirements* for more details. This value is minimum value of max configurable timing.
5. Default value for T_{vinok_off} is 4ms and can be configured using the T_{vinok_off} register described in *Table 12-73 Power supply timing configuration*.
6. Using minimum capacitance specified in *Table 7-7 Capacitive loading conditions* and 100% of rated load.
7. Regulation limits are defined as 11.40V to 12.60V for this table to keep backwards compatibility with legacy systems.

8. Refer to *Table 5-5 AC/DC, 240VDC and* HVDC holdup / dropout for different values at various loads.

Figure 7-6 Turn ON/OFF Timing (Power Supply Signals)

Figure 7-7 VINOK assertion logic

Notes:

1. Averaging window can go from 75ms to 120ms depending on the input frequency.
2. 5th cycle is counted after the 12Vstby is within regulation limits.
3. Smart Ride-Through logic is described in *Section 12.3 Smart Ride-Through (SmaRT)*.

Figure 7-8 Toff_latch flow diagram

7.16 PWOK Signal Timing Requirements

The PWOK signal timing shall be as stated in *Table 7-13*. Timing requirements when the power supply is being energized (AC/DC is applied), however the warning time established by T_{pwok_off} shall be configurable via PMBus command MFR_PWOK_WARNING_TIME (F0h) using linear format it is recommended to use 1ms steps and the power supply shall guarantee at least the minimum warning time configured, it is recommended to have a jitter no more than 1.5ms. *Figure 7-9* shows the timing diagram. T_{pwok_off} value shall return to default after an AC/DC input cycle only. The figure below shows the timing diagram. T_{pwok_off} value shall return to default after an AC/DC input cycle only with a complete PSU power off (indicator LED off and secondary side MCU de-energized).

Figure 7-9 Configurable PWOK warning time timing diagram for High voltage power supplies

Note:

1. The main output shall have a slope decay of 1-10ms from 11.40V to 10.5V when going down using a 10% loading condition and the minimum capacitance across the main output as defined in *Table 7-7 Capacitive loading conditions*.

7.17 12V Internal Transfer Switch

It is recommended for 12V output M-CRPS to have an internal transfer switch between the 12Vmain output and the 12VSB as shown in *Figure 7-10 12Vmain to 12VSB transfer switch* to help increase efficiency.

Figure 7-10 12Vmain to 12VSB transfer switch

Note: The droop control shall be disabled when the transfer switch between the 12Vmain output and 12VSB output is ON.

8 Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shut down. If the power supply latches OFF due to a protection circuit tripping, by default an AC/DC input power cycle OFF for 15 sec and a PSON# signal cycle HIGH for 1 sec shall be able to reset the power supply. Optionally the power supply can reset its latching faults with a PSON# cycle when the *ClearFaultsWithPSONCycle* bit in *Table 12-74 Power supply latch on fault condition configuration block* is set.

The power supply shall have over current protection (OCP), over current warning (OCW), and overpower protection (OPP) limits as defined in the subsequent sections. These are defined to protect the power supply and to allow peak currents to power the system without the PSU shutting down.

Fast OCW and Slow OCW levels are defined to assert SMBAlert# to allow the system to throttle power to protect the power supply; but also, to allow peak current to the system without throttling the system.

When OCP trips and the bit *ClearFaultsWithPSONCycle* in *Table 12-74 Power supply latch on fault condition configuration block* is cleared; it shall shutdown and latch OFF the PSU. This will be cleared only by an AC/DC input power cycle. The power supply shall not be damaged from repeated power cycling in this condition.

When clearing the faults by using a PSON# cycle option the system or agent needs to provide a reasonable time between the fault event and the reset of the faults to protect the system from overheating due to repeated fast power cycling into a faulted short condition in the system.

12VSB will be auto recovered after removing OCP limit (hiccup mode).

8.1 Main Output

8.1.1 Current sense

The PSU shall have the ability to measure output current, which is inclusive of the current delivered by the output filter capacitance within the PSU. The monitored current shall be used, at a minimum, as the input into the constant current, peak detect and overcurrent warning / protection control solution and is available as I_{mon} output from the PSU.

Figure 8-1 Main output current sense block diagram

Notes:

1. Signal or information that represents the Main output current. Derivation of this signal/information shall be derived via secondary side sensing, post the output filter stage. Current sense element shall be located on either rail.
2. The I_{mon} block and I_{mon} output stage blocks are detailed in *Section 9.5 Imon Signal (Output).*

8.1.2 Averaging Mechanism

The power supplies shall have the ability to sample output current and perform a block / window average calculation to support OCW behaviors. Select thresholds shall have the ability to be programmable inclusive of sampling rate and averaging window size. It is required that the PSU uses an average output current value when taking action on applicable OCW behaviors. Refer to *Table 8-2 OCW Thresholds.* The PSU will be required to utilize one sampling rate that will be used across the OCW levels prescribed in this specification.

Figure 8-2 OCWPL1 average window logic

Notes:

1. OCWPL1 Minimum detectable pulse width for averaging window assertion = 40uS ±5us.

Figure 8-3 OCWPL3 average window logic

Notes:

1. OCWPL3 Minimum detectable pulse width for averaging window assertion = 20uS.

8.1.3 Over Current Warning (OCW)

8.1.3.1 Over Current Warning Level 1 (OCWPL1)

This is a programmable output current warning level intended for maintaining an average PSU load. It is the slower mechanism, compared to that of the peak detect solution of OCW_{PL3}. The PSU shall use an average output current, derived over a specified time window, to compare against a programmable threshold. This OCW level shall have a hysteresis (refer to *Table 8-2 OCW Thresholds*), between assertion and deassertion thresholds. The output current averaging window shall start when the PSU (output current) > (hysteresis de-assertion threshold and the previous timer has expired). If the average current exceeds the OCW_{PL1} set point, over the specified averaging window, the PSU shall declare an OCW_{PL1} event and apply the appropriate logic to SMBAlert#. Please refer to the timing diagrams for OCW_{PL1} for further details.

8.1.3.2 Over Current Warning Level 3 (OCWPL3)

OCW_{PL3} is the fixed overcurrent protection threshold. The assertion & de-assertion threshold levels are fixed values. If the average current exceeds the OCW_{PL3} assertion set point, over the specified averaging window, the PSU shall declare an OCW_{PL3} event and apply the appropriate logic to SMBAlert#. It will then start a 15ms average window. If the average output current continues to remain above the de-assertion threshold, over the specified 15ms average window, the PSU shall shutdown due to overcurrent. In the case, which OCW_{PL3} has been asserted and the average output current < de-assertion threshold over the second (15ms) averaging window, the PSU shall not shut down. The output current averaging window shall start when the (PSU output current) > (OCW_{PL3} hysteresis de-assertion threshold and the previous timer has expired).

8.1.3.3 Over Current Warning Level 4 (OCWPL4)

This warning level is intended to be a high-speed peak output current detection and reporting solution. It shall provide the end system with a rapid response logic signal to declare the PSU output current has exceeded a programmable threshold. The PSU shall declare an OCW_{PL4} event based on peak PSU output current, which includes the discharging of the internal PSU output capacitance. The PSU shall use a window averaging method for establishing de-assertion of applicable alert signals. The output current averaging window for de-assertion shall start when the following statement is true:

(PSU output current) > (OCW_{PL4} assertion threshold & minimum detectable current pulse width & previous OCW_{PL4} window has expired).

Table 8-1 OCWPL4 Timings

Specification	Description	Min	Typ	Max	Units
OCW_{PL4} Detectable Current Pulse Width	Represents the minimum output current pulse that shall be detected by the PSU for OCW_{PL4} assertion. Current pulses ≤ the minimum time specified shall not assert an OCW_{PL4} event. Output current pulses > than the maximum time specified shall assert an OCW_{PL4} event.	20			us
OCW_{PL4} Report Time	Report Time represents the time period starting after the minimum detectable PSU output current pulse to the assertion of SMBAlert#.	0		30	us
OCW_{PL4} Total Detect + Report Time	The Detection + Report time is measured from the moment the actual PSU output current crosses the assertion level, to the moment the SMBAlert# signal is asserted.	0		1.9	ms
OCWPL 1/3/4 PSU Output Current Slew Rate Measurement Location	Represents the output PSU current slew rate measurement location for OCWPL 1/3/4. It shall be measured directly on the output of the PSU. Please refer to *Figure 8-4 PSU Output Current – Slew Rate Measurement*.	0.2		2.5	A/us

Figure 8-4 PSU Output Current – Slew Rate Measurement

Figure 8-5 SMBAlert# flow

Table 8-2 OCW Thresholds

Item	OCW_{PL1}[1]	OCW_{PL3}	OCW_{PL4}	OCP
Function / Purpose	OCW Sustained for PL1	OCW for PL3	OCW for PL4	Short circuit protection
Default Set Point Threshold	130%	116%	156%	170%
Set Point Tolerance	-5% / +0%	-0% / +5%	-0% / +5%	-0% / +5%
Hysteresis	5%	5%	5%	
Programmable Threshold Capability	Yes	N/A	N/A	N/A
Programmable Range	15% - 130% (Programmable Range remains unchanged with input line range).	N/A	N/A	N/A
Programmable Sampling Rate Capability	No	N/A	N/A	N/A
Programmable Sampling Rate Range	N/A	N/A	N/A	N/A
Sampling Rate Set Point Tolerance	+/-5%	N/A	N/A	N/A

Default Sampling Rate (Min)	50kHz	50kHz	50kHz	50kHz
Default Averaging Window Set Point	250ms	10ms	20us	N/A
SMBAlert# assertion time post window average termination	Max = 100uS	Max = 10ms	Max = 1.9ms	N/A. Assertion is triggered on a peak reading.
Programmable Averaging Window Capability	Yes	No	No	No
Averaging Window Range	0.25s to 60s	N/A	N/A	N/A
Averaging Window Set Point Tolerance	(+/-50uS)	(+0/-50uS)	N/A	N/A
T_BLNK	1mS (+/-100uS)	1mS (+/-100uS)		

Notes:

1. OCW_{PL1} is used for testing purposes, having the threshold at 130% by default it disables it, the user can change the threshold to a lower value but not a higher one.
2. Values expressed in %, in this table, are based on the full +12V main rail capacity located in *Section 7 Output Requirements*. For those PSU have different capacities for high line and low line, use the higher main rail capacity for both high line and low line if the difference of power is equal or lower than 50W. For example, an 1100W PSU Main (90.16A @ +12.2V) and 36W Aux (3A@12V) has a hysteresis of 5% of 90.16A = 4.508A for both high line and low line.
3. T_BLNK: Blanking time for programmable averaging window and OCW thresholds that apply only when consecutive window averages have been issued. A system writes to change an OCW threshold or window average, during the T_BLNK period, will result in a value change after the completion of the following window period.

8.1.4 Over Current Protection & Over Power Protection (OCP & OPP)

For purposes of definition, the operational range (over the specified time segment per *Figure 8-6 PSU Output Current vs. Time)* of the power supply has been divided up into 4 categories. The graph is intended to provide an illustrative means of describing PSU regulation & protection behaviors based on time vs. load. It does not capture tolerances and or programmable aspects such as assertion thresholds and timings.

- **<100% Load:** This load range represents the sub 100% loading area of the PSU. The voltage regulation limits, slew rate and capacitance are called out in this specification.
- **Extended Voltage Regulation:** This load range represents load step levels >50% to ≤ 100%the PSU. Depending on the size of the load step and starting point, will dictate the regulation range the PSU shall comply with *Table 7-5 Transient load requirements.*
- **Constant Current:** This load range represents the PSU transitioning from a voltage controlled current source to a fixed current source. This mode of operation is considered a protection mode, for which the PSU shall limit its current to a fixed value.
- **Primary Power Limit:** PSU shall contain a primary pulse by pulse current / power limit set at the equivalent output current levels located in *Table 8-3* below. Upon entering this range, the PSU shall limit the power until such time as secondary constant current has been asserted.

Table 8-3 PSU vs. Load Behaviors – Constant Current and Primary Power Limit

Specification	Description	Min	Typ	Max	Units
Initial Constant Current Set Point	Value represents the constant current set point of the PSU. This set point represents the output current that the PSU will clamp its output to.	157.5	160	162.5	(% of full load rating)
Constant Current Level Drift	Value represents the amount of change in the output current once it is clamped to its set point value. This is measured over a 5ms time period.			+/- 2.5	(% of full load rating)
Constant Current Assertion Time	PSU shall not transition to constant current mode in less time than the minimum time specified. This time is used to establish the amount of time it takes the PSU output to transition from being a voltage controlled current source to a fixed constant current source.	2		3	ms
Constant Current Settling Time	The amount of time starting from constant assertion to the PSU output current reaching the initial constant current set point. Measurement made with minimum output capacitance under section 3.4	200		6000	us
Transition Limits Constant Curent to Constant Voltage	Upon the PSU clamping its output current to its fixed value, the criteria for exiting constant current mode shall be the load falling below the clamped output current level. During this transition the PSU shall maintain the extended output voltage regulation.	Refer to Section *Table 7-5 Transient load requirements* at the location referred to as regulation limits.			
Primary Power Limit	PSU shall contain a primary pulse by pulse current / power limit set at the equivalent output current levels located to the right.	170		180	(% of full load rating)

Figure 8-6 PSU Output Current vs. Time

8.1.4.1 Constant Current During Start Up into Overcurrent Condition

In an event when output current exceeds constant current thresholds defined in *Table 8-3 PSU vs. Load Behaviors – Constant Current and Primary Power Limit*, the power supply shall go into constant current mode. In the event of an overcurrent start up condition, in which PWOK does not assert and the start condition is valid the PSU shall issue an OC_FAULT, the OCW_{PL1}, OCW_{PL3} and the under-voltage protection (UVP) shall remain disabled. In an overcurrent startup condition, in which PWOK is asserted before the 495ms window has expired, OCW_{PL1}, OCW_{PL3} and Vout_UV shall be enabled before the PSU is Turned ON.

The reporting of status register related with over current conditions and Status Word are as shown in the flowchart shown in *Figure 8-7 PSU Start up into Over Current Condition*.

Figure 8-7 PSU Start up into Over Current Condition

8.1.5 Fast Output Current Sensing for Fast Over Current Warning

The power supply shall have a circuit to quickly assert the SMBAlert# signal when the output current exceeds the over power protection threshold in the PSU. The SMBAlert# signal must always assert before the overpower protection threshold is exceeded. SMBAlert# must always latch for about 100msec before being released.

8.1.6 Over Voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed and hardware based. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing the OVP limit.

Table 8-4 Over Voltage Protection (OVP) Limits

Output Voltage	MIN (V)	MAX (V)
+12V	13.60	14.50
+54V (High voltage input)	58.50	59.50
+54V (+54V input)	58.50	59.50
+12VSB	13.60	14.50

8.1.7 Under Voltage Protection (UVP)

The power supply under voltage protection shall be locally sensed and hardware based. The power supply shall shutdown and latch off after an under-voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never trip any higher than the maximum levels when measured at the power connector.

Table 8-5 Under Voltage Protection (UVP) Limits

Output Voltage	MIN (V)	MAX (V)
+12V	9.50	10.00
+54V (High voltage input)	45.90	48.60
+54V (+54V input)	41.00	42.00
+12VSB	9.50	10.00

8.1.8 Over Temperature Warning (OTW)

The power supply shall be able to alert the system by asserting the SMBAlert# signal to take action when the temperature in any of the temperature sensors reach a predefined threshold in the Temperature Configuration Block (see *12.8.3.2 Temperature Configuration Block*) of the configuration file (see *12.8 Configuration File*)

8.1.9 Over Temperature Protection (OTP)

The power supply shall be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. OT warning SMBAlert# assertion must always precede the OTP shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip temperature level shall be at least 4°C higher than Over Temperature Warning threshold level. The Over Temperature Protection threshold shall be configurable, See *12.8.3.2 Temperature Configuration Block* in section *12.8 Configuration File* for more details.

8.2 Auxiliary (Stand-by) Output

8.2.1 Over Current Protection Behavior

During initial power on, 12VSB output OCP is blanked for a period *Tblank_startup* to allow starting into rated load with the maximum external capacitive loading across the auxiliary (Stand-by) output. At end of the period *Tblank_startup* 12VSB output shall be in regulation if the 12VSB current is ≤ ISTBY_RATED.12VSB output shall support peaks currents (after start-up – 12VSB output in regulation) as defined in the diagram shown in figure below.

$D = t1/(t1+t2)$

$I_{STBY_Average} = I_1 + D * (I_{STBY_PK} - I_1)$

$I_{STBY_Average} \leq I_{STBY_RATED}$

Figure 8-8 Auxiliary (Stand-by) OCP behavior

Notes:

1. If either the duration of ISTBY_ PK > t1 AND / OR the peak current is > ISTBY_ PK, 12VSB output shall enter in OCP Mode.
2. Standby Output shall be capable of handling repetitive peaks as long as the Average value of 12VSB output current is (Averaged over 100ms- 120ms) ≤ ISTBY_RATED. If the Average during repetitive peak events exceeds ISTBY_RATED (-0%,+5%), but falls within the 12VSB OCP limits, 12VSB output shall enter in OCP Mode.

3. If the Average value of 12VSB output current exceeds ISTBY_RATED but is lower than value of ISTBY_OCP, 12VSB output is allowed to Droop, but should remain > UVP Limit and shall continue to operate without hazard OR may shut down due to OTP.
4. Each PSU design shall be tested by disabling OCP on 12VSB and setting the 12VSB load to 0.95 * Max Value of ISTBY_OCP limit of the design (which should be the maximum value of OCP obtained by WCEPTA) to ensure that the PSU satisfies either of the conditions defined in "1" above. This test is only a design validation test performed at each stage during development.

8.3 Short Circuit Protection

A short circuit applied to any output during start-up or while running will not cause any damage to the power supply (connectors, components, PCB traces, etc.), even when output/s remain shorted. Short circuit conditions applied to any of the outputs including the Standby may generate very high peak currents because of the time delay until the output will latch off or PSU enters hiccup mode of operation depending on the configuration file. The peak current (ISC) and peak current duration (t_{SC}) must be limited, so the resulting thermal energy is below the I_{OC2} x t_D levels: (I_{SC2} x t_{SC}) < (I_{OC2} x t_D), where I_{OC} is the over-current limit set by the specification and t_D = 1sec.

Note: Short circuit impedance shall be 10mΩ maximum for the 12Vmain output, 200mΩ maximum for 54V output and 100mΩ maximum for the 12VSB output.

When the Standby output is shorted the output shall go into "hiccup" mode. When the Standby output attempts to restart 1st peak current should meet (I_{SC2} x t_{SC}) < (I_{OC2} x t_D) defined above. If the PSU remains in this condition, the repetitive peak current should not exceed the limit defined as STBY Short Circuit Peak Current in EE Specs and maximum average current, considering the "hiccup" duty cycle, should not exceed the limit defined as Standby Short Circuit Average Current in the design specification.

Note: Peak current should be measured between PSU connector and capacitors for ripple current. All components (including primary circuit) supporting peak short circuit current (including the 1st peak) should be rated to handle the peak current and power dissipation (at worst case temperatures on the components) during the event. This should be proven with calculations assuming worst case tolerances on components and worst-case component temperatures and impedance of the short is assumed at 0Ω. No external capacitor (other than used on ripple and noise measurements) to be used for validating STBY short circuit peak current.

8.4 Input Over Current Protection

The power supply must have internal primary over current protection. A defined fuse type utilizing high-breaking-capacity must be placed in the input circuit. The fuse is not to be considered replaceable for the purposes of determining power supply reliability and life as specified in *Section 13 Reliability*. Common parameters for all PSUs related to Input Over Current Warning – Averaging Window, Hysteresis are defined in the table below.

Table 8-6 Input OCW Averaging window and hysteresis

Parameter	Min.	Typical	Max.	Units
Input OCW Averaging window	600	650	700	ms

Input OCW Hysteresis	0.40	0.50	0.60	A

8.4.1 Input Over Current Warning – AC Input

The power supply shall have an input over-current warning. Input Over-Current warning shall be enabled only if PWOK is asserted, and the reported input voltage is within the operating range of the PSU. The thresholds for Input Voltage and Current should be the actual reported values by the PSU.

If Input Over current warning is enabled by end user on a wide range PSU, then the PSU behavior in terms of turn ON/OFF thresholds will change to match spilt range PSU (in short – the wide range PSU will then behave as a split range PSU and would turn OFF if operating at high line and input drops below its high line turn off threshold and will stay off – until input returns back and is above its high line turn on threshold value if the PSU is back biased (operating in n+1 config or otherwise) OR will turn ON if the input is above the turn on threshold for low line in case when the PSU got reset due to loss of input with no back bias present) please refer to *Section 12.1.44 IIN_OC_WARN_LIMIT (5Dh)* for more details.

8.4.2 Input Over Current Warning – DC Input

The power supply shall have an input over-current warning. Input Over-Current warning should be enabled only if PWOK is asserted, and the reported input voltage is within the operating range of the PSU. The thresholds for Input Voltage and Current should be the actual reported values by the PSU.

9 Control and Indicator Functions

9.1 PSON# Signal (Input)

The power supply shall have a PSON# signal to remotely turn ON/OFF the power supply. It shall be able to be configured via firmware to work as a two-state (default) or multi-state PSON# signal based on the configuration provided by the configuration file. To accomplish the two/multi-state modes the power supply shall incorporate the circuit below.

Figure 9-1 Required PSON# input signal circuit for two/multi-state operation

Notes:

1. Applying a logic 1 to the MOSFET will configure the PSON# input signal as multi-state.
2. Applying a logic 0 to the MOSFET will configure the PSON# input signal as two-state.
3. 3.3VSB in the voltage divider shall be taken from a precision voltage reference.

The specifications for these two different configurations are described in the following subsections.

9.1.1 Two-State Signal

When the PSON# signal is configured as two-state, it shall be active low to turn ON the +12V main power output. When this signal is not pulled low by the system, or left open, the +12V main output shall be turned OFF while the 12VSB output shall remain ON. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. The table below lists the required characteristics of the PSON# signal when configured as two-state input.

Table 9-1 Two-state PSON# signal characteristics

Signal Type	**Accepts an open collector/drain input from the system. Pull-up to 3.3VSB located in power supply.**	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	**MAX**
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, Vpson = low		4 mA
Power off delay: Tpson_off_delay		5 msec
Power up delay: Tpson_on_delay	5 msec	400 msec
PWOK delay: T pson_pwok		5 msec

Figure 9-2 Two-state PSON# required signal characteristics.

9.1.2 Multi-State Signal

When configured as multi-state input, the PSON# signal shall be able to detect logic 0, logic 1 and high impedance (pin floating or open) and additional 3 states. The different states are needed for the following reasons:

- Provide an electrical keying for the 54V output M-CRPS, a 54V output M-CRPS will turn ON only when the PSON# signal voltage is within the S1 state.
- Provide a full power cycle mechanism (FPC) for the system, this will essentially emulate disconnection and re-connection of the input power cord.
- Provide compatibility for systems that can have a scenario when there are no nodes or agents (like the Open Compute DC-SCM module) to keep asserting the PSON# signal.

The thresholds to detect these new states are depicted in the following figure.

Figure 9-3 Multi-state PSON# Required signal characteristics.

Table 9-2 Multi-state PSON# voltage ranges definition

State	Power supply must detect PSON# voltage within this range			System must set PSON# voltage within this range			M-CRPS Main output			
							12V M-CRPS		54V M-CRPS	
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Main Output	12VSB	Main Output	12VSB
Logic high	2	-	3.46	2.05	-	3.46	OFF	ON	OFF	ON
Open	1.7	1.85	<2	1.73	1.85	1.87	See *Table 9-3*	ON	See *Table 9-3*	ON
S3	1.5	1.6	<1.7	1.53	1.6	1.67	OFF	OFF	OFF	OFF
S2	1.3	1.4	<1.5	1.33	1.4	1.47	OFF	ON	OFF	ON
S1	1	1.15	<1.3	1.03	1.15	1.27	OFF	ON	ON	ON
Logic Low	0	-	<0.8	0	-	0.75	ON	ON	OFF	ON

Notes:

1. Every transition state shall incorporate a 10ms debounce period except for the Main Output turn OFF which needs to be maximum 5ms to comply with *Tpson_off_delay* in *Table 7-13 Timing requirements*.

PSON# stage shall be designed to follow the logic as shown in the table below for assertion and deassertion states when used in Multi-state PSON# mode.

Table 9-3 PSON# transition states when using multi-state mode

#	VINOK	System State Of PSON#	PSON# Transition State	PSU Main Output State
1	HIGH	Initialization (HI-Z, HIGH)	Hi-Z, High	Remain OFF
2	HIGH	LOW	LOW	Stays ON
3			HIGH	Turns OFF
4			HI-Z	Stays ON
5	HIGH	HIGH	LOW	Turn ON
6			HIGH	Remain OFF
7			HI-Z	Remain OFF
8	HIGH	HI-Z	LOW	Turn ON if OFF || Remain ON
9			HIGH	Turn Off if On || Remain OFF
10			HI-Z	Preserve Last State
11	LOW	LOW	LOW	Remain ON until PWOK drops
12			HIGH	Turn off
13			HI-Z	Remain ON until PWOK drops
14	LOW	HIGH	LOW	Turn ON until PWOK drops
15			HIGH	Remain OFF
16			HI-Z	Remain OFF
17	LOW	HI-Z	LOW	Turn ON until PWOK drops
18			HIGH	Turn Off if On || Remain OFF
19			HI-Z	Preserve Last State

9.1.2.1 Full Power Cycle

The M-CRPS shall be able to shutdown both Main and 12VSB outputs when the PSON# signal stays in the in the voltage range of the S3 stage for 10ms, triggering a process called Full Power Cycle (FPC), this process is used to emulate an input power cord disconnection without the need for the user to physically go and disconnect the power cord, the M-CRPS shall autonomously wake back up with the 12VSB output ON providing the proper rise time dictated by *Tvout_rise* in *Table 7-13 Timing requirements*, the state diagram of this process is shown in the figure below including the scenarios for all the PSON# states.

Figure 9-4 Multi-State PSON# signal state diagram

Notes:

1. Direct transition from Logic Low OR S1 to S3 (FPC request) requires internal logic to transition to Vmain=OFF until its discharged threshold is reached and preset time elapses before removal of 12VSB. 12VSB=OFF is maintained until its discharged threshold is reached and preset time elapses (where one setting includes forever until all input power is cycled) and PSON# is not still in the S3 range before exiting S3.
2. VSB refers to 12V standby and Vmain refers to either 12V Main or 54V Main depending on the M-CRPS capability.

The pseudocode for the M-CRPS behavior upon Full Power Cycle request shall be the following:

```
12VMain = OFF; //If not already
Count down from TMain_MinOFF to 0;
IF (VMain <= VMainDischargeMax)
{
        12VSB = OFF;
        Count down from T12VSB_MinOFF to 0;
        IF ((12VSB <= VsbDischargeMax)&&(PSON# !=S3)
                12VSB = ON;
        ELSE
                Exit; //Another PSU is holding up AUX or the system is holding S3 request
}
ELSE
        Exit; //Another PSU is holding up main
```

Notes:

1. This algorithm always includes the minimum main off time because the Full Power Cycle request may be received immediately following Main = OFF. This allows a common algorithm regardless of which state the M-CRPS is in when the Full Power Cycle request is received.
2. It is system logic responsibility to request Full Power Request to all M-CRPSs at the same approximate time to ensure no peer M-CRPS is holding up either voltage rail/output.

The timing diagram for the Full Power Cycle process is shown in figure below.

Figure 9-5 Full Power Cycle timing diagram

Notes:

1. *FPCMainMinOFFTime* and FPCVsbMinOFFTime can be extended from their default values by sending the command MFR_FPC_MAIN_MIN_OFF_TIME and MFR_FPC_12VSB_MIN_OFF_TIME respectively, refer to *Section 12.1.56 MFR_FPC_MAIN_MIN_OFF_TIME* and *Section 12.1.57 MFR_FPC_12VSB_MIN_OFF_TIME* for more details.

9.2 PWOK Signal (Output)

PWOK is a power OK output signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See the table below for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall be inhibited as long as any power supply output is in current limit.

Table 9-4 PWOK signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to 3.3VSB located in the power supply.**	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	**MAX**

Logic level low voltage, Isink=400uA	0V	0.4V
Logic level high voltage, Isource=200µA	2.4V	3.46V
Sink current, PWOK = low		400uA
Source current, PWOK = high		2mA
PWOK delay: Tpwok_on	380ms	420ms
PWOK rise and fall time		100µsec
Power down delay: T pwok_off	1ms	
Any PSU fault to PWOK deasertion delay		100µsec

A required circuit implementation of the Power Ok circuit is shown below. The Power Ok circuits shall be compatible with 5V pull up resistor (>10k) and 3.3V pull up resistor (>6.8k).

Figure 9-6 PWOK circuit implementation

9.3 SMBAlert# Signal (Output)

This signal indicates that the power supply is experiencing a problem that the user should investigate. This signal shall be asserted due to Critical events or Warning events as configured in the configuration file. The signal shall activate in the case of critical component temperature reaching a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits. This SMBAlert# signal is to be asserted in parallel with LED color code selected in the configuration file.

Table 9-5 SMBAlert# signal characteristics

Signal Type (Active Low)	**Open collector / drain output from power supply. Pull-up to 3.3VSB located in the system.**	
Alert# = High	OK	
Alert# = Low	Power Alert to system	
	MIN	**MAX**
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 µA		3.46 V
Sink current, Alert# = low		4 mA
Sink current, Alert# = high		50 µA

9.4 VINOK Signal (Output)

VINOK signal indicates that the input voltage is within the range where the power supply can operate normally. Details of the operation are described in section *7.15 Timing Requirements*.

Table 9-6 VINOK Signal characteristics

Signal Type (Active High)	**Open collector/drain output from power supply. 1KΩ Pull-up to 3.3VSB located in the power supply.**	
VINOK = High	Input voltage is within the operational range	
VINOK = Low	Input voltage not within the operational range	
	MIN	**MAX**
Logic level low voltage, Isink=10mA	0V	0.4V
Logic level high voltage, Isource=4mA [1]	3.0V	3.46V
Sink current, VINOK = low		10 mA
Source current, VINOK = high		4mA
VINOK rise and fall time		100µsec

Notes:

1. Using 100KΩ load resistor in the system side.

9.5 Imon Signal (Output)

The power supply shall incorporate an output current monitoring pin which will act as a current mirror of the main 12V output, I_{mon} signals from other power supplies in the system can be tied together to provide a mechanism for the system to measure the total output current of all the power supplies combined. The signal shall include an output diode to prevent the current from other power supplies' I_{mon} signal from entering a power supply that is not energized. The characteristics of the signal are described in the table below.

Table 9-7 I_{mon} signal characteristics

Signal type	**Current source**
Sensitivity (configurable via configuration file)[1]	0 to 2mA (representing 0 to 200% of rated current) or 10uA/A[4] with a range of 0 to 200%[5] of rated current.
Minimum bandwidth	40 kHz
Compliance voltage	3.3V[7]
Signal delay[2]	<= 20us
Input leakage[3]	< 500nA

Notes:

1. The I_{mon} signal shall be able to provide information beyond PL4 levels.
2. Signal delay shall be tested using a load step from 5% to 105% and a di/dt of 8A/us without external capacitance connected to the power supply's main output.
3. Input leakage is defined when the power supply is not energized, when in standby state or when in Cold Redundant mode, and it shall be guaranteed at 85°C and 12V.
4. User selectable in the configuration file.
5. Based on the maximum rated power of the M-CRPS irrespective of the input voltage

Figure 9-7 Imon block diagram concept

Notes:

1. Resistor R1 is used to select the sensitivity of the current sense amplifier.
2. FB1 & C1 these components shall be located as close as possible to the Imon output pin of the power supply's output connector.
3. Q1, Q2, R2 & R3 are used to create backwards compatibility with the presence pin, the user can select to have an Imon signal or presence by configuring the option in *Table 12-75 Miscellaneous configuration block* the configuration file.
4. **GPO1** is used to change the transconductance between two sensitivities; 0-2mA representing 0 to 200% load condition and 10uA/A as stated in *Table 9-7 Imon signal characteristics.*
5. **GPO2** is used to enable/disable the Imon output, when this signal is low the Imon output is activated, when GPO2 is high the Imon output will be held connected to ground, effectively disabling Imon. This behavior is configurable in the Configuration file and the purpose of this is to add compatibility with the presence detect pin in systems using Legacy CRPS power supplies.
6. **Q1** low leakage P-CH JFET like MMBFJ177L to prevent errors in the Imon signal.
7. The I_{mon} signal shall never exceed 3.3V under any normal or abnormal operating condition.

The required accuracy for the I_{mon} signal shall be:

% Base Tolerance = ±1% (10% ≤ Iout ≤ 140%); N/A (140% < Iout ≤200%)
% Read Tolerance = ±1% (10% ≤ Iout ≤ 140%); ±2% (140% < Iout ≤200%)

Total tolerance = Base Tolerance + Read Tolerance

Figure 9-8 Imon signal % of tolerance versus % of loading condition

Figure 9-9 Imon signal delay step response

9.6 A0 and A1 Signals (Inputs)

The power supply shall be able to set its SMBus address and FRU address by checking the voltage levels in the A0 and A1 input pins, up to 6 SMBus addresses can be set combining logic states and analog voltage levels in these signals, the characteristics of these two signals are described in the following sections.

9.6.1 A0 Input Addressing

The power supply A0 input pin shall be analog and able to measure a voltage from 0 to 3.3V to select between logic addressing mode and analog addressing mode. The power supply shall sample the A1 and A0 pins and average the voltage to filter out noise/glitches as defined in the table below.

Table 9-8 A0 input signal characteristics

Signal Type	**Analog input. 47KΩ 1% 100ppm Pull-up resistor to 3.3VSB located in the power supply.**	
	MIN	**MAX**
Dynamic range	0V	3.3V
Sampling period (T)	0.9ms	1.1ms
Number of samples (N)	8	8

The power supply shall follow the flow diagram shown in Figure *9-10 Flow diagram to detect between logic and analog SMBus addressing* to determine if the addressing mode is based on logic levels or analog levels.

Figure 9-10 Flow diagram to detect between logic and analog SMBus addressing

Notes:

1. Refer to *Table 9-8 A0 input signal characteristics* for N and T values.
2. Start is defined as 12VSB being within the regulation limits.
3. The M-CRPS shall obtain the value of A1 pin to acquire the PMBus address and in a maximum of 50us execute the DSSI flow described in *Section 12.7.5 Interface Initialization*.

Table 9-9 Power supply's SMBus addressing using logic levels (up to 4 addresses)

	SMBus address			Power supply must detect A1 / A0 voltage within this range			System must set A1 / A0 voltage within this range		
PSU Number	PSU / FRU	A1 state	A0 state	Min (V)	Nominal (V)	Max (V)	Min (V)	Nominal	Max (V)
0	0xB0 / 0xA0	Logic 0	Logic 0	0 / 0	-	0.8 / 0.8	0 / 0	-	0.5 / 0.5
1	0xB2 / 0xA2	Logic 0	Logic 1	0 / 2	-	0.8 / 3.3	0 / 2.4	-	0.5 / 3.3
2	0xB4 / 0xA4	Logic 1	Logic 0	2 / 0	-	3.3 / 0.8	2.4 / 0	-	3.3 / 0.5
3	0xB6 / 0xA6	Logic 1	Logic 1	2 / 2	-	3.3 / 3.3	2.4 / 2.4	-	3.3 /3.3

Table 9-10 Power supply's SMBus addressing using A0 analog levels (up to 6 addresses)

	SMBus address			Power supply must detect A0 voltage within this range			System must set A0 voltage within this range		
PSU Number	PSU / FRU	A1 Voltage (V)	A0 Voltage (V)	Min (V)	Nominal (V)	Max (V)	Min (V)	Nominal	Max (V)
0	0xB0 / 0xA0	N/A[1]	0.9	0.8	0.9	1	0.85	0.9	0.95
1	0xB2 / 0xA2	N/A[1]	1.1	1	1.1	1.2	1.05	1.1	1.15
2	0xB4 / 0xA4	N/A[1]	1.3	1.2	1.3	1.4	1.25	1.3	1.35
3	0xB6 / 0xA6	N/A[1]	1.5	1.4	1.5	1.6	1.45	1.5	1.55
4	0xB8 / 0xA8	N/A[1]	1.7	1.6	1.7	1.8	1.65	1.7	1.75
5	0xBA / 0xAA	N/A[1]	1.9	1.8	1.9	2	1.85	1.9	1.95

Notes:

1. A1 pin is used as Data & Sidebands Serialization Interface when the addressing mode is based on analog levels, see *12.7 Data & Sideband Serialization Interface (DSSI)*.

To establish the address using the A0 analog level mode the system shall place a 1% tolerance 100ppm resistor from the A0 pin to ground with the required value for a given SMBus address as shown in table below.

Table 9-11 Recommended 1% tolerance 100ppm temperature coefficient resistor values for A0 analog addressing mode

PSU Number	Nominal voltage	Required resistor value 1% Tol 100ppm
0	0.9	17.8 KΩ
1	1.1	23.7 KΩ
2	1.3	30.9 KΩ
3	1.5	39.2 KΩ
4	1.7	49.9 KΩ
5	1.9	63.4 KΩ

9.6.2 A1 as Data & Sideband Serialization Interface (DSSI)

The A1 pin shall be dual purpose, the first purpose is to establish the SMBus address of the power supply based on the method described in the previous section *9.6.1 A0 Input Addressing*. The second purpose is as a 1-wire communication link. This communication link is only available when the PSU has the connections shown in section *12.7 Data & Sideband Serialization Interface (DSSI)*.

9.7 Remote Sense And Return Sense / PSKILL

The power supply shall have a remote sensing pair called Remote Sense (RS+) for the positive terminal and Return Sense for the negative terminal (RS-) to compensate voltage droops at the point of load. The Return Sense (RS-) pin shall be dual purpose acting as a PSKILL signal also as described below.

1) It shall be able to measure the most negative voltage at the load to regulate it at the point of load,

2) It shall be able to work as a PSKILL signal when the power supply is being extracted or inserted without removing the AC/DC cord, shutting down the main output of the power supply fast enough or preventing it from turning ON until PSKILL contacts with the system, thus preventing arcing at the connector, the RS-/PSKILL pin has a shorter length in the card edge than other signals to allow this functionality. The 12VSB output shall remain ON as long as input voltage stays within the specified range.

Table 9-12 Remote Sense +/- And PSKILL signal parameters

Parameter	Specification
Delay between RS-/PSKILL signal being disconnected and PSU main output's ramping down	< 100 us
Maximum DC resistance of remote sensing wires/traces (each)	2.5 Ω
Maximum voltage drop compensation	+-200 mV

Figure 9-11 +12V output M-CRPS RS+- pair usage

9.8 Pin Ripple/Noise and Capacitance

The power supply shall have a maximum internal capacitance for each one of the interface signals as described in the table below.

Table 9-13 Pin capacitance summary

Signal Name	Maximum allowed capacitance	Maximum noise level[2]	Input/Output	Comments
SCL[1]	100pF	300mV$_{pk-pk}$	Input	
SDA[1]	100pF	300mV$_{pk-pk}$	Input/Output	
SMBAlert#	100pF	300mV$_{pk-pk}$	Output	
PWOK	100pF	300mV$_{pk-pk}$	Output	
PSON#	1nF	300mV$_{pk-pk}$	Input	
Ishare	100pF	100mV$_{pk-pk}$[4]	Input/Output	
VINOK	100pF	300mV$_{pk-pk}$	Output	
CR bus	100pF	300mV$_{pk-pk}$	Input/Output	
DSSI	100pF	300mV$_{pk-pk}$	Input/Output	
Imon[3] 10uA/A For M-CRPS <= 150A at full load	100pF	Base Ripple = 75mV$_{pk-pk}$[3] Ripple + Noise = 300mV$_{pk-pk}$[3]	Output	Measure using 1KΩ load resistor + 100pF
Imon[3] 10uA/A For M-CRPS > 150A at full load	100pF	Base Ripple = 75mV$_{pk-pk}$[3] Ripple + Noise = 300mV$_{pk-pk}$[3]	Output	Measure using 499Ω load resistor + 100pF

Imon[3] 0-2mA = 0-200% load	100pF	Base Ripple = $75mV_{pk-pk}$[3] Ripple + Noise = $300mV_{pk-pk}$[3]	Output	Masure using 1.65kΩ load resistor + 100pF

Notes:

1. Refer to PMBus specification for aggregate requirements.
2. Noise measurements shall be performed using 20MHz bandwidth otherwise noted.
3. Measured at 1MHz bandwidth.
4. Measured at 10KHz bandwidth.

10 Environmental Requirements

10.1 Temperature

Minimum start-up and operating ambient: -5°C
Maximum operating ambient: See *Section 3.1* for operating requirements.
Non-operating ambient: -40°C to +70°C (Maximum rate of change of 20°C/hour)

10.2 Humidity

Operating: To 85% relative humidity (non-condensing)
Non-Operating: To 95% relative humidity (non-condensing)

NOTE: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

10.3 Altitude

Operating: to 3050 m
Non-operating: to 15200 m

10.4 Mechanical Shock

Non-operating: 50 G Trapezoidal Wave, Velocity change = 170 in. / sec.
Three drops in each of six directions are applied to each of the samples

10.5 Random Vibration

Non-operating
Sine sweep:
5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15 min at each of 3 resonant points;
Random profile:
5Hz @ $0.01g^2/Hz$ to 20Hz @ $0.02g^2/Hz$ (slope up); 20Hz to 500Hz @ $0.02g^2/Hz$ (flat);
Input acceleration = 3.13gRMS; 10 min. per axis for 3 axis on all samples

10.6 Thermal Shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30*C/min. * transition time * 15*C/min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

11 FRU Requirements

The FRU can be implemented using a physical EEPROM or alternatively using a non-volatile area of the secondary side MCU.

11.1 FRU Data

The FRU data format shall be compliant with the IPMI ver.2.0 specification. The current version of these specifications is available at https://www.intel.com/content/www/us/en/products/docs/servers/ipmi/ipmi-second-gen-interface-spec-v2-rev1-1.html the following is the exact listing of the EEPROM content. During testing this listing shall be followed and verified.

11.2 Device Protocol

The FRU device will implement the same protocols as the commonly used AT24C02 device, including the Byte Read, Sequential Read, Byte Write, Page Write and Random Read protocols.

11.2.1 Data Format

The minimum information to be contained in the FRU device is shown in the following table.

Table 11-1 Minimum FRU contents

Area Type	Description	
Common Header	As defined by the IPMI FRU document	
Product Info Area	As defined by the IPMI FRU document.	
MultiRecord Area	Record 1	Power Supply Info
	Record 2	Main Output
	Record 3	12VSB Output
	Record 4[1]	M-CRPS Identifier[1]
	…	…

Notes:

1. Refer to *Table 11-2 M-CRPS FRU MultiRecord definition*.

Table 11-2 M-CRPS FRU MultiRecord definition

Offset (decimal)	Field length (decimal)	Field	Value	Comments
0	1	Record Type ID	0xC2	
1	1	[7] – End of list [6:4] – Reserved [3:0] – Record format version	000b	
2	1	Record length		
3	1	Record Checksum (zero checksum)		
4	1	Header Checksum (zero checksum)		

5	3	Manufacturer ID	Byte 0	LSB
			Byte 1	
			Byte 2	MSB
8	1	Record version	01h – Version 1	
9	2	M-CRPS Revision [15:8] – Major number [7:0] – Minor number	 01h 00h	Revision 1.0
11	1	M-CRPS Version [7:4] – Major number [3:0] – Minor number	 1h 0h	Version 1.0
12	1	M-CRPS Type [7:4] – Input [3:0] – Output	[7:4] Input 0h – AC/DC 240VAC/240VDC Input 1h – AC/DC Input 277VAC/380VDC 2h – -48VDC Input 3h – +54V Input 4h-Fh – Reserved [3:0] Output 0h – +12V Output 1h – +51V Output 2h – +54V Output 4h-Fh – Reserved	
13	1	M-CRPS Outline	00h – 73.5 x 185.0 mm 01h – 73.5 x 265.0 mm 02h – 60.0 x 185.0 mm 03h-FFh – Reserved	
14	1	M-CRPS Cooling Type [7:4] – Cooling [3:0] – Temperature range	[7:4] Cooling 0h – Regular airflow 1h – Reversed airflow 2h – Immersion 4h-Fh – Reserved [3:0] Temperature range 0h – Enterprise -5degC to 55degC 1h – Storage -5degC to 70degC 2h – Telecom -40degC to 65degC 3h-Fh – Reserved	
15	1	M-CRPS output derating [7:5] – Reserved [4] – Output will be derated if the M-CRPS has insufficient input voltage.		
		M-CRPS Efficiency [3] – Reserved [2] – Titanium [1] – Platinum [0] – Gold	Example: 04h = Titanium efficiency	Efficiency of the M-CRPS
16	16	OEM		OEM Info

11.2.2 Write Protection

The contents of the FRU shall have write protection mechanism using the PMBus command MFR_FRU_PROTECTION with the hexadecimal number DBh using Write Byte and Read Byte types of commands with PEC. A read value of 00h means the FRU can be written and a value of 01h means the device can't be written (write protection activated), same values apply for Write operation.

12 Firmware Requirements

12.1 PMBus

12.1.1 Related Documents

- PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.2
- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.2
- System Management Bus (SMBus) Specification Version 2.0
- System Management Bus (SMBus) Specification Version 3.0

12.1.2 Addressing

The PSU PMBus device address locations are shown below. For redundant systems there are up to two signals to set the address location of the PSU once it is installed in the system: Address1 (A1) and Address0 (A0). For non-redundant systems the PSU device address location should be B0h.

Table 12-1Power supply PMBus device address locations

Addresses used:	**X**	**X**	**X**	**X**	**X**	**X**
System addressing Address1/ Address0	0/0	0/1	1/0 [3]	1/1 [3]	Note 3	Note 3
PMBus device read / write addresses [2]	B0h/B1h[1]	B2h/B3h	B4h/B5h	B6h/B7h	B8h/B9h	Bah/BBh

Notes:

1. Non-redundant systems (single PSU) will use the 0/0 address location.
2. The addressing method uses the 7 MSBs bits to set the address and the LSB to define whether a device is reading or writing. The addresses defined above use 8 bits including the read/write bit.
3. See more details in section *9.6 A0 and A1 Signals (Inputs)*.

The PSU shall have an IPMI FRU (field replaceable unit) serial EEPROM. It shall be located at the following addresses. This might be a separate physical device from the PMBus device or MCU emulated using a non-volatile memory area. This is intended to align with existing IPMI standards.

Table 12-2 Power supply IPMI FRU device address locations

Addresses used:	**X**	**X**	**X**	**X**	**X**	**X**
System addressing Address1/ Address0	0/0	0/1	1/0 [3]	1/1 [3]	Note 3	Note 3
FRU device read/write addresses [2]	A0h/A1h [1]	A2h/A3h	A4h/A5h	A6h/A7h	A8h/A9h	Aah/Abh

Notes:

1. Non-redundant systems (single PSU) will use the 0/0 address location.
2. The addressing method uses the 7 MSBs bits to set the address and the LSB to define whether a device is reading or writing. The addresses defined above use 8 bits including the read/write bit.

3. See more details in section *9.6 A0 and A1 Signals (Inputs)*.

12.1.3 Hardware

The device in the power supply shall be compatible with both SMBus 2.0 'high power' specification for I2C Vdd based power and drive (for Vdd = 3.3V). This bus shall operate at 3.3V.

12.1.4 PMBus Power Sourcing

The circuits inside the power supply shall derive their power from the standby output. For redundant power supplies the device(s) shall be powered from the system side of the OR'ing device. The PMBus device shall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system.

12.1.5 Pull Ups

Only 100KΩ pull-up resistors shall be on SCL or SDA inside the power supply connected to 3.3VSB. The main pull-up resistors are provided by the system and may be connected to 3.3V or 5V. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail.

12.1.6 Data Speed

The PMBus device in the power supply shall operate at the SMBus speed stated in below table and avoid using clock stretching that can slow down the bus. For example, the power supply can clock stretch while parsing a command or a power supply servicing multiple internal interrupts or NACK may require some use of clock stretching. Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

Table 12-3 SMBus speed range

Parameter	Value
SMBus speed	50 kHz to 400 kHz

The PMBus device shall support SMBus cumulative clock low extended time (Tlow:sext) of < 25msec. This requires the device to extend the clock time no more than 25msec between START and STOP for any given message.

12.1.7 Bus Errors

The PMBus device shall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions 10ms later.

The device must recognize SMBus START and STOP conditions on ANY clock interval. (These are requirements of the SMBus specifications but are often missed in first-time hardware designs.) The device must not hang due to 'runt clocks', 'runt data', or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup, or hold times that are shorter than the minimums specified by the SMBus specification. The device is not required to operate normally but must return to normal operation once 'in spec' clock and data timing is again received. Note if the device 'misses' a clock from the initiator due

to noise or other bus errors, the device must continue to accept 'in spec' clocks and re-synch with the initiator on the next START or STOP condition.

12.1.8 Additional SMBus hardware requirements

- 300ns maximum fall time with a 400pF capacitive load and 2.7Kohm pull up to 3.3V.
- 10ns minimum fall time with a 20pF capacitive load and 2.7Kohm pull up to 3.3V.
- The power supply shall not load the SMBus if it has no input power.

12.1.9 Writing to the power supply

When responding to read commands the power supply shall extend the clock until all writing of data to the command is complete. The power supply must still meet the Tlow:sext max time of 25msec described in section *12.1.6 Data Speed*. This is needed to make sure if the system performs a series of writes and then an immediate read to the same command the power supply returns the value just written to the power supply.

12.1.10 PAGE

Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR_FAULT command.

12.1.11 PAGE_PLUS_WRITE and PAGE_PLUS_READ (05h/06h)

The new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands are used with the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, and STATUS_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own initiator in the system. The instances at PAGE 00h are controlled by the system management agent 1 and the instances at PAGE 01h are controlled by the system management 2. Below are the protocols used to read and clear the STATUS_ commands using the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands.

Reading STATUS_WORD
Block Write – Block Read Process Call with PEC

Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write – Block Read Process Call with PEC

Figure 12-1 Writing/Reading STATUS commands with PAGE_PLUS_READ

Clearing STATUS commands (write '1' to clear a bit)
STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write with PEC

STATUS_WORD cannot be cleared directly It is cleared based on lower level status commands

Figure 12-2 Clearing STATUS commands using PAGE_PLUS_WRITE

12.1.12 Sensors

The following PMBus commands shall be supported for the purpose of reporting current, voltage, power, and temperature. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output of the PSU shall be zero amps and zero volts. Sensors shall meet requirements from 100VAC to 127VAC and from 200VAC to 240VAC (or -36VDC to -75VDC for DC input power supplies). They shall be tested down to 5% load.

Table 12-4 Current/Power/Temperature monitoring PMBus commands

PMBus command	Description
READ_EIN	New input energy counter described below. Added to PMBus rev 1.2 spec. Uses direct format for the power accumulator; unsigned integer value for the sample count.
READ_PIN	Input power meter based on PMBus rev 1.1 spec. Uses Linear formatting.
READ_IOUT	Output current in amps for the total 12V current. The other outputs are not sensed. Uses linear format.

READ_EOUT	New output energy counter described below. Added to PMBus rev 1.2 spec. Uses direct format for the power accumulator; unsigned integer value for the sample count.
READ_TEMPERATURE_1	Returns the temperature in °C of the inlet temperature. Based on PMBus rev 1.1 spec. Uses linear format.
READ_TEMPERATURE_2	Returns the temperature in °C of the hot spot temperature. Based on PMBus rev 1.1 spec. Uses linear format.

12.1.13 Sensor Functionality in Different PSU States and Configurations

The functionality of READ_EIN and READ_EOUT in different PSU configurations is stated in the below table. The PSU must continue incrementing the sample counter even if AC power is not present to the PSU but the PMBus device in the PSU is powered from the other power supplies in parallel.

Table 12-5 READ_EIN & READ_EOUT Functioning in differing states

Number of PSUs in system	One PSU state (PSU_1)	Rest of PSU states (PSU_n)	PSU_1 Power Accumulator	PSU_1 Sample counter
1 or more	ON & AC present	All ON & AC present	New power values continue to add to the power accumulator based on loading condition	Sample counter increments every sample period
1 or more	*Stby & AC present*	*All ON & AC present*	*New power values continue to add to the power accumulator based on loading condition*	*Sample counter increments every sample period*
1 or more	OFF & no AC present	All OFF & no AC present	Reset power accumulator values to 00 when AC power is reapplied	Reset sample counter to 00 when AC power is re-applied
2 or more	AC power not present	Rest of PSUs in standby mode & AC present	Continue adding 0W to accumulator every sample period	Incrementing sample counter every sample period
2 or more	AC power not present	Rest of PSUs ON & AC present	Continue adding 0W to accumulator every sample period	Incrementing sample counter every sample period

READ_PIN, READ_IOUT, and READ_TEMPERTURE_x shall continue to report accurate values when the PSU is in standby mode or when it has no AC power but is in parallel with another PSU(s) with AC power and standby power present.

12.1.14 READ_PIN (97h)

The power supply shall provide input power data in watts. The data shall be reported using the PMBus linear format. The data shall be the average input power or filtered input power. If a simple average is used to provide average input power, the minimum averaging duration shall be 2 seconds. If filtering is used; the maximum filter bandwidth shall be 0.5 Hz. The accuracy shall be tested by polling with the READ_PIN command at a rate ranging from 1 sample / second to 10 samples / second.

Table 12-6 READ_PIN requirements summary

	MIN	MAX	Description
Format	PMBus linear format		PMBus data format; refer to PMBus specification for details
Averaging period	2 seconds	10 seconds	The AC input power shall be averaged using a simple averaging method of a filtering method. This defines the max/min period for simple averaging and the bandwidth range if the filter method is used.
Filtering bandwidth	0.1 Hz	0.5 Hz	
Accuracy	+/-1%		

(>125W – Max load/Peak Power)			The input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy (50W – 125W load)	+/-1.25W		
Accuracy (<50W load)	+/-5W		
System polling rate	1 sample/ second	10 samples / second	The power supply shall be polled over this range of rates while testing accuracy.

12.1.15 READ_IOUT (8Ch)

The power supply shall provide output current data in amperes. The data shall be reported using the PMBus linear format. The data shall be the average output current or filtered output current. If a simple average is used to provide average output current, the minimum averaging duration shall be 2 seconds. If filtering is used; the maximum filter bandwidth shall be 0.5 Hz. The minimum accuracy is specified in the table below. The accuracy shall be tested by polling with the READ_IOUT command at a rate ranging from 1 sample / second to 10 samples / second.

Table 12-7 READ_IOUT requirements summary

	MIN	MAX	Description
Format	PMBus linear format		PMBus data format; refer to PMBus specification for details
Averaging period	2 seconds	10 seconds	The output current shall be averaged using a simple averaging method of a filtering method. This defines the max/min period for simple averaging and the bandwidth range if the filter method is used.
Filtering bandwidth	0.1 Hz	0.5 Hz	
Accuracy (300W – Max load/Peak Power)	+/-1%		The output current data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy (150W – 300W load)	+/-3%		
Accuracy (40W – 150W load)	+/- 0.9A		
System polling rate	1 sample/ second	10 samples / second	The power supply shall be polled over this range of rates while testing accuracy.

12.1.16 READ_EIN (86h)

The new READ_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of the number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 12-8 READ_EIN requirements summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details.
P_{sample} averaging period	4 AC cycles		Period instantaneous input power is averaged over to calculate P_{sample}.
READ_EIN update period	80/66.7ms (50/60Hz)		Period at which the power accumulator and sample counter are updated
Accuracy	+/-1%		

(>125W – Max load/Peak Power)			The input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy (50W – 125W load)	+/-1.25W		
Accuracy (<50W load)	+/-5W		
Range of System polling period	1 sec	100 ms	The PSU shall be polled over this range of rates while testing accuracy.
IMPORTANT: The PSU READ_EIN update period MUST always be less than the system polling period. To make sure the PSU is compatible with all possible system polling periods; the PSU must update the READ_EIN power accumulator and sample counter at a period less than 100msec (required period is 4 AC cycles 80/67msec).			

12.1.17 READ_EOUT (87h)

The new READ_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of the number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 12-9 READ_EOUT requirements summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details.
P_{sample} averaging period	Nominal 8 msec		Period instantaneous input power is averaged over to calculate P_{sample}.
Sampling period	Nominal 8 msec		Period at which the power accumulator and sample counter are updated
[P_{accum} / N] Accuracy (5% to 100% load)	±2%		The calculated output power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
System polling rate	1 sample /s	10 samples /s	The PSU shall be polled over this range of rates while testing accuracy.

12.1.18 READ_EIN & READ_EOUT Formats

The READ_EIN and READ_EOUT commands shall use the PMBus direct format to report an accumulated power value and the sample count. The PMBus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the PMBus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

READ_EIN and READ_EOUT shall use the SMBus Block Read with PEC protocol in the below format.

Figure 12-3 READ_EIN command format

READ_EIN and READ_EOUT Accumulators

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached (> 7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

Important note: When the PSU responds to the system requesting READ_EIN or READ_EOUT data; the data in the sample count must always align with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ_EIN and READ_EOUT register at the same time.

Figure 12-4 READ_EIN functional diagram

Table 12-10 READ_EIN variables description

Parameter	Description
Psample:	The sampled power value in linear or direct format
Paccum:	2 bytes in PMBus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + … + Psample(n)
N:	3 byte unsigned integer value. The number of accumulated power values summed in Paccum
Prollover:	The max value of Paccum before a rollover will occur
Paccum_rollover_count:	1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h

12.1.19 COEFFICIENT (30h)

The power supply shall support the PMBus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ_EIN and READ_EOUT accumulated power values.

Table 12-11 m, B, R coefficients

Command	COEFFICIENTS support	m	B	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h
all other commands	*Optional*	*X*	*X*	*X*

12.1.20 Status Commands

The following PMBus STATUS commands shall be supported. All STATUS commands stated in Table below as supporting PAGE instances shall support the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared using one of the methods shown in section 10.1.21.

The STATUS commands that are supported with the PAGE_PLUS_READ and PAGE_PLUS_WRITE commands shall still support direct access of the base STATUS_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS_FAN_1_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the SMBAlert# signal. The new SMBALERT_MASK command is used to define which status event control the SMBAlert# signal. Default values for these mask bits are shown in the table below.

Table 12-12 PMBus STATUS commands summary

PMBus command	Bit location	PSU state when bit is asserted ('1')	Instances No PAGE'ing [2] PAGE 00h = BMC PAGE 01h = ME	**SMBALERT_MASK defaults** for each of the three instances (No PAGE, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#
STATUS_WORD			No PAGE, 00h, 01h	
OFF	6 (lower)	OFF		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
TEMPERATURE	2 (lower)	Refer to STATUS_TEMPERATURE		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
CML	1 (lower)	ON		NA
VOUT	7 (upper)	Refer to STATUS_VOUT		NA
IOUT/POUT	6 (upper)	Refer to STATUS_IOUT		NA
INPUT	5 (upper)	Refer to STATUS_INPUT		NA
POWER_GOOD (Negated)	3 (upper)	PWOK is deasserted		NA

FANS	2 (upper)	Refer to STATUS_FANS		NA
STATUS_VOUT			No PAGE'ing	
VOUT_OV_FAULT	7	OFF		1, NA, NA
VOUT_OV_WARNING	6	ON		1, NA, NA
VOUT_UV_WARNING	5	ON		1, NA, NA
VOUT_UV_FAULT	4	OFF		1, NA, NA
STATUS_IOUT			No PAGE'ing, 00h, 01h	
IOUT_OC_FAULT	7	OFF		1, 1, 1
IOUT_OC_WARNING	5	ON		1, 1, 0
POUT_OP_FAULT	1	OFF		1, 1, 1
POUT_OP_WARNING	0	ON		1, 1, 1
STATUS_INPUT			No PAGE'ing, 00h, 01h	
VIN_OV_FAULT	7	OFF		1, 1, 0
VIN_OV_WARNING	6	ON		1, 1, 1
VIN_UV_WARNING	5	ON		1, 1, 1
VIN_UV_FAULT [1]	4	OFF		1, 1, 0
Unit off for low input voltage	3	OFF		1, 1, 1
IIN_OC_WARNING	1	ON		1, 1, 1
PIN_OP_WARNING	0	ON		1, 1, 1
STATUS_TEMPERATURE			No PAGE'ing, 00h, 01h	
OT_FAULT	7	OFF		1, 1, 1
OT_WARNING	6	ON		1, 1, 0
STATUS_FANS_1_2			No PAGE'ing	
Fan 1 fault[3]	7	OFF		1, NA, NA
Fan 1 warning[3]	5	ON		1, NA, NA

Notes:

1. The Vin Fault bit in STATUS_INPUT shall get asserted if the input power has dropped below the PSU's operating range for any duration of time, even if the PSU continues to operate normally through a momentary input dropout event.
2. 'No PAGE' is the standard STATUS_ commands accessed directly without using the PAGE_PLUS commands.
3. 3 All fans/rotors in the PSU shall be OR'ed into a single fan status bit for fault and warning conditions.

12.1.21 Resetting Status Bits

The STATUS_ commands shall be reset only by the below methods. If the event is still present that caused the assertion of the status bit, the bit shall stay asserted after clearing.

- Writing a '1' to any given bit location shall reset only that bit of the command.

- Sending a CLEAR_FAULTS command to the PSU shall reset all STATUS_ bits to '0'. CLEAR_FAULTS shall clear all STATUS commands at a given PAGE if PAGE command is supported. If the PAGE is set to FFh; all STATUS bits in all PAGEs shall be cleared.
- Cycling input power OFF for 1 second or more then ON shall reset all STATUS_ bits to '0'.
- Systems with redundant power supplies where only one of the supplies cycle input power ON/OFF; the power cycled PSU shall reset the STATUS_ bits to '0' only when powered back ON. If the PSU is kept OFF, the STATUS_ bits shall not be reset.
- Cycling the PSON# signal from de-asserted to asserted shall reset the STATUS_ bits to '0'. The bits shall be reset only on the assertion of PSON#; not the de-assertion.

  Note: Exception for Over Current Fault shutdown; By default, PSON# cycling shall NOT reset the over current fault bit or cause the power supply to restart. Only a cycle of the input power shall reset the over current fault bit and allow the PSU to power on again. To configure this behavior the user shall change the proper register in the configuration file described in *Section 12.8.3.3 Main Output Configuration Block.*

12.1.22 Default Limits for Warning and Faults

Warning limits shall be set with enough margin to guarantee no false warnings will occur if PSU operates within the specified requirements, but before the PSU shuts down. Fault limits shall be set at limits equal to or greater than the level at which the PSU shuts down.

12.1.23 Resetting to Default Limits

The PSU shall reset the warning and fault limits to default values for the following case.

- Input power cycling
- PSON power cycling

Notes:

1. Programmed values shall not change unless secondary biasing to the MCU is lost.

12.1.24 Faults and Error Checking

The PSU shall support PEC per the SMBus 2.0 specification.

12.1.25 Packet Error Checking

The PSU shall support packet error checking to support error checking and handling.

12.1.26 Capability and Inventory Reporting

The following commands shall be supported for discovery of the power supplies capabilities.

Table 12-13 PMBus PSU capability & inventory commands summary

PMBus command	Value	Description
CAPABILITY	PEC = supported Bus speed = 400kHz SMBAlert# = supported	Defines the power supplies PEC support, bus speed, and support of SMBAlert

QUERY	Linear formats for all but READ_EIN / READ_EOUT which is Direct	Used to determine if the PSU supports a specific command. It should return the proper information about any commands listed in Table 12-38 Summary of PMBus commands
PMBUS_REVISION	0010 0010	Used to verify the PMBUS_REVISION the PSU is based on. This shall be set to revision 1.2.
MFR_TEMP1_MAX	Trip threshold for the ambient temperature sensor (TEMP1) to assert SMBAlert#	Defines the maximum inlet temperature to generate a warning condition in the STATUS_TEMPERATURE command.
MFR_TEMP2_MAX	Trip threshold for the hot spot temperature sensor (TEMP2) to assert SMBAlert#	Defines the maximum hotspot temperature to generate a warning condition in the STATUS_TEMPERATURE command.
MFR_IOUT_MAX	Rated output current using the linear format	Defines the maximum rated output current on the 12V rail.
MFR_POUT_MAX	Rated output power using the linear format	Defines the maximum rated output power of the PSU.
APP_PROFILE_SUPPORT	05h	Defines that the PSU supports this application profile.

12.1.27 SMBAlert# Signal

The SMBAlert# signal may be asserted by the PSU for any of the supported STATUS events. The events that control SMBAlert# can be masked using the SMBALERT_MASK command. Default masking is shown in *Section 12.1.29 SMBALERT_MASK (1Bh)*.

By default, the SMBAlert# signal is asserted for the following cases:

1. STATUS_INPUT (UV Fault bit): input voltage drops below the fault threshold of the PSU for > 2ms.
2. STATUS_IOUT (Iout OC Warning bit): Output current exceeds the PSU capability, but PSU has not shutdown.
3. STATUS_TEMPERATURE (OT Warning): Thermal sensor for PS inlet temperature or on a hot spot inside the PSU has exceeded its warning temperature.

Table 12-14 PSU SMBAlert# timing requirements

Item	Description	PMBus command	MIN	MAX
T_{alert_input}	Timing from input voltage dropping to 0VAC to SMBAlert# going low	STATUS_INPUT UV Fault		2 msec
$T_{OC_Warning}$	Timing from output over current warning to SMBAlert# going low	STATUS_IOUT	10 msec	20 msec[1]
$T_{OC_Warning_latch}$	Time the PSU holds the SMBAlert# signal asserted after an over current warning event	STATUS_IOUT	145 msec	155 msec[3]
$T_{OC_pmaxprotection}$	Timing from output tripping	None		20µsec
T_{over_temp}	Hot spot temp > warning threshold	STATUS_TEMPERATURE Over temp warning		1 sec
$T_{smbalert_shutdown}$	Minimum time PSU must continue to operate within voltage regulation limits and PWOK asserted after the SMBAlert# signal has been asserted due to an over temperature event.	NA	1sec	
$T_{max_warning}$	Hot spot temperature inside the PSU that causes SMBAlert# to assert.	MFR_TEMP2_MAX	Tmax_continuous	Tshutdown

Notes:

1. This time must be shorter than the OCP trip delay.
2. 2 msec Max Talert_input only applies to loads higher than 10% of the rated load where SmarRT is meaningful, refer to *Section 12.3 Smart Ride-Through (SmaRT)* for more details.
3. If bit SMBAlertPL4Behavior of register 001Ah in *Table 12-75 Miscellaneous configuration block* is 1 the SMBAlert# shall keep asserted (low) until a clear command has been received.

12.1.28 SMBAlert# Operation in Standby Mode

The PSU shall assert the SMBAlert# signal only when the main outputs are ON. SMBAlert# shall stay de-asserted when the PSU is in standby mode when any bits in the STATUS commands get asserted.

12.1.29 SMBALERT_MASK (1Bh)

This allows the system to mask events from asserting the SMBAlert# signal and to read back this information from the PSU. SMBALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a '1' to the associated STATUS bits. The SMBALERT_MASK command is used in conjunction with the PAGE_PLUS command and STATUS_ commands. It is not supported for masking the Non-PAGE'd STATUS_ commands. Below are the protocols.

Reading mask values using PAGE_PLUS
Block Write – Block Read Process Call with PEC

Figure 12-5 PAGE_PLUS_READ command

Writing mask values using PAGE_PLUS
Block Write with PEC

STATUS_WORD is not used with SMBALERT_MASK. Only the 'root' event bits are used to control the SMBAlert signal

Figure 12-6 PAGE_PLUS_WRITE command

12.1.30 Alert Response Address (ARA)

The PSU shall not support ARA. After asserting the SMBAlert# signal, the PSU shall keep its address at its standard address; not change to 18h.

12.1.31 Setting and Resetting the SMBAlert# Signal

The SMBAlert# signal shall be asserted whenever any un-masked event has occurred. This is a level detected event. Whenever the event is present SMBAlert# shall be asserted. The SMBAlert# signal shall not de-assert at any time if the event that has caused the assertion is still present.

The SMBAlert# signal shall be cleared and re-armed by the following methods:

- Clearing STATUS bits causing the asserted SMBAlert# signal.
- Power cycling with PSON or with input power
- Masking the event with SMBALERT_MASK

12.1.32 Fan Speed Control

The PSU shall support the PMBus commands to allow the system to control and monitor the PSU's fan.

12.1.33 FAN_CONFIG_1_2 (3Ah)

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

Table 12-15 FAN_CONFIG_1_2 command

Bits	Value	Meaning
7	1	Fan in position 1
6	0	Fan 1 commanded in Duty Cycle
5:4	Not used	
3	0	Far or No fan in position 2
2	Not used	
1:0	Not used	

12.1.34 FAN_COMMAND_1 (3Bh)

The system may increase the power supply's fan speed through using the FAN_COMMAND_1 command. This command can only increase the power supply's fan speed; it cannot decrease the PSU fan speed below what the PSU commands.

The control is configured to be duty cycle controlled using the linear format of the PMBus protocol.
The exponent N is fixed to a value of 0 (N = 0).

12.1.35 READ_FAN_SPEED_1 (90h)

The system will read the fan speed by using the READ_FAN_SPEED_1 command. This data shall return the fan speed in the PMBus linear format.

12.1.36 PSU Commands Supported For Testing Purposes

The PSU shall support commands for PSU testing purposes only please refer to *Section 12.1.58 Status Simulation Commands* for more details.

12.1.37 OT_WARN_LIMIT (51h)

The PSU shall allow the system to set new values to the warning threshold for the hot spot temperature sensor using the OT_WARN_LIMIT command, in degrees Celsius. The two data bytes are formatted in the Linear Data format.

This may be used by the system test FW to simulate an assertion of the SMBAlert# signal due to a temperature warning event. This value shall be reset to the default value with any input power cycle or PSON power cycle.

12.1.38 IOUT_OC_WARN_LIMIT(4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current that causes an output over-current warning. The two data bytes are formatted in the Linear Data format. This may be used by the system test FW to simulate an assertion of the SMBAlert# signal due to an over-current warning event.

12.1.39 Modification to 10.2.6 and 10.3 of PMBus Part II revision 1.2

Some changes/clarifications to the PMBus revision 1.2 specification as stated in this section to allow compatibility with server systems.

12.1.40 PMBUS_REVISION

This is a correction to the table in the PMBus part II specification regarding the PMBUS_REVISION command.

Table 12-16 PMBUS_REVISION command

Bits [7:4]	Part I revision	Bits [3:0]	Part II Revision
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2

12.1.41 Continuous Assertion After Clearing If Condition Is Still Present

If the warning or fault condition is present when a bit is cleared, the bit and associated SMABLERT# signal stays asserted with no momentary transition to a de-asserted state.

12.1.42 Conceptual View of How Status Bits and SMBAlert# Work

Figure 12-7 and *Figure 12-8* show conceptual schematics of how the status bits and SMBALERT# are to function. When a warning or fault event is detected, a latch is set. The output of this latch becomes the status bit in the lower level status register (such as STATUS_INPUT). The latch output is OR'ed with other status bits in this command to create the corresponding bit in STATUS_BYTE or STATUS_WORD. The output of the latch is also used to drive the SMBALERT# circuitry. The output of the latch passed through a gate controlled by the corresponding SMBALERT_MASK bit. If this bit is set, the output of the latch is

blocked from driving the SMBALERT# circuit. If the SMBALERT_MASK bit is cleared, the latch output is allowed to pass and drive the SMBALERT# circuit. When the SMBALERT# sees the rising edge of the latch output it asserts the SMBALERT# signal (output goes low). The SMBALERT# signal remains asserted until it is cleared. Note the behavior of the latch output and the SMBALERT_MASK. If the latch output is set, and the SMBALERT_MASK bit is changed from set to clear, the latch output is passed to the SMBALERT# circuit and will cause the SMBALERT# signal to assert. If this is not desired, the latch must be cleared before clearing the SMBALERT_MASK bit. As described above, the latch can be cleared by writing a 1 to corresponding bit in the status register. It can also be cleared with the CLEAR_FAULTS command.

Commands to clear a bit are gated by the PAGE command. CLEAR_FAULTS can be made to clear all faults on all pages by setting the page command to FFh. Conceptually the bit clearing commands act as pulses, driving the reset pin on the latch only momentarily. This means that if the event is ongoing (the event detector is still active) the output latch will stay asserted (1). This will cause the SMBALERT# to also stay asserted (or stay low) if the event is ongoing and the SMBALERT_MASK bit is not set. This also means that a host won't be able to see the status bit get cleared. If a host sends the command to clear a status bit and then reads the bit as set, it should interpret that to mean that the event is still happening.

Latch Logic

Set (S)	Clear (R)	Q
0	0	No change
1	0	1
0	1	0
1	1	1

*Figure 12-7 Conceptual Schematic of STATUS bits and SMBAlert# for commands that support PAGE_PLUS_*

*Figure 12-8 Conceptual schematic of STATUS bits and SMBAlert# without PAGE_PLUS_*

Notes:

1. When direct CLEAR_FAULTS command PAGE 0 shall be cleared also.

12.1.43 MFR_MAX_IOUT_CAPABILITY (F1h)

The PSU shall provide the Current levels which it can support along with their durations for the system to read using a Block Read command with a length of 14 bytes + PEC. The contents of each field are described in the following table.

Table 12-17 MFR_MAX_IOUT_CAPABILITY ccommand

Field name	Size (Bytes)	Magnitude
Irating (PL1)	2	Amperes[1]
Ipeak (PL2)	2	Amperes[1]
Ipeak (PL2) duration	2	ms[2]
Ipeak.pl3 (PL3)	2	Amperes[1]
Ipeak.pl3 (PL3) duration	2	ms[2]
Ipeak.pl4 (PL4)	2	Amperes[1]
Ipeak.pl4 (PL4) duration	2	us[2]

Note: Fields with 0 as value means not supported for a given level.

Figure 12-9 MFR_MAX_IOUT_CAPABILITY command

Notes:

1. Current values shall be represented using linear format (L11).
2. Time values shall be represented using Direct format.

3. The values on this command shall be dynamically adjusted based on the input voltage range the M-CRPS is operating.

12.1.44 IIN_OC_WARN_LIMIT (5Dh)

The register is used to program the input current warning limit. It uses block write-read protocol. Please refer to each design specification for the detailed values.

Table 12-18 IIN_OC_WARN_LIMIT (5Dh) Command definition

Input OCW (5Dh)		
Byte	**Definition**	**Comments**
0	Input OCW (Programmed value)	Read/Write
1		
2	Input OCW (current PS setting)	Read only
3		
4	Input OCW maximum (current PS setting)	Read only
5		
6	Input OCW minimum (current PS setting)	Read only
7		

Notes:

1. Definitions.
   a. **Input OCW (programmed value):** The initial value is the Input OCW maximum default value after the power supply has established its line status. Afterwards, if the OCW set point is programmed to a different value, the new value will be retained.
   b. **Input OCW (current PS setting):** This value in most cases will be the same value as item #a above. The only exception would be if a line status (the actual operational voltage after 500mS) change occurred and the programmed value is now outside of the new range for that line condition. In that case, either the minimum or the maximum value of the new range will be set.
   c. **Input OCW maximum:** This item is the maximum allowable programmed value which corresponds to the operational line voltage condition. The maximum over current value is called out in the parametric electrical specification which is typically at ≤95Vac, ≤197.5Vac, ≥192Vdc or ≥40Vdc.
   d. **Input OCW minimum:** This item is the minimum allowable programmed value which corresponds to the operational line voltage condition. The minimum set point is the greater of 25% of the Input OCW maximum or 1A.
2. If no line status has been determined, for example the power supply was installed into a redundant system, and no input power has been applied, the power supply will ACK the command and respond with FF's.
3. The initial setting of the default values will occur after the line status has been established and prior to asserting VINOK.
4. The Input OCW ranges will be set as a function of the line status algorithm. Once the line status has been established the Input OCWs default value ranges (Input OCW Maximum and Minimum) will be latched. The only time these values can change is if one of the conditions as called out in the line status is met.

5. The average window is as defined in the design specification of the PSU.
6. Hysteresis for deserting the OCW setting is as defined in the main body of the Design Specification.
7. If the program value is outside the specified range: For values above the maximum OCW the power supply will set the OCW to the specified maximum value; For values below the minimum OCW the power supply will set the OCW to its minimum value. No CML bit is to be set.
8. Flow chart definitions:
    a. Line Condition: Is the current line voltage (real time) that is being applied to the power supply
    b. Line Status: This is the current line status of the power supply as called out in the Line Status register described in *Section 12.1.45 MFR_LINE_STATUS (E1h)*. The line status and line condition are usually in alignment with each other but there are conditions when they will not be aligned. A good example would be with a non-split rated power supply where the line status is set as a high line power supply but is operating under a low line condition.
9. Input OCW flow chart

Figure 12-10 Input OCW flowchart

a. **Line Status:** This is the operational line condition of the power supply as called out in the Line Status Register described in *Section 12.1.45 MFR_LINE_STATUS (E1h)*.
b. **Line Condition** (real time input voltage)
   i. Maximum Line Condition: is defined as the operational voltage range for the input OCW maximum setting. For example, a power supply may have two input over current maximum settings when operating at as a high line power supply: Input Voltages ≤197.5V and Input Voltages ≥ 197.5V.
   ii. Minimum Line Condition: The minimum Input OCW for a line condition, unlike the maximum setting for line condition, is a fixed value as called out in the electrical parametric specification for the operational line status.

12.1.44.1 High Line Voltage Excursion

Figure 12-11 shows the expected behavior of the power supply when operating as a high line power supply and the "Input OCW has been unmasked". Typically, there will be two different maximum input current default values for the high line power supply as a function of its operating voltage. Once the input voltage has transition from one state to the other, a 500mS timer is initiated. If after 500mS the input voltage remains at its new state, the input current OCW setting will default to the new value of that state. The only exception in this example is if the input OCW was set at a lower value than the default state value. For example, in this example, if the programmed value was set at 7A there would be no change in the input OCW setpoint. The Input OCW will always be the lower of the maximum default value for the high line condition or the programed setting.

Figure 12-11 High line voltage excursion representation

12.1.44.2 High Line to Low Line Status Change

Figure 12-12 shows the expected behavior when a high line power supply transitions to a low line power supply. Once the voltage drops into the low line state a 10-second timer (reference the line status section for line status behavior within this specification) is initiated by the power supply to inform the system of its new input voltage condition. It is up to the system whether it allows the power supply to proceed with

the change to its new low line condition or leaves it as a high line power supply. Once the system informs the power supply to proceed to change its line status state the power supply changes its line status and sets the Input OCW setting to its new default condition for that line voltage.

Figure 12-12 High line to low line status change representation

12.1.44.3 Low Line Voltage Excursion

Figure 12-13 shows the expected behavior of the power supply when operating as a low line power supply and the "Input OCW has been unmasked". Typically, there will be two different maximum input current default values for the low line power supply as a function of its operating voltage. Once the input voltage has transition from one state to the other, a 500mS timer is initiated. If after 500mS the input voltage remains at its new state, the input current OCW setting will default to the new value of that state. The only exception in this example is if the input OCW was set at a lower value than the default state value. For example, in this example, if the programmed value was set at 10A there would be no change in the input OCW setpoint. The Input OCW will always be the lower of the maximum default value for the low line condition or the programed setting.

Figure 12-13 Low line voltage excursion representation

12.1.44.4 Low Line to High Line Status Change

Figure 12-14 shows the expected behavior when a low line power supply transitions to a high line power supply. Once the voltage increases into the high line state a 10-second timer (reference the line status section for line status behavior within this specification) is initiated by the power supply to inform the system of its new input voltage condition. It is up to the system whether it allows the power supply to proceed with the change to its new low line condition or leaves it as a low line power supply. Once the system informs the power supply to proceed to change its line status state the power supply changes its line status and sets the Input OCW setting to its new default condition for that line voltage.

For "Input OCW has been unmasked", when a PSU with low line status and its input voltage is 100Vac as an example, the current PS setting should be the "$_{Iin_OCW}$ for V_{in} ≥95Vac". When the input voltage is changed to 200Vac, the current PS setting should still be the "$_{Iin_OCW}$ for Vin ≥95Vac". It will adjust to "$_{Iin_OCW}$ for V_{in} ≥ 197.5Vac" only when the line status is allowed to change to a high line status. It means there are only two line conditions (one is V_{in} ≥95Vac and the other one is V_{in} <95Vac) for a low line status PSU.

IIN_OC_WARNING can only be cleared if next averaging window of the input current is below threshold.

Figure 12-14 Low line to high line status change representation

12.1.45 MFR_LINE_STATUS (E1h)

This contains the power input line status and the power input line source type that PSU supports. At the initial start-up, prior to turning on the main output, PWOK is low, and the bulk is greater than 100V, the power supply will determine its input type. There are several types of PSUs which is defined as below.

- Dual wattage PSU: PSU has different output wattage depending on input voltage.
- Wide ranged PSU: PSU supports full range of input without turning off.
- Telecom PSU: PSU supports Telecom input 48 Vdc.
- Extended High Line AC/High Line DC Mixed-mode PSU.

12.1.45.1 Mixed mode Input PSU (including dual wattage and wide ranged PSUs)

12.1.45.1.1 Initial Line

When PSU first initial the input before its bulk voltage reaches 100Vdc, the MFR_LINE_STATUS shall report depending on PSU type as one of the following:

- “0001b” – “No Power Input for wide-range AC PSU”, or
- “0101b” – “No Power Input for extended wide-range AC”, or
- “1000b” – “No Power Input for wide-range AC/low line DC mixed-mode PSU”, or
- “1001b” – “No Power Input for high line only AC”, or

- “1011b” – “No Power Input for extended wide-range AC/wide-range DC mixed-mode PSU”

In addition, all power settings will default to the high line settings (e.g. input power, output power, OCW threshold, etc.). When the input voltage is applied, and the bulk voltage reaches 100Vdc, the PSU starts the process of evaluating the input. When five consecutive AC cycles read the same voltage, or a DC steady voltage is present for more than 100ms the PSU will declare itself one of the following:

- “0000b” – “Low line, 50Hz, AC Detected”, or
- “0010b” – “High line, 50Hz, AC Detected”, or
- “0100b” – “Low line, 60Hz, AC Detected”, or
- “0110b” – “High line, 60Hz, AC Detected”, or
- “1100b” – “Low line DC, DC detected”, or
- “1010b” – “High line DC, DC detected”, or
- “1101b” – “Extended high-line 50Hz, AC Detected”, or
- “1110b” – “Extended high-line 60Hz, AC Detected”

Once the above settings have been determined, the power supply will latch the operational settings and not change its operational state during the PSU operation. If AC input, the frequency will not change from initial determination. The initial assessments will only be re-evaluated by the power supply under the following conditions:

- The secondary MCU resets due to the loss of input voltage and internal bias (not-redundantly powered) or
- The system issues a request to re-evaluate the line status. (MFR_LINE_STATUS(0xE1)[7]==1b)
- The PSU is reset due to programming.
- Secondary Bias Lost.

For AC voltage operation, a power supply will declare itself as a low-line power supply for input voltage that meets the minimum turn on voltage (84-90Vac) up to the high-line operation declared voltage (160Vac +/-5V).

For example: if a dual wattage power supply’s high-line declared set point is 158Vac and the input voltage is 157Vac the power supply would declare itself as a low-line power supply. In the case when the line voltage falls between the high-line declared voltage (160Vac +/-5V) and the minimum high-line turn-off voltage, the dual wattage power supply will declare itself as a high-line power supply but remain off due to low voltage input for high-line operation. When power supply remains off, the STATUS_INPUT (0x7C) shall show “Unit Off for Low Input Voltage”.

In the case where the line voltage is above the minimum high-line turn-on threshold, the power supply shall declare itself as a high-line power supply and is ready to operate as a high-line power supply over the range of the high-line turn off voltage to 264Vac once PSON# has been enabled.

For a wide range power supplier, it will declare high-line power supplier as long as the line voltage over high line declared voltage (160Vac +/-5V). The wide range power supplier will always remain on if input voltage meets the low-line minimum turn on voltage (84-90Vac).

For DC voltage operation, a power supply will declare itself as a DC low-line power supply for input voltage that meets the minimum turn on voltage (180Vdc). If power supplier supports DC high-line, and input voltage meets 328Vdc, it shall declare voltage to DC high-line.

If input voltage meets the turn-on threshold as description above, the VINOK signal shall be asserted.

12.1.45.1.2 Pre-Set

If initial line is done and line status is latched, the power supply shall continue to monitor the line voltage to re-assess whether or not the current line status for the power supply has changed under the conditions: The input voltage has changed to meet a different line status condition.

The behavior shall follow the "Pre-set Block" in the flowchart. If there is any status change the power supply shall notify system with bit-4 of STATUS_MFR_SPECIFIC (0x80) and bit-4 of High byte STATUS_WORD (0x79). Power supply shall depend on the bit-7 of MFR_LINE_STATUS (0xE1h) which is set by system to update the MFR_LINE_STATUS and related parameters (e.g. power ratings, OCW settings, and etc.). If the bit-7 of MFR_LINE_STATUS (0xE1) is not set, power shall keep previous settings without changing. The detail is in "Notify Task Block" in *Figure 12-18 MFR_LINE_STATUS Notify task flow diagram.*

For wide range PSU, there are different behaviors depending on the mask of input OCW. If the input OCW is unmasked, the behavior shall be the same as dual wattage PSU. If the input OCW is masked, PSU shall directly notify the system with bit-4 of STATUS_MFR_SPECIFIC (0x80) and bit-4 of High byte STATUS_WORD (0x79).

12.1.45.2 Telecom Power Supply

When PSU first initial the input before its bulk voltage reaches 100Vdc, the MFR_LINE_STATUS shall report "0011b"– "No Power Input for Telecom DC PSU". When the input voltage is applied, and the bulk voltage reaches 100Vdc, the PSU starts the process of evaluating the input. A DC steady voltage is present for more than 100ms the PSU will declare itself as "0111b" – "Input is Telecom DC". The detail is in the Telecom PSU in *Figure 12-19 MFR_LINE_STATUS Telecom flow diagram*.

12.1.45.3 Extended High Line AC/High Line DC Mixed-mode PSU

When PSU first initial the input before its bulk voltage reaches 100Vdc, the MFR_LINE_STATUS shall report "1011b"– "No Power Input for extended wide-range AC/wide-range DC mixed-mode PSU, or No Power Input for extended high AC/high line DC mixed-mode PSU". When the input voltage is applied, and the bulk voltage reaches 100Vdc, the PSU starts the process of evaluating the input. An input steady voltage is present for more than 100ms the PSU will declare itself as:

- "1101b" – "Extended high-line 50Hz, AC Detected", or "1110b" – "Extended high-line 60Hz, AC Detected", or
- "1010b" – "High line DC, DC Detected".

The detail is in the PSU Page of the flowchart.

Table 12-19 MFR_LINE_STATUS definition

E1h	LINE_STATUS			
Bits	**Name**	**Value**	**Description**	**Note**
7	CHANGE_LINE_STATUS	1	PSU is able to update LINE_STATUS	Read/Write
		0	LINE_STATUS has been updated by PSU	
6	PSU_MISMATCH	0	No mismatch	Read/Write
		1	Power Supply mismatched	Read/Write
5:4		00	Reserved	
3:0	LINE_STATUS	0000	Low line, 50Hz, AC Detected	See Table 12-20
		0001	No Power Input for wide-range AC PSU	Identifies unpowered unit as a wide-range AC type, See Table 12-21
		0010	High line, 50Hz, AC Detected	
		0011	No Power Input for Telecom DC PSU	Identifies unpowered unit as a Telecom DC type, See Table 12-21
		0100	Low line, 60Hz, AC Detected	See Table 12-20
		0101	No Power Input for extended wide-range AC	Identifies unpowered unit as an extended wide-range AC type, See Table 12-21
		0110	High line, 60Hz, AC Detected	See Table 12-20
		0111	Input is Telecom DC	See Table 12-20
		1000	No Power Input for wide-range AC/low-line DC mixed-mode PSU	Identifies unpowered unit as a mixed type, See Table 12-21
		1001	No Power Input for high line only AC PSU	Identifies unpowered unit as a high line only AC, See Table 12-21
		1010	High line DC, DC Detected	See Table 12-20
		1011	No Power Input for extended wide-range AC/wide-range DC mixed-mode PSU Or No Power Input for extended high AC/high line DC mixed-mode PSU	Identifies unpowered unit as a mixed type, See Table 12-21
		1100	Low line DC, DC Detected	See Table 12-20
		1101	Extended high-line 50Hz, AC Detected	See Table 12-20
		1110	Extended high-line 60Hz, AC Detected	See Table 12-20
		1111	Reserved	

Notes:

1. The PSU initialized values for 'No Power Input for wide range AC', 'No Power Input for extended wide range AC', 'No Power Input for Telecom DC' and 'No Power Input for wide-range AC/low-line DC mixed-mode PSU' and 'No Power Input for extended wide-range AC/wide-range DC mixed-mode PSU' eases the board management controller's determination of type and edibility for system incorporation prior to the unit's line cord insertion.
2. Change_Line_Status is a command from the system to the power supply to change its line status and power ratings based upon a recent change in input line voltage. An example

would be if the power supply originally came up as a low line power supply operating on a 115Vac input line that eventually changed to 230Vac. Since the power capabilities at high line would allow the power supply to deliver more power to the system the system would write to bit-7 to inform the power supply to proceed to change its line status and all associated power settings to the new higher power ratings. The dual wattage power supply can only update its power capabilities using this command when the power supply is in an OFF condition: PWOK is de-asserted, and the power supply has set bit-4 of the STATUS_MFR_SPECIFIC register. Once the line status and power capabilities have been changed, the power supply will reset bit-4 of the STATUS_MFR_SPEC register followed by resetting the Change_Line_Status. For wide range PSU and Input_OCW bit is masked, it can switch immediately once system writes 1 to Change_Line_Status without waiting for OFF condition.

3. Only bit 7 is a read/write bit while bits 0-6 are read only bits. Therefore, any value written to bits 0-6 will be ignored by the power supply.
4. If PSU started up into high line 230Vac, then AC changed to 120Vac, PSU should raise up bit 4 in STATUS_MFR_SPECIFIC and bit 4 in STATUS_WORD.
5. PSU_MISMATCH is a command from the system to mismatch a power supply. The system (BMC) writes 40h (set the PSU_MISMATCH bit) to the MFR_LINE_STATUS register (E1h) and disables PSON # to turn the power supply off. The power supply will set the LED behavior for the mismatch state. As long as the secondary bias voltage within the power supply is present the status bit will remain set. There are 2-conditions where the mismatch bit can be reset as follows:
    a. The internal secondary bias voltage is removed. Upon reassertion of the bias voltage the mismatch bit will reset to its default state (bit 6 is cleared).
    b. The system can also clear the mismatch bit at any time. An example would be if the system requires that all power supplies in the system needs to be the same wattage. A dual rated power supply has a lower power rating at low line (120Vac) than at high line (240Vac). Therefore, the system may mismatch the low line power supply and turn it off. When the correct input is applied (high line), and the power capability is now matched, the system can clear the mismatch bit. The LED behavior will then change to the operational setting based upon the new state of the power supply.

Table 12-20 Power input line type definition

Power Input Type		Nominal Voltage	PSU Operational Voltage range	Representative Voltave Range in MFR_LINE_STATUS
DC input	Telecom DC	-48VDC	Defined in the design specification	36VDC to 72VDC
	Low Line DC	240VDC		192-328VDC
	High Line DC	380VDC		>328VDC
AC input	Low Line AC	100-120VAC		90VAC High line turn ON
	High Line AC	200-240VAC		High Line Turn ON 264VAC
	Extended High Line AC	277VAC		Refer to design specification

Table 12-21 PSU AC/DC Supporting type definition

PSU AC/DC Supporting Type	Nominal Voltage	PSU Operational Voltage Range
Wide Range AC	100-240Vac	Defined in the design specification
Extended Wide Range AC	100-277Vac	
Wide Range DC	240-380Vdc	

12.1.45.4 Flow Charts

Figure 12-15 MFR_LINE_STATUS Main page flow diagram

Figure 12-16 MFR_LINE_STATUS Initial line flow diagram

Figure 12-17a MFR_LINE_STATUS Preset flow diagram (AC Low Line)

Figure 12-17b MFR_LINE_STATUS Preset flow diagram (AC High Line)

Figure 12-17c MFR_LINE_STATUS Preset flow diagram (AC Ext. High Line)

Figure 12-17d MFR_LINE_STATUS Preset flow diagram (DC)

Figure 12-18 MFR_LINE_STATUS Notify task flow diagram

Figure 12-19 MFR_LINE_STATUS Telecom flow diagram

12.1.46 MFR_SYSTEM_LED_CNTL (E2h)

The system shall be able to override the blinking pattern of the power supply's LED by writing to the MFR_SYSTEM_LED_CNTL (E2h) command with the selected pattern value. If the system wants to return the control of the LED to the power supply, then it needs to write the value 0x0007.

Table 12-22 MFR_SYSTEM_LED_CNTL (E2h) command bitfield definition

Parameter	Bitfield	Options	Comments
Style	[2:0]	0 = LED OFF 1 = LED ON 2 = Blinking 3 = Blink N times then OFF 4 = Blink N times then ON 5 = PWM 6 = Reserved 7 = PSU controlled LED	
Color	[5:3]	0 = OFF 1 = GREEN 2 = AMBER 3 to 7 = Reserved	
Flashing Times	[8:6]	0 = Zero time 1 = One time 2 = Two times 3 = Three times 4 = Four times 5 = Five times 6 = Six times 7 = Seven times	
Frequency	[11-9]	0 = 0.5 Hz 1 = 1 Hz 2 = 2 Hz 3 = 3 Hz 4 = 4 Hz 5 = 5 Hz 6 = 6 Hz 7 = 7 Hz	
PWM T_{High}	[13:12]	0 = 250 ms 1 = 1000 ms 2 = 2000 ms 3 = 3000 ms	Time in high state
PWM T_{Low}	[15:14]	0 = 250 ms 1 = 1000 ms 2 = 2000 ms 3 = 3000 ms	Time in low state

Notes:

1. The default value at boot time for MFR_SYSTEM_LED_CNTL shall be 0x0007, meaning power supply-controlled LED.
2. *PWM Thigh* and *PWM TLow* are only used when PWM is selected in Style.

12.1.47 MFR_READ_CONFIG_FILE_SIZE (D1h)

This command shall be used to retrieve the size of configuration file currently stored in the M-CRPS. The command is a Read Block type with a 3-byte length plus PEC which represents a 24-bit number, this means the maximum size of the configuration file is 16MiB.

Table 12-23 MFR_READ_CONFIG_FILE_SIZE byte ordering

Data byte	bits	Definition
0	[0:7]	Least significant byte
1	[8:15]	
2	[16:23]	Most significant byte

12.1.48 MFR_READ_CONFIG_BLOCK_SIZE (D2h)

This command shall be used to retrieve the block size to be used to read the configuration file from the M-CRPS. The command is a Read Word type plus PEC.

12.1.49 MFR_READ_CONFIG_FILE (D3h)

This command will set the read address pointer and retrieve a block of data from the configuration file stored in the M-CRPS, the type of command shall be Write Block-Read Block process call plus PEC, where Write Block with block length = 3 represents the 24-bit read pointer (starting at 0x000000), following SMBus format for the payload:

Byte 1 = Read pointer [7:0] Least significant byte
Byte 2 = Read pointer [15:8]
Byte 3 = Read pointer [23:16] Most significant byte

Read Block will read a block of *MFR_READ_CONFIG_BLOCK_SIZE* length each time, the Host is the responsible to increment the read pointer in every transaction, if the Host tries to read more than *MFR_READ_CONFIG_BLOCK_SIZE* the M-CRPS shall respond accordingly to PMBus specification.

Figure 12-20 MFR_READ_CONFIG_FILE command byte ordering

If the read pointer is outside of the configuration file area, then the M-CRPS shall respond as follows:

- Send all ones (FFh) as long as the host keeps clocking and acknowledging,
- Set the CML bit in the STATUS_BYTE.
- Set bit [1] ("Other" fault) bit in the STATUS_CML register.

12.1.50 MFR_EFFICIENCY_DATA (B3h)

The first byte of data contains input type information as shown in the below table. The second and third byte of data represent sleep power consumption in Linear-16 format with Unit = watt, Exponent = -4 (Resolution = 0.0625watt). And then the rest will contain 11 data points for the efficiency of the power supply for efficiencies (5%, 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, 100%). Each efficiency returns 2 bytes per data point. LSB, MSB. The two-byte efficiency data are in Linear-16 format with Unit = %, Exponent = -4 (Resolution = 0.0625%).

There will be total 25-byte data. It uses block read protocol. Data bytes 3 to 24 are input level dependent.

The Efficiency numbers populated are average value from batch of factory build units and are all hard coded in the firmware.

Notes:

1. Efficiency measurement for this command shall be done including the fan power.

Table 12-24 Efficiency data definition

Data byte	bits	Name	Value	Description	Notes
0	[6:7]	Reserved			This byte is for input type
	[4:5]	AC Voltage source	11b	Extended high line AC	
			10b	High line AC	
			01b	Low line AC	
			00b	Not an AC input	
	[2:3]	Reserved			
	[0:1]	DC Voltage source	11b	High line DC	
			10b	Low line DC	
			01b	Telecom DC	
			00b	Not a DC input	
1	[0:15]	Sleep power	Vendor's data	Input power during sleep	Linear-16 format with Unit = watt, Exponent = -4 (Resolution = 0.0625 watt)
2					
3	[0:15]	Efficiency at 5% load	Vendor's data	Efficiency data at 5% load	Linear-16 format with Unit = %, Exponent = -4 (Resolution = 0.0625%)
4					
5 to 24	[0:15] of every two-byte	Efficiency from 10% to 100% (10% interval)	Vendor's data	Efficiency data at 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, 100% load	Linear-16 format with Unit = %, Exponent = -4 (Resolution = 0.0625%)

The power supply shall change the efficiency data in bytes 3 to 24 based on the input voltage, for example if the power supply is operating at low line the power supply shall provide the efficiency measurements of low line, in the other hand if the power supply is operating at high line then the power supply shall provide the efficiency measurements for high line.

12.1.51 MFR_PEAK_CURRENT_RECORD (E9h)

The command is used for recording two peak current values with one that can be cleared by system and one that is never cleared such that it always provides peak current ever observed by PSU (Cleared in factory). It uses the block read/write protocol. Writing any values (except 0xFFFFFFFF) to this command has no effects.

Value Clearance:

- Writing 0xFFFFFFFF to this command results in resetting peak current value (byte 0 and byte 1).
- While PS_ON changes from de-asserted to asserted state, peak current value (byte 0 and byte 1) .is reset to 0x0000.
- Only MFR_CLEAR_BLACKBOX (E0h) can reset historical peak current (byte 2 and byte 3).
- There is no average window for both values. The values are from current sampling.

Table 12-25 MFR_PEAK_CURRENT_RECORD byte definition

Data byte	bits	Definition	Notes
0	[0:15]	Peak current (Linear-16, Units = Amps, Exponent = -2)	• The resolution is 250mA • Writing 0xFFFFFFFF to this command results in resetting peak current value (byte 0 and byte 1) • Stored in dynamic memory
1			
2	[0:15]	Historical peak current (Linear-16, Unit = Amps, Exponent = -2)	• The resolution is 250mA • Only MFR_CLEAR_BLACKBOX can reset historical peak current (byte 2 and byte 3) • Stored in non-volatile memory
3			

12.1.52 MFR_COMPONENT_ID (EBh)

This number will be assigned by the user/customer and shall correspond to a unique vendor power supply. The length shall be 4 bytes.

12.1.53 MFR_TOT_POUT_MAX (ECh)

This is a read of the unit's maximum output power delivery capacity with respect to input line level. Example: A 1050W output power advertised when input voltage is lower than 140Vac, else 1100W.

Power on default value should be the same as MFR_POUT_MAX (A7h).

12.1.54 MFR_VOUT_MARGINING (EDh)

This command uses the Read/Write Word protocol. The bit 1 of byte 0 is "Margin Function" writing 1 is to enable margin function and writing 0 is to disable the function. Margin Function shall reset to default if cycling of the PSON# signal from asserted (low) to de-asserted (high) and then back to asserted.

Table 12-26 MFR_VOUT_MARGINING command bit field definition

Data byte	bits	Name	Value	Definition	Notes
0	[2:7]	Reserved	0	Reserved	Default value is 0
	1	Margining function	0	Disable function	Default value is 0
			1	Enable function	
	0	Reserved	0	Reserved	Default value is 0
1	[0:7]	Reserved	0	Reserved	Default value is 0

Figure 12-21 Write MFR_VOUT_MARGINING protocol format

Figure 12-22 Read MFR_VOUT_MARGINING protocol format

Notes:

1. This command must be unlocked before use by setting the correct bit in the configuration file refer to *Table 12-75 Miscellaneous configuration block* for details.

12.1.55 MFR_OCWPL1_SETTING (EEh)

This command is used for setting the threshold value and the average window time length of OCW_{PL1}. It uses the Block Read / Block Write protocol.

If values that are programmed and not within the range that is defined in Design Specification, the command will be accepted but values will be ignored and STATUS_CML[6] shall be set to indicate invalid/unsupported data.

Table 12-27 MFR_OCWPL1_SETTING command bit field definition

Data byte	bits	Definition	Notes
0	[0:1]	Reserved	
	[2]	Assertion threshold value setting: 0b = Not selected 1b = Selected	
	[3]	Average window length setting 0b = Not selected 1b selected	
	[4:7]	reserved	
1	[0:15]	Assertion threshold value (Linear-16, Unit = Amps, Exponent = -2)	• Resolution is 250mA • If byte0[2] is Not selected, set value will be ignored
2			
3	[0:15]	Average window length (Linear-11, Unit = msec, Exponent = 6)	• Default setting is 250ms • If byte0[3] is Not selected, set value will be ignored
4			

Notes:

1. This command must be unlocked before use by setting the correct bit in the configuration file refer to *Table 12-75 Miscellaneous configuration block* for details.

12.1.56 MFR_FPC_MAIN_MIN_OFF_TIME

This command is used to establish or read the Main output's minimum OFF time including the discharging time of the rail. The initial value when the M-CRPS is energized shall be the one in *FPCMainMinOFFTime* in the configuration file on *Table 12-75 Miscellaneous configuration block*. The valid range of values are listed below.

Table 12-28 MFR_FPC_MAIN_MIN_OFF_TIME command valid range

Value	Description
0000h	Reserved – If received, the command will be ignored.
0001h	*TMain_MinOFF* 1 second delay after Main rail is below threshold at the M-CRPS.
…	…
0008h	*TMain_MinOFF* 8 seconds delay after Main rail is below threshold at the M-CRPS.
0384h (900 decimal)	*TMain_MinOFF* 900 seconds delay after Main rail is below threshold at the M-CRPS. This is the maximum supported value.
0385h – FFFFh	Reserved – If received, the command will be ignored.

12.1.57 MFR_FPC_12VSB_MIN_OFF_TIME

This command is used to establish or read the Standby output's minimum OFF time including the discharging time of the rail. The initial value when the M-CRPS is energized shall be the one in

FPCVsbMinOFFTime in the configuration file on *Table 12-75 Miscellaneous configuration block*. The valid range of values are listed below.

Table 12-29 MFR_FPC_12VSB_MIN_OFF_TIME command valid range

Value	Description
0000h	Reserved – If received, the command will be ignored.
0001h	*T12Vsb_MinOFF* 1 second delay after Main rail is below threshold at the M-CRPS.
…	…
0008h	*T12Vsb_MinOFF* 8 seconds delay after Main rail is below threshold at the M-CRPS.
0384h (900 decimal)	*T12Vsb_MinOFF* 900 seconds delay after Main rail is below threshold at the M-CRPS. This is the maximum supported value.
0385h – FFFFh	Reserved – If received, the command will be ignored.

12.1.58 Status Simulation Commands

This function is to simulate different status for system validation. The behavior of fault and warn status shall simulate the real behavior as same as possible. To activate the feature the bit *EnableStatusSimulationCmd* in the *Table 12-75 Miscellaneous configuration block* of the configuration file shall be set to 1, then the agent shall write 01h using the command MFR_EN_STATUS_SIMULATION_CMD (E4h). The flowchart to set the status is shown in figure below.

Figure 12-23 Enable status simulation commands process flow

Figure 12-24 PAGE_PLUS_WRITE command structure for status simulation

Table 12-30 PAGE_PLUS_WRITE (05h) command definition for status simulation

Data byte	Name	Value	Description
0	PAGE	00h	PAGE 0: The behavior is same as normal mode
		01h	PAGE 1: The behavior is same as normal mode
		F0h	Debug Page F0h: • Writing Data byte can directly change the status of STATUS_CMD for both page 0 and page 1 if PAGE is set to F0h. • The status bit shall be cleared per the *Section 12.1.21 Resetting Status Bits.* • SMBAlert signal will assert or not assert based on the SMBAlert mask for the status register (same as normal response to status bit assertion). • SMBAlert signal will de-assert upon the clearing of the error status condition as noted above.
		F1h	Debug Page F1h: • Writing Data byte can directly change the status of STATUS_CMD for both page 0 and page 1 if PAGE is set to F1h. • The status bit shall be cleared per the *Section 12.1.21 Resetting Status Bits.* • SMBAlert signal will assert or not assert based on the SMBAlert mask for the status register (same as normal response to status bit assertion). • SMBAlert signal will remain asserted until the fault is cleared via the setting of the status data byte to 00h as noted above. • Except VIN_UV_FAULT, any faults are generated by page 0F1h shall be recorded in black box.
1	STATUS_CMD	7Ah~7Fh, and 81h	Support STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, STATUS_FAN, and STATUS_OTHER
2	Data	00h ~FFh	• If PAGE is 00h or 01h, the data byte is used to clear fault. • If PAGE is F0h or F1h, the data byte is used to set status.

Table 12-31 STATUS_VOUT Register Behaviors for Page F0h/F1h Writes

Bits	Name	Description	Latching	STATUS_WORD bit to set		Power OFF	
				High byte	Low byte	PAGE F0h	PAGE F1h
7	Vout OV Fault	VOUT_OV_FAULT (Output Overvoltage Fault)	Yes	7	5	No	Yes
6	Not implemented		N/A	N/A	N/A	No	No
5	Not implemented		N/A	N/A	N/A	No	No
4	Vout UV Fault	VOUT_UV_FAULT (Output Undervoltage Fault)	Yes	7	N/A	No	Yes
3	Not implemented		N/A	N/A	N/A	No	No
2	TON MAX Fault	Set when supply has not been able to turn on and assert PWOK within 4 seconds of detecting PSON# assertion when input power available	Yes	7	N/A	No	Yes
1	Not implemented		N/A	N/A	N/A	No	No
0	Not implemented		N/A	N/A	N/A	No	No

Table 12-32 STATUS_IOUT Register Behaviors for Page F0h/F1h Writes

Bits	Name	Description	Latching	STATUS_WORD bit to set		Power OFF	
				High byte	Low byte	PAGE F0h	PAGE F1h
7	Iout OC Fault	IOUT_OC_FAULT (Output Overcurrent Fault) Short circuit should also set this bit	Yes	6	4	No	Yes
6	Not implemented		N/A	N/A	N/A	N/A	N/A
5	Iout OC Warning	PSU primary output overcurrent warning	Yes	6	N/A	No	No
4	Not implemented		N/A	N/A	N/A	N/A	N/A
3	Not implemented		N/A	N/A	N/A	N/A	N/A
2	Not implemented		N/A	N/A	N/A	N/A	N/A
1	Not implemented		N/A	N/A	N/A	N/A	N/A
0	Not implemented		N/A	N/A	N/A	N/A	N/A

Table 12-33 STATUS_INPUT Register Behaviors for Page F0h/F1h Writes

Bits	Name	Description	Latching	STATUS_WORD	Power OFF

				bit to set			
				High byte	Low byte	PAGE F0h	PAGE F1h
7	Not implemented		N/A	N/A	N/A	N/A	N/A
6	Not implemented		N/A	N/A	N/A	N/A	N/A
5	VIN_UV_WARNING	Line input undervoltage warning	Yes	5	N/A	No	No
4	VIN_UV_FAULT	Line input undervoltage fault	Yes	5	3	No	Yes
3	Unit Off for Low Input Voltage	This indicates the supply is off or was not able to turn on due to Low input voltage	Yes	5	N/A	No	Yes
2	Not implemented		N/A	N/A	N/A	N/A	N/A
1	IIN_OC_WARNING	Input Overcurrent Warning Occurred	Yes	5	N/A	No	No
0	PIN_OP_WARNING	Input Overpower Warning Occurred	Yes	5	N/A	No	No

Table 12-34 STATUS_TEMPERATURE Register Behaviors for Page F0h/F1h Writes

Bits	Name	Description	Latching	STATUS_WORD bit to set		Power OFF	
				High byte	Low byte	PAGE F0h	PAGE F1h
7	OT_FAULT	Overtemperature Fault Occurred	Yes	N/A	2	No	Yes
6	OT_WARNING	Overtemperature Warning Occurred	Yes	N/A	2	No	No
5	Not implemented		N/A	N/A	N/A	N/A	N/A
4	Not implemented		N/A	N/A	N/A	N/A	N/A
3	Not implemented		N/A	N/A	N/A	N/A	N/A
2	Not implemented		N/A	N/A	N/A	N/A	N/A
1	Not implemented		N/A	N/A	N/A	N/A	N/A
0	Not implemented		N/A	N/A	N/A	N/A	N/A

Table 12-35 STATUS_CML Register Behaviors for Page F0h/F1h Writes

Bits	Name	Description	Latching	STATUS_WORD bit to set		Power OFF	
				High byte	Low byte	PAGE F0h	PAGE F1h
7	Invalid/Unsupported Command	Slave received an invalid or unsupported command.	Yes	N/A	1	No	No
6	Invalid/Unsupported Data	Data Format Error occurred.	Yes	N/A	1	No	No
5	Packet Error Check Failed	Slave received an error PEC code. Note: This bit must be updated within 100usec from time PEC error is detected.	Yes	N/A	1	No	No
4	Not implemented		N/A	N/A	N/A	N/A	N/A
3	Not implemented		N/A	N/A	N/A	N/A	N/A
2	Not implemented		N/A	N/A	N/A	N/A	N/A
1	Other Communication Fault	Failed to communication between Primary and secondary MCUs	Yes	N/A	1	N/A	Yes
0	Not implemented		N/A	N/A	N/A	N/A	N/A

Table 12-36 STATUS_OTHER Register Behaviors for Page F0h/F1h Writes

Bits	Name	Description	Latching	STATUS_WORD bit to set		Power OFF	
				High byte	Low byte	PAGE F0h	PAGE F1h
7:1	Not Implemented	Reserved	N/A	N/A	N/A	N/A	N/A
0	Cold Redundancy Feature Event	A Primary Protection Trigger External Cold Redundancy feature event has occurred.	Yes	1	N/A	No	No

Table 12-37 STATUS_FANS_1_2 Register Behaviors for Page F0h/F1h Writes

Bits	Name	Description	Latching	STATUS_WORD bit to set		Power OFF	
				High byte	Low byte	PAGE F0h	PAGE F1h
7	Fan 1 Fault	Fan 1 fault occurred.	Yes	2	N/A	No	Yes
6	Fan 2 Fault	Fan 2 fault occurred.	N/A	N/A	N/A	No	No

5	Fan 1 Warning	Fan 1 warning occurred.	Yes	2	N/A	No	No
4	Fan 2 Warning	Fan 2 warning occurred.	N/A	N/A	N/A	No	No
3	Fan1 Speed Override	Fan1 Speed Override condition occurred.	Yes	N/A	N/A	No	No
2	Fan2 Speed Override	Fan2 Speed Override condition occurred.	N/A	N/A	N/A	No	No
1	Not implemented		N/A	N/A	N/A	No	No
0	Not implemented		N/A	N/A	N/A	No	No

12.1.59 Summary of PMBus commands

Table 12-38 Summary of PMBus commands

Code	Pages	Command	SMBus Transaction Type Status bit mapping
00h		PAGE	Read Byte / Write Byte w/PEC
01h		OPERATION	Read Byte / Write Byte w/PEC
02h		ON_OFF_CONFIG	Read Byte / Write Byte w/PEC
03h		CLEAR_FAULTS	Send Byte w/PEC
05h	NA	PAGE_PLUS_WRITE (used with STATUS_WORD, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE)	Block Write w/PEC Used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT
06h	NA	PAGE_PLUS_READ (used with STATUS_WORD, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE)	Write Block Read Block Process Call w/PEC Used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, STATUS_WORD
10h		WRITE_PROTECT	Read Byte / Write Byte w/PEC
11h		Reserved	
12h		Reserved	
15h		Reserved	
16h		Reserved	
19h	NA	CAPABILITY	Read Byte w/PEC
1Ah	NA	QUERY (used with any command)	Block Write Block Read Process Call w/ PEC
1Bh	NA	SMBALERT_MASK (used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT)	Reading: Write Block Read Block Process Call w/PEC Writing: Write Word
20h		Reserved	
21h		Reserved	
22h		Reserved	
24h		Reserved	
25h		Reserved	
26h		Reserved	
27h		Reserved	
28h		Reserved	
29h		Reserved	
2Ah		Reserved	
30h	NA	COEFFICIENT (used with READ_EIN)	Block Write Block Read Process Call w/PEC
33h		FREQUENCY_SWITCH	Read word w/PEC
35h		VIN_ON	Read word w/PEC
36h		VIN_OFF	Read word w/PEC

38h		Reserved	
39h		Reserved	
3Ah	NA	FAN_CONFIG_1_2	Read byte w/PEC
3Bh	NA	FAN_COMMAND_1	Read word / Write word w/PEC
40h		VOUT_OV_FAULT_LIMIT	Read word w/PEC
41h		VOUT_OV_FAULT_RESPONSE	Read byte w/PEC
42h		VOUT_OV_WARN_LIMIT	Read word w/PEC
43h		VOUT_UV_WARN_LIMIT	Read word w/PEC
44h		VOUT_UV_FAULT_LIMIT	Read word w/PEC
45h		VOUT_UV_FAULT_RESPONSE	Read byte w/PEC
46h		IOUT_OC_FAULT_LIMIT	Read word w/PEC – See Note 1
47h		IOUT_OC_FAULT_RESPONSE	Read byte w/PEC
4Ah		IOUT_OC_WARN_LIMIT	Write Word / Read Word w/PEC – See Note 1
4Fh		OT_FAULT_LIMIT	Read word w/PEC
50h		OT_FAULT_RESPONSE	Read byte w/PEC
51h		OT_WARN_LIMIT (used to support testing CLST)	Read/Write word w/PEC
55h		VIN_OV_FAULT_LIMIT	Read word w/PEC
56h		VIN_OV_FAULT_RESPONSE	Read byte w/PEC
57h		VIN_OV_WARN_LIMIT	Read word w/PEC
58h		VIN_UV_WARN_LIMIT	Read word w/PEC – See Note 1
59h		VIN_UV_FAULT_LIMIT	Read word w/PEC – See Note 1
5Ah		VIN_UV_FAULT_RESPONSE	Read byte w/PEC – See Note 1
…			
5Dh		IIN_OC_WARN_LIMIT	Read/Write word w/PEC – See Note 1
…			
6Bh		PIN_OP_WARN_LIMIT	Read word w/PEC
…			
78h		STATUS_BYTE	
79h	00h, 01h	STATUS_WORD	Read Word w/PEC
(Low) 6		OFF	PS off
4		IOUT_OC	Indeterminate (Use STATUS_IOUT)
2		TEMPERATURE	Indeterminate (Use STATUS_TEMPERATURE)
3		VIN_UV	Indeterminate (Use STATUS_INPUT)
1		CML	
(High) 7		VOUT	Failure
6		IOUT/POUT	Indeterminate (Use STATUS_IOUT)
5		INPUT	Indeterminate (Use STATUS_INPUT)
4		MFR_SPECIFIC (Incompatible Power Supply)	
3		POWER_GOOD#	
2		FANS	Indeterminate (Use STATUS_FANS)
7Ah	NA	STATUS_VOUT	Read Byte w/PEC
7		VOUT_OV_FAULT	Failure
6		VOUT_OV_WARNING	
5		VOUT_UV_WARNING	

4		VOUT_UV_FAULT	Predictive failure
2		TON_MAX_FAULT	
7Bh	00h, 01h	STATUS_IOUT	Read Byte w/PEC
7		Iout OC fault	Failure
5		Iout OC warning	Predictive failure
1		Pout OP fault	Failure
0		Pout OP warning	Predictive failure
7Ch	00h, 01h	STATUS_INPUT	Read Byte w/PEC
7		VIN_OV_FAULT	
6		VIN_OV_WARNING	
5		Vin UV warning	Predictive failure
4		Vin UV fault	AC Loss
3		Unit off for insufficient input	AC Loss
1		Iin over current warning	Predictive failure
0		Pin over power warning	Predictive failure
7Dh	00h, 01h	STATUS_TEMPERATURE	Read Byte w/PEC
7		OT fault	Fault
6		OT warning	Predictive fault
7Eh	00h, 01h	STATUS_CML	Read Byte w/PEC
7		Invalid Or Unsupported Command Received	
6		Invalid Or Unsupported Data Received	
5		Packet Error Check Failed	
4		Memory Fault Detected	
3		Processor Fault Detected	
2		Reserved	
1		A communication fault other than the ones listed in this table has occurred	
0		Other Memory Or Logic Fault has occurred	
7Fh	00h, 01h	STATUS_OTHER	Read Byte w/PEC
80h	00h, 01h	STATUS_MFR_SPECIFIC	Read Byte w/PEC
4		Power supply line status change	Asserted when the power supply detects a line status condition change
2		High Line input, power derated	This bit is used for power supplies that have two power levels for voltages greater that 200Vac (nominal). Asserted when the power supply's input voltage falls below the voltage required to achieve the higher power level. Refer to the design specification for voltage thresholds.
81h	00h	STATUS_FANS_1_2	Read Byte w/PEC
7		Fan 1 fault	Failure
6		Fan 2 fault	Failure
5		Fan 1 warning	Predictive failure
4		Fan 2 warning	Predictive failure
...			
86h	NA	READ_EIN	Block Read w/ PEC

87h	NA	READ_EOUT	Block Read w/ PEC
88h		READ_VIN	Read word w/PEC
89h		READ_IIN	Read word w/PEC
8Ah		READ_VCAP	Read word w/PEC
8Bh		READ_VOUT	Read word w/PEC
8Ch	NA	READ_IOUT	Read Word w/PEC
8Dh	NA	READ_TEMPERATURE_1 (Ambient)	Read Word w/PEC
8Eh	NA	READ_TEMPERATURE_2 (Hot Spot)	Read Word w/PEC
8Fh		READ_TEMPERATURE_3 (Exhaust)	Read Word w/PEC
90h	NA	READ_FAN_SPEED_1	Read Word w/PEC
91h		READ_FAN_SPEED_2	Read Word w/PEC
94h		READ_DUTTY_CYCLE	Read Word w/PEC
96h		READ_POUT	Read Word w/PEC
97h	NA	READ_PIN	Read Word w/PEC
98h	NA	PMBUS_REVISION	Read Byte w/PEC
99h		MFR_ID	Block read w/PEC – Length = 12 bytes
9Ah	NA	MFR_MODEL	Block Read w/PEC – Length = 16 bytes including \0 ending character, if string is shorter fill with spaces
9Bh	NA	MFR_REVISION	Block Read w/PEC – Length = 16 bytes including \0 ending character, if string is shorter fill with spaces
9Ch		MFR_LOCATION	Block Read w/PEC – Length = 16 bytes including \0 ending character, if string is shorter fill with spaces
9Dh		MFR_DATE	Block Read w/PEC – Length = 6 bytes
9Eh		MFR_SERIAL	Block Read w/PEC – Length = 14 bytes
9Fh	NA	APP_PROFILE_SUPPORT	Read Byte w/PEC
A0h		MFR_VIN_MIN	Read word w/PEC
A1h		MFR_VIN_MAX	Read word w/PEC
A2h		MFR_IIN_MAX	Read word w/PEC
A3h		MFR_PIN_MAX	Read word w/PEC
A4h		MFR_VOUT_MIN	Read word w/PEC
A5h		MFR_VOUT_MAX	Read word w/PEC
A6h	NA	MFR_IOUT_MAX	Read Word w/PEC
A7h	NA	MFR_POUT_MAX	Read Word w/PEC
A8h		MFR_TAMBIENT_MAX	Read word w/PEC
A9h		MFR_TAMBIENT_MIN	Read word w/PEC
ADh		IC_DEVICE_ID	Block read w/PEC
AEh		IC_DEVICE_REV	Block read w/PEC
B0h		USER_DATA_00	Block read / Block write w/PEC
B1h		USER_DATA_01	Block read / Block write w/PEC
B2h		USER_DATA_02	Block read / Block write w/PEC
B3h		MFR_EFFICIENCY_DATA	Read Block w/PEC
B4h		USER_DATA_04	Block read / Block write w/PEC
B8h		USER_DATA_08	Block read / Block write w/PEC
C0h	NA	MFR_MAX_TEMP_1 (Ambient)	Read Word w/PEC
C1h	NA	MFR_MAX_TEMP_2 (hot Spot)	Read Word w/PEC
C2h		MFR_MAX_TEMP_3	Read Word w/PEC

…			
D0h	NA	MFR_COLD_REDUNDANCY_CONFIG	Read/Write Byte w/PEC
D1h	NA	MFR_READ_CONFIG_FILE_SIZE	Read Block w/PEC
D2h	NA	MFR_READ_CONFIG_BLOCK_SIZE	Read Word w/PEC
D3h	NA	MFR_READ_CONFIG_FILE	Write Block-Read Block process call w/PEC
D4h	NA	MFR_HW_COMPATIBILITY	Read Word w/PEC
D5h	NA	MFR_FWUPLOAD_CAPABILITY	Read Byte w/PEC
D6h	NA	MFR_FWUPLOAD_MODE	Read/Write Byte w/PEC
D7h	NA	MFR_FWUPLOAD	Block Write w/ PEC (size = block size from image header)
D8h	NA	MFR_FWUPLOAD_STATUS	Read Word / Write Word w/PEC
D9h	NA	MFR_FW_REVISION	Block Read w/PEC (7 bytes)
DAh	NA	MFR_SPDM	Block Write – Block Read Process Call w/ PEC
DBh	NA	MFR_FRU_PROTECTION	Read/Write byte w/PEC
DCh	NA	MFR_BLACKBOX	Block Read w/ PEC (230 byes)
DDh	NA	MFR_REAL_TIME_BLACK_BOX	Block Write/Read w/ PEC (4 bytes)
DEh	NA	MFR_SYSTEM_BLACK_BOX	Block Write/Read w/ PEC (40 bytes)
DFh		MFR_BLACK_BOX_CONFIG	Read/Write Byte with PEC
E0h		MFR_CLEAR_BLACK_BOX	Write Byte w/PEC
E1h		MFR_LINE_STATUS	Read/Write Byte w/PEC
E2h		MFR_SYSTEM_LED_CNTL	Read/Write Word w/PEC
E3h		MFR_FWUPLOAD_BLOCK_SIZE	Read Word w/PEC
E4h		MFR_EN_STATUS_SIMULATION_CMD	Read/Write Byte w/PEC
E5h		MFR_SPECIFIC_21	Reserved
E6h		MFR_SPECIFIC_22	Reserved
E7h		MFR_SPECIFIC_23	Reserved
E8h		MFR_SPECIFIC_24	Reserved
E9h		MFR_PEAK_CURRENT_RECORD	Block Write/Read w/ PEC
EBh		MFR_COMPONENT_ID	Read block w/PEC
ECh		MFR_TOT_POUT_MAX	Read Word w/PEC, Total output power with respect to line status. – See Note 1
EDh		MFR_VOUT_MARGINING	Read Word / Write Word w/PEC
EEh		MFR_OCWPL1_SETTING	Block Read / Block Write w/PEC
EFh		MFR_SPECIFIC_31	Reserved
F0h	NA	MFR_PWOK_WARNING_TIME	Read/Write Word w/PEC
F1h	NA	MFR_MAX_IOUT_CAPABILITY	Block Read w/PEC (14 bytes)
F2h	NA	MFR_FPC_MAIN_MIN_OFF_TIME	Read/Write Word w/PEC
F3h	NA	MFR_FPC_12VSB_MIN_OFF_TIME	Read/Write Word w/PEC
F4h to FDh		MFR_SPECIFIC_36 to MFR_SPECIFIC_45	Reserved
FEh	NA	MFR_SPECIFIC_COMMAND EXT	Customer specific command set extension

Notes:

1. These commands will have different values based upon line status if the power supply is a dual rated power supply based upon line status.

12.1.60 Summary of PMBus Telemetry Accuracies

Table 12-39 Input Parameter Measurement Accuracy as a function of Input Current

PMBus Command	AC or DC input current			
	< 200mA	200mA – 475mA	475mA – 1A	> 1 A
READ_VIN	±1.25%	±1.25%	±1.25%	±1.25%
READ_IIN	±70mA	±70mA	±5%	±3%
READ_PIN	Defined in *Section 12.1.14 READ_PIN (97h)*			
READ_EIN	Defined in *Section 12.1.16 READ_EIN (86h)*			

Table 12-40 Output Parameter Measurement Accuracy as a function of Output Load

PMBus command	< 2.5%	2.5% ≤ Load < 5%	5% ≤ Load < 10%	10% ≤ Load < 20%	20% ≤ Load < 50%	50% ≤ Load < 100%
READ_VOUT	±2%	±2%	±2%	±2%	±1%	±1%
READ_IOUT	Defined in *Section 12.1.15 READ_IOUT (8Ch)*					
READ_POUT	N/A	±10%	±7%	±5%	±2%	±2%
READ_EOUT	Defined in *Section 12.1.17 READ_EOUT (87h)*					
READ_TEMPERATURE_n	Defined in *Section 3.3 Thermal Sensors*					
READ_FAN_SPEED_n	±250 RPM					

12.2 Thermal Closed Loop System Throttling (Thermal CLST)

The power supply shall assert the SMBAlert# signal whenever any component in the power supply selected by the configuration file reaches a temperature warning threshold. Upon reduction of the load within 2msec after the SMBlert# signal is asserted if the load is reduced to less than the power supply rating; the power supply shall continue to operate and not shutdown.

Figure 12-25 Thermal CLST timing requirements

12.3 Smart Ride-Through (SmaRT)

The power supply shall assert the SMBAlert# signal in less than the specified time in table below after AC/DC input voltage is lost to 0VAC/0VDC to throttle the system/load and allow longer hold-up time.

Table 12-41 SMBAlert# input lost delay time

Power supply input type	SMBAlert# delay
High voltage AC/DC (240VAC/240VDC or 277VAC/380VDC)	>500us and <2ms
Low voltage +54VDC (Rack power)	< 100us

Low voltage -48VDC (Telecom)	< 100us

Note: The SMBAlert# assertion due to an input lost condition can be enabled/disabled in the configuration file.

12.4 Cold Redundancy

This is a common specification defining Cold Redundancy requirements used in redundant power supplies. It covers both power supply and system requirements supporting redundant configurations of 1+1, 2+2, and 3+1. Cold Redundancy uses the PMBus manufacturer specific command area to define SMBus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring.

When configured as Cold Redundant, the power supply shall have a maximum input power as specified in table below.

Table 12-42 Maximum input power when configured as Cold Redundant mode

4 Watts

Note: Input power shall be measured at the lowest nominal input voltage.

12.4.1 Overview

Below is a block diagram showing the Cold Redundancy architecture. When the power subsystem is in Cold Redundant mode; only the needed power supply to support the best power delivery efficiency are ON. Any additional power supplies, including the redundant power supply, are in Cold Standby state.

Each power supply has an additional signal that is dedicated to supporting Cold Redundancy; CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted (pulled low) when there is a fault in any power supply OR the power supply's output voltage falls below the Vfault threshold. Asserting the CR_BUS signal causes all power supplies in the Cold Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a PMBus command.

Whenever there is no Cold Redundant active power supply on the Cold Redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined Cold Redundant role (active or Cold Standby). This guarantees that incorrect programming of the Cold Redundancy states of the power supply will never cause the power subsystem to shutdown or become overloaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in Cold Redundant Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.

Figure 12-26 Cold Redundancy 1+1 functional block diagram

Figure 12-27 Cold Redundancy 2+2 & 3+1 functional block diagram

Table 12-43 Logic matrix for Cold Standby power supplies

CR_BUS	Load Share	dc/dc_active#	Cold Standby Power Supply State(s)
High	< V_{CR_ON}	High	Cold Standby
Low	< V_{CR_ON}	Low	Active
High	> V_{CR_ON}	Low	Active
Low	> V_{CR_ON}	Low	Active

12.4.2 Cold Standby Power Supply Operating State

A power supply is put into Cold Standby whenever PSON# is asserted, CR_ON# is de-asserted, and COLD_RED_CONFIG value is set to 02h, 03h, or 04h. In the cold standby mode, the power supply must:

1. Power ON in < 100µsec when Cold_Red bus is driven LOW.
2. Turn off its output OR'ing FET
3. Keep its internal output capacitor before the output OR'ing FET charged.
4. Keep PWOK asserted.
5. Disconnect any output dummy loads to prevent discharging of the recharged output capacitor.
6. Power off any internal fans.
7. Pre-bias its voltage error amplifier to maximum duty cycle (preventing the loop compensation from slowing up the turn on process)
8. Disable its output slow start circuit.
9. Keep the PFC stage ON at lowest possible operating frequency and its output bulk capacitor charged.
10. No PMBus fault or warning conditions reported via STATUS commands.

12.4.3 Powering on Cold Standby Supplies to Maintain Best Efficiency

Power supplies in Cold Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, 3, etc.) the system defines that power supply to be in the cold standby configuration; will slightly change the load share threshold that the power supply shall power on at. The CR_BUS of any power supply may be in one of three different states; pulled low, pulled high, or tri-stated. In tri-state the CR_BUS is a high impedance to ground; only a high impedance resistor pulling the signal to ground.

Table 12-44 Example load share threshold for activating supplies

	Enable Threshold for $V_{CR_ON_EN}$	Disable Threshold for $V_{CR_ON_DIS}$	CR_BUS De-asserted / Asserted States
Standard Redundancy	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = Tri-state Fault = Low
Cold Redundant Active	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = High Fault = Low
Cold Standby 1 (02h)	3.2V (40% of max)	90% x (3.2V x 1/2) = 1.44V	OK = Tri-state Fault = Low
Cold Standby 2 (03h)	5.0V (62% of max)	90% x (5.0V x 2/3) = 3.01V	OK = Tri-state Fault = Low
Cold Standby 3 (04h)	6.7V (84% of max)	90% x (6.7V x 3/4) = 4.52V	OK = Tri-state Fault = Low

Notes:

1. Maximum load share voltage = 8.0V at 100% of rated output power.
2. These are example load share bus threshold; for any power supply model these thresholds could be customized to maintain the best efficiency curve that specific model.
3. The defined thresholds can be change using the configuration file.

12.4.4 Powering on Cold Standby Supplies During a Fault or Over Current Condition

When an active power supply asserts its CR_BUS signal (pulling it low), all parallel power supplies in cold standby mode shall power on within 100µsec.

12.4.5 Cold Redundancy SMBus Commands

The PMBus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to cold redundancy. The command shall be called COLD_REDUNDANCY_CONFIG (D0h). Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

The power supplies setup to be the cold standby power supplies; shall change to standard redundancy mode (D0h = 00h) whenever the CR_BUS is pulled low.

Table 12-45 COLD_REDUNDANCY_CONFIG (D0h) values

Value	State	Description
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply's CR_BUS signal shall be in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active [1]	Defines this power supply to be the one that is always ON in a cold redundancy configuration.
02h	Cold Standby 1 [1]	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2 [1]	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3 [1]	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.
05h	Always Standby [1]	Defines this power supply to be always in cold redundant configuration no matter what the load condition.
06h	Cold Standby 4 [1]	Defines the power supply that is 4th to turn on in a cold redundant configuration as the load increases.
07h	Cold Standby 5 [1]	Defines the power supply that is 5th to turn on in a cold redundant configuration as the load increases.
08h – FFh	Reserved	

Notes:

1. When the CR_BUS transitions from a high to a low state; each PSU programmed to be in Cold Standby state shall be put into Standard Redundancy mode (COLD_REDUNDANCY_CONFIG = 00h). For the power supplies to enter Cold Redundancy mode the system must re-program the power supplies using the COLD_REDUNDANCY_CONFIG command.

12.4.6 Cold Redundant Signals

There is an additional signal defined supporting Cold Redundancy. This is connected to a bus shared between the power supplies; the CR_BUS.

12.4.7 Cold Redundancy Bus (CR_BUS)

This is a tri-state output signal of the power supply used to communicate a fault or over current has occurred in one of the power supplies. This is used to power on all the power supplies in the system via the CR_BUS. When the signal is pulled high it allows all power supplies in cold standby mode to go into cold standby state when the load is light enough. When the signal I left open on all power supplies it forces them all cold standby power supplies ON.

Table 12-46 CR_BUS state table

Cold Redundant Config	Operating State	PSU Fault State	CR_BUS
Active	On	OK	High
Cold Standby 1,2,3…	On	OK	Tri-state
Cold Standby 1,2,3…	Cold Stby	OK	Tri-state
Always standby	Cold Stby	OK	Tri-state
Active	Off	Fault	Low
Cold Standby 1,2,3…	On	Fault	Low
Cold Standby 1,2,3…	Cold Stby	Fault	Low
Always standby	Cold Stby	Fault	Low

Figure 12-28 CR_BUS signal circuit

Table 12-47 CR_BUS signal characteristics

Parameter	Value	
Signal type	Custom	
	MIN	MAX

Logic level low (power supply ON)	0V	Vil_cr_bus
Logic level high (power supply OFF)	Vih_cr_bus	
Source current, Cold Red = high	Ioh_cr_bus	
Sink current, Cold_Red = low		Iol_cr_bus
Cold_Red fault delay		10 µs
Cold_Red turn on delay		100 µs

12.4.8 System BMC Requirements

The BMC uses the COLD_REDUNDANCY_CONFIG command to define/configure the power supply's roll in cold redundancy and to turn on/off cold redundancy.

The BMC shall schedule a rolling change for which PSU is the Active, Cold Stabdby1, Cold Standby 2, and Cold Standby 3 power supply. The allows for equal loading across power supply over their life.

Events that trigger a re-configuration of the power supplies using the COLD_REDUNDANCY_CONFIG command.

- AC power ON
- PSON power ON
- Power Supply Failure
- Power supply inserted into system

12.4.9 Power Supply Turn ON Function

Powering ON and OFF of the cold standby power supplies is only controlled by each PSU sensing the Ishare bus. Once a power supply turns on after crossing the enable threshold; it lowers its threshold to the disable threshold. The system defines the 'position' of each power supply in the Cold Redundant operation. It will do this each time the system is powered on, a power supply fails, or a power supply is added to the system.

The system is relied upon to tell each power supply where it resides in the Cold Redundancy scheme.

When load ramps up and crosses the CR threshold module wake up time must be <3ms
When load ramps down and crosses the CR threshold module go-to-sleep (sdby) time must be <5ms

Table 12-48 Cold Redundancy reaction delays

Parameter	Value
CR Threshold for wake-up	< 3ms[1]
CR Threshold for sleep-mode (Standby)	< 5ms[2]

Notes:

1. When load represented by the Ishare bus ramps up and crosses the CR wake-up threshold.
2. When the load represented by the Ishare bus ramps down and crosses the CR go-to-sleep (standby) threshold.

Figure 12-29 Power ON/OFF example of power supplies in Cold Redundant mode (4x750W PSUs)

Notes:

1. The turn ON and turn OFF thresholds for up to 15 Cold Redundant M-CRPS can be configured using the registers in *Table 12-75 Miscellaneous configuration block*.

12.5 In-System Firmware Upload

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). Any other microcontroller in the power supply also shall be able to be updated with this same process (example: primary side microcontroller).

12.5.1 FW Image Mapping

The power supply firmware image shall be made up of two parts; 1) Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

1. Boot Loader: This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power ON into the boot loader mode no matter the state of the power supply's main program. This code shall support the In-System FW update code and basic power supply functions to power ON/OFF, fan cooling, and protections (UV, OV, OC).
2. Main Program: This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

Figure 12-30 In-System FW Update Memory Mapping

The firmware image can be created by translating the .hex file to binary representation and adding the header and the signature, as a result the Firmware image will have the header at the beginning of the file, then the executable code and then the signature. The figure below shows the process flow to create the firmware image.

Figure 12-31 Firmware image creation process flow

The transfer of the Firmware image is done by using block write commands with PEC with a payload size established by the BLOCK SIZE field in the header, the data field shall contain the packet counter using the

sequence 0, 1, 2, 3… etc. This sequencing allows the MCU of the M-CRPS to be aware of where in the memory the data shall be placed. The sequence field is a 32-bit number at the beginning of the payload ordered in a LSB first as shown in the figure below.

Figure 12-32 MFR_FWUPLOAD D7h command with PEC

12.5.2 Summary of Commands & Capabilities Supported in Bootloader Mode

When the power supply is in FW Upload mode the following commands shall be supported. Additionally, the Data & Sideband Serialization Interface (DSSI) shall be operational while in FW Upload mode.

Table 12-49 Supported commands during FW upload mode

Code	Command	SMBus Transaction Type
19h	CAPABILITY	Read Byte w/PEC
1Ah	QUERY (used with any command)	Block Write Block Read Process Call w/ PEC
78h	STATUS_BYTE	Read Byte w/PEC
79h	STATUS_WORD	Read Word w/PEC
7Ah	STATUS_VOUT	Read Byte w/PEC
7Bh	STATUS_IOUT	Read Byte w/PEC
7Ch	STATUS_INPUT	Read Byte w/PEC
7Dh	STATUS_TEMPERATURE	Read Byte w/PEC
7Eh	STATUS_CML	Read Byte w/PEC
80h	STATUS_MFR_SPECIFIC	Read Byte w/PEC
81h	STATUS_FANS_1_2	Read Byte w/PEC
98h	PMBUS_REVISION	Read Byte w/PEC
9Ah	MFR_MODEL	Block Read
D4h	MFR_HW_COMPATIBILITY	Read Word w/PEC
D5h	MFR_FWUPLOAD_CAPABILITY	Read Byte w/PEC
D6h	MFR_FWUPLOAD_MODE	Read/Write Byte w/PEC
D7h	MFR_FWUPLOAD	Bloack Write w/ PEC (size = block size from image header)
D8h	MFR_FWUPLOAD_STATUS	Read Word w/PEC
D9h	MFR_FW_REVISION	Block Read w/PEC (7 bytes)
E3h	MFR_FWUPLOAD_BLOCK_SIZE	Read Word w/PEC
Basic Function	**Operating Capability**	
Fan control	Fan can run at a high fixed speed to make sure power supply is cooled in the system for the duration of the FW update.	

PWOK	The PWOK signal must still function properly during power on / off cycles to reset the system	
PSON#	The PSON# signal must still be able to power ON/OFF the power supply.	
UV	Under voltage protection	
OV	Over voltage protection	
OC	Over current protection	

Notes:

1. If the power supply's firmware structure only supports one application image, then these commands must be available in the bootloader along with maintaining the outputs within regulation.
2. If the firmware structure supports 2-application images it is not necessary to have these commands in the bootloader since they will be available in the operational application image.

12.5.3 LED Status

While the PSU FW image is being updated the PSU shall blink using a pattern selected in the LED behavior configuration block of the configuration file, see *12.8.3.1 LED Behavior Configuration Block* for details.

12.5.4 Power Supply Operating Mode During and After Firmware Update

Firmware update mode in ON state with no power cycle needed:

Power supply shall be able to support FW upload in the ON state. The new FW will take effect once it is taken out of FW upload load and the bootloader has determined that the Application is good to be executed.

Bad image after firmware update:

The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode, the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.

12.5.5 Firmware Image Header

The power supply's FW image shall contain a header at the beginning of the file as described in the table below.

Table 12-50 PSU FW Image header

Byte	Definition
Byte 1	CRC LowByte
Byte 2	CRC HighByte
Byte 3	Image Information
Byte 4	Image Information
Byte 5	Image Information
Byte 6	Image Information
Byte 7	Image Information
Byte 8	Image Information
Byte 9	Image Information
Byte 10	Image Information
Byte 11	M
Byte 12	-

Byte 13	C
Byte 14	R
Byte 15	P
Byte 16	S
Byte 17	00h
Byte 18	M-CRPS Revision – Major number = 01h
Byte 19	M-CRPS Revision – Minor number = 00h
Byte 20	M-CRPS Version = Major number = 01h
Byte 21	M-CRPS Version = Minor number = 00h
Byte 22	00h
Byte 23	00h
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).
Byte 25	FW_MINOR_PRIMARY
Byte 26	FW_MINOR_SECONDARY
Byte 27	HW_COMPATIBILITY_FIRST
Byte 28	HW_COMPATIBILITY_SECOND
Byte 29	BLOCK SIZE LowByte
Byte 30	BLOCK SIZE HighByte
Byte 31	Write Time LowByte
Byte 32	Write Time HighByte
M-CRPS FW image header extension	
Bytes 33 to 56	24-byte Model name ending in terminator character
Byte 57	FW_MINOR_THIRD
Byte 58	FW_MINOR_FOURTH
Byte 59	MCU Target: 0 = Reserved 1 = Secondary side MCU (Main application) 2 = Configuration file 3 = Primary side MCU (Main application) 4 = Third Microcontroller 5 = Fourth Microcontroller 6 = Multi-image package[4] 7 – 255 = Reserved
Byte 60	Test FW revision, 00h = Production revision
Byte 61	Bulk Erase time (in seconds)
Byte 62	Options: Bit 0 = if 1, M-CRPS needs a PSON# cycle to run the new firmware after the FW upgrade process has finished. Bit 1 to 3 = Reserved. Bit 4 to 7 = Reset time before turn ON after a FW update when PSON# cycle is needed. Valid values:[5] 0h = Reserved 1h = 1 second 2h = 2 seconds … Fh = 15 seconds
Bytes 63 to 64	Reserved.

Notes:

1. Bytes 11 to 16 allow the system to detect an M-CRPS FW image and use the FW image header extension area.
2. Block size is specified bytes.
3. Write time is specified in milliseconds.

4. Partitioning of the image shall be based on vendor requirements.
5. The M-CRPS shall ignore PSON# signal for the specified amount of time to allow the FW to be verified.

12.5.6 Firmware Update Process

Figure 12-33 FW update process

Notes:

1. PSU may be in standby mode or ON mode during FW update process.
2. If the FW update process is interrupted at any point during the process, the PSU must always be able to return to the bootloader mode.
3. The PSU must always check that the application program is not corrupted, and it is verified using its signature before starting to run from the application program.
4. During the FW upload process the PSU must always respond to any communication on the bus acknowledging its address and the supporting commands without holding the bus. for unsupported bootloader commands the PSU may respond with Not Acknowledge or 00h.

Figure 12-34 PSU Boot flow during powering ON

12.5.7 Power Supply Commands

Name: MFR_HW_COMPATIBILITY
Format: Read Word
Code: D4h

Table 12-51 MFR_HW_COMPATIBILITY command format

Bytes	Value	Description
low	ASCI code for first letter/number of the PSU HW compatibility.	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.
high	ASCI code for second letter/number of the PSU HW compatibility.	

Name: MFR_FWUPLOAD_CAPABILITY
Format: Read Byte
Code: D5h
The system can read the power supply's FW upload mode capability using this command. For any given power supply, more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

Table 12-52 MFR_FWUPLOAD_CAPABILITY command format

Bit	Value	Description

0 (for future use)	*1 = PSU support FW uploading in standby mode only*	*For future use*
1 (for future use)	*1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON.*	*For future use*
2	1 = PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3	1 = PSU supports MFR_FWUPLOAD_BLOCK_SIZE command	Bit used to indicate whether the bootloader supports the MFR_FWUPLOAD_BLOCK_SIZE command
4-7	Reserved	

Name: MFR_FWUPLOAD_MODE
Format: Read/Write Byte
Code: D6h

Table 12-53 MFR_FWUPLOAD_MODE command format

Bit	Value	Description
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restarts This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1-7		Reserved

Name: MFR_FWUPLOAD
Format: Block Write (block = size as defined by the image header)
Code: D7h

Table 12-54 MFR_FWUPLOAD command format

Bytes	Value	Description
Block size defined in header	Image header & image data	Command used to send each block of the FW image. Header should follow the format described in S*ection 12.5.5 Firmware Image Header* The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.

Name: MFR_FWUPLOAD_STATUS
Format: Read Word / Write Word
Code: D8h
At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.
Reset: all bits get reset to ‘0’ when the power supply enters FW upload mode.

Table 12-55 MFR_FWUPLOAD_STATUS command format

Bit	Description	Can be cleared by BMC/Host?
0	1 = Full image received successfully	No
1	1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.	No
2	1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.	No
3	1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features.	No
4	1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.	No
5	1 = Full image received, but failed security checks. Power supply's FW image failed security check at boot, it can power ON, but only in 'safe mode' with minimal operating capability.	No
6	1 = Configuration file has a value set beyond the capabilities of the power supply. Wrong value.	No
7	1 = MFR_FWUPDATE Block write failed due to PEC error. Refer to *Figure 12-35 MFR_FW_UPLOAD_STATUS PEC Error bit 7 assertion flow diagram* for the process to assert this bit.	Yes
8	1 = Block write failed due to flash write error	No
9	1 = M-CRPS is ready to switch to the new image on the next PSON# cycle. This bit goes back to 0 when the M-CRPS is running the most recent FW image.	No
10	1 = Full image received, and it is being verified. MCU shall clear this bit once verification is finished	No
11	1 = MFR_FWUPDATE Block write received successfully. 0 = MFR_FWUPDATE block write failed.	Yes
12-15	Reserved	N/A

Figure 12-35 MFR_FW_UPLOAD_STATUS PEC Error bit 7 assertion flow diagram

Name: MFR_FW_REVISION
Format: Block Read, 7 bytes
Code: D9h

Table 12-56 MFR_FW_REVISION command format

Byte	Value	Description
0	0 - 255	Minor revision; secondary
1	0 - 255	Minor revision; primary
2	0 - 255	Bit 7: 1-> Down grading of PSU FW must be avoided. System BMC can elect to ignore this bit if needed but recommended to follow. 0→ No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision
3	0 – 255	Minor revision; Third MCU
4	0 – 255	Minor revision; Fourth MCU
5	0 – 255	Bootloader revision
6	0 – 255	Test firmware revision, 00 = Production version.

Name: MFR_MODEL (existing PMBus command)
Format: Block Read, Maximum of 24-byte value; ending in terminator character '\0'
Code: 9Ah

Name: MFR_REVISION (existing PMBus command)
Code: 9Bh

Name: MFR_FWUPLOAD_BLOCK_SIZE
Format: Read Word
Code: E3h
The system can read the FW image block size supported by the power supply's firmware update process using this command. This value shall match the value in the FW image header.

12.6 Black Box

This specification defines the requirements for power supplies with PMBus capability to store PMBus and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shutdown. The data can be accessed via the PMBus interface by applying power to the 12VSB pins. No AC power need to be applied to the power supply.

12.6.1 When is Data Saved to the Black Box?

Data is saved to the Black Box for the following fault events:

- General fault

- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

12.6.2 Black Box Events

There are two types of data saved in the Black Box; 1) System Tracking Data, 2) Power supply event data. System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system.

12.6.3 Black Box Process

- System writes system tracking data to the power supply RAM at power ON
- System writes the real time clock data to the PSU RAM once every ~5 minutes
- Power supply tracks number of PSON and AC power cycles in EEPROM
- Power supply tracks ON time in EEPROM
- Power supply loads warning and fault event counter data from EEPROM into RAM
- Upon a warning event, the PSU shall increment the associated counter in RAM.
- Upon and fault event the PSU shall increment the associated counter in RAM
- Upon a fault event that causes the PSU to shutdown all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC & PSON power cycles, PSU ON time, warning event counters and fault event counters.

12.6.4 Commands

Command name: MFR_BLACKBOX
Format: Read Block with PEC (238 bytes)
Code: DCh

Table 12-57 MFR_BLACKBOX record format

Field	Item	Number of Bytes	Description
System Tracking Data	System top assembly number	10	The system will write its part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	System serial number	10	The system shall write the system serial number to the power supply when it is powered ON. This include the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard part number for the assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	Motherboard serial number	10	The system shall write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code.

	Present total PSU ON time	3	Total on time of the power supply with PSON asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached.
	Present number of PSON power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data
Time Stamp			The power supply shall track these time and power cycle counters in RAM. When a Black Box event occurs, the data is saved into the Black Box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real Time Clock Data from System (Reserved for future use)	4	This time stamp does not need to be generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long-standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON# signal is asserted.
	Number of PSON power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event. This is only counted when AC power is present to the power supply.
PMBus			The power supply shall save these PMBus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the PMBus sensors.
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERTATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	

	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	
	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Counters			The power supply shall track the total number for each of the following events. This value shall be saved to the Black Box when a Black Box event occurs. Once a value has reached 15, it shall stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted.
	Thermal shutdown	Upper ½	
	Over current or over power shutdown on output	Lower ½	
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	
	Shutdown due to over voltage on output	Upper ½	
	Input voltage warning; no shutdown	Lower ½	The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	
Power supply event data (N-1)		38	
Power supply event data (N-2)		38	
Power supply event data (N-3)		38	
Power supply event data (N-4)		38	

Command name: MFR_REAL_TIME_BLACK_BOX
Format: Write/Read Block with PEC (4 bytes)
Code: DDh

The system shall use this command to periodically write the real time clock data to the power supply. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long-standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.

Command name: MFR_SYSTEM_BLACK_BOX
Format: Write/Read Block with PEC (40 bytes). Low byte first.
Code: DEh

The system uses this command to write the following data to the PSU.

Table 12-58 MFR_SYSTEM_BLACK_BOX command format

Item	Bytes	Comments
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High bytes

Command name: MFR_BLACKBOX_CONFIG
Format: Read/Write Byte with PEC
Code: DFh

Table 12-59 MFR_BLACKBOX_CONFIG command format

Bit	Value	Description
0	0 = disable black box function 1 = enable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling. The customer shall receive the power supply with the black box function enabled; bit 0 = '1'.
1-7		reserved

Command name: MFR_CLEAR_BLACKBOX
Format: Send Byte with PEC
Code: E0h

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously.
This command is write only. There is no data byte for this command.

12.6.5 Hardware Requirements

The SMBus interface shall be used to access the Black Box data. It may be accessed when the power supply is ON or in standby mode. It also may be accessed when no input power is applied, and power is only applied at the standby output pins by an external source (12VSB).

12.7 Data & Sideband Serialization Interface (DSSI)

This specification defines the requirements for a Modular Common Redundant Power Supply (M-CRPS) Data & Sideband Serialization Interface (DSSI) communication protocol along with its different profiles. DSSI is a single-wire half-duplex protocol created to avoid the need for a higher pin count output interface connector in the power supply. Instead of using individual pins on the output interface connector, DSSI is used to serialize those I/O signals to be consumed by a host MCU or FPGA.

The M-CRPS shall have a physical layer compatible with M-PESTI interface and shall be discoverable though the DSSI link by using M-PESTI Discovery command (00h) replying with the payload described in

Table 12-63 M-CRPS Payload format in the following sections. The M-CRPS shall also be able to accept M-PESTI virtual wire command (01h) and reply to it.

More information about the DC-MHS M-PESTI Interface can be found here:
https://www.opencompute.org/wiki/Server/Working

> ***Note:*** The M-CRPS does not support simple presence by default, the SetA1AsPresenceDetect bit described in *Table 12-75 Miscellaneous configuration block* of the configuration file shall be set to support simple presence.

12.7.1 Physical Layer

The DSSI Protocol requires a physical layer that comprises an UART element, and the input/out circuit shown in below figure, for the power supply as shown in the figure below.

Figure 12-36 Required physical layer in the power supply for data serialization interface

> ***Note:*** Optional buffer might be required for the power supply to measure the pin A1 and establish a logic 0 or 1 for logic addressing mode. Optionally the UART-RX pin of the MCU can be configured as analog input to measure the voltage, a proper sampling time is required to allow the ADC's sampling capacitor to be charged through resistor R1.

The connection between a Client (power supply) and a Host is shown below.

Figure 12-37 Physical layer and connections for point-to-point communication between Host and Client

Notes:

1. Resistor ***Raddr*** (10KΩ) is used to set logic 0 (when placed) or logic 1 (when not placed) for logic addressing mode, and to allow the DSSI communication in the M-CRPS. Choosing a different resistor value for ***Raddr*** might prevent the M-CRPS from communicating through the DSSI. The implementer can choose to not populate ***Raddr*** to improve noise immunity if the plan is to use only M-CRPS in the system and use analog addressing to make use of the DSSI in the pin A1.
2. shorting A1 pin to ground will establish a logic 0 but it will prevent the M-CRPS from communicating through the DSSI.
3. Shorting A1 pin to 3.3V will establish a logic 1 but it will prevent the M-CRPS from communicating through the DSSI.
4. Transistor Q1 shall be activated only after the process described in *Figure 9-10 Flow diagram to detect between logic and analog SMBus addressing* has finished.
5. An extra series resistor might be needed in the A1 pin outside the PSU based on signal integrity simulations of the system.

12.7.2 Default configuration

The UART module used for the DSSI protocol shall be configured by default at boot time with the parameters shown in the table below.

Table 12-60 DSSI UART configuration

Parameter	
Signal type	Bi-directional 3.3V Open-Drain[1]/Totem-Pole Logic[2]
Communication protocol	Half-duplex UART
Port settings	• Data bits: 8 • Parity: Odd • Stop bits: 1 • Flow control: None
Link speed	250,000 bps (Default)

Notes:

1. UART shall be capable of enabling open-drain output in its transmitter pin when is in reception mode.
2. UART shall be capable of enabling totem-pole output in its transmitter pin when is in transmission mode and the baud rate is more than the default 250,000 bps.

12.7.3 Electrical Characteristics

Table 12-61 DSSI electrical characteristics

Parameter	Value
Bus voltage	2.9V - 3.465V
V_{IH}	2.0V min.
V_{IL}	0.8V max.
Rise time	120 ns

Fall time	120 ns

12.7.4 DSSI Protocol Phases

The M-CRPS DSSI protocol has three phases described in below subsections.

12.7.4.1 Configuration Phase

The DSSI shall have a configuration phase activated at any time by sending the UART break character (11 bits in logic 0), this UART break character is used to prevent a misconfiguration from happening. After the UART break character is received the M-CRPS shall accept configuration commands stated in *Table 12-62 Configuration commands set.* If the host/initiator doesn't need to change the default parameters, then it can skip this phase.

12.7.4.2 Discovery Phase

The presence and discovery of the attached peripheral must occur prior to the active phase. During discovery, a payload of static attributes is captured from an M-CRPS to the host/initiator (i.e., baseboard FPGA)

12.7.4.3 Active phase

The active phase is characterized by a repetitive exchange of virtual wires and/or samples between the host/initiator (Baseboard FPGA) and the target M-CRPS.

12.7.5 Interface Initialization

The DSSI interface shall be initialized at MCU boot time following the steps listed below and depicted by the *Figure 12-38 DSSI Flow diagram*.

1. Configure UART Rx pin as input.
2. Configure UART Tx pin as open drain.
3. Write logic 1 to UART Tx pin.
4. Configure UART Tx pin as output.
5. Configure UART with the parameters shown in *Table 12-60 DSSI UART configuration*.
6. Wait for the SMBus address detection process described in *Section 9.6.1 A0 Input Addressing* to be completed.
7. Check the state of SetA1BehaviorForDSSIActive in the configuration file and:
    a. If SetA1BehaviorForDSSIActive is 0, then go to step 8.
    b. If SetA1BehaviorForDSSIActive is 1, then execute the flow in Figure 12-38 DSSI Flow diagram to detect the stimulus from the Agent, then go to step 8.
8. Turn ON the transistor Q1 to bias the bus with the strong pull-up resistor R2.
9. Check the logic state of the bus:
    a. If the bus is logic 0 state disable the DSSI interface.
    b. If the bus is logic 1 state, then continue to the next step.
10. Activate UART Rx interrupts.
11. Wait for a break character or a discovery command (00h) to be received from the host.

a. If a discovery command is received (00h), then respond by sending the payload described in *Table 12-63 M-CRPS Payload format*.
b. If a UART break character is received, then enter in configuration mode defined in *Figure 12-41 DSSI configuration flow diagram example*.

12. Continue replying to commands.

Figure 12-38 DSSI Flow diagram

Figure 12-39 Default DSS transition to active sequence (SetA1BehaviorForDSSIActive = 0)

Notes:

1. M-CRPS shall turn ON Q1 in a maximum of 50us after acquiring the state of A1 pin.

Figure 12-40 Alternative DSSI transition to active sequence (SetA1BehaviorForDSSIActive = 1)

Notes:

1. M-CRPS shall turn ON Q1 by looking at the A1 transition from low to high or high to low depending on the state of A1 pin when the PMBus was acquired, e.g., if the state of A1 was low, then the M-CRPS shall look for a low to high transition.
2. Agent/HPM not ON during this period.

Figure 12-41 DSSI configuration flow diagram example

Note: All configuration changes will take place after receiving the Exit Configuration command 7Eh.

The host can skip some configurations commands if there is no need to change those values. The host shall send the Exit configuration command 7Eh to restart the communication.

12.7.6 Protocol

At boot time the A1 signal shall be sustained in logic 1 establishing an IDLE state. DSSI communication is always initiated by the Host device when data needs to be sent/retrieved. The Host device could set the proper communication settings if the default settings do not satisfy the communication preference of the Host

Profile configuration shall be done after communication settings, the available profiles are described in *Section 12.7.8 Profiles.*

To provide a deterministic behavior the data is transferred from and to the Host following the timing diagrams shown below.

Figure 12-42 Timing diagram for bi-directional DSSI protocol

> ***Note:*** The Host/Initiator shall always initiate the communication to send/retrieve data from the Client/Target (M-CRPS).

The refresh rate of the communication shown in *Figure 12-42 Timing diagram for bi-directional DSSI protocol* shall be calculated based in the following equation:

$$Refresh\ rate = T_{IncomingPacket} + tTAR + T_{OutgoingPacket}$$

Where:

- $T_{IncomingPacket}$ is the time it takes for a packet from the host to be received using back-to-back transmission (e.g. no wait time between bytes).
- $T_{OutgoingPacket}$ is the time it takes for a packet from the M-CRPS to be transmitted to the host using back-to-back transmission (e.g. no wait time between bytes).
- *tTAR* is the time it takes the M-CRPS to start transmitting the reply after receiving a packet from the host.

The host shall not send packets to the M-CRPS at a faster rate than the M-CRPS can receive them, otherwise the M-CRPS will ignore these requests.

The protocol is divided into configuration commands, reply packets, and data packets for discovery and profile data exchange. The configuration command format is depicted in the following figure.

COMMAND	PARAM. LSB	PARAM. MSB	CHECKSUM

Figure 12-43 Configuration command packet structure.

> ***Note:*** Checksum CRC-8 polynomial = 0x07, Seed = 0x00.

The Client/Target shall reply to the configuration commands from the Host with the reply packet structure as shown in the figure below.

REPLY

Figure 12-44 Reply packet structure.

Other commands are detailed in the following subsections.

12.7.7 Command Set

The total amount of commands is 127 (7Fh), the defined commands are listed in the following table.

Table 12-62 Configuration commands set

Profile data exchange commands			
Command (Hex)	**Parameter**	**Reply**	**Description**
BREAK SEQ.	None	00h = OK	Restarts the communication to allow reconfiguration. (11-bits in logic 0).
00h	None	Payload defined in *Table 12-63*	DSSI/M-PESTI Discovery command
01h	Virtual wires (inputs of the power supply)	Virtual wires (outputs of the power supply)	DSSI/M-PESTI Virtual wires command, refer to *Section 12.7.8.1 Basic GPIO Expander Profile (Virtual Wires)*
10h	Analog channels (inputs of the power supply)	Analog channels (outputs of the power supply)	Analog IO channels command, refer to *Section 12.7.8.2 Analog IO Expander Profile*
11h	Virtual wires plus analog channels (inputs of the power supply)	Virtual wires plus analog channels (outputs of the power supply)	Virtual wires plus analog IO channels command, refer to *Section 12.7.8.3 GPIO + Analog IO Expander Profile*
20h	None	AAh = OK	DSSI ping for the host to check if an M-CRPS is present
81h	Virtual wires (inputs of the power supply) With checksum	Virtual wires (outputs of the power supply) With checksum	DSSI/M-PESTI Virtual wires command, refer to *Section 12.7.8.1 Basic GPIO Expander Profile (Virtual Wires)*
90h	Analog channels (inputs of the power supply) With checksum	Analog channels (outputs of the power supply) With checksum	Analog IO channels command, refer to *Section 12.7.8.2 Analog IO Expander Profile*
91h	Virtual wires plus analog channels (inputs of the power supply) With checksum	Virtual wires plus analog channels (outputs of the power supply) With checksum	Virtual wires plus analog IO channels command, refer to *Section 12.7.8.3 GPIO + Analog IO Expander Profile*
A0h	None	AAh = OK With checksum	DSSI ping for the host to check if an M-CRPS is present
Configuration commands			
Command (Hex)	**Parameter**	**Reply**	**Description**
40h	[15:0] 0 = 62,500 bps 1 = 125,000 bps **2 = 250,000 bps** 3 = 500,000 bps 4 = 1,000,000 bps 5 = Reserved …	00h = OK FCh = Not supported FDh = Can't execute FEh = Checksum Error	Change communication baud-rate. Note: baud rates higher than 250,000bps might require activating totem-pole output during transmission.
41h	[15:8] **0 = bi-directional** 1 = Reserved 2 = Reserved 4 = Reserved … [7:0] **0 = Point-to-point** 1 = Reserved 2 = Reserved …	00h = OK FCh = Not supported FDh = Can't execute FEh = Checksum Error	Communication and connection type selection
42h	[15:0] **0 = Simple GPIO expander** 1 = Analog IO expander 2 = GPIO + Analog IO expander 3 = Reserved …	00h = OK FCh = Not supported FDh = Can't execute FEh = Checksum Error	Profile selection
43h	[15:0] 0 = 250 us (reserved) 1 = 500 us (reserved) **2 = 750 us** 3 = 1ms (reserved) …	00h = OK FCh = Not supported FDh = Can't execute FEh = Checksum Error	Communication refresh rate. Default is 750 us
44h	[15:0] 0 = Not supported 1 = 1 second 2 = 2 seconds … 900 = 900 seconds (15 min.)	00h = OK FCh = Not supported FDh = Can't execute FEh = Checksum Error	Shut down the 12VSB output for the required time. This command can be executed only when the power supply is OFF (PSON# = high) if the power supply is ON (PSON# = low) the response shall be FDh Can't execute.

	901-65,535 = Not supported		
45h	[15:8] Reserved [7:0] SMBus address in 8-bit format	00h = OK FCh = Not supported FEh = Checksum Error	Change the SMBus address of the power supply.
46h	[15:8] Reserved [7:0] FRU address in 8-bit format	00h = OK FCh = Not supported FDh = Can't execute FEh = Checksum Error	Change the SMBus address of the FRU memory
47h	[15:0] Threshold 0 = Not supported 1 = 0.1 Amperes 2 = 0.2 Amperes … 65535 = 6553.5 Amperes	00h = OK FCh = Not supported FDh = Can't execute FEh = Checksum Error	Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition in the main output, this command writes to the PMBus IOUT_OC_FAULT_LIMIT (46h) command.
48h	[15:0] 0 = 100 ms 1 = 1 second **2 = 2 seconds** 3 = 3 seconds … 10 = 10 seconds 11 = 65535 = Not supported	00h = OK FCh = Not supported FEh = Checksum Error	Command 44h execution delay. The M-CRPS shall wait for the time configured by this command (2 seconds as default) prior to shutdown the 12Vstby output after receiving command 44h.
7Eh	[15:0] All zeroes	00h = OK FCh = Not supported FDh = Can't execute FEh = Checksum Error	Configuration lock. After this command is sent the M-CRPS shall not execute any command from 40h to 7Fh unless a new break command is sent.
7Fh	Reserved	FDh = Can't execute FEh = Checksum Error	Reserved

Notes:

1. Bold characters shall be the default options at boot time.
2. When the Client's replies "not supported" it will keep the previous configuration.
3. Commands 40h through 7Eh shall be executed only if a prior UART break sequence was detected.
4. Checksum CRC-8 polynomial = 0x07, Seed = 0x00.

Table 12-63 M-CRPS Payload format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	PAYLOAD_VERSION [7:0] = 00h							
01h	DEVICE_CLASS [7:0] = 01h (M-CRPS)							
02h	STATIC_PAYLOAD [7:0] = 04h (32 bytes)							
03h	NUM_VIRTUAL_WIRE_OUTPUT_BYTES [3:0] = 0001b (1 Out Byte)				NUM_VIRTUAL_WIRE_INPUT_BYTES [3:0] = 0001b (1 in Byte)			
04h	NUM_ANALOG_OUTPUT_CHANNELS [3:0] = 0001h (1 Output analog channel)				NUM_ANALOG_INPUT_CHANNELS [3:0] = 0001b (1 Output analog channel)			
05h	DSSI version Minor (e.g. 03h)							
06h	DSSI version Major (e.g. 01h)							
06h – 1Eh	Padding (00h all bytes)							
1Fh	Checksum							

Note: Checksum CRC-8 polynomial = 0x07, Seed = 0x00.

12.7.8 Profiles

12.7.8.1 Basic GPIO Expander Profile (Virtual Wires)

When using a single byte virtual wire exchange (command 01h) the communication shall be as depicted in the following figure.

Figure 12-45 8-Single byte virtual wire exchange

> ***Note:*** The number of bytes for the virtual wires is defined in the payload described in *Table 12-63*.

When using a multi byte virtual wire exchange (command 01h) the communication shall be as depicted in the following figure.

Figure 12-46 Multi-byte virtual wire exchange

> ***Note:*** The number of bytes for the virtual wires is defined in the payload described in *Table 12-63*.

12.7.8.2 Analog IO Expander Profile

When using a single-channel analog channels exchange (command 10h) the communication shall be as depicted in the following figure.

Figure 12-47 Single-channel analog channels exchange

> ***Notes:***
> 1. Each analog channel is 16-bit wide and is encoded as LSB first.

When using a multi-channel analog channels exchange (command 10h) the communication shall be as depicted in the following figure.

Figure 12-48 Multi-channel analog channels exchange

> ***Notes:***
> 1. The number of analog channels is defined in the payload described in *Table 12-63*.
> 2. Each analog channel is 16-bit wide and is encoded as LSB first.

12.7.8.3 GPIO + Analog IO Expander Profile

This protocol supports a combination of general GPIO expander (virtual wires) and analog OI expander profiles, the virtual wires are sent first and then the analog channels for both inputs and outputs.

Figure 12-49 Virtual wires plus analog channels exchange

Notes:

1. The number of bytes for the virtual wires is defined in the payload described in *Table 12-63*.
2. The number of bytes for the analog channels is defined in the payload described in *Table 12-63*.
3. Each analog channel is 16-bit wide and is encoded as LSB first.

12.7.8.3.1 Data and Sideband Selection

Which virtual wires are going to be transferred will be defined in the design specification of the power supply, selected by the customer.

12.8 Configuration File

12.8.1 Overview

This section defines the requirements for a Modular Common Redundant Power Supply (M-CRPS) that provides the ability to modify the behavior of the Power Supply based in the following main areas:

- Thresholds for all the implemented protections like Over Current Protection, Over Temperature Protections, etc.
- LED behavior based in different events.
- Embedded executable code like Fan Speed Control algorithms.
- Data tables.

Note: Power Supply vendors shall provide their configuration file per power supply model with the limits for the values of each register including OTP, OTW, etc. and checked by the customer's development team to see if a change is needed within the capabilities of the design.

The configuration file shall be in binary format and shall be transferred at the factory line or on field by using the PMBus of the Power Supply and shall be able to update its configuration file in run time mode (live update). Figure 1 shows the four main areas that the configuration file shall be made of: 1) File header, 2) Configuration area, 3) Embedded code area, 4) Data table area.

1. **File Header:** This area contains general information about the file like CRC16, file size, customer name and offsets to other areas.

2. **Configuration area:** This is the part where all the thresholds and timings for the protections and warnings are defined along with the LED behavior based on different events that can happen in the power supply.
3. **Embedded code area:** This area contains executable code to be run by the MCU, this area can be used to have specific fan speed control or debug algorithms.
4. **Data table area:** This area contains customer specific data to be used by the power supply like extra FRU data.

Figure 12-50 Main areas of the configuration file.

Note: The file transfer header is the same as defined in *Table 12-50 PSU FW Image header.*

The entire configuration file shall be made of an array of 16-bit unsigned values using Little Endian encoding otherwise noted, and the addressing is represented in bytes, as an example the value 1234h is stored at address 0x0020 as follows:

Figure 12-51 Endianess (Little Endian example)

Address	Data
0020h	34h
0021h	12h

The configuration file header shall include the offsets for the beginning of each area, each one of the areas shall be made of a linked list of blocks, each block shall contain an offset to point to the next block, this offset is always an unsigned 16-bit value. A graphical representation of this structure is shown in the following figure.

Figure 12-52 Representation of the file header and the different configuration blocks that make the areas

Note: An offset to the next block equal to 0000h means the end of the linked list or area not present.

12.8.2 Configuration File Header

The header area shall contain the information shown in the table below.

Table 12-64 Header area

Offset	Element	Description
0000h	CRC16	16-bit CRC, the calculation must exclude the CRC16 field in the file
0002h	configFileVersion	Configuration file version, 0001h for this release.
0004h	fileSizeLow	Size of the entire configuration file in bytes. Least significant 16-bit word
0006h	fileSizeHigh	Size of the entire configuration file in bytes. Most significant 16-bit word
0008h	customerInfo[16]	Customer specific information field. The string “DEFAULT” means the configuration file has the default configurations from the power supply vendor. Null terminated.
0018h	configAreaOffset	Offset in bytes from this location to the beginning of the configuration area
001Ah	codeAreaOffset	Offset in bytes from this location to the beginning of the executable code area
001Ch	dataTableAreaOffset	Offset in bytes from this location to the beginning of the data table area
…	…	…

Note: CRC16 Polynomial is 8D95h, seed = 0000h

12.8.3 Configuration Area Definition

The configuration area shall contain the information shown in the table below.

Table 12-65 Configuration block types

Configuration block type	Value
LED Behavior	0001h
Temperature	0002h
Main output	0003h
Standby output	0004h
Input	0005h
Fans	0006h
Timing	0007h
Latch on Fault condition	0008h
Data serialization	0009h
Miscellaneous	000Ah
…	…

12.8.3.1 LED Behavior Configuration Block

Table 12-66 LED descriptor

Parameter	Bitfield	Options	Comments
Style	[2:0]	0 = LED OFF 1 = LED ON 2 = Blinking 3 = Blink N times then OFF 4 = Blink N times then ON 5 = PWM 6 = Reserved 7 = Reserved	
Color	[5:3]	0 = OFF 1 = GREEN 2 = AMBER 3 to 7 = Reserved	
Flashing Times	[8:6]	0 = Zero time 1 = One time 2 = Two times 3 = Three times 4 = Four times 5 = Five times 6 = Six times 7 = Seven times	
Frequency	[11-9]	0 = 0.5 Hz 1 = 1 Hz 2 = 2 Hz 3 = 3 Hz 4 = 4 Hz 5 = 5 Hz 6 = 6 Hz 7 = 7 Hz	
PWM T_{High}	[13:12]	0 = 250 ms 1 = 1000 ms 2 = 2000 ms 3 = 3000 ms	Time in high state
PWM T_{Low}	[15:14]	0 = 250 ms 1 = 1000 ms 2 = 2000 ms 3 = 3000 ms	Time in low state

Table 12-67 Power supply event table

Offset	Event	Description
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block
0002h	configBlockType	Configuration block type based on *Table 12-65 Configuration block types*
0004h	UVPinput	Input Under Voltage Protection
0006h	OVPmain	Main Output Over Voltage Protection
0008h	OCWmain	Main Output Over Current Warning
000Ah	OCPmain	Main Output Over Current Protection
000Ch	OTWcrit	Critical Component Over Temperature Warning
000Eh	OTWamb	Ambient Over Temperature Warning
0010h	OTPamb	Ambient Over Temperature Protection
0012h	NonCompatible	Non-compatible power supply
0014h	FWUpgrade	PSU is in FW upgrade mode
0016h	Mismatched	Mismatched PSU
0018h	UVPmain	Main Output Under Voltage Protection
0020h	OVWmain	Main Output Over Voltage Warning
0022h	FanWarning	Fan warning, fan not able to establish the speed setpoint.
0024h	FanFault	Fan has completely stopped
0026h	OVPsb	Standby output Over Voltage Protection
0028h	UVPsb	Standby output Under Voltage Protection
002Ah	MainOutputONStbyON	Power supply is ON (PSON# asserted and working properly)
002Ch	MainOutputOFFStbyON	Power supply is in standby state (PSON# de-asserted and working properly)
002Eh	MainOutputOFFStbyOFF	Power supply is OFF (PSON# in S3 state, with AC/DC input within the limits)
0030h	ColdRedundantEnabled	Power supply is in Cold Redundancy mode
0032h	AlwaysColdRedundantEnabled	Power supply is in Always Cold Redundancy mode
0034h – FFFh	Reserved	Reserved

Note: Values in each one of the events are based on the previous table. LED descriptor.

12.8.3.2 Temperature Configuration Block

Table 12-68 Power supply temperature thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-65 Configuration block types*	
0004h	OTWCriticalComponent1		1 ºC
0006h	OTPCriticalComponent1		1 ºC
0008h	OTWCriticalComponent2		1 ºC
000Ah	OTPCriticalComponent2		1 ºC
000Ch	OTWAmbient		1 ºC
000Eh	OTPAmbient		1 ºC
0010h	OTWExit		1 ºC
0012h	OTPExit		1 ºC
…	…	…	

Note: The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage and it shall set bit 6 of the register MFR_FWUPLOAD_STATUS described in *Table 12-55 MFR_FWUPLOAD_STATUS command format*.

12.8.3.3 Main Output Configuration Block

Table 12-69 Power supply main output's thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-65 Configuration block types*	
0004h	Over Voltage Protection		0.1 Volt
0006h	Over Voltage Warning		0.1 Volt
0008h	Under Voltage Protection		0.1 Volt
000Ah	Under Voltage Warning		0.1 Volt
000Ch	Over Power Protection		1 Watt
000Eh	Over Power Warning		1 Watt
0010h	Over Current Protection		0.1 Ampere
0012h	PL4 Level		0.1 Ampere
0014h	PL4 Duration		1 us
0016h	PL3 Level		0.1 Ampere
0018h	PL3 Duration		1 ms
001Ah	PL2 Level		0.1 Ampere
001Ch	PL2 Duration		1 ms
001Eh	PL1 Level		0.1 Ampere
0020h	PL1 Duration		1 ms

Notes:

1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage and it shall set bit 6 of the register MFR_FWUPLOAD_STATUS described in *Table 12-55 MFR_FWUPLOAD_STATUS command format*.
2. A value of 0 (Zero) in any of the Duration fields will indicate that the power supply shall not wait to trigger the event.

12.8.3.4 Standby Output Configuration Block

Table 12-70 Power supply standby output's thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-65 Configuration block types*	
0004h	Over Voltage Protection		0.1 Volt
0006h	Over Voltage Warning		0.1 Volt
0008h	Under Voltage Protection		0.1 Volt
000Ah	Under Voltage Warning		0.1 Volt
000Ch	Over Power Protection		1 Watt
000Eh	Over Power Warning		1 Watt
0010h	Over Current Protection		0.1 Ampere
0012h	PL2 Level		0.1 Ampere
0014h	PL2 Duration		1 ms
0016h	PL1 Level		0.1 Ampere
0018h	PL1 Duration		1 ms
…	…	…	…

Notes:

1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage and it shall set bit 6 of

the register MFR_FWUPLOAD_STATUS described in *Table 12-55 MFR_FWUPLOAD_STATUS command format*.

2. A value of 0 (Zero) in any of the Duration fields will indicate that the power supply shall not wait to trigger the event.

12.8.3.5 Input Configuration Block

Table 12-71 Power supply input thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-65 Configuration block types*	
0004h	Over Voltage Protection		0.1 Volt
0006h	Over Voltage Warning		0.1 Volt
0008h	Under Voltage Protection		0.1 Volt
000Ah	Under Voltage Warning		0.1 Volt
000Ch	Over Power Protection		1 Watt
000Eh	Over Power Warning		1 Watt
0010h	Over Current Protection		0.1 Ampere
0012h	Over Current Warning		0.1 Ampere
…	…	…	…

Notes:

1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage and it shall set bit 6 of the register MFR_FWUPLOAD_STATUS described in *Table 12-55 MFR_FWUPLOAD_STATUS command format*.
2. A value of 0 (Zero) in any of the fields will indicate that the power supply shall not trigger the event.

12.8.3.6 Fans Configuration Block

Table 12-72 Power supply fans thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-65 Configuration block types*	
0004h	Fan1FaultLowRPM		1 RPM
0006h	Fan1FaultLowRPMDelay		1 ms
0008h	Fan1MinRPM		1 RPM
000Ah	Fan1MaxRPM		1 RPM
000Ch	Fan2FaultLowRPM		1 RPM
000Eh	Fan2FaultLowRPMDelay		1 ms
0010h	Fan2MinRPM		1 RPM
0012h	Fan2MaxRPM		1 RPM
…	…	…	…

Notes:

1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage and it shall set bit 6 of

the register MFR_FWUPLOAD_STATUS described in *Table 12-55 MFR_FWUPLOAD_STATUS command format*.

2. A value of 0 (Zero) in any of the Duration fields will indicate that the power supply shall not wait to trigger the event.

12.8.3.7 Timing Configuration Block

Table 12-73 Power supply timing configuration

Offset	Parameter	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-65 Configuration block types*	
0004h	Toff_latch		1 ms
0006h	Tpson_on_delay		1 ms
0008h	Tpwok_on		
000Ah	Tpwok_off		
000Ch	Tpwok_low		
000Eh	InputLostToSMBAlertDelay		1 ms
0010h	InputLostToVINOKDelay		1 ms
0012h	InputRegainToVINOKDelay		1 ms
0014h	InputTurnONVoltage		0.1 Volt
0016h	InputTurnOFFVoltage		0.1 Volt
0018h	InputAvrgCycles		AC cycles
001Ah	Tvinok_off		LSB = 200us
001Ch to FFFFh	Reserved		

Notes:

1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage and it shall set bit 6 of the register MFR_FWUPLOAD_STATUS described in *Table 12-55 MFR_FWUPLOAD_STATUS command format*.

12.8.3.8 Latch on Fault Condition Configuration Block

Table 12-74 Power supply latch on fault condition configuration block

Offset	Bit	Event	Description	Options
0000h		offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h		configBlockType	Configuration block type based on *Table 12-65 Configuration block types*	
0004h	0	MainOutputOCP		1=Latch, 0=No Latch
0004h	1	MainOutputOVP		1=Latch, 0=No Latch
0004h	2	MainOutputUVP		1=Latch, 0=No Latch
0004h	3	MainOutputOPP		1=Latch, 0=No Latch
0004h	4	StbyOutputOCP		1=Latch, 0=No Latch
0004h	5	StbyOutputOVP		1=Latch, 0=No Latch
0004h	6	StbyOutputUVP		1=Latch, 0=No Latch
0004h	7	StbyOutputOPP		1=Latch, 0=No Latch
0004h	8	InputOCP		1=Latch, 0=No Latch
0004h	9	InputOVP		1=Latch, 0=No Latch
0004h	10	InputUVP		1=Latch, 0=No Latch

0004h	11	InputOPP		1=Latch, 0=No Latch
0004h	12	AmbientTempOTP		1=Latch, 0=No Latch
0004h	13	CritComponent1TempOTP		1=Latch, 0=No Latch
0004h	14	CritComponent2TempOTP		1=Latch, 0=No Latch
0004h	15	ExitTempOTP		1=Latch, 0=No Latch
0006h	0	FanFault		1=Latch, 0=No Latch
0006h	[15:1]	Reserved		
0008h	0	ClearFaultsWithPSONCycle		1 = Clear faults with PSON# cycle (no need for input cycle), 0 = Clear faults only with an input (AC or DC) cycle.
0008h	[15:1]	Reserved		
…	…	…	…	…

12.8.3.9 Data & Sidebands Serialization Interface Configuration Block

The sidebands and/or data to be serialized through the DSSI shall be provided in the Design Specification.

12.8.3.10 Miscellaneous Configuration Block

Table 12-75 Miscellaneous configuration block

Offset	Bit	Name	Description	Options
0000h		offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h		configBlockType	Configuration block type based on *Table 12-65 Configuration block types*	
0004h	0	OTPConfigFile	One-time programmable configuration file. If this bit is set the configuration file can no longer be updated in the M-CRPS	1 = One Time programmable only (factory), 0 = Allow multiple configuration file updates on field.
0004h	1	Multi-StatePSON	Configure Multi-state or 2-state PSON input signal	1 = Multi-state, 0 = 2-state PSON
0004h	2	ImonSensitivity	Configures 0-2mA equals 0 to 200% or 10uA/A sensitivities for the Imon output signal	1 = 0-2mA, 0 = 10uA/A
0004h	3	Imon/presence	Configures pin S13 of the power supply as Imon or as Presence	1 = Imon active, 0 = Imon disabled, and pin is held low (presence)
0004h	4	Reserved		
0004h	5	Reserved		
0004h	6	Reserved		
0004h	7	Reserved		
0004h	8	Reserved		
0004h	9	Reserved		
0004h	10	Reserved		
0004h	11	Reserved		
0004h	12	Reserved		
0004h	13	Reserved		
0004h	14	Reserved		
0004h	15	Reserved		
0006h	[15:0]	ColdStandby1Enable	Enable threshold for $V_{CR_ON_EN}$	0 to 8V; Resolution of 1mV/LSB
0008h	[15:0]	ColdStandby1Disable	Disable threshold for $V_{CR_ON_DIS}$	0 to 8V; Resolution of 1mV/LSB
000Ah	[15:0]	ColdStandby2Enable	Enable threshold for $V_{CR_ON_EN}$	0 to 8V; Resolution of 1mV/LSB
000Ch	[15:0]	ColdStandby2Disable	Disable threshold for $V_{CR_ON_DIS}$	0 to 8V; Resolution of 1mV/LSB
000Eh	[15:0]	ColdStandby3Enable	Enable threshold for $V_{CR_ON_EN}$	0 to 8V; Resolution of 1mV/LSB
0010h	[15:0]	ColdStandby3Disable	Disable threshold for $V_{CR_ON_DIS}$	0 to 8V; Resolution of 1mV/LSB
0012h	[15:0]	ColdStandby4Enable	Enable threshold for $V_{CR_ON_EN}$	0 to 8V; Resolution of 1mV/LSB
0014h	[15:0]	ColdStandby4Disable	Disable threshold for $V_{CR_ON_DIS}$	0 to 8V; Resolution of 1mV/LSB
0016h	[15:0]	ColdStandby5Enable	Enable threshold for $V_{CR_ON_EN}$	0 to 8V; Resolution of 1mV/LSB

0018h	[15:0]	ColdStandby5Disable	Disable threshold for $V_{CR_ON_DIS}$	0 to 8V; Resolution of 1mV/LSB
001Ah	0	VoutMarginingUnlock	Unlock vout margining function command	0 = locked 1 = unlocked
001Ah	1	OCWPL1SettingUnlock	Unlock OCWPL Setting command	0 = locked 1 = unlocked
001Ah	2	SetA1BehaviorForDSSIActive	Selects when to bias the DSSI bus in pin A1.	0 = A1 pin default DSSI transition to active, M-CRPS biases the bus after A1 PMBus address has been acquired. 1 = A1 pin alternative DSSI transition to active, M-CRPS waits for a stimulus to the bias the bus.
001Ah	3	Use1BitPMBusAddressing	Use only A0 for PMBus addressing and ignore A1.	0 = A0 & A1 are used for PMBus addressing. 1 = Only A0 is used for PMBus addressing.
001Ah	4	DisablePSKILL	Disable PSKILL	0 = PSKILL is enabled 1 = PSKILL is disabled
001Ah	5	EnableStatusSimulationCmd	Enable status simulation command	0 = disabled 1 = enabled
001Ah	6	SMBAlertPL4Behavior	Select SMBAlert signal assertion behavior to a PL4 event	0 = Legacy, latch for 150ms then release SMBAlert# 1 = Latch, must receive clear command to release SMBAlert#
001Ah	[15:7]	Reserved	Reserved	Reserved
001Ch	[15:0]	Reserved	Reserved	Reserved
001Eh	[15:0]	Reserved	Reserved	Reserved
0020h	[15:0]	Reserved	Reserved	Reserved
0022h	[15:0]	Reserved	Reserved	Reserved
0024h	[15:0]	Reserved	Reserved	Reserved
0026h	[15:0]	Reserved	Reserved	Reserved
0028h	[15:0]	Reserved	Reserved	Reserved
002Ah	[15:0]	Reserved	Reserved	Reserved
002Ch	[15:0]	Reserved	Reserved	Reserved
002Eh	[15:0]	Reserved	Reserved	Reserved
0030h	[15:0]	Reserved	Reserved	Reserved
0032h	[15:0]	Reserved	Reserved	Reserved
0034h	[15:0]	Reserved	Reserved	Reserved
0036h	[15:0]	Reserved	Reserved	Reserved
0038h	[15:0]	Reserved	Reserved	Reserved
003Ah	[15:0]	Reserved	Reserved	Reserved
003Ch	[15:0]	Reserved	Reserved	Reserved
003Eh	[15:0]	Reserved	Reserved	Reserved
0040h	[15:0]	Reserved	Reserved	Reserved
0042h	[15:0]	Reserved	Reserved	Reserved
0044h	[15:0]	VMainDischargeMax	Main output's discharge threshold	0 to 1V; Resolution 1 1mV/LSB
0046h	[15:0]	VsbDischargeMax	Standby output's discharge threshold	0 to 1V; Resolution 1 1mV/LSB
0048h	[15:0]	FPCMainMinOFFTime	Main output's full power cycle minimum OFF time	Range from 1 to 900
004Ah	[15:0]	FPCVsbMinOFFTime	Standby output's full power cycle minimum OFF time	Range from 1 to 900
004Ah to FFFFh		Reserved	Reserved	Reserved

12.8.4 Embedded Code Area Definition

The configuration file shall have an embedded executable code area so the user-defined code can be run. The endianness of the executable area will depend on the MCU's endianness. Each one of the embedded

code blocks shall include an offset pointing to the next block and the type of embedded code base in the following table.

Table 12-76 Embedded executable code block types

Executable code block type	Value
Fan speed control	0001h
Over temperature	0002h
Output over current	0003h
Input voltage	0004h
Data serialization	0005h
Debug	0006h
…	…

Depending on the type of embedded executable code listed in the previous table the return structure will change accordingly, the definition of each return structure is defined on each one of the following subsections.

12.8.4.1 Executable Code Block Definition

Table 12-77 Power supply event table

Offset	Event	Description
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block
0002h	codeBlockType	Configuration block type based on *Table 12-76 Embedded executable code block types*
0004h	TaskName[16]	String with the code block name, null terminated
0006h	ExecRateMs	Execution rate of the task in milli-seconds
0016h	RAMScratchpadSize	Amount of RAM needed by the executable code block in bytes
0018h	TaskSize	Size of the executable code block in bytes
002Ah	executableCode	Beginning of the executable code
…	…	…

12.8.5 Data Table Area Definition

If used, the content of the data table will be defined in the configuration file provided by the customer.

12.8.6 Configuration File Creation

Figure 12-53 Configuration file creation graphical representation

Figure 12-54 MCU memory map example

12.9 Security

12.9.1 Security Architecture

The security solution for the M-CRPS shall be designed such that the device responding to SPDM requests has a cryptographically secure method of responding to the SPDM Requester. Another component in the

DC-MHS system is the SPDM Requester, the M-CRPS is the SPDM Responder. The device on the M-CRPS that communicates on the PMBus as the SPDM Responder shall be protected by and compliant with the Secure Boot, Code Protection, and Code Signing Infrastructure sections of this standard.

For guidance purposes, four architectures are presented. The first is a non-compliant example. The others are compliant.

Figure 12-55 Example Non-Compliant Architecture

The non-compliant example fails compliance because the MCU in question has no support for Secure Boot or Secure Firmware Update. The lack of these features means that we cannot trust its firmware to operate properly even if the SPDM protocol itself is secure. The MCU could lie to the SPDM responder about its code. So even though the SPDM MEASUREMENTS response is tamper-evident and cannot be spoofed or replayed, the measurement it contains is inaccurate. This situation is arguably worse than doing nothing. If you did not do any SPDM protocol sequences, you would have no expectation about the security of the system. However, getting cryptographic measurements of firmware gives the receiver confidence that the system is secure. If those measurements are based on lies, the user has misplaced trust in a broken system.

Figure 12-56 Example Compliant Architecture - Secure MCU

Secure Boot gives us confidence that the firmware running on the system is authentic. Secure Firmware Update ensures that firmware cannot be updated outside of the secure mechanism and that updates are not applied to the MCU unless they meet the signing requirements. In the Secure MCU compliant architecture example, this gives us confidence that the code running on the MCU was signed by the code creator and is not lying about its own measurements. A compliant variant of this architecture could move the Secure SPDM Responder outside the Secure MCU. This architecture can be useful when the MCU has non-volatile, mutable code storage that is only accessible internally. In that case, an external Root of Trust would be unable to attest to that code as it has no direct access to the code.

Figure 12-57 Example Compliant Architecture – eRoT

In the external Root of Trust (eRoT) example, the eRoT is protected by Secure Boot and, if its firmware is updateable, Secure Firmware Update. The eRoT performs the Secure Boot and Secure Firmware Update functions for the MCU. If this architecture is used, the eRoT must be able to hold the MCU in reset or otherwise prevent the MCU from running if the firmware loaded on it is inauthentic (e.g. fails a signature check). The Secure SPDM Responder function can be inside the MCU because that code will be verified by the eRoT and will not run unless the verification succeeds. The eRoT prevents the insecure MCU and SPDM code from lying to the SPDM Requester. This architecture is useful in the case where the non-volatile code storage is accessible by an external entity like the eRoT. This architecture assumes that the eRoT has direct access to the mutable code, for example, if the mutable code is stored in an external chip or the MCU exposes its internal memory on an external interface.

Figure 12-58 Example Compliant Architecture – Dual

The Dual architecture example is a special case of the Secure MCU idea. It could enable the use of a simpler MCU with the basic required features but focused on the normal M-CRPS firmware operations, off-loading some or all SPDM functions to a simple chip capable of securely storing keys, certificates, and/or the required SPDM functions.

12.9.2 Secure Boot

There shall be at least one device in the security architecture that complies with the OCP Hardware Secure Boot White Paper, version 1.0 or later [2]. This includes compliance with Section 11, Device Recovery [2].

If the device compliant with this section is a separate chip from the chip connected to the PMBus, the compliant device shall have the capability to prevent the M-CRPS from running unless the failure is corrected and verified successfully by a RoT.

12.9.3 Secure Firmware Update

All microcontrollers within the M-CRPS shall enable code protections such that the firmware on the device may not be read/written/erased or otherwise altered via any method other than authenticated signed images. This includes all debugging/programming pins.

If the firmware update cannot be completed and there is no automatic recovery capability, the M-CRPS shall set bit 5 of MFR_FWUPLOAD_STATUS to indicate to the system that it requires a firmware update to return to Operating Mode.

12.9.4 Code Signing Infrastructure

Mutable code shall be signed with a key pair generated and stored on an HSM according to security best practices. Code signing certificates may be signed by a Certificate Authority (CA) maintained by the M-CRPS manufacturer itself, or a well-respected third-party CA such as one trusted to sign web infrastructure.

The code signing scheme as well as all outputs of it, including the required SPDM device certificate chain shall follow the requirements of the Algorithm Support section of this document.

12.9.5 Algorithm Support

The M-CRPS shall support algorithms as described in Section 7 of the OCP Hardware Secure Boot White Paper [2].

12.9.6 Attestation

12.9.6.1 Required SPDM Support

The M-CRPS shall support Firmware attestation and device authentication via Security Protocol and Data Model (SPDM) v1.2 [1] over PMBus using the command DAh.

Figure 12-59 General SPDM Request/Response Flow

Figure 12-60 Selected SPDM Messages

Support for secure sessions is not required.

Certificate provisioning support may be provided. If it is provided, then secure sessions shall be implemented.

Mutual authentication support is not required.

The M-CRPS shall support the Large SPDM message transfer mechanism (CHUNK_CAP in [1]). This feature is described in Section 10.26 of [1].

The following table describes the required and optional SPDM Device Responses:

Table 12-78 SPDM Device responses

Response	Code	M-CRPS Requirement
DIGESTS	0x01	Required
CERTIFICATE	0x02	Required
CHALLENGE_AUTH	0x03	Required
VERSION	0x04	Required
CHUNK_SEND_ACK	0x05	Required
MEASUREMENTS	0x60	Required
CAPABILITIES	0x61	Required
ALGORITHMS	0x63	Required
KEY_EXCHANGE_RSP	0x64	Optional
FINISH_RSP	0x65	Optional
PSK_EXCHANGE_RSP	0x66	Optional
PSK_FINISH_RSP	0x67	Optional
HEARTBEAT_ACK	0x68	Required
KEY_UPDATE_ACK	0x69	Optional
ENCAPSULATED_REQUEST	0x6A	Optional
ENCAPSULATED_REQUEST_ACK	0x6B	Optional
END_SESSION_ACK	0x6C	Optional
CSR	0x6D	Optional
SET_CERTIFICATE_RSP	0x6E	Optional
VENDOR_DEFINED_RESPONSE	0x7E	Not Required
ERROR	0x7F	Required

12.9.6.2 Measurements & Firmware Attestation

All measurements within the M-CRPS shall be made using a secure, cryptographic hashing algorithm that meets the requirements of the Algorithm Support section of this document. The following areas of memory shall be individually measured at boot time with an immutable boot ROM:

Table 12-79 Measurement areas

Memory Area	SPDM Measurement Block ID
Main Application (Secondary side Microcontroller)	01h
Configuration File Area	02h
Main Application (Primary side Microcontroller)	03h
Third Microcontroller	04h
Fourth Microcontroller	05h
Reserved	06h-FFh

The M-CRPS shall respond to a GET_MEASUREMENTS request with signed measurements for each area requested. Section 10.11 of [1] describes the protocol for this Request/Response pair. M-CRPS do not require support for recomputing all measurements without requiring a Reset. It is acceptable for the M-CRPS' SPDM capability flag MEAS_FRESH_CAP to be 0.

12.9.6.3 Device Authentication

To support device authentication, the M-CRPS shall support a digital signature scheme that meets the requirements of the Algorithm Support section of this document. The M-CRPS shall respond to a CHALLENGE request. This Request/Response pair is described in Section 10.9 of [1].

12.9.7 References

[1] Security Protocol and Data Model (SPDM) Specification, Version 1.2.0, 2021-12-14, IETF, Document Identifier: DSP0274, https://www.dmtf.org/content/dmtf-releases-security-specification-12

[2] Hardware Secure Boot, Version 1.0, Open Compute Project Security Workgroup, https://www.opencompute.org/documents/secure-boot-2-pdf

[3] NIST Special Publication 800-57 Part 1 Revision 5, Recommendation for Key Management: Part 1 – General, NIST, May 2020, https://doi.org/10.6028/NIST.SP.800-57pt1r5

[4] Commercial National Security Algorithm Suite 1.0, National Security Agency, https://media.defense.gov/2021/Sep/27/2002862527/-1/-1/0/CNSS%20WORKSHEET.PDF

13 Reliability

13.1 Component De-Rating

A component derating analysis shall be completed in accordance with internal derating procedure which based on Electronic Derating for Optimum Performance by Reliability Analysis Center (RAC). A limited life component identification and analysis shall be performed on all aluminum electrolytic capacitors or any

other potentially limited life components used in the design of the assembly. The latest supplier's equation shall be used to calculate capacitor life expectancy

Test Conditions

- Multiple sources shall be included in this analysis.
- All components used in PSU shall be qualified in accordance with the appropriate JEDEC standard as well as Internal Component Engineering qualification procedures and requirements.
- Input Voltage: Nominal (HL $200V_{AC}$ – $240V_{AC}$; LL $100V_{AC}$ – $120V_{AC;}$ -48Vdc – -60Vdc; 277Vac; 336Vdc; +54Vdc)
- Output current: 80%, 100% full load on all rails including standby.
- Inlet Ambient Temperature: Max Ambient (per Safety submittal conditions of the Design Specification)
- Altitude: Sea Level
- Back Pressure: 0" of H_2O
- Pass/Fail Criteria
    - PSU shall comply with internal Component Derating Specification at ≤80% load.
    - Components shall not exceed specs limits at >80% & ≤100% load.

The following component de-rating guidelines shall be followed. Any exceptions are subject to final approval.

Table 13-1 Component de-rating guidelines

Component Type	Parameter	Derating Criteria
Capacitors		
Aluminum Liquid Capacitor (Fixed Aluminum Liquid Electrolyte Type)	DC Voltage Ambient Rated Temperature Minimum life determined using worst-case operating condition for the capacitor and 100% System Duty Cycle. Rated Ripple Current (no adjustment for frequency or temperature factors) Minimum Life High Voltage Bulk Storage Cap Max Voltage (≥ 100V) at peak steady state conditions.	85% ≥105°C See below for detail 80% 100% for High voltage bulk cap (≥ 100V) 5 years @ 80% load 7 years at 50% load 100%

Component Type	Parameter	Derating Criteria
Aluminum Solid Capacitor (Fixed Aluminum Solid Electrolyte Type (includes Organic Semi-conductive (OSCON), Conductive Polymer, Solid Aluminum))	Applied DC Voltage (Working Voltage) AC Ripple + DC (Operating Voltage) Ambient Rated Temperature Maximum measured Case Temp below Ambient Rated Temperature Minimum life calculated using worst-case operating condition for the capacitor and 100% System Duty Cycle. Ripple Current Minimum Life	80% 95% ≥105°C Tmax - 15°C See below for detail 80% 5 years @ 80% load 7 years at 50% load
Aluminum Hybrid Capacitor (Fixed Aluminum Hybrid Electrolytic Type)	DC Voltage Ambient Rated Temperature Minimum life determined using worst-case operating condition for the capacitor and 100% System Duty Cycle. Rated Ripple Current (no adjustment for frequency or temperature factors) Minimum Life High Voltage Bulk Storage Cap Max Voltage (≥ 100V) at peak steady state conditions.	85% ≥105°C See below for detail 80% 5 years @ 80% load 7 years at 50% load 100%
Tantalum Capacitor (Fixed Solid Tantalum Type)	Working DC Voltage: Ambient Rated Temperature Maximum Case Temperature below Max Ambient Limit Ripple Current Reverse Voltage (% of Forward Voltage)	30% ≥105°C Tmax - 20°C 70% 2%
Ceramic Capacitor (Fixed Ceramic – Pin Through Hole (PTH))	DC Voltage Ambient Temperature	85% Tmax - 10°C
MLCC (Fixed Multilayer Ceramic Capacitors – Surface Mount Device (SMD))	All Applications and Temperature Ratings Requirements: DC Voltage Ambient Temperature *Additional* Power and Critical Function Applications Requirements: Ambient Rated Temperature Surface temp Max 105°C Ambient rated 125°C Ambient rated	 85% Tmax - 10°C ≥105°C 90°C 110°C

Component Type	Parameter	Derating Criteria
MLPC (Multilayer Polymer Aluminum Capacitor)	Applied DC Voltage (Working Voltage) AC Ripple + DC (Operating Voltage) Ambient Rated Temperature Maximum measured Case Temp below Ambient Rated Temperature Minimum life calculated using worst-case operating condition for the capacitor and 100% System Duty Cycle. Ripple Current Minimum Life	80% 95% ≥105°C Tmax - 15°C See below for detail 80% 7 years
Plastic Film Capacitor (Fixed Film (Paper/Plastic) Capacitor)	Voltage (% of Max rated) Ambient Temperature	90% Tmax - 10°C
X-Y Capacitor (Fixed X and Y Capacitor (Ceramic or Film, including Safety Agency certified))	Voltage (% of Max rated) Ambient Temperature	90% Tmax - 10°C
Tantalum Polymer Capacitor (Fixed Tantalum Polymer Type (includes POS-CAP, KOCAP, Neocap, SP caps))	Applied DC Voltage (Working Voltage) Applied AC Ripple + DC Voltage (Operating Voltage) Ambient Rated Temperature Measured Case (surface) Temp rise above Measured Ambient Operating temperature Surge Current Reverse Voltage Minimum life calculated using worst-case operating condition and 100% System Duty Cycle. Ripple Current Minimum Life	80% 95% ≥105°C 10°C 10 Amp peak 5% or 0.5V (Whichever is smaller) See below for detail 80% 7 years

Component Type	Parameter	Derating Criteria
EDLC Capacitor (EDLC radial lead (includes Supercaps))	Applied DC Voltage Case Temp below Max Case Operating Limit Charge / Discharge Current Minimum life calculated using worst-case operating condition and 100% System Duty Cycle. Regarding the selection of the life formula used, failure is defined as when an EDLC's capacitance changes ±30% from its initial value. Life Formula used shall apply this definition. (Example: If EDLC's initial capacitance equals 10F, then failure is when the measured capacitance is less than 7F or greater than 13F.) Minimum Life	80% 20°C 90% See below for detail 7 years
Resistors		
Fixed Film Resistor (Fixed Film (Chip Discrete and SMD))	Power Dissipation Ambient Temperature	70% Tmax - 24°C
Zero Ohm Resistor (Zero Ohm Resistor)	Current	84%
Composition (Composition)	Power Dissipation Ambient Temperature	70% Tmax - 18°C
Variable Resistor (Variable)	Power Dissipation Ambient Temperature Non-wirewound Wirewound	70% Tmax - 31°C Tmax - 19°C
Thermistor Resistor (Thermistor)	Power Dissipation Ambient Temperature	50% Tmax - 50°C
Wirewound Power Resistor (Wirewound Power)	Power Dissipation Voltage Ambient Temperature	70% 70% Tmax - 10°C
Miscellaneous		
Metal Oxide VAR Resistor (Metal Oxide Varistors (MOV))	Power Dissipation Max Steady State Operating Voltage/or Clamping Voltage Max Current	60% 35% 90%
Module (Module) (includes Flash Memory devices)	Ambient Temperature	100%
Non-certified Circuit Breakers (Circuit Breakers)	Current	90%
Certified Circuit Breakers (Circuit Breakers with Safety Agency Rating)	Current	100%
Non-certified Fuses (Fuses)	Current Current (time delay fuse)	90% 85%
Certified Fuses (Fuses with Safety Agency Rating)	Current	100%
PTC (Polymeric Positive Temperature Coefficient (PTC) Overcurrent Protector)	Derating is to follow the PTC manufacturer's derating recommendations. Key parameters to consider in derating are current (Ihold, Imax) and component ambient temperature.	Manufacturer recommendation
Signal Connectors (Connectors, Signal)	Ambient Temperature *Note: Wire size used in application shall comply with connector specification and rated current.* Voltage (% of Dielectric Withstand Voltage) Current	Tmax - 25°C 80% 85%

Component Type	Parameter	Derating Criteria
Power Connectors (Connectors, Power)	Ambient-Temperature Note: Wire size used in application shall comply with connector specification and rated current. Voltage (% of Dielectric Withstand Voltage) Current (per pin, single or parallel pin configuration) Current (per pin, parallel pin configuration with one broken pin)	Tmax - 25°C 80% 85% 100%
Dual Connector (Connectors, Combined (Signal and power pins in same connector housing))	Signal pins and power pins shall be derated separately using the worst-case-power pin and worst-case signal pin stresses. Signal pins, use same criteria as Connectors, Signa l Power pins, use same criteria as Connectors, Power	 See above See above
Certified Connectors (Connectors, Power or Combined with Safety Agency Rated)	Only power or combined connectors may have a safety agency rating. Rating shall include current, voltage, and temperature.	100%
Application Specific Connectors (Connectors, Application Specific)	Derating not required for connectors developed and qualified for a specific application and are being used in that application (for example, processor sockets and DIMM sockets)	N/A
2-30 Conductors Bundled Wire Conductor (Bundled Wire Conductor) (Rack level cabling only)	2-5 Conductors, Current 6-15 Conductors, Current 16-30 Conductors, Current	70% 60% 50%
Relay (Relays)	Resistive Load Current Capacitive Load Current Inductive Load Current Ambient Temperature Motor Load Current Filament (Lamp) Contact Power	90% 90% 75% Tmax - 20°C 30% 20% 70%
General Purpose Switch / Power Switch (Switches (General Purpose and Power))	Contact Current Resistive Load Capacitive Load Motor Load Filament (Lamp) Load Contact Current Inductive Load Contact Power Contact Surge Current	 90% 90% 30% 20% 75% 70% 80%
Certified Power Switch (Switches (Power) with Safety Agency Rating)	Contact Current Ambient Temperature	100% 100%
ESD Device (ESD & Surge Suppression components)	For all parameters use per manufacturer's specifications *Note: These are components that are used to protect system or circuit elements from transient stresses beyond those encountered during normal operation*	-
Crystals / Oscillators (Crystals and Oscillators)	Shall meet all parameters use per manufacturer's specifications considering all modes of operation including fan fault condition	-
Diodes		
Diode General Purpose General Purpose (Signal, Switching, or Power Rectifier)	Reverse Voltage Maximum Tj Forward Current	80% 0.75(Tjmax - 25°C) + 20°C <100%
Diode SiC Silicon Carbide (SiC) Power Rectifier Note: Do not avalanche SiC diodes	Reverse Voltage Maximum Tj Forward Current	80% 0.75(Tjmax - 25°C) + 20°C <100%
Diode Regulator / Zener Voltage Regulator / Reference (including Zener)	Maximum Tj Maximum Power Dissipation	0.75(Tjmax - 25°C) + 20°C 100%

Component Type	Parameter	Derating Criteria
Diode Thyristor / SCR Thyristor, SCR, and Triac	On-State Current (It) Off-State Voltage (Vr) Maximum Tj	90% 70% 0.75(Tjmax - 25°C) + 20° C
Microcircuits		
IC DrMOS (Driver MOS (DrMOS), Power Stage, Smart Power Stage)	The parameters stated in the component specification's "Absolute Maximum Ratings" table shall be used in conjunction with the derating criteria presented herein to determine maximum allowable stress levels. For the specific functions/pins (Vboot – Vsw, VCC, VCCP) DC voltage only (Working Voltage) AC + DC (Operating Voltage) For all other non-logic pins not listed above (NOTE: Logic pins require no derating) AC + DC voltage (Operating Voltage) When only $V_{(DC)}$ is specified (with no visible sign of Avalanche) Maximum duration of AC voltage excursion above derated Vdc (when only V(DC) is specified.) Maximum Junction Temperature (Tj) With worst-case steady state application loading When stressing with approved thermal virus DC voltage only (Working Voltage)	90% 95% 95% 95% 25ns 0.75(Tjmax – 25°C) + 20°C Tjmax – 30°C 95%
IC POL (Point of Load Voltage Regulator, Voltage Controller IC, Multi Chip Module (MCM), Monolithic devices)	Derating criteria is the same as for DrMOS	N/A
IC Digital / Linear / Linear-Fixed Voltage Silicon Digital & Linear IC's (MOS & Bipolar)	Maximum Junction Temperature (Tj) Max rated Tj > 125°C Max Rated Tj ≤ 125°C	 The greater of 115°C and 0.75(Tjmax - 25°C) + 20°C Tj (rated) – 10°C

Component Type	Parameter	Derating Criteria
Transistors		
Transistor Silicon FET (Silicon FET)	Maximum Junction Temperature (Tj)	0.75(Tjmax – 25°C) + 20°C
	Avalanche Energy	50%
	Gate – Source Voltage (Vgs)	
	DC voltage only (Working Voltage)	85%
	AC + DC voltage (Operating Voltage)	95%
	Drain – Source Breakdown Voltage (Vds)	
	DC voltage only (Working Voltage)	80%
	AC + DC voltage (Operating Voltage)	95%

Component Type	Parameter	Derating Criteria
Dual Silicon FET (Dual MOSFET)	The same derating criteria applies to Dual FET as for a single FET. The derating on both FETs shall require stress data entry for each one individually.	See Silicon FET derating criteria
Transistor Silicon Bipolar (Silicon Bipolar)	Collector-Emitter Breakdown Voltage (Vce) Maximum Junction Temperature (Tj)	80% 0.75(Tjmax - 25°C) + 20°C
Transistor Gallium Nitride (GaN)	Maximum Junction Temperature (Tj) Avalanche Energy Gate – Source Voltage (Vgs) DC voltage only (Working Voltage) AC + DC voltage (Operating Voltage) Drain – Source Breakdown Voltage (Vds) DC voltage only (Working Voltage) AC + DC voltage (Operating Voltage)	0.75(Tjmax – 25°C) + 20°C 50% 85% 95% 80% 95%
Transistor Silicon Carbide (SiC)	Maximum Junction Temperature (Tj) Avalanche Energy Gate – Source Voltage (Vgs) DC voltage only (Working Voltage) AC + DC voltage (Operating Voltage) Drain – Source Breakdown Voltage (Vds) DC voltage only (Working Voltage) AC + DC voltage (Operating Voltage)	0.75(Tjmax – 25°C) + 20°C 50% 85% 95% 80% 95%
Transistor, GaAs, GaN, PHEMT (GaN)	Breakdown Voltage (Vce or Vds) Maximum Junction Temperature (Tj)	80% 0.75(Tjmax - 25°C) + 30°C
Magnetics		
Transformer (Transformers – Pulse & Power)	Current Surge (% of max rated) Voltage Surge (% of max rated) Current (Continuous) Hot Spot temperature: (measured on hotspot of core surface) For transformers with UL/IEC 62368-1 class rating Class 105 (A) Class 120 (E) Class 130 (B) Class 155 (F) Class 180 (H) For transformers not covered by UL/IEC 62368-1	<100% <100% 90% 90°C 105°C 110°C 130°C 155°C

Component Type	Parameter	Derating Criteria
	Temp below Max Rated Hot Spot	25°C
Inductor Iron Powder (Inductor – Iron Powder Core with Organic binders)	Max peak current (including ripple, transient, and unbalance, where applicable) as % of rated Isat at 100°C defined with -20% inductance roll-off (Excluded are inductors when used in high frequency / noise decoupling applications) Max operating Temperature (measured on hotspot of core surface)	100% Tmax – 35°C
Inductor Ferrite (Inductor – Ferrite Core)	Max operating Temperature (measured on hotspot of core surface) Max peak current (including ripple, transient, OCP and unbalance, where applicable) as % of rated Isat at 100°C defined with -20% inductance roll-off (Excluded are Ferrite Core Inductors – Rod and Bead Type when used in high frequency / noise decoupling applications)	Tmax – 25°C 100%
Inductor Other (Inductor – Other [High-temp powder alloys, Cool-µ, Sendust, MPP, Metaglas, etc.])	Max operating Temperature (measured on hotspot of core surface) Max peak current (including ripple, transient, and unbalance, where applicable) as % of rated Isat at 100°C defined with -20% inductance roll-off (Excluded are inductors when used in high frequency / noise decoupling applications)	Tmax – 25°C 100%
Inductor Wound (Inductor, Wound)	Current Surge (% of max rated) Voltage Surge (% of max rated) Current (Continuous) Temp below Max Hot Spot (measured on hotspot of core surface) Max peak current (including ripple, transient, and unbalance, where applicable) as % of rated Isat at 100°C defined with -20% inductance roll-off (Excluded are inductors when used in high frequency / noise decoupling applications)	85% <100% <100% 90% 100%
Optoelectronics		
LED (Light Emitting Diode)	Average Forward Current Ambient Temperature	90% <100%
Opto Coupler (Optocouplers)	Power Dissipation Current Voltage Maximum Tj	80% 75% 75% 0.75(Tjmax - 25°C) + 20°C

13.2 Life Requirement

The power supply shall support **5 years** calculated life under the following conditions:

- 200-240VAC input
- 55°C inlet temperature
- 100% of the time at 80% load
- Altitude: Sea level

The power supply shall support **7 years** calculated life under the following conditions:

- 200-240VAC input
- 55°C inlet temperature
- 100% of the time at 50% load
- Altitude: Sea level

13.3 Meantime Between Failures (MTBF)

MTBF prediction shall be completed in accordance with Telcordia SR-332, Method 1 Case 3, 40°C.

- Input Voltage: Nominal (HL 200VAC – 240VAC; LL 100VAC – 120VAC)
- 100% average power (Dynamic loading per profile defined in Design Specification)
- Airflow: as specified in the PSU product specification
- Temperature: Maximum operating temperature
- Quality Level II parts required
- Greater than 400K Hours unless otherwise specified in PSU product specification
- Correction factor may be applied with supporting evidence at Reliability Engineer's discretion.

13.4 Reliability Demonstration Test

A Reliability Demonstrated Test shall be conducted as an audit to demonstrate an MTBF goal of 400k hours (or greater if specified by the PSU Product Specification) at 90% Confidence Level using Arrhenius and Chi-Square Statistical methods. Criteria shall be based on new design and/or high-volume products.

- Input Voltage: Nominal (HL $200V_{AC}$ – $240V_{AC}$; LL $100V_{AC}$ – $120V_{AC}$; $277V_{AC}$; $336V_{DC}$)
- Load: 80%
- Power Cycling: 45 minutes On, 15 minutes Off
- Temperature: 55°C
- Sample Size: 100
- Test duration: 64 days
- Monitor output voltages and/or PWOK signal
- Record time to fail when failure occurs

$$MTBF = \frac{2 * t * n * AF}{X^2_{\alpha;2r+2}}$$

Where:

- t = Time required to demonstrate 400,000 hours MTBF.
- n = Number of samples needed to demonstrate a predetermined MTBF target.
- $X^2_{\alpha;2r+2}$ = Chi-square factor, for 0 fail, 90% confidence level, 2 degrees of freedom.
- AF = Arrhenius Acceleration Factor.

$$AF = \left[\frac{RH_{op}}{RH_{test}}\right]^{-n} \left[e^{\left(-E_a/k\right)\left[\frac{1}{T_{test}+273} - \frac{1}{T_{op}+273}\right]}\right]$$

Where:

- AF = The acceleration factor.
- RH_{op} = The relative humidity in the operational environment.
- RH_{test} = The relative humidity in the test environment.
- n = A constant which is determined through testing (Default 2.7).
- E_a = The activation energy and is determined through testing (Default = 1eV/°K). Larger Ea's indicate a higher reliability sensitivity to temperature.
- k = Boltzmann's constant.

- T_{test} = The test temperature (°C).
- T_{op} = The operational temperature (°C).

13.5 Fan Reliability Qualification

- Derating - Electronic Derating for Optimum Performance (RAC)
- Reliability prediction – Telcordia SR-332
- Worst Case Electrical Parts Tolerance Analysis (WCEPTA)
- Fan L10 Bearing Life: 43,200 hours at max system ambient
- Probability Ratio Sequential Test (PRST): 128, 70C, Max RPM, 1000 hours

Figure 13-1 Fan accelerated life test (FALT) profile

- Combined Temperature Humidity Test (refer to TH profile below)
- Design Verification Test (DVT)
  Test shall use 12 random samples with the same bearing, lubricant, and lubricant seal as production level fans. DVT report shall include the following test sequence:
  - RPM, current and dBA measurement – T0
  - Hot /cold and humid storage test (Four corners)
  - RPM, current and dBA measurement – T1
  - Hot /cold operation test (Four corners)
  - RPM, current and dBA measurement – T2
  - Thermal shock test -40oC to 70oC, 50 cycles, 20 minutes dwell time.
  - RPM, current and dBA measurement – T3
  - RPM, current and dBA shall be within the specification at each stage
- Shock and Vibration
  The following tests shall be performed per Fan Shock and Vibration Test Procedure
  - A Non-Operational Vibration test shall be completed.
  - A Non-Operational Half Sine Shock test shall be completed.
  - A Non-Operational Square Wave Shock test shall be completed.

Table 13-2 TH profile

Test	Specification Test Parameter	Margin Test Parameter

Operational Random Vibration	• 0.5 G_{RMS} using break points listed below in *Table 13-3* • All 6 sides tested • 30 minutes per side	N/A
Non-Operational Random Vibration	• 2.2 G_{RMS} using break points listed below in *Table 13-4* • 15 minutes per side • All 6 sides tested	• 3.12 G_{RMS} using break points listed below in *Table 13-5* • 15 minutes per side • All 6 sides tested
Operational Half Sine Shock	• 82 G ±5% with pulse duration of 2 msec ±10% (equivalent to 40 in/sec [102 cm/sec]) • All 6 sides tested	• Increase in **40G** increments until failure or **202G (2ms)**, whichever occurs first • All 6 sides tested
Non-Operational Half Sine Shock	• 142 G ±5% with pulse duration of 2 msec ±10% (equivalent to 70 in/sec [178 cm/sec]) • All 6 sides tested	• Increase in **60G** increments until failure or **322G (2ms)**, whichever occurs first • All 6 sides tested
Non-Operational Square Wave Shock	• 40 G Faired Square Wave w/Velocity Change @ 200 In/Sec [508 cm/sec] or greater • All 6 sides tested	• Increase in **20G** increments until failure or **80G (200in/sec),** whichever occurs first. • All 6 sides tested

Table 13-3 Operational random test 0.5G_{RMS} profile

Frequency (Hz)	G^2/Hz
7	0.00015
20	0.014
140	0.014
312	.000065
400	.000035
600	.000035
800	.000023

Table 13-4 Non-operational random specification test 2.2 G_{RMS} profile

Frequency (Hz)	G^2/Hz
5	0.01
20	0.01
500	0.01

Table 13-5 Non-operational random margin Test 3.12 G_{RMS} profile

Frequency (Hz)	G^2/Hz
5	0.02
20	0.02
500	0.02

13.6 Solder Assembly Qualification

Shall be completed in accordance with Level 2 of Internal Solder-Assembly Reliability Qualification Requirements. The general lead-free qualification procedure is as described below:

1. Obtain component information (BOM, heat resistance, moisture sensitivity level).
2. Obtain printed circuit board assembly (PCBA), solder paste and process information (including measured reflow profile)
3. Ensure board assembly process, profile and factory conditions are compatible with PCB & component specifications.

4. Conduct board (PCBA) level test
    - Assemble boards at specified conditions
    - Perform C-SAM, X-ray on selected components
    - Perform thermal cycling
    - Perform post thermal cycling cross section analysis
5. Compile results and review with Reliability Engineer

PSU suppliers shall conduct a full lead-free qualification at least once per PCBA production site. An ECR need to be submitted for approval if any changes in the production site, solder paste, or re-flow profile.

13.7 Worst Case Electrical Parts Tolerance Analysis

The purpose of a Worst Case Electrical Parts Tolerance Analysis (WCEPTA) is to evaluate the performance of an electrical circuit under expected operating conditions considering component environmental variances, temperature effects, and degradation over product expected lifetime.

Typically for component sources of variation include:

- Initial tolerance
- Temperature Coefficient of Resistance
- Load Life Stability (Aging)
- Short Time Overload
- Effects of Soldering
- Temperature Cycling
- Moisture Resistance (Humidity Exposure)
- Low Temperature Operation
- High Temperature Operation
- Terminal Strength-Bend (Manufacturing Associated Stress)
- Thermal Shock
- Vibration

WCEPTA should be calculated for following parameters:

- Bulk Voltage ← Calculate all set points if Bulk Voltage Modulation is used
- Bulk Voltage OVP
- Main Output Regulation
- STBY Output Regulation
- Main Output OVP, UVP
- STBY Output OVP, UVP
- Main Output OCWPL3
- STBY Output OCP
- Tvout_holdup - calculate from 0% load to 100% load
- Tpwok_holdup - calculate from 0% load to 100% load

Note: When calculating Holdup timings, Capacitance value should be taken at its minimum with considerations to temperature range; Bulk Voltage should be minimum value obtained from WCEPTA; Fan power should be considered in loading and may vary depending on % load.

13.7.1 Circuit Schematic Example

The circuit schematic shown below is for a 1.5V voltage regulation with a specification tolerance of +/-3%; therefore, the lower specification limit is 1.455V and the upper specification limit is 1.545V:

Figure 13-2 Voltage Regulation Circuit

The component assignments for the above circuit are as follows:

- R1: zero Ω jumper, +/-5% initial tolerance
- R2: 2210Ω, +/-1% initial tolerance
- R3: 2490Ω, +/-1% initial tolerance
- R4: 10Ω, +/-1% initial tolerance
- R5: 2210Ω, +/-1% initial tolerance
- R6: 2490Ω, +/-1% initial tolerance
- V feedback: Single Phase PWM Controller, 0.6V, +/-0.8%

13.7.2 Collect Component Datasheets

The analyst must review the current Bill-of-Materials (BOM) to determine which component vendors have been approved for use in the circuit identified for analysis. The WCEPTA will evaluate each of the approved component vendors for suitability of use given the voltage regulation specification limits of +/-3%. In addition, the analyst will confirm that the component nominal values and initial tolerances specified in the schematic are identical to the BOM values for each given reference designator. The component datasheets for the thick film 1/16W resistors are as follows:

13.7.3 Quantify Component Sources of Variation

A compilation of the appropriate component initial and environmental tolerances is required to develop component mean and standard deviation estimates. The product's specified operating range and worst-case component electrical stress analysis (electrical de-rating) are used to determine the temperature

coefficient of resistance (TCR) effects. The de-rating analysis provides the worst-case temperature which in combination with the product's low temperature operating requirements produces a temperature spread or delta. Components identified in the circuit schematic that will be used to develop the circuit transfer function are grouped in a summary matrix. The matrix affords a means of collecting all environmental component variances to develop summary statistics (mean and standard deviation) for each circuit component. *Table 13-6* below illustrates the combined 3σ tolerances.

Table 13-6 Summary of 3σ component tolerances

Reference Designator	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**Vfb**
Part Description	Zero Ohm Jumper	Thick Film Resistor	Thick Film Resistor	Thick Film Resistor	Thick Film Resistor	Thick Film Resistor	Phase PWM Controller
Applicable Parameter	Resistance	Resistance	Resistance	Resistance	Resistance	Resistance	Voltage
Nominal Parameter Value	0.05	2210	2490	10	2210	2490	0.8
Derating Report Component Tc, deg C	77	77	77	77	77	77	77
3 Sigma Sources of Variation							
Initial Tolerance	5.00%	1.00%	1.00%	1.00%	1.00%	1.00%	0.80%
Tolerance of B-value							
Tolerance with VKA variation							
Temp Coefficient (350ppm/C) or 0.035%/C	2.35%						
Temp Coefficient (200ppm/C) or 0.02%/C		1.34%	1.34%	1.34%	1.34%	1.34%	
Temp Coefficient (100ppm/C or 0.01%/C)							
Temp Coefficient (4041ppm/C or 0.4041%/C)							
Long Term Voltage Stability							
Load Life Stability	5.00%	3.00%	3.00%	3.00%	3.00%	3.00%	
Short time overload							
Effect of Soldering	1.00%	1.00%	1.00%	1.00%	1.00%	1.00%	
Temp Cycling	1.00%	1.00%	1.00%	1.00%	1.00%	1.00%	
Moisture Resistance	5.00%	3.00%	3.00%	3.00%	3.00%	3.00%	
Low Temp Operation							
High Temp Operation							
Terminal Strength-Bend	1.00%	1.00%	1.00%	1.00%	1.00%	1.00%	
Thermal Shock							
Vibration							

3σ Total Standard Deviation,	0.0914	0.0488	0.0488	0.0488	0.0488	0.0488	0.0080
1σ	0.0305	0.0163	0.0163	0.0163	0.0163	0.0163	0.0027
1σ in terms of parameter	0.00152	35.93514	40.48801	0.16260	35.93514	40.48801	0.0021

13.7.4 Circuit Transfer Function Determination

For a given circuit under WCEPTA evaluation a mathematical representation of the circuit's output is required in order to conduct a Monte Carlo Analysis (MCA) and assess circuit compliance to specification limits. The formulation of the transfer function (1st order) is the responsibility of the Electrical Engineering Design Team or original equipment manufacturer (ODM), as applicable. For the electrical schematic shown above, the transfer function derivation utilizing Kirchhoff's and Ohm's Law is as follows:

Monte Carlo Analysis (MCA)– Syntax:

```
MTB > Random 5000 'R1';
SUBC>   Normal 0.05 0.00152.
MTB > Random 5000 'R2';
SUBC>   Normal 2210 35.93514.
MTB > Random 5000 'R3';
SUBC>   Normal 2490 40.48801.
MTB > Random 5000 'R4';
SUBC>   Normal 10 0.16260.
MTB > Random 5000 'R5';
SUBC>   Normal 2210 35.93514.
MTB > Random 5000 'R6';
SUBC>   Normal 2490 40.48801.
MTB > Random 5000 'U79';
SUBC>   Normal 0.8 0.0021.
MTB > let c8=(c7/c6)*(c4+c5+c6)+((c7/c6)+(((c7/c6)*(c4+c5+c6))/(c2+c3)))*c1
```

Figure 13-3 Monte Carlo analysis output example

13.7.5 Non-Conforming Circuit

The circuit shown above falls below the required Cpk, Ppk=1.33. Consequently, the overall circuit performance is noncompliant to circuit specification limits. From a visual perspective the circuit is off nominal target with an obvious shift to the right of nominal. The overall circuit performance, in this case, is falling below the lower specification limit and above the upper specification limit. The parts-per-million noncompliant to the lower specification limit is approximately 293 events and above the upper specification limit approximately 32,682 events.

he next step(s):

1. Conduct a sensitivity analysis on the circuit transfer function to affect a component value change (standard value) that would significantly affect the MCA circuit output.
2. Evaluate a +/-1% resistor with tighter environmental tolerances in the circuit, for example, migrating to a 0.5% tolerance passive device.
3. Given the above step(s) do not produce a fully capable circuit, evaluate the use of a tighter initial tolerance resistor with reduced environmental tolerances.
4. In some cases, the active device in the circuit, for example, a precision voltage reference would require a tighter tolerance.
5. All proposed circuit component value, tolerances, etc. changes must be approved by the product electrical engineering (EE) design team prior to implementation.
6. Since the WCEPTA is conducted during the engineering development phase of a product's life cycle some of the active devices suggested for use may have preliminary data sheets. All WCEPTA's must be revised prior to pilot launches with final datasheets.

13.8 Stress Life Test (STRIFE)

Output Overload Test I – OTP enable

1. Sample size = 5 (the test units shall have passed all functional tests)
2. Do not disable any protections. Critical components, all thermal sensors and hot spot areas within the PSU shall be thermo-coupled. (Shall verify IR image)
3. Run the supply at the maximum operating ambient temperature, low AC input voltage, and 100% load for two hours. Evaluate for any functional failures.
4. Repeat the test with a 5% of full load increments until the system shuts down due to OTP or OCP. At each load point, prior to the PSU shutting down, the junction temperature and electrical parameters of each thermo-coupled component shall be verified to ensure all components are within specification. Design team shall provide confirmation of which protection triggered. (OCP and OTP WCEPTAs shall be reviewed and approved prior to start of strife test)

Output Overload Test II – OTP disable

1. Sample size = 5 (the test units shall have passed all functional tests, recommend using the units that went through Output overload test I)
2. Disable all temperature and over current protection circuits
3. Set output load to the point at which the PSU protected itself in line item 4 above. A reduction of load by 10% shall be the starting load for this test.
4. Repeat the test at a 5% incremental rate.

5. When failure occurs, a complete FA shall be performed and provided to the respective reliability and power engineer for review and approval.

Pass / Fail Criteria:

1. All 5 PSU(s) shall be able to operate up to the max OCP 3 sigma limit as calculated from the WCEPTA.
2. Test units that do not meet the max OCP 3 sigma limits shall demonstrate that the failure occurs above the max OTP 3 sigma limits as calculated from the WCEPTA.
3. Vendors shall ensure that prior to OTP or OCP protecting the PSU, all components are below their max rated junction temperature Tj.

Failure Reporting:

Any failures observed for the tests described in this section shall have the following information provided:

1. During what test did the failure occur?
2. What time during the test did the failure occur?
3. What was the failure symptom?
4. What was the failure mode (failure mechanism)?
5. What change(s) could be made to correct the problem? Change(s) to increase design margin shall be evaluated by Power Engineer.

13.9 Reliability Validation

Baseline test a 24-hour bench test at ambient to verify UUT stability shall be performed prior to Reliability Validation testing.

13.10 Temperature Humidity

A Temperature Humidity Test shall be completed in accordance with Internal Procedure.

- Temperature Humidity Test – Includes, operating, non-operating, low and high humidity elements. Operating temperatures (typically 5°C to 45°C) based on product ASHRAE or custom classification. Non-operating temperatures from 65°C @ 8% and 90%RH to -40°C

Figure 13-4 Temperature humidity profile

13.11 Mechanical Life

A Mechanical Life Test shall be completed in accordance with Internal Procedure.

- Mechanical Life Test – All mechanical elements or field replaceable unit (FRU) customer has access to. Cycles based on assembly, deployment, and typical customer utilization models. Supplemental to element, component, or subsystem qualification testing.
- Based on features that are customer can interface. For PSU the most common features are:
  - PSU – 60 Cycles – 4 samples
  - Power Connector – 55 Cycles – 2 samples

13.12 Power Cycling

Power Cycling test shall be completed:

- Input Voltage: Nominal (HL 200VAC – 240VAC; LL 100VAC – 120VAC)
- Load: 100%
- Temperature: A4 Category per Climatic & Airborne Contaminant Specification
- Sample Size: 3
- Test profile: 45 minutes On, 15 minutes OFF
- Test duration: 42 cycles each at high and low temperature
- All samples shall pass functional test before and after power cycling

13.13 Shock and Vibration

The following tests shall be performed per Power Supply Shock and Vibration Test Procedure

Test	Specification Test Parameter	Margin Test Parameter

Operational Random Vibration	• 0.5 G_{RMS} using break points listed below in *Table 13-7* • All Sides except AC connector down • 30 minutes per side	N/A
Non-Operational Random Vibration	• 2.2 G_{RMS} using break points listed below in *Table 13-8* • 15 minutes per side • All 6 sides tested	• 3.12 G_{RMS} using break points listed below in *Table 13-9* • 15 minutes per side • All 6 sides tested
Operational Half Sine Shock	• 82 G +/- 5% with pulse duration of 2 msec +/- 10% (equivalent to 40 in/sec [102 cm/sec]) • All sides except AC connector down	• 122 G +/- 5% with pulse duration of 2 msec +/- 10% (equivalent to 60 in/sec [152 cm/sec]) • All sides except AC connector down
Non-Operational Half Sine Shock	• 142 G +/- 5% with pulse duration of 2 msec +/- 10% (equivalent to 70 in/sec [178 cm/sec]) • All 6 sides tested	• 202 G +/- 5% with pulse duration of 2 msec +/- 10% (equivalent to 100 in/sec [252 cm/sec]) • All 6 sides tested
Non-Operational Square Wave Shock	• 40 G Faired Square Wave w/Velocity Change @ 200 In/Sec [508 cm/sec] or greater • All 6 sides tested	• 60 G Faired Square Wave w/Velocity Change @ 200 In/Sec [508 cm/sec] or greater • All 6 sides tested

Table 13-7 Operational random test 0.5 G_{RMS} profile

Frequency (Hz)	G^2/Hz
7	0.00015
20	0.014
140	0.014
312	.000065
400	.000035
600	.000035
800	.000023

Table 13-8 Non-operational random specification test 2.2 G_{RMS} profile

Frequency (Hz)	G^2/Hz
5	0.01
20	0.01
500	0.01

Table 13-9 Non-operational random margin test 3.12 GRMS profile

Frequency (Hz)	G^2/Hz
5	0.02
20	0.02
500	0.02

14 Regulatory & Ecology Requirements

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability

of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

14.1 Scope

This section covers the design requirements for integral (internal) enclosed power supplies, including hot-swappable supplies for use in servers, networking and storage products with ac or dc or mix mode ac/dc input. This document specifies standard industry requirements for use during the development and/or qualification of internal power supplies.

14.2 EMC Requirements and Standards

The PSU shall be designed, tested, and certified to comply with the latest version of CISPR 32 Emissions standards for Class A or Class B as applicable, CISPR 24 and CISPR 35 Immunity standards, IEC 61000-3-2 or IEC 61000-3-11 Current Harmonics standards, IEC 61000-3-3 or IEC 61000-3-12 Voltage Fluctuations/Flicker standards and applicable national differences.

Test setup and methodology shall address ANSI C63.4 and CISPR standards and note the worst-case where applicable in test reports. It is recommended the certification include applicable country requirements for each country where placed on the market including US CFR Title 47, FCC Part 2 and 15, and Canada ICES-003, and to the standards under the European Union Directive 2014/30/EU.

14.3 Safety Requirements and Standards

The PSU shall be designed, tested, and certified to comply with the latest version of IEC/EN/UL/CSA 62368-1 and applicable national differences.
It is recommended that the PSU shall be certified to the latest national standard based on IEC 62368-1 by the same agency issuing the CB Certificate or at least one EU Notified Body with a factory surveillance program

The following shall be addressed:

a) The declared maximum ambient temperature for safety certification shall not be less than 45 degrees C, including stand-by mode.
b) If the power supply can be removed from the end product without disconnecting the power cord, investigation that no energy hazard (below 240 VA) exists at the PSU outputs in the removed condition shall be considered.
c) When the power supply can be removed from host system without requiring first the removal of the power cord, the power contact receptacle portion of output connectors of removable power supplies must be investigated for the interruption of current in accordance with the Overload, Temperature and Resistance to Arcing Test sequence in UL 1977, the Standard for Component Connectors for Use in Data, Signal, Control and Power Applications in accordance with the output ratings of the power supply.
d) Proper engineering consideration should be made for operation at the altitude as defined for the product. UL 62368-1, 3rd Edition, Clause 5.4.2.5 should be used for creepage and clearance compliance of altitudes higher than 2000 m. Clearances must meet the requirements for an

altitude of 5000 m for use in many countries. NOTE: Creepage distances must not be lower than clearance.

e) For power supplies with a voltage selector switch, abnormal testing of the voltage selector switch should be conducted.
For a power supply rated with dual voltages and with auto range circuitry, a statement in the abnormal test section of applicable regulatory reports that the auto range circuit does not constitute a hazard should be included.

f) Use tropic conditions for humidity conditioning in accordance with IEC 62368-1:2018, clause 5.4.8.

g) The ground continuity must comply with IEC 62368-1:2018, 5.6.6.2. NOTE: Protective Currents > 30A require longer test durations.

h) Output returns must be grounded within the power supply chassis. Outputs cannot be floating and must be referenced to ground.
For dc-dc PSU, the power supply chassis shall also be provided with a grounding terminal, e.g., a metal stud secured to the chassis that is to be connected to dc mains supply earth connection. NOTE: The terminal size must take into account lowest nominal voltage (with tolerance, e.g. 40 VDC) for maximum available current and branch circuit protection, refer to IEC 62368-1:2018, clause 5.6.5. A dc return pin or additional grounding pin integrated in the dc input connector is not acceptable to NEBS.

i) Power supply must include relevant end product testing for system enclosure (e.g. impact, accessibility, fire enclosure vent openings, leakage, and ground bond, etc.), such that Condition of Acceptability (CoA) and/or Engineering Consideration(s) requiring design requirements or testing on the end product is minimized.

j) Because power supplies can be incorporated in a system containing more than one power supply, the following marking shall be provided in the power supply's label in accordance with IEC 60417-6172. Label example is shown below:

Figure 14-1 Multiple input sources IEC 60417-6172 symbol

NOTE:

1. For acoustic requirements, refer to *Section 4 Acoustics and Vibration Requirements.*
2. DC Output voltage power source shall be evaluated, tested, classified, and certified to ES1 output in accordance with applicable national requirements for Information Technology Equipment and complies with IEC/EN/UL 62368-1.

14.4 Fire and Electrical Enclosure

A power supply must provide fire and electrical enclosures. Surface of the enclosure exposed to the user (non-service persons) when installed in the end system must comply with the opening requirements with respect to its orientation (top, side, bottom) as defined in the safety standards of IEC 62368-1, EN 62368-1, and UL/CSA 62368-1.:

1) Minimize the possibility of entry of a foreign object into the power supply and contacting hazardous voltages
2) Minimize the possibility of emission of burning material from the power supply, by using flame-rated materials in accordance with IEC 62368-1:2018, control of fire spread method. NOTE: For NEBS, additional requirement may apply. Refer to GR-63-CORE for smoke and self-extinguishment criteria.

14.4.1 Safeguard Robustness

Enclosures must meet IEC 62368-1:2018 4.4.3 safeguard robustness requirements, including the following:

1) **30 N and 250 N tests**: Tests in accordance with IEC 62368-1, EN 62368-1, and UL/CSA 62368-1 standards shall be conducted and reported in the product safety certification and CB test reports.
2) **Impact test** should be conducted per the IEC 62368-1, EN 62368-1, and UL/CSA 62368-1 standards
3) **Accessibility:** All covers that will serve as enclosures in the end product shall comply with accessibility requirements addressed in IEC 62368-1, EN 62368-1, and UL/CSA 62368-1 standards and comply with various mechanical tests as applicable.

The enclosure shall have the Hot surface label at the AC/DC input side, please refer to Supplemental Material sections for the exact location in the mechanical drawing of each type of power supply.

Figure 14-2 Hot surface label example

14.5 Telecommunications DC Mains Powered Power Supplies

Power supplies to be used in telecommunication applications shall comply with the requirements of IEC 62368-1, EN 62368-1, and UL/CSA 62368-1 standards. An input power of -48 Vdc for USA and Canada and -60 Vdc for EU member countries is used for equipment used in the central office in the telecommunications applications. Under float conditions these voltages may go up to -56.5 Vdc and -75 Vdc respectively.

In addition, the following shall be considered:

1) UL 891: Switchboards
2) CSA C22.2 no. 31: Switchgear Assemblies
3) IEC TR 62102: Electrical safety – Classification of interfaces for equipment to be connected to information and communications technology networks
4) Telcordia GR-1089

Notes:

1. Some customers, such as telecommunication utilities or other customers, may require compliance to NEBS standards specifications. Such requirements should be considered for the specific use for the particular power supply and end product.

NEBS requires that the equipment must be UL certified before the utilities consider it for NEBS evaluation.

14.5.1 Output Grounding Requirements

To facilitate compliance with Telecordia GR-1089, the output returns must be grounded within the power supply chassis. The outputs cannot be floating and must be referenced to ground. For dc-dc PSU, the power supply chassis shall also be provided with a grounding terminal, e.g., a metal stud secured to the chassis that is to be connected to dc mains supply earth connection. A dc return pin or additional grounding pin integrated in the dc input connector is not acceptable to NEBS.

14.6 Components

Any or all of the components listed in this specification may be used in the power supply. Components deemed critical other than those listed in this specification may be used if they meet relevant component standards and are certified per the requirements of the country of use.

14.6.1 Flammability requirements

Minimum flammability ratings for the following components per the test methods in the Annexes of UL/CSA 62368-1 standard.

a) Printed circuit boards, including all daughter cards: V-1 or better.
b) Power connectors on the Motherboards to be V-0 for hot swappable power supplies
c) All other PSU connectors to be V-1 or better

Flammability of other components should be considered for the location and use of the component in accordance with IEC 62368-1:2018. ***NOTE:*** This includes plastic parts.

14.6.2 Capacitors

14.6.2.1 Tantalum Capacitors

Tantalum capacitors are not allowed in the Power Supply.

14.6.2.2 X Type Capacitors and Y Type Capacitors

Line to line or line to neutral X Type capacitors, or line to ground or primary to secondary Y Type capacitors must be certificated to IEC 60384-14 or equivalent national standard and bear the Mark of the certifying agency.

14.6.2.3 X Type Capacitors

X-capacitors must comply with requirements specified in IEC 62368-1:2018, G.11. The voltage rating of X-capacitors must not be less than the rated voltage of the intended end use equipment. The peak impulse test voltage of X-capacitors must not be less than the applicable required withstand voltage.

14.6.2.4 Connectors

Designer must carefully select the connector that has adequate voltage, current and temperature ratings for the intended purpose. The location of the connector within the product will determine the required safety certification requirements. Safety Certification and certifying agency Marks shall be considered depending on the final end product market. If size of the connector allows, the manufacturer should provide required Safety Approval Marks and ratings on each part.

14.6.2.5 Fuses

The designer must use extreme care when selecting the type and V/A-rated fuse to ensure that fuse opens under abnormal conditions. At a minimum, the fuse must be certified to UL and CSA standards as applicable. The following guidelines shall be followed:

- **DO NOT** substitute IEC 60127 (Miniature Fuses)-type fuses for UL 198G (Fuses for Supplementary Overcurrent Protection)-type fuses, or vice versa. They are radically different in blow characteristics.
- For fuses certified to IEC 60127, it is recommended to use high breaking capacity fuses (HBC).
- If fuses are located on a printed wiring board, then the fuse rating must be provided on the PWB via label, silk-screen, stamp or etching. Rating must include voltage, current, and type if the type is special (slow blow, fast blow, etc.).
- Fuse type and rating selection must ensure that the fuse **DOES NOT** blow under normal operating conditions. It is recommended that failure/abnormal conditions be simulated to ensure that the fault current and power source cause the fuse to open. The fuse must not shatter when it opens.

Primary Circuit Fuse: For Pluggable Type A PSUs, the primary circuit fuse of greater than 16-amp rating generally are not permitted.

14.6.2.6 Inductors and Filters

These types of devices are typically located in the power supply in the AC input stage and are designed to filter noise before it can get out of the product. Normally one side is “line” and the other is “neutral.” Ensure the wire size is adequate for carrying the current in normal and abnormal conditions without burning open.

Plastic materials used to provide isolation between the two windings must be able to withstand extreme temperatures without softening or deforming. All headers/bobbins must be molded from UL-recognized plastic with a flame rating of V-1 or better.

Toroid-type inductors must be securely mounted such that the core cannot break loose from base/header during use or shipment. Toroid-type cores must be insulated.

14.6.2.7 Metal Oxide Varistor

All Metal Oxide Varistors (MOVs) used from Line-to-Line must be UL recognized; and comply with IEC 62368-1:2018 Clause 5.5.7 and Annex G.8. Refer to component standards IEC 61051-1 and IEC 61051-2, IEC 61643-331:2017 standards. MOV’s must be properly placed or shielded to prevent a compromise of safety insulation in the event of a failure. A MOV must be selected with a high enough voltage trip point that it cannot operate with the normal variation of input voltage.

MOVs may be connected from mains to protective earth only if a gas discharge tube is connected in series with it or if the protective earth meets the requirements for reliable earthing.

An MOV must not be used to bridge double or reinforced insulation.

14.6.2.8 Plastics Including Foam

Covers plastic and foam parts not used within a critical component otherwise specified within this specification.

Plastic and foam parts should be UL Recognized unless they are decorative only. It is recommended that material identification be molded into all parts that are large enough to bear the markings. An optional method of providing traceability is to print the information on each box or provide a certificate of compliance in each box of parts. Traceability markings include: (a) manufacturer of plastic; (b) UL designation for the plastic; (c) part number and date of manufacture.
It is recommended that a "Certificate of Compliance" be required with each lot for the traceability of plastics.

NOTE: For plastic recycling marking requirements refer to *Section 14.10 Environmental Requirements and Standards.*

Externally Accessible Parts used in GS certified products may also be subject to Polycyclic Aromatic Hydrocarbon requirements per GS specification AfPS GS 2019:01 PAK "Examination and assessment of polycyclic aromatic hydrocarbons (PAHs) for awarding the GS Mark"" and "Supplementation of the PAH Decision 01-08".

Do not use a metal insert or fastener that is 1) molded-in 2) heat or ultrasonically inserted, or 3) glued-in unless the metal component is either separable from plastic parts (Fan impellers are excluded). Do not use adhesive, coating, paint, or finish that impedes recycling (unless plastic part contains at least 25% PCR). (Excluding Printed circuit board, wires, cables, connectors, electronic component, optical component, acoustic component, ESD component and EMI component. If plastic is painted or coated, suppliers shall provide IZOD testing reports.

14.6.2.9 Printed Wiring Boards

All printed wiring boards (PWBs) must be UL-Recognized with a minimum V-1 flame rating and a minimum 105°C temperature rating. It is recommended that PWB's be a minimum V-0 flame rating and a minimum of 130°C temperature rating. Depending on application, the flammability and temperature rating may need to be rated higher.

Each PWB should be marked according to UL approval: manufacturing identification and type designation. During the design of a PWB, consider the voltage between adjacent etch runs ensuring adequate electrical isolation. If etches are too close, arcing, tracking and carbonization of the PWB material might occur.
If the PWB is provided with a fuse location(s), the location must be provided with the reference designator and voltage/current rating of the fuse. PWB assembly suppliers use UL-recognized PWBs.

14.6.2.10 Transformers

Transformers perform step voltage functions and provides electrical isolation between primary circuits and secondary circuits. The transformer must comply with relevant clauses in IEC 62368-1:2018, Clause

5 for isolation from shock as well as the construction and test requirements in IEC 62368-1:2018, Annex G.5.3. The transformer may have UL, CSA and VDE certification depending on the requirements of the power supply certification.

Ensure that the materials do not adversely interact chemically, causing a failure of the insulation. UL has evaluated many combinations of insulating systems for use in transformers. The dielectric of this insulation system is dependent on a maximum temperature rating. If the operating temperature is above class A limits, then the insulation system must be UL recognized. Use a designated mark to identify the UL insulation system.

The manufacturers are required to perform production line (routine testing) dielectric strength tests. Test voltage settings depend on the electrical ratings of the transformer, and whether its construction includes a grounded metal barrier between primary and secondary circuits. Refer to UL Standards or IEC Standards for appropriate test voltages.

Consider electrical isolation concepts when designing a transformer: Creepage distance, clearances, and the distance through insulation and types of insulation (i.e., functional, basic, supplementary, reinforced, and double).

14.6.2.11 Wire and Cable

- **Minimum Rating:** 80°C, 300V (AVLV2) and a minimum flame rating of VW-1
- **Marking:** The wire insulation surface shall depict UL and CSA Approval Marks and required markings: voltage, temperature, AWG, flame- rating, UL File Number and CSA File Number. The spool of wire must have UL and CSA approval marks and the following required markings: voltage, temperature, AWG, flame rating, UL file number, and the CSA file number. The ground conductor shall be as short as possible. In no case shall the ground conductor be smaller than the power supplying conductors, including consideration of conductors' size used in cord-connected equipment.
- **Routing:** Wire and Cable shall be routed away from mechanically moving parts, sharp edges, heat source, and shall be managed to prevent any damage to insulation.
- **Protective Earth (Safety Ground):** Wire used to provide safety ground must be of suitable wire size and jacket color: "Green with Yellow Stripe". NOTE: This color is reserved for use ONLY as "Safety Earth Ground".
- **Fully Insulated Winding wire (FIW):** When FIW is used in transformer construction, it must comply with requirements in IEC 62368-1:2018, G.5.3.4.

14.6.2.12 Wiring Harness

A Wiring Harness is an individual wire or multi-conductor cable that has one or more terminating devices provided (connectors).

- **Material:** During material selection (connectors/wire/cable/insulating tubing or sleeving) designer must consider the application to ensure adequate voltage, current, temperature and flame ratings and appropriate safety agency certifications and meet all Marking requirements

- **Insulating tubing or Sleeving:** Insulating tubing or Sleeving shall be rated at a minimum: 105°C, 300V. The material may be FEP, PTFE, PVC, TFE or Neoprene, and shall have a flame rating of VW-1.
- **Manufacturer Selection:** Manufacturer must have UL Wiring Harness Factory Approval.
- **Routing:** Wire harness shall be routed away from mechanically moving parts, sharp edges, heat source, and shall be managed to prevent any damage to wire/cable insulation, insulating tubing, or sleeving.

14.7 Type Testing

14.7.1 General

All testing for safety and EMC/EMI compliance for the PSU and all critical components where necessary shall be conducted with the relevant test reports issued from a test lab that has been accredited by an internationally recognized third-party testing laboratory accreditation authority such as APLAC, A2LA, ILAC or NVLAP.

14.7.2 Wireless GSM Test

14.7.2.1 Background

The purpose of the test is to evaluate a system's immunity to radiated fields generated by a GSM wireless device (e.g., GSM/GPRS PCMCIA Card) when placed in close proximity to the system under test. This requirement is in addition to the legal requirements set forth in CISPR 35 and IEC 61000-4-3.

The following test method was developed - Wireless Immunity "Wand Test" for this requirement. The "Wand Test" utilizes a small test antenna (Wand Antenna) to create an E-field closely matching the frequency, field level, and modulation characteristics generated by the wireless device in question. The use of the "Wand Test" allows the tester to replicate any of several GSM device transmit frequencies, as well as to replicate the typical maximum output drive that such GSM devices might produce when attempting to communicate with a remote cell tower.

The preferred equipment is:

- Boonton 4232A RF Power Meter
- IFR 2032 10kHz – 5.4 GHz Signal Generator
- Amplifier Research 10S1G4A, 10-Watt (0.8-4.2GHz) Power Amplifier
- HP8566B Spectrum Analyzer (Used for monitoring of field level – not calibrated measurement.)
- Amplifier Research DC7420 Directional Coupler (0.8-18 GHz)
- Boonton 51011(4B) Power Sensors
- Small Vertical Antenna (Log periodic dipole)
- Wireless Immunity "Wand" Antenna

The Wand antenna is a stub antenna which is fixed in length to the wavelength for the frequency band of concern. For the GSM band 850/900 and 1800/1900 bands, the antenna stub length has been set to 8.4 cm, which closely matches the λ/4 and λ/2 wavelengths of these bands, respectively. A 3/8-inch dielectric spacer is placed around the Wand antenna to maintain a consistent spacing during the actual "Wand Test.

The antenna stub portion is created by stripping back the outer shield portion of a semi-rigid coaxial cable and leaving a stub of length as defined above.

The test setup is as illustrated in *Figure 14-3 Wireless Immunity "Wand Test" Setup (PSU Level)* and *Figure 14-4 Wireless Immunity "Wand Test" Setup (External Power Supply)*. *Figure 14-3* is the test setup for a system level test. *Figure 14-4* is the test setup for an external power supply test. The signal generator is set to the signal characteristics as described in the Procedure Section and the forward power is monitored to ensure the correct field level is applied.

Figure 14-3 Wireless Immunity "Wand Test" Setup (PSU Level)

Figure 14-4 Wireless Immunity "Wand Test" Setup (External Power Supply)

14.7.2.2 Procedure

In performance of the "Wand Test", the wand antenna is used to create an E-field to match the frequency, field level, and modulation characteristics generated by a wireless device. The actual forward power applied to the Wand antenna is dependent on the GSM band.

For the GSM 850/900 bands the forward power is set to 5.5-Watts CW.

Test Frequencies:

- GSM 850 – 824, 836, & 849 MHz
- GSM 900 – 880, 900, & 915 MHz

Forward Power: 5.5 Watts (37.4 dBm) CW. (Forward power set without modulation).
Modulation: Pulsed with rep rate at 220 Hz and pulse width at 500 µs (11% Duty Cycle).

For the GSM 1800/1900 bands the forward power is set to 1.5-Watts CW.
Test Frequencies:

- GSM 1800 – 1710, 1750, & 1785 MHz
- GSM 1900 – 1850, 1880, & 1910 MHz

Forward Power: 1.5 Watts (31.8 dBm) CW. (Forward power set without modulation).
Modulation: Pulsed with rep rate at 220 Hz and pulse width at 500 µs (11% Duty Cycle).

Forward power to the wand is initially set without modulation applied. After the proper forward power drive level is established, the modulation is then applied.

Modulation shall be set to pulse modulation with a repetition rate of 220Hz and a pulse width of 500 µs. These levels and modulation characteristics were obtained from both product technical specifications and empirical data taken in the lab.

In general, the Wand antenna is swept across the system/power supply (front, back, sides, top and bottom) in two orthogonal planes and the system is monitored for susceptibility.

14.7.2.3 Severity Levels and Performance Criteria

For System Level Testing:
The system under test should be immune to the frequencies, modulation and field levels listed above. After the test, the EUT shall continue to operate as intended without operator intervention (i.e., Performance Criteria B).

For External Power Supplies:
The performance criteria for the external power supply test is given below:

- Power good signal: Test with PS_ON high (inactive) and low (active). A good signal should not change from high to low or from low to high.
- All DC output voltages: Test with PS_ON low (active). All DC output voltages should stay within the power supply specification.

Environmental Conditions

- The environmental conditions for this testing are the same as specified in EN 61000-4-3:
- Ambient temperature: 15°C to 35°C
- Relative humidity: 30% to 60%
- Atmospheric pressure: 86 kPa (860 mbar) to 106 kPa (1060 mbar)

14.8 Production (Routine) Testing

The test method, test voltage values, and test record requirements are specified in IEC 62911: Audio, video, and information technology equipment – Routine electrical safety testing in production.

14.8.1 Dielectric Strength Testing

If a PSU is dual rated for both AC & DC Mains, the dielectric strength test voltage must use the highest peak voltage specified by the 2 test methods. Additionally, power supply vendor must provide the customer with written confirmation of dielectric withstand test which includes voltage level, duration of test and identification detailing how each power supply is marked to indicate dielectric withstand test had been completed successfully.

14.8.1.1 Dielectric Strength for AC Input Power Supplies

Each unit of production must pass a routine hi-pot test between primary to chassis ground in accordance with EN 62911, Table 1 test voltage for accessible parts connected to protective earth.

If a PSU is intended to be used in an ungrounded system, each unit of production must pass a routine hi-pot test between primary to chassis ground using the test voltage for accessible parts not connected to protective earth.

14.8.1.2 Dielectric Strength for DC Input Power Supplies

Each unit of production must pass a routine hi-pot test between DC Mains supply terminals, tied together, to chassis protective earth connection in accordance with EN 62911, Table 2 test voltage for accessible parts connected to protective earth.

If a PSU is intended to be used in an ungrounded system, each unit of production must pass a routine hi-pot test between DC Mains supply terminals, tied together, to chassis protective earth connection using the test voltage for accessible parts not connected to protective earth.

14.8.2 Ground Continuity Testing

Each unit of production must pass a routine ground continuity test at 25 A for at least 1 s with less than 0.1 ohm from the safety ground (third wire) input pin to the power supply chassis. Each unit must be marked to indicate it.

14.9 Energy Efficiency Requirements and Standards

The power supply must meet the following energy efficiency requirements as applicable for its use. The following are mandatory.

- When referenced in this section, “ErP Lot 3” means the European Union Energy-related Product regulation: EcoDesign Directive 2009/125/EC and Implementing measure (EU) No 617/2013.
- When referenced in this section, “ErP Lot 9” means the European Union Energy-related Product regulation: EcoDesign Directive 2009/125/EC and Implementing measure (EU) 2019/424.

The following standards for transitional methods of measurement are provided for reference (but not all inclusive, for complete details refer to EU publication on transitional methods):

- EN 62623:2013 — Desktop and notebook computers — Measurement of energy consumption:
- EN 50563:2011/A1:2013 - External a.c. — d.c. and a.c. — a.c. power supplies — Determination of no-load power and average efficiency of active modes
- EN 50564:2011 - Electrical and electronic household and office equipment - Measurement of low power consumption IEC 62301:2011 (Modified)

Link: https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=uriserv:OJ.C_.2014.110.01.0108.01.ENG

For Power supplies, standards in the transitional methods include:

- Power Supply Efficiency: EPRI and Ecova - Generalized Test Protocol for Calculating the Energy Efficiency of Internal AC-DC and DC-DC Power Supplies Revision 6.7
- Power Supply Power Factor: EPRI and Ecova - Generalized Test Protocol for Calculating the Energy Efficiency of Internal AC-DC and DC-AC Power Supplies Revision 6.7

NOTE: Testing shall be conducted at an appropriate EU voltage and frequency (e.g. 230v, 50Hz).

Table 14-1 Mandatory regulation requirements

Regulation	Version	Comments
ErP Lot 3		
ErP Lot 9	Tier I or Tier II	
ErP Lot 9	Tier III	For products shipping after the effective date of 1/1/2023
Japanese Energy Law (JEL)	Phase I Implementation, voluntary disclosure	Power supply to support the end product compliance
	Phase II mandatory disclosure	Power supply to support the end product compliance
	Phase III mandatory compliance	Power supply to support the end product compliance For products shipping after the effective date of 4/1/2022

Consider the intended use of the power supply in the final end product to comply with the following voluntary requirements.

Table 14-2 Voluntary regulation requirements

Regulation	Version	Comments
China CEC	-	
China CECP	-	
ENERGY STAR ® [2]	Server 3.0	
EPEAT for servers	NSF-426	Allowable temperature and humidity specifications
Brazil INMETRO	Small scale servers	

Table 14-3 Brazil INMETRO Efficiency Requirements for Internal Power Supplies (tested @ 127V/60Hz)

Small- scale server

Loading Condition (Percentage of Nameplate Output Current)	Minimum Efficiency	Minimum Power Factor
20%	0.82	-
50%	0.85	-
100%	0.82	0.90

Table 14-4 European Union ErP Lot 9 Efficiency Requirements for Internal Power Supplies (tested @ 230V/50Hz)

Computer Servers (1 March 2020) - Computer servers all single output (AC-DC) power supplies							
10% Load		20% Load		50% Load		100% Load	
Efficiency	Power Factor	Efficiency	Power Factor	Efficiency	Power Factor	Efficiency	Power Factor
-	-	90%	-	94%	0.95	91%	-
					-		
Computer Servers (1 January 2023) - Computer servers all single output (AC-DC) power supplies							
10% Load		20% Load		50% Load		100% Load	
Efficiency	Power Factor	Efficiency	Power Factor	Efficiency	Power Factor	Efficiency	Power Factor
90%	-	94%	-	96%	0.95	91%	-
					-		

Table 14-5 ENERGY STAR Requirements for Servers 3.0

ENERGY STAR Servers 3.0 Efficiency Requirements for PSUs					
Power Supply Type	Rated Output Power	10% Load	20% Load	50% Load	100% Load
Single-output (AC-DC)	All Output Levels	83%	90%	94%	91%
ENERGY STAR Servers 3.0 Power Factor Requirements for PSUs					
Power Supply Type	Rated Output Power	10% Load	20% Load	50% Load	100% Load
AC-DC Single-output	Output Rating ≤ 500 W	N/A	0.80	0.95	0.95
	Output Rating > 500 W and Output Rating ≤ 1,000 W	0.65	0.80	0.95	0.95
	Output Rating > 1,000 watts	0.80	0.90	0.95	0.95

Table 14-6 ENERGY STAR Requirements for Data Center Storage 2.0

ENERGY STAR Data Center Storage 2.0 Efficiency Requirements for PSUs				
Power Supply Type	Rated Output Power	20% Load	50% Load	100% Load
Single-output (AC-DC)	All Output Levels	90%	94%	91%
ENERGY STAR Data Center Storage 2.0 Power Factor Requirements for PSUs				
Single-output (AC-DC)	Rated Output Power	20% Load	50% Load	100% Load

Power consumption requirements for the following should be considered as a best design practice as part of an ecolabel.

- Energy efficiency for internal power supplies:
  - 1 full 80 Plus efficiency level above minimum efficiency level U.S. ENERGY STAR specification.
  - 2 full 80 Plus efficiency level above minimum efficiency level U.S. ENERGY STAR specification.
- Make use of energy-efficient components and techniques to reduce power consumption whenever possible.
- Consider low power components and design options as well as efficient power supply components.
- Properly specify the power supply rating to match the loading profile for an energy efficient design.

- Ensure power supplies and components meet requirements for energy efficiency.
- Consider design options to automatically switch from one power mode to another where practical.
- Consider ASIC's and other IC's that have been optimized for low power consumption.
- Consider selection of silicon device technologies noted for higher power efficiencies (CMOS over linear, etc.).
- Keep clock frequencies as low as possible to achieve a given functional task.
- For non-critical impedance circuits, keep bias currents to a minimum (pull-up/down resistors as high as possible for instance).

14.10 Environmental Requirements and Standards

The following is required by law or mandated in ecolabel criteria

- Power supply must comply with applicable restrictions on hazardous substances as referenced in RoHS, REACH, or other environmental and material requirements, including relevant national, regional, and international requirements.
- Consideration must be given to supporting the TCO and EPEAT declarations for the platform level commodities. The power supply must meet all TCO requirements and all EPEAT "Required' criteria at a minimum and any requirements imposed by the platform level declarations. Refer to the latest TCO and EPEAT (NSF-ANSI-426 latest edition) standards for a full list of the requirements.
- Plastic parts exceeding 25 g and printed circuit board laminates shall not contain greater than 1000 ppm chlorine or greater than 1000 ppm Bromine. Reduction of Br/Cl content of plastic parts > 25 grams (Ref EPEAT 6.1.3)
- Halogenated flame retardants and plasticizers - Product housing above 0.5 grams and the power PCB laminate of the internal/external power supply unit must not contain intentionally added (additive or reactive) flame retardants or plasticizers with halogenated substances. Exempted are all other parts, such as electronic components, other PCB laminates and all kinds of cable insulation. Maximum concentration values tolerated for a restricted substance (including decaBDE) is 0.1% by weight of the material in homogeneous materials. (Ref TCO 7.2.1)
- The power supply must not contain Polybrominated biphenyls (PBB), polybrominated diphenyl ethers (PBDE) and Hexabromocyclododecane (HBCDD) (No parts of the product are exempt). (Ref to TCO 7.2.1)
- Non-Halogenated flame retardants - Product housing above 0.5 grams and the power PCB laminate of the internal/external power supply unit must only contain intentionally added (additive or reactive) non-halogenated flame retardants that have been assigned a GreenScreen benchmark score of 2, 3 or 4 by a licensed GreenScreen Profiler and appear on the public TCO Certified Accepted Substance List. All substances of a mixture must be accounted for. Non-accepted substances must not exceed concentration levels of 0.1% by weight of the flame retardant. (Ref TCO 7.3.1)
- Plasticizers – Plasticizers used in product housing and cable insulations must have been assigned a Green Screen benchmark score of 2, 3 or 4 by a licensed Green Screen profiler and appear on the public TCO Certified Accepted Substance List. The product must not contain Bis (2-ethylhexyl) phthalate (DEHP), Butyl benzyl phthalate (BBP), Dibutyl phthalate (DBP), and Di-isobutyl phthalate (DIBP). No parts of the product are exempted. All substances of a plasticizer mixture must be

accounted for. Non-accepted ingredients must not exceed concentration levels of 0.1% by weight of the plasticizer. (Ref TCO 7.4.1)

The following materials are restricted by the EU RoHS Directive (2011/65/EU) and cannot be used in Power Supplies unless used as described in the exemptions.

- Lead and its compounds (0.1% w/w)
- Mercury and its compounds (0.1% w/w)
- Cadmium (0.01% w/w)
- Hexavalent Chromium (0.1% w/w)
- Polybrominated Biphenyls (PBB) (0.1% w/w)
- Polybrominated Diphenyl Ethers (PBDE) (0.1% w/w)
- Bis(2-Ethylhexyl) phthalate (DEHP) (0.1% w/w)
- Benzyl butyl phthalate (BBP) (0.1% w/w)
- Dibutyl phthalate (DBP) (0.1% w/w)
- Diisobutyl phthalate (DIBP) (0.1% w/w)

Plastic parts over 25 grams or 200 mm2 planar area must be labeled according to ISO 11469 standard which includes ISO 1043-1, ISO 1043-2, ISO 1043-3, and ISO 1043-4 standards.

Materials restricted under multiple country RoHS rules include but not limited to
Lead and it compounds – not detectable

Suppliers using chemicals called out in the Montreal protocol should be avoided.

14.11 Applicable RoHS Exemptions

Only the following RoHS exemptions can be used.

Table 14-7 RoHS Exemptions

Exemption Number	Exemption
4(f)	Mercury in other discharge lamps for special purposes not specifically mentioned in this Annex
6(a)-I	Lead as an alloying element in steel for machining purposes containing up to 0.35% lead by weight and in batch hot dip galvanized steel components containing up to 0.2% lead by weight
6(b)-I	Lead as an alloying element in aluminum containing up to 0,4 % lead by weight, provided it stems from lead-bearing aluminum scrap recycling
6(b)-II	Lead as an alloying element in aluminum for machining purposes with a lead content up to 0,4 % by weight
6(c)	Copper alloy containing up to 4 % lead by weight
7(a)	Lead in high melting temperature type solders (i.e., lead- based alloys containing 85 % by weight or more lead)
7(c)-I	Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g., piezo electronic devices, or in a glass or ceramic matrix compound
7(c)-II	Lead in dielectric ceramic in capacitors for a rated voltage of 125 V AC or 250 V DC or higher
13(a)	Lead in white glasses used for optical applications
15(a)	Lead in solders to complete a viable electrical connection between the semiconductor die and carrier within integrated circuit flip chip packages where at least one of the following criteria applies: • • a semiconductor technology node of 90 nm or larger. • • a single die of 300 mm2 or larger in any semiconductor technology node. • • stacked die packages with die of 300 mm2 or larger, or silicon interposers of 300 mm2 or larger.

14.12 Sustainable Materials

Consider the criteria in IEEE 1680.1 (2009 & 2018) & NSF 426 for percentages of Post-Consumer Recycled plastics. The use of post-consumer recycled materials in plastic components is recommended. (Reference EPEAT conformity packets.) Suppliers must provide a declaration when any part contains recycled content or other sustainable material.

The power supply shall support the end product qualification for the TCO process and product sustainability certification for servers. The specific TCO criteria for the end product type is available at:

https://tcocertified.com/files/certification/tco-certified-generation-8-for-servers.pdf
https://tcocertified.com/files/certification/tco-certified-generation-9-for-servers-edition-2.pdf

14.13 EPEAT

Consideration must be given to supporting the EPEAT declaration for the platform level commodities, the power supply must meet the following criteria at a minimum. Refer to the EPEAT criteria for a full list of the requirements.

1) All criteria listed as 'Required' (where applicable for commodities & peripherals – some criteria are at the system level).
2) Power Supply vendors should declare conformance in writing on company letterhead and signed by the appropriate authority within the company.
3) Power supply vendors should make available the EPEAT material declaration template.
4) Power supply vendors should make available upon demand third party Analytical Test Reports from a reputable lab.

14.14 Design for Recyclability

All products shall be designed with the following recyclability elements. Designing products with specific features, materials, or manufacturing processes that support ease of disassembly and reuse, recovery, or recycling efforts can meet these criteria.

The following is required by law or mandated ecolabel criteria

- Ease of disassembly by one person using commonly available tools. (Ref EPEAT)
- Ease of upgrading and/or reuse of original hardware. (Ref EPEAT)
- Ease of separation of different commodity types (i.e., minimizing fused metal-plastic parts). (Ref EPEAT)
- Elimination of molded-in or glued parts. (Ref EPEAT)
- Paints and coating on plastic parts should be compatible with the recycling process (IZOD impact. Reference ASTMD256). (Ref EPEAT)
- All large chassis plastics should be composed of a single plastic type. (Ref EPEAT)
- Information identifying the presence and location of all materials and components that require selective treatment. (Ref EPEAT)

- Mark all plastic components weighing 25 g or more with material code in accordance with ISO 11469:2016 labeling scheme. (Ref EPEAT)
- WEEE Documentation: Demonstrate compliance to EU WEEE directive Article 15 by keeping WEEE End of life Instructions available on a website accessible to recyclers for guidance on the presence of materials and components at the product / family level that need to be removed for treatment including disassembly instructions via owners/service manual. Disassembly instruction must show all parts and material as required per Annex VII of the European WEEE Directive, Directive 2012/19/EU. To meet the NSF 426 standard for Server the WEEE End of life instruction must be kept for at least 7 years following end of products of the product. (Ref EPEAT)

As part of an ecolabel and/or a recommended design practice, all products should be designed considering the following recyclability elements:

- Choose materials which are commonly accepted in recycling programs or are easily recyclable.
- Utilize a modular architecture that allows upgrades or repairs to occur easily.
- Provide ease of access to parts or components containing hazardous materials that should be removed before mechanical processing.
- Minimize adhesive backed materials on recoverable components.
- Post-consumer recycled content of rare earth elements in hard drive(s) in product - Products that contain a hard drive(s) with actuator/voice coil or spindle magnets shall contain 5% or more PCR content neodymium or dysprosium by weight of neodymium or dysprosium in the magnet (Ref EPEAT – NSF 426)

The power supply design and manufacturing processes should support the certification/registration of the end product for the following:

- EU WEEE
- EU RoHS
- EPEAT
- ISO 11469:2016
- China RoHS
- CECP
- China Environment Certification

14.15 Expectation of the Supplier

14.15.1 Change Notification

If the material, component, assembly, or product being supplied to the purchaser does not meet one or more of the applicable requirements of this specification, the supplier must immediately notify the purchaser. This notification also applies if the supplier or a subcontractor(s) makes changes in their operations that will cause a material, component, assembly, or product to no longer comply with this specification.

If a restricted substance is used in a nonexempt application above the threshold limit, the following actions may be required to resolve any deviations from this specification:

- Requalification of parts to comply with specification/ phase out and replacement of use, which may result in removal of non-compliant suppliers from the approved vendors list.
- Delay of product launch
- Stop ship of product to affected regions

14.15.2 Required Documentation

The supplier shall provide copies of the latest version of the following items submitted to End-User upon request:

- All agency approval certificates and supporting test reports for EMC, Harmonics, Energy and Product Safety
- UL Descriptive and CB Test Reports
- List of any End User approved Conditions of Acceptability (CoA). While CoA are expected to be detailed in the UL report , this list is the documentation showing End User sign-off and approval/acceptance of the PSU CoA.
- Schematics
- BOM (Bill of Material)
- Copy of the PSU label

Note: A non-disclosure agreement between the supplier and end-user company is required before sharing of confidential information.

14.15.3 Regulatory Model Designation

PSU vendors shall utilize a separate Regulatory Model designation for their PSU and should not use their manufacturer part designation/ marketing name/ etc for Regulatory Agency certification purposes. The Regulatory Model designation should not change due to non-Regulatory/ Safety design related features such as firmware updates, etc.

The Regulatory Model designation may include variables, e.g. XXYYZZ to preserve possible Regulatory concerned changes, and the naming scheme shall be approved by the End User Regulatory staff.

14.16 Compliance Certifications

The power supply shall comply with the following safety and EMC/EMI agency approvals.

Table 14-8 Country approval and marking requirements

Country	Agent/Agency	Certification Requirement M=Mark C=Cert [a)] D=DoC	Deliverables C=Cert [a)] D=DoC	Comments
Australia/NZ	ACA	M, D	D	Hot Swappable power supplies that are offered as Customer orderable kits require agency certification and marking. Also applies to internal power supplies if shipped as customer orderable kit or spare parts.
Canada	SCC Accredited Agency (Safety)	M, C	C	
Canada	ISED (EMC)	M, D	D	

Country	Agent/Agency	Certification Requirement M=Mark C=Cert [a)] D=DoC	Deliverables C=Cert [a)] D=DoC	Comments
China	CNCA (Safety, EMC)	M, C	C	China does not require safety certifications for PSUs rated more than 6A but CQC quality mark is required.
European Union	CE (Safety, EMC)	M, D	D	CE Marking. For Class A PSU, the label shall also state "WARNING: Operation of this equipment in a residential environment could cause radio interference"
International CB certificate and report	NCB (Safety)	CB report and certificate	C, CB report	
European Certification Agency with factory surveillance	NCB (Safety)	M,C	C	Recommended to use the same agency issuing the CB Certificate. Must have a factory surveillance program.
India	BIS (Safety)	M, C	C, BIS report	Apply to power supply used for the host systems in BIS scope (e.g. server, storage, workstation, AIO, etc.)
Morocco	Morocco (Safety, EMC)	M, D	D	Morocco DoC based on Safety and EMC is required for PSUs.
Korea, Republic of (South Korea)	KC certification (EMC, Safety) EMC – MSIP, Ministry of Science, ICT, and Future Planning	M, C	C	KC mark for EMC applies to Hot Swappable power supplies offered as Customer orderable kits. KC mark for safety applies to power supplies if shipped as customer orderable kit or spare parts.
Eurasia Economic Commission (EEC) (Armenia, Belarus, Kazakhstan, Kyrgyzstan and Russian Federation)	Eurasia Economic Commission (EEC) AKA Customs Union mark and certificate (Safety, EMC)	M, C	C	Hot Swappable power supplies that are offered as Customer orderable kits require agency certification and marking. Also applies to internal power supplies if shipped as customer orderable kit or spare parts.
Taiwan	BSMI (Safety, EMC)	M, C	C	A dc-to-dc power supply does not require BSMI approval. NOTE: Mixed mode high voltage DC PSU that may operate with either an ac or dc input is required to obtain BSMI approval.
Ukraine		M, C, D	C, D	Hot Swappable power supplies that are offered as Customer orderable kits require agency certification and marking. Also applies to internal power supplies if shipped as customer orderable kit or spare parts.
United Kingdom	UK CA (Safety, EMC)	M, D	D	UK CA Marking. For Class A PSU, the label shall also state "WARNING: Operation of this equipment

Country	Agent/Agency	Certification Requirement M=Mark C=Cert [a] D=DoC	Deliverables C=Cert [a] D=DoC	Comments
				in a residential environment could cause radio interference"
United States	NRTL (Safety)	M, C	C	
United States	FCC (EMC)	M, D	D	The 2-part FCC statement on all PSU.

[a] Pursuant to respective Agency certification requirements, it can be CoC (certificate of compliance); LoA (letter of authority); PC: product certificate; RC: Registration certificate; TER: Technical Evaluation Report.

NOTES:

1) The Korea KC-Safety regulates PSU Safety certification installed in a Server. For example:
   a) If PSU is used for server and storage at the same time, it is under KC-Safety scope.
   b) If PSU is used for storage only, it is not under KC-Safety scope.
2) Korea MSIP (KC-EMC), regulates certification if a PSU is sold alone, separate from the system, regardless of the end-system that the PSU is used for. For example:
   a) Factory installed PSUs used for server, network switch or storage are certified with MSIP (KC-EMC) as a component of the host system. PSUs that are shipped for service purpose of host are exempted to pursue KC-EMC certificate on PSU.
   b) PSU used for desktop, workstation, server, network switch or storage that are certified with MSIP (KC-EMC) as a component of the host system and are marketed/sold/shipped separately from the host system as spare part or expansion part shall have its own KC-EMC certificate for the PSU.
   c) For any redundant or hot-swappable PSU must obtain KC-EMC certification
   d) PSU's intended for use in server and shipped separately as spare parts must have the KC Safety certification and marking

15 Quality Assurance

15.1 Vendor Responsibility

When the power supply vendor takes orders for units to this specification, this vendor then assumes the responsibility of maintaining a standard of quality that meets or exceeds that of units originally qualified in the Design Verification Test.

15.1.1 General

The power supply manufacturer shall establish and maintain an effective quality program, to be submitted and approved by the customer, which will assure adequate quality in all phases of design, procurement, fabrication, and test of power supplies procured in accordance with this specification. The manufacturer shall provide to the customer with all quality program data upon request.

15.1.2 Scope

The power supply manufacturer's quality program shall control all aspects of the acquisition, inspection, storage, and handling of all materials, and the process of fabrication, assembly, test and inspection, packaging, and shipment of power supply assemblies. The program should include, but not be limited to the following elements:

1. Change control of drawings and specifications.
2. Review and control of procurement of parts, materials, and services.
3. Control of vendor/supplier quality.

4. Inspection and test of received parts and materials.
5. Control of non-conforming materials.
6. Material review.
7. Calibration control of tools, gauges, and test equipment.
8. In-process control of test and manufacturing processes.
9. Failure/non-conformance detection, analysis, and correction.
10. Inspection/Test planning.
11. Final inspection/test.
12. Control of packaging and packing.
13. Workmanship standards in conformance with customer's requirements.
14. Corrective action program.

The vendor documentation will be evaluated by The customer to ensure that the documentation is complete and accurate. The power supply will not be fully qualified until the customer approves the documentation. The vendor may be provisionally qualified pending customer's documentation approval. The vendor must provide updated information that accurately reflects any changes or modifications to the power supply.

15.2 Inspection

15.2.1 Responsibility for Inspection/Test

The power supply manufacturer is responsible for performing all inspections and tests required to verify conformance of the power supply to the requirements of this specification.

15.2.2 Inspection and Test Procedure

Inspections or tests which are required to verify that the performance of the power supply assembly complies with the performance requirements of this specification. The customer must approve these procedures prior to incorporating the procedures for production power supply inspection or test. Approval of procedures will include approval of any special test equipment used to verify conformance to the requirements of the specification.

15.2.3 Qualification Inspection/Test Procedures

When qualification is required, the power supply manufacturer will prepare a detailed procedure for the qualification of the power supply to be produced in conformance with this specification. The procedure will specify the test routines, test conditions, number of test units, and duration of tests, test data to be recorded, and the criteria for establishing qualification of the power supply. Qualification procedures are subject to approval by the customer prior to beginning the qualification program.

15.2.4 Acceptance Inspection/Test

The power supply manufacturer shall prepare a detailed procedure specifying the inspection and test routines that will verify that each production power supply conforms to the performance requirements of this specification. The acceptance procedure is subject to approval by the customer. The customer reserves the right to 100% screening or testing for lot acceptance/rejection based upon sampling per MIL-STD-105K, LEVEL II, per parameters specified in paragraphs 3 through 9 of this specification.

15.3 Final Test Data

The vendor shall ship final test data with each supply until full product qualification.

15.4 Rejection and Retest

Failure of a power supply during acceptance testing to comply with the requirements of this specification shall be cause for rejection. Rejected items will be returned to the vendor for full credit. Rejected items may be reworked and retested for acceptance.

15.5 Corrective Action Program

The power supply manufacturer shall prepare and maintain a corrective action program to be approved by The customer, for the correction of incoming inspection, in process, and field problems when failures are in excess of 0.2%.

15.6 Failure Analysis

The power supply vendor shall provide failure analysis data on all units returned. All units returned to the vendor, shall be at full credit.

15.7 Vendor Burn-In

Minimum initial operating burn-in at 40°C ± 5°C and maximum load is to be included as part of the power supply manufacturing program. The customer may permit fewer hours upon mutual agreement. The customer may require a longer burn-in on a new product. Burn-in must be followed by a final test and inspection. Final test shall include functional, Hi-pot, ground continuity, and AC polarity testing of 100% of units after burn-in.

15.8 Enhanced Burn-In

Enhanced Burn-In test must be performed by vendor in stages EVT & DVT as mandatory and in PVT stage when is required using the following conditions:

AC input	230-240VAC
Temperature	40°C
AC cycling and DC cycling	1 per minute
Slow slew rate dynamic loading (case 1)	D = 50%; Load 0% -100% (5sec at zero, 5 sec –ramp up to 100%, 5 sec at 100%, 5 sec – ramping down)
Fast slew rate dynamic loading (case 2)	D = 50% load 0-60%; 40-100% di/dt=max
Run time	4 hours each condition
Pass criteria	no PWOK de-assertion whenever AC is applied and PSON is asserted

Figure 15-1 AC/DC input cycling pattern.

Figure 15-2 Slow slew rate dynamic loading.

Figure 15-3 Fast slew rate dynamic loading, case 1.

Figure 15-4 Fast slew rate dynamic loading, case 2.

15.8.1 Preparation for Delivery

Each power supply shall be packaged to enable damage-free shipping and handling by commercial carriers to assure safe delivery to the customer facilities worldwide.

Supplemental Material A. 185mm by 73.5mm M-CRPS mechanical drawing

3 INSULATOR TO BE APPLIED TO THE REAR SHEET METAL SURFACE WITH ADHESIVE AND COVER EXPOSED REAR SHEET METAL AS SHOWN.
A. MATERIAL: FORMEX GK-5 SERIES POLYPROPYLENE SHEET OR APPROVED EQUIVALENT.
B. COLOR: PATONE 877 SILVER.
C. PRIMARY SUBSTRATE MINIMUM THICKNESS TO BE 0.13MM (0.0005"). THIS DOES NOT INCLUDE ADDITIONAL LAMINATE.
D. THERMAL TRANSFER COEFFICIENT 1.0 OR LESS.
E. MATERIAL TO BE RATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS TEMPERATURE.
F. ADHESIVE TO BE TREATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS ENVIRONMENT ON SHEET METAL SURFACE.
G. MATERIAL AND ADHESIVE TO BE UL RECOGNIZED AND MEET THE REQUIREMENTS OF UL 94 V-0 OR 94 VTM-0 AND UL 746D.
REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 09/05/2022 CTA
- 2 DRAWING UPDATED ACORDING WITH THE REFERENCE OF THE VENDOR 03/06/2023 AURELIO R.
- 3 -THE THICKNESS OF THE BOARD WAS CHANGE FROM 1.60mm TO 1.57mm -KOZ IS INCLUDED IN THE BOTTOM OF THE BOARD -NEW HANDLE AND EMBOSS IS INCLUDED IN THE DESIGN. -DESIGN UPDATED FOR RELEASE SPEC 1.1 06/26/2023 CTA
- 4 DIMENSION AND NOTES ARE UPDATED ACORDING WITH LAST REVISION. 07/19/2023 CTA
- 5 MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC 08/18/2023 CTA
- 6 MODEL UPDATED ACORDING WITH THE M-CRPS 1.04 SPEC 02/09/2024 CTA
- 7 MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC 08/13/2024 CTA
40 FAN
WATTAGE LABEL SPEC
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
1.7 LATCH TO AC SOCKET
4.8 LED
2MM MAXIMUM CHASSIS PIN HEIGHT
KOZ BOARD RESTRICTION -BOTTOM-
SECTION A-A
HOT SURFACE LABEL 60417-1-IEC-5041
185.0
33.5 (40.1mm TALL AREA)
30.1 [THE FAN LOCATION MUST NOT EXCEED THE DIMENSION INDICATED]
1.3
0.60
40 FAN
SPEC
65.74±0.2
188.4±0.35
SEE DETAIL A
2.16 EMI SPRING
2X 0.800
40±0.5 RAMP
12.00
12.00
THUMB GRIP FEATURES
(28.63)
4.00
20.5
2.00
39±0.4
16.05±0.5
8.5±0.2
1.57±0.13
Ø5
16.50±0.25
11.00±0.25
14.34±0.25
7 MIN
55.68
19 MAX
2MM MAX CHASSIS PIN HEIGHT
SECTION A-A
CONTINUOUS SHEARED EDGE
(NO EMBOSSING OR OTHER FEATURE THAT DISTORTS THE EDGE IS ALLOWED)
CHAMFER 0.3mm FOR PSU BOTTOM HOUSING
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
7.1
34.66
LED PIPE HANDLE
73.5±0.4
1 FAN MUST BE EQUAL TO OR LOWER THAN THE SHEET METAL RAMP FORM AFTER ASSEMBLY
2. MATERIAL: 0.8mm MIN. THK +/- 0.08mm GALVANIZED STEEL. JIS G3302 SGCC Z08 SKIN PASSED MINIMUM OR NO SPANGLE. CHROMATE TREATED CHEM. TREAT DRY (NO OIL), 50-65 ROCKWELL B.
OR
JIS G3302 SGCC Z08, CHROMATE-FREE ANTI-FINGER PRINT TREATED. 50-65 ROCKWELL B, SMOOTH FINISH (SKIN PASS), NO OIL. CONDUCTIVITY - SURFACE RESISTANCE <1.0 MΩ AS MEASURED ACCORDING TO MITSUBISHI LORESTA MCP T350, ASP-PROBE.
PLACE WARNING LABEL WITH SYMBOL 60417-1-IEC-5041 WITH EMBOSS
LABEL MUST HAVE YELLOW BACKGROUND WITH BLACK TEXT
EMBOSS LOCATION AND SIZE MUST MATCH DATABASE AND WARNING LABEL MUST FIT WITHIN EMBOSS (GAP=0.2MM REF. EMBOSS DEPTH=0.2MM)
THE LABEL POSITION AND LABEL SIZE WILL BE BASED ON DESIGN OF EACH VENDOR AND NEED TO APPROVED
R1
8.5
7.6
2.75±0.2
DETAIL A SCALE 1.500
TOLERANCES (MM):
X.X ± 0.50
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_TA_73_5_REP_TA
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 09/05/2022
DRAWN BY C. TERRIQUEZ DATE 09/05/2022
CHECKED BY A. RODRIGUEZ DATE
APPROVED BY DATE
MATERIAL SEE NOTES FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS MECHANICAL SPEC PSU 73.5mm
SIZE A2 DRAWING NUMBER REV 7
SCALE: NONE DO NOT SCALE DRAWING SHEET 1 OF 5

SPEC
12V OUTPUT
REGULAR AIRFLOW
16.50±0.25
11.00±0.25
ø5
2X 30°
14.34±0.25
55.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
7
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 2 OF 5

SPEC
12V OUTPUT
REVERSED AIRFLOW
Ø5
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
7
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 3 OF 5

SPEC
Ø5
2X 45°
25.00±0.2
11.00±0.2
16.50±0.25
11.00±0.25
2X 30°
14.34±0.25
55.68
2X 5.20
54V OUTPUT
REGULAR AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
7
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 4 OF 5

SPEC
Ø5
2X 45°
25.00±0.2
11.00±0.2
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
54V OUTPUT
REVERSED AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
7
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 5 OF 5

Supplemental Material B. 185mm by 60mm M-CRPS mechanical drawing

REVISION HISTORY
ZONE | REV | DESCRIPTION | DATE | APPR
- | 1 | INITIAL DRAWING RELEASE | 09/06/2022 | AURELIO R.
- | 2 | DRAWING UPDATED ACORDING WITH THE REFERENCE OF THE VENDOR | 03/06/2023 | AURELIO R.
- | 3 | -THE THICKNESS OF THE BOARD WAS CHANGE FROM 1.60mm TO 1.57mm -NEW HANDLE AND EMBOSS IS INCLUDED IN THE DESIGN. -DESIGN UPDATED FOR RELEASE SPEC 1.1 | 06/26/2023 | CTA
- | 4 | DIMENSION AND NOTES ARE UPDATED ACORDING WITH LAST REVISION. | 07/19/2023 | CTA
- | 5 | MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC | 08/18/2023 | CTA
- | 6 | MODEL UPDATED ACORDING WITH THE M-CRPS 1.03 SPEC | 11/28/2023 | CTA
- | 7 | MODEL UPDATED ACORDING WITH THE M-CRPS 1.04 SPEC | 02/09/2024 | CTA
- | 8 | MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC | 08/26/2024 | CTA
40.1 FAN
ALL VENT OPENINGS TO BE OPTIMIZED BY VENDOR
WATTAGE LABEL SPEC
1.7 LATCH TO AC SOCKET
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
4.4 LED
8.6 LED
HOT SURFACE LABEL 60417-1-IEC-5041
185.0
59.51 (THE FAN LOCATION MUST NOT EXCEED THE DIMENSION INDICATED)
0.60
33.86 (40.1mm TALL AREA)
2.91±0.3
40 FAN
SPEC
57.09±0.2
188.4±0.35
SEE DETAIL A
60±0.4
2.16 EMI SPRING
121.86±0.3 HARD STOP
2X 0.800
R0.5±0.2
11±0.3
39.9±0.25 HARD STOP
40.1±0.5 RAMP
12.00
39.9±0.25
100°±2°
2.00
39±0.4
16.05±0.5
8.5±0.2
2MM MAXIMUM CHASSIS PIN HEIGHT KOZ BOARD RESTRICTION -BOTTOM-
THUMB GRIP FEATURES
1.57±0.13
SECTION A-A
4.00
(28.63)
20.5
Ø5
16.50±0.25
11.00±0.25
14.34±0.25
2MM MAX CHASSIS PIN HEIGHT
SECTION A-A
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
7.1
CONTINUOUS SHEARED EDGE (NO EMBOSSING OR OTHER FEATURE THAT DISTORTS THE EDGE IS ALLOWED)
7 MIN
19 MAX
45.66
CHAMFER 0.3mm FOR PSU BOTTOM HOUSING
34.66
LED PIPE HANDLE
1 FAN MUST BE EQUAL TO OR LOWER THAN THE SHEET METAL RAMP FORM AFTER ASSEMBLY
2. MATERIAL: 0.8mm MIN. THK +/- 0.08mm GALVANIZED STEEL. JIS G3302 SGCC Z08 SKIN PASSED MINIMUM OR NO SPANGLE. CHROMATE TREATED CHEM. TREAT DRY (NO OIL), 50-65 ROCKWELL B.
OR
JIS G3302 SGCC Z08, CHROMATE-FREE ANTI-FINGER PRINT TREATED. 50-65 ROCKWELL B, SMOOTH FINISH (SKIN PASS), NO OIL, CONDUCTIVITY - SURFACE RESISTANCE <1.0 MΩ AS MEASURED ACCORDING TO MITSUBISHI LORESTA MCP T350, ASP-PROBE.
PLACE WARNING LABEL WITH SYMBOL 60417-1-IEC-5041 WITH EMBOSS LABEL MUST HAVE YELLOW BACKGROUND WITH BLACK TEXT EMBOSS LOCATION AND SIZE MUST MATCH DATABASE AND WARNING LABEL MUST FIT WITHIN EMBOSS (GAP=0.2MM REF, EMBOSS DEPTH=0.2MM) THE LABEL POSITION AND LABEL SIZE WILL BE BASED ON DESIGN OF EACH VENDOR AND NEED TO APPROVED
R1
8.5
2.75±0.2
7.6
DETAIL A SCALE 2.000
TOLERANCES (MM):
X.X ± 0.50
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_REP_60MM
QTY | ITEM NO | PART NUMBER | DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 09/06/2022
DRAWN BY C. TERRIQUEZ DATE 09/06/2022
CHECKED BY AURELIO R. DATE
APPROVED BY DATE
MATERIAL SEE NOTES
FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS MECHANICAL SPEC PSU 185mm X 60mm
SIZE A2
DRAWING NUMBER
REV 8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 1 OF 5

SPEC
12V OUTPUT
REGULAR AIRFLOW
16.50±0.25
11.00±0.25
Ø5
2X 30°
14.34±0.25
45.66
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 2 OF 5

SPEC
12V OUTPUT
REVERSED AIRFLOW
Ø5
16.50±0.25
11.00±0.25
29.34±0.25
2X30°
30.66
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 3 OF 5

SPEC
11.00±0.20
Ø5
2X 45.2°
25±0.2
16.50±0.25
11.00±0.25
Ø5
2X30°
14.34±0.25
45.66
2X 5.20
54V OUTPUT
REGULAR AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 4 OF 5

SPEC
11.00±0.20
Ø5
2X 45.2°
25±0.2
16.50±0.25
11.00±0.25
Ø5
29.34±0.25
2X 30°
30.66
2X 5.20
54V OUTPUT
REVERSED AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 5 OF 5

Supplemental Material C. 265mm by 73.5mm M-CRPS mechanical drawing

REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 09/06/2022 CTA
- 2 DRAWING UPDATED ACORDING WITH THE REFERENCE OF THE VENDOR 03/06/2023 AURELIO R.
- 3 -THE THICKNESS OF THE BOARD WAS CHANGE FROM 1.60mm TO 1.57mm -KOZ IS INCLUDED IN THE BOTTOM OF THE BOARD -NEW HANDLE AND EMBOSS IS INCLUDED IN THE DESIGN. -DESIGN UPDATED FOR RELEASE SPEC 1.1 06/26/2023 CTA
- 4 DIMENSION AND NOTES ARE UPDATED ACORDING WITH LAST REVISION. 07/19/2023 CTA
- 5 MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC 08/18/2023 CTA
- 6 MODEL UPDATED ACORDING WITH THE M-CRPS 1.04 SPEC 02/09/2024 CTA
- 7 MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC 08/26/2024 CTA
60.9
(40.1mm TALL AREA)
56.8 [THE FAN LOCATION MUST NOT EXCEED THE DIMENSION INDICATED]
265.0
0.60
HOT SURFACE LABEL 60417-1-IEC-5041
40 FAN
WATTAGE LABEL SPEC
1.1 LATCH TO AC SOCKET
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE
4.8 LED
SEE DETAIL A
SPEC
65.74±0.2
73.5±0.4
268.4±0.35
3.48±0.15
2.16 EMI SPRING
2X 0.800
1
FAN MUST BE EQUAL TO OR LOWER THAN THE SHEET METAL RAMP FORM AFTER ASSEMBLY
2. MATERIAL: 0.8mm MIN. THK +/- 0.08mm GALVANIZED STEEL. JIS G3302 SGCC Z08 SKIN PASSED MINIMUM OR NO SPANGLE. CHROMATE TREATED CHEM. TREAT DRY (NO OIL), 50-65 ROCKWELL B.
OR
JIS G3302 SGCC Z08, CHROMATE-FREE ANTI-FINGER PRINT TREATED. 50-65 ROCKWELL B, SMOOTH FINISH (SKIN PASS), NO OIL. CONDUCTIVITY - SURFACE RESISTANCE <1.0 MΩ AS MEASURED ACCORDING TO MITSUBISHI LORESTA MCP T350, ASP-PROBE.
40.1±0.5 RAMP
12.00
12.00
2.00
39±0.4
16.05±0.5
8.5±0.2
1.57±0.13
2MM MAXIMUM CHASSIS PIN HEIGHT
KOZ BOARD RESTRICTION -BOTTOM-
SECTION A-A
THUMB GRIP FEATURES
4.00
(28.63)
20.5
16.50±0.25
Ø5
11.00±0.25
14.34±0.25
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
7.1
2MM MAX CHASSIS PIN HEIGHT
SECTION A-A
7 MIN
19 MAX
55.68
34.66
LED PIPE HANDLE
CONTINUOUS SHEARED EDGE
(NO EMBOSSING OR OTHER FEATURE THAT DISTORTS THE EDGE IS ALLOWED)
CHAMFER 0.3mm FOR PSU BOTTOM HOUSING
PLACE WARNING LABEL WITH SYMBOL 60417-1-IEC-5041 WITH EMBOSS
LABEL MUST HAVE YELLOW BACKGROUND WITH BLACK TEXT
EMBOSS LOCATION AND SIZE MUST MATCH DATABASE AND WARNING LABEL MUST FIT WITHIN EMBOSS (GAP=0.2MM REF, EMBOSS DEPTH=0.2MM)
THE LABEL POSITION AND LABEL SIZE WILL BE BASED ON DESIGN OF EACH VENDOR AND NEED TO APPROVED
R1
8.5
7.6
2.75±0.2
DETAIL A
SCALE 1.700
TOLERANCES (MM):
X.X ± 0.5
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
QTY ITEM NO PART NUMBER DESCRIPTION
TOP M-CRPS_73_5MM_265MM_TA M-CRPS MECHANICAL SPEC PSU 73.5MM X 265MM
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 09/07/2022
DRAWN BY C. TERRIQUEZ DATE 09/07/2022
CHECKED BY AURELIO R. DATE
APPROVED BY DATE
MATERIAL SEE NOTES FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS MECHANICAL SPEC PSU 73.5MM X 265MM
SIZE A2 DRAWING NUMBER REV 7
SCALE: NONE DO NOT SCALE DRAWING SHEET 1 OF 5

SPEC
12V OUTPUT
REGULAR AIRFLOW
16.50±0.25
11.00±0.25
Ø5
2X 30°
14.34±0.25
55.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
7
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 2 OF 5

SPEC
12V OUTPUT
REVERSED AIRFLOW
Ø5
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
7
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 3 OF 5

SPEC
Ø5
2X 45°
25±0.2
11.00±0.2
Ø5
16.50±0.25
11.00±0.25
2X 30°
14.34±0.25
55.68
2X 5.20
54V OUTPUT
REGULAR AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
7
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 4 OF 5

SPEC
Ø5
2X 45°
25±0.2
11.00±.20
Ø5
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
54V OUTPUT
REVERSED AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
7
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 5 OF 5

Supplemental Material D. 73.5mm in width M-CRPS card edge mechanical drawing

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	1	INITIAL DRAWING RELEASE	08/19/2022	CTA
-	2	THE GOLD FINGERS ARE UPDATED ACORDING WITH THE ELECTRICAL REQUIREMENT	08/24/2022	CTA
-	3	SOME DIMENSION ARE INCLUDED IN THE FINAL REVISION, SHEET 1 AND 3	08/31/2022	CTA
-	4	THE THICKNESS OF THE BOARD WAS CHANGE FROM 1.60mm TO 1.57mm	05/08/2023	CTA
-	5	MODEL UPDATED FOR THE SPEC RELEASE 1.01	06/26/2023	CTA
-	6	GOLD CONTACT, TOLEANCE AND DIMENSIONS ARE UPDATED ACORDING WITH THE LAST REFERENCE.	07/19/2023	CTA
-	7	MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC	08/18/2023	CTA

TOP VIEW

PARTS LIST

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	M-CRPS_CARD_EDGE_73_5MM	M-CRPS_CARD_EDGE_73.5mm

TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY	C. TERRIQUEZ	DATE	03/30/2022
DRAWN BY	C. TERRIQUEZ	DATE	08/24/2022
CHECKED BY	A. RODRIGUEZ	DATE	
APPROVED BY		DATE	
MATERIAL	SEE NOTES	FINISH	SEE NOTES

DEPARTMENT

TITLE: CRPS_CARD_EDGE 73.5mm

SIZE: A3 | DRAWING NUMBER | REV: 7

SCALE: NONE | DO NOT SCALE DRAWING | SHEET 1 OF 3

SEE DETAIL B
BOTTOM VIEW
19.16
41.5
42.02
64.36
65.74
1.75
1.25
SCALE 2.200
11.00
1.10
3X 1.75
3X 2.25
2.39
17.63
7X 1.5±0.05
6X 2.54±0.05
DETAIL B
SCALE 3.200
TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°
DEPARTMENT
SIZE A3
DRAWING NUMBER
REV 7
SCALE:NONE
DO NOT SCALE DRAWING
SHEET 2 OF 3

GOLD CONTACT

SCALE 4.000

PLATING REQUIREMENT:

- 30μ IN GOLD / 100μ IN NICKEL

TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°

DEPARTMENT		SIZE A3	DRAWING NUMBER	REV 7
		SCALE: NONE	DO NOT SCALE DRAWING	SHEET 3 OF 3

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	1	INITIAL DRAWING RELEASE	08/31/2022	CTA
-	2	THE THICKNESS OF THE BOARD WAS CHANGE FROM 1.60mm TO 1.57mm	05/08/2023	CTA
-	3	MODEL UPDATED FOR THE SPEC RELEASE 1.01	06/26/2023	CTA
-	4	GOLD CONTACT, TOLEANCE AND DIMENSIONS ARE UPDATED ACORDING WITH THE LAST REFERENCE.	07/19/2023	CTA
-	5	MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC	08/18/2023	CTA

TOP VIEW

DETAIL A
SCALE 3.300

TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°

PARTS LIST

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	M-CRPS_CARD_EDGE_73_5MM-NOTCH	CRPS_CARD_EDGE 73.5mm NOTCH

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY C. TERRIQUEZ	DATE 08/31/2022	DEPARTMENT
DRAWN BY C. TERRIQUEZ	DATE 08/31/2022	TITLE CRPS_CARD_EDGE 73.5mm NOTCH
CHECKED BY A. RODRIGUEZ	DATE	
APPROVED BY	DATE	SIZE A3 / DRAWING NUMBER / REV 5
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE / DO NOT SCALE DRAWING / SHEET 1 OF 3

SEE DETAIL B
BOTTOM VIEW
19.52
33.52
42.38
64.00
65.74
1.75
1.25
SCALE 2.300
11.00
1.10
3X 1.75
3X 2.25
2.39
17.63
7X 1.5±0.05
6X 2.54±0.05
DETAIL B
SCALE 3.500
TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°
DEPARTMENT
SIZE A3
DRAWING NUMBER
REV 5
SCALE:NONE
DO NOT SCALE DRAWING
SHEET 2 OF 3

GOLD CONTACT

SCALE 4.000

PLATING REQUIREMENT:

- 30µ IN GOLD / 100µ IN NICKEL

TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°

DEPARTMENT		SIZE A3	DRAWING NUMBER	REV 5
		SCALE: NONE	DO NOT SCALE DRAWING	SHEET 3 OF 3

M-CRPS Output Card Edge's Receptacle Connector Dimensions, Datums and Footprint for DC-MHS

PRIMARY SIDE VIEW

SCALE 0.250

DETAIL H
SCALE 1.000

NOTE: PIN LOCATIONS SHOWN ARE A SUPERSET THAT ARE COMPATIBLE WITH BOTH 60MM & 73.5MM M-CRPS CONNECTORS.

BOARD DESIGNERS MAY IMPLEMENT A SUPERSET OF PIN LOCATIONS TO ACCOMMODATE AND MAXIMIZE COMPATABILITY WITH VENDOR OFFERINGS.

BOARD DESIGNERS MAY CHOOSE TO IMPLEMENT A SINGLE CONNECTOR FOOTPRINT, IF DESIRED.

CONNECTOR BODY SHALL NOT EXCEED BOUNDING BOX.

THE POWER PIN ZONE SHOWN IS FOR A KNOWN SUPERSET OF POWER PIN LOCATIONS. ANY FUTURE VARIANTS SHOULD MAINTAIN POWER PINS WITHIN THIS POWER PIN ZONE.

Supplemental Material E. 60mm in width M-CRPS card edge mechanical drawing

REVISION HISTORY
ZONE | REV | DESCRIPTION | DATE | APPR
- | 1 | INITIAL DRAWING RELEASE | 08/19/2022 | CTA
- | 2 | THE GOLD FINGERS ARE UPDATED ACORDING WITH THE ELECTRICAL REQUIREMENT | 08/24/2022 | CTA
- | 3 | THE MECHANICAL MODELWAS UPDATED ACORDIGN WITH THE SPEC OF THE VENDOR | 08/31/2022 | CTA
- | 4 | THE WIDTH AND THE GOLDFINGERS WAS CHANGED ACORDING WITH THE CONNECTOR | 06/09/2023 | CTA
- | 5 | MODEL UPDATED FOR THE SPEC RELEASE 1.01 | 06/26/2023 | CTA
- | 6 | GOLD CONTACT, TOLERANCE AND DIMENSIONS ARE UPDATED ACORDING WITH THE LAST REFERENCE. | 07/19/2023 | CTA
- | 7 | MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC | 08/18/2023 | CTA
1.57±0.13
TOP VIEW
1.25
1.75
56.74
57.09
58.78
42.02
33.88
19.16
SEE DETAIL A
6X 2.54±0.05
7X 1.5±0.05
17.63
2.39
3.25
2X 2.75
3X 2.25
1.75
11.00
DETAIL A
SCALE 3.000
TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°
QTY | ITEM NO | PART NUMBER | DESCRIPTION
TOP | M-CRPS_CARD_EDGE_60MM | CRPS_CARD_EDGE_60mm
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 03/30/2022
DRAWN BY C. TERRIQUEZ DATE 08/19/2022
CHECKED BY A. RODRIGUEZ DATE
APPROVED BY DATE
MATERIAL SEE NOTES
FINISH SEE NOTES
DEPARTMENT
TITLE
CRPS_CARD_EDGE_60mm
SIZE A3
DRAWING NUMBER
REV 7
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 1 OF 3

SEE DETAIL B
BOTTOM VIEW
19.16
33.88
42.02
56.74
57.09
58.78
1.75
1.25
SCALE 2.300
11.00
1.10
3X 1.75
3X 2.25
2.39
17.63
7X 1.5±0.05
6X 2.54±0.05
DETAIL B
SCALE 3.500
TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°
DEPARTMENT
SIZE A3
DRAWING NUMBER
REV 7
SCALE:NONE
DO NOT SCALE DRAWING
SHEET 2 OF 3

2X 2.00
2X 45°±5°
GOLD CONTACT
2X 0.05 GOLD CONTACT
CARD EDGE
SCALE 4.000
PLATING REQUIREMENT:
- 30µ IN GOLD / 100µ IN NICKEL
TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°
2X 0.77
2X 30°±5°
DEPARTMENT
SIZE
A3
DRAWING NUMBER
REV
7
SCALE:NONE
DO NOT SCALE DRAWING
SHEET 3 OF 3

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	1	INITIAL DRAWING RELEASE	08/30/2022	CTA
-	2	THE WIDTH AND THE GOLDFINGERS WAS CHANGED ACORDING WITH THE CONNECTOR	06/09/2023	CTA
-	3	MODEL UPDATED FOR THE SPEC RELEASE 1.01	06/26/2023	CTA
-	4	GOLD CONTACT, TOLEANCE AND DIMENSIONS ARE UPDATED ACORDING WITH THE LAST REFERENCE.	07/19/2023	CTA
-	5	MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC	08/18/2023	CTA

PARTS LIST

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	M-CRPS_CARD_EDGE_60MM-NOTCH	CRPS_CARD_EDGE_60mm NOTCH

TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY C. TERRIQUEZ	DATE 08/30/2022	DEPARTMENT	
DRAWN BY C. TERRIQUEZ	DATE 08/19/2022	TITLE CRPS_CARD_EDGE_60mm NOTCH	
CHECKED BY A. RODRIGUEZ	DATE		
APPROVED BY	DATE	SIZE A3	DRAWING NUMBER / REV 5
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE	DO NOT SCALE DRAWING / SHEET 1 OF 3

SEE DETAIL B
BOTTOM VIEW
19.16
33.88
42.02
56.74
57.09
58.78
1.75
1.25
SCALE 2.300
11.00
1.10
3X 1.75
3X 2.25
2.39
17.63
7X 1.5±0.05
6X 2.54±0.05
DETAIL B
SCALE 3.400
TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°
DEPARTMENT
SIZE
A3
DRAWING NUMBER
REV
5
SCALE:NONE
DO NOT SCALE DRAWING
SHEET 2 OF 3

2X 2.00
2X 45°±5°
GOLD CONTACT
2X 0.05 GOLD CONTACT
CARD EDGE
SCALE 4.000
PLATING REQUIREMENT:
- 30µ IN GOLD / 100µ IN NICKEL
TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.10
X.XXX ± ---
ANGLES ± 0.5°
2X 0.77
2X 30°±5°
DEPARTMENT
SIZE
A3
DRAWING NUMBER
REV
5
SCALE:NONE
DO NOT SCALE DRAWING
SHEET 3 OF 3

Supplemental Material F. M-CRPS handle mechanical drawing

MATERIAL: OPTICALLY CREAR POLYCARBONATE

1 THE PSU ASSEMBLY MUST UNDERGO HANDLE PUSH TEST (6 SEPARATE FOR ONE KIND OF FORCE, 3 TESTED IN EACH DIRECTION. TOTALLY, 12 SEPARATE SAMPLE FOR 2 KINDS OF FORCE, 66N AND 133N) SO THE HANDLE DIMENSIONS 33.5MM DOES NOT YIELD OVER FOLLOWING LIMITS.
YIELD IS DEFINED AS THE DIFFERENCE IN DIMENSION 33.5MM BEFORE AND AFTER HANDLE PUSH TEST:
YIELD MUST BE LESS THAN 0.25MM WITH 66N SIDE LOAD.
YIELD MUST BE LESS THAN 1.00MM WITH 133N SIDE LOAD.

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	1	INITIAL DRAWING RELEASE	08/19/2022	CTA
-	2	DESIGN UPDATED FOR RELEASE SPEC 1.01	07/20/2023	CTA
-	3	MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC	08/17/2023	CTA
-	4	MODEL UPDATED ACORDING WITH THE M-CRPS 1.03 SPEC	12/05/2023	CTA
-	5	MODEL UPDATED ACORDING WITH THE M-CRPS 1.04 SPEC	01/30/2024	CTA

PARTS LIST

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	CRPS-BL-HNDL-ID_1	

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY C. TERRIQUEZ	DATE 03/30/2022	DEPARTMENT	
DRAWN BY C.TERRIQUEZ	DATE 08/19/2022	TITLE M-CRPS PIPE HANDLE	
CHECKED BY A. RODRIGUEZ	DATE		
APPROVED BY	DATE	SIZE A3	DRAWING NUMBER / REV 5
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE	DO NOT SCALE DRAWING / SHEET 1 OF 1

Supplemental Material G. M-CRPS latch mechanical drawing

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	1	INITIAL DRAWING RELEASE	03/30/2023	CTA
-	2	THE SNAP AND LATCH ARE UPDATED IN THE SPEC	06/17/2022	CTA
-	3	ADDED MATERIAL TYPE	08/22/2022	CTA
-	4	MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC	08/18/2023	CTA
-	5	MODEL UPDATED ACORDING WITH THE M-CRPS 1.03 SPEC	10/04/2023	CTA

SCALE 1.500

MATERIAL: SUS 301 1/2 HARD

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	M-CRPS_LATCH_73_5MM_185MM_DR	M-CRPS PSU LATCH

PARTS LIST

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY C. TERRIQUEZ	DATE 03/30/2022	DEPARTMENT	
DRAWN BY C. TERRIQUEZ	DATE 08/22/2022	TITLE M-CRPS PSU LATCH	
CHECKED BY A. RODRIGUEZ	DATE		
APPROVED BY	DATE	SIZE A3	DRAWING NUMBER / REV 5
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE	DO NOT SCALE DRAWING / SHEET 1 OF 1

Supplemental Material H. M-CRPS latch plastic grip option 1 (snap-in version)

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	-	INITIAL DRAWING RELEASE	08/19/2022	A. RODRIGUEZ

MATERIAL: PC ABS OR PMS POLY-ALPHA-METRYISTYRENE
COLOR: 3275C (DEFAULT GREEN, CUSTOMER SELECTABLE)

PARTS LIST

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	M-CRPS LATCH FINGER GRIP	

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY	DATE	DEPARTMENT	
DRAWN BY C. TERRIQUEZ	DATE 08/19/2022	TITLE M-CRPS_LATCH_FINGER_GRIP	
CHECKED BY A. RODRIGUEZ	DATE 08/19/2022		
APPROVED BY	DATE	SIZE A3	DRAWING NUMBER / REV 1
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE	DO NOT SCALE DRAWING / SHEET 1 OF 1

Supplemental Material I. M-CRPS latch plastic grip option 2 (over molded version)

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	-	INITIAL DRAWING RELEASE	08/19/2022	-

MATERIAL: PC ABS OR PMS POLY-ALPHA-METRYISTYRENE
COLOR: 1525C (DEFAULT TERRACOTA, CUSTOMER SELECTABLE)

PARTS LIST

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	M-CRPS_LATCH_FINGER_GRIP	

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY	DATE	DEPARTMENT	
DRAWN BY C. TERRIQUEZ	DATE 08/19/2022	TITLE M-CRPS_LATCH_FINGER_GRIP	
CHECKED BY A. RODRIGUEZ	DATE		
APPROVED BY	DATE	SIZE A3 / DRAWING NUMBER	REV
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE / DO NOT SCALE DRAWING	SHEET 1 OF 1

Supplemental Material J. 185mm by 73.5mm +54VDC input M-CRPS mechanical drawing

3 INSULATOR TO BE APPLIED TO THE REAR SHEET METAL SURFACE WITH ADHESIVE AND COVER EXPOSED REAR SHEET METAL AS SHOWN.
A. MATERIAL: FORMEX GK-5 SERIES POLYPROPYLENE SHEET OR APPROVED EQUIVALENT.
B. COLOR: PATONE 877 SILVER.
C. PRIMARY SUBSTRATE MINIMUM THICKNESS TO BE 0.13MM (0.0005"). THIS DOES NOT INCLUDE ADDITIONAL LAMINATE.
D. THERMAL TRANSFER COEFFICIENT 1.0 OR LESS.
E. MATERIAL TO BE RATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS TEMPERATURE.
F. ADHESIVE TO BE TREATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS ENVIRONMENT ON SHEET METAL SURFACE.
G. MATERIAL AND ADHESIVE TO BE UL RECOGNIZED AND MEET THE REQUIREMENTS OF UL 94 V-0 OR 94 VTM-0 AND UL 746D.
REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 09/05/2022 CTA
- 2 DRAWING UPDATED ACORDING WITH THE REFERENCE OF THE VENDOR 03/06/2023 AURELIO R.
- 3 -THE THICKNESS OF THE BOARD WAS CHANGE FROM 1.60mm TO 1.57mm -NEW HANDLE AND EMBOSS IS INCLUDED IN THE DESIGN. 06/26/2023 CTA
- 4 DIMENSION AND NOTES ARE UPDATED ACORDING WITH LAST REVISION. 07/19/2023 CTA
- 5 MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC 08/18/2023 CTA
- 6 MODEL UPDATED ACORDING WITH THE M-CRPS 1.03 SPEC 10/02/2023 CTA
- 7 MODEL UPDATED ACORDING WITH THE M-CRPS 1.04 SPEC 02/09/2024 CTA
- 8 MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC 08/26/2024 CTA
40 FAN
WATTAGE LABEL SPEC
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE
1.5 LATCH TO AC SOCKET
HOT SURFACE LABEL 60417-1-IEC-5041
185.0
33.5 (40.1mm TALL AREA)
30.1 THE FAN LOCATION MUST NOT EXCEED THE DIMENSION INDICATED
0.6
40 FAN
SPEC
65.74±0.2
73.5±0.4
188.4±0.35
SEE DETAIL A
2X 0.800
2.16 EMI SPRING
1 FAN MUST BE EQUAL TO OR LOWER THAN THE SHEET METAL RAMP FORM AFTER ASSEMBLY
2. MATERIAL: 0.8mm MIN. THK +/- 0.08mm GALVANIZED STEEL. JIS G3302 SGCC Z08 SKIN PASSED MINIMUM OR NO SPANGLE. CHROMATE TREATED CHEM. TREAT DRY (NO OIL), 50-65 ROCKWELL B.
OR
JIS G3302 SGCC Z08, CHROMATE-FREE ANTI-FINGER PRINT TREATED. 50-65 ROCKWELL B, SMOOTH FINISH (SKIN PASS), NO OIL. CONDUCTIVITY - SURFACE RESISTANCE <1.0 MΩ AS MEASURED ACCORDING TO MITSUBISHI LORESTA MCP T350, ASP-PROBE.
2 MM MAXIMUM CHASSIS PIN HEIGHT
KOZ BOARD RESTRICTION -BOTTOM-
SECTION A-A
40.1±0.5 RAMP
12
12
2.00
39±0.4
16.05±0.5
8.5±0.2
1.57±0.13
THUMB GRIP FEATURES
4.00
(34.9)
20.5
16.50±0.25
Ø5
11.00±0.25
14.34±0.25
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
7.1
2MM MAX CHASSIS PIN HEIGHT
SECTION A-A
7 MIN
34.66
LED PIPE HANDLE
CONTINUOUS SHEARED EDGE (NO EMBOSSING OR OTHER FEATURE THAT DISTORTS THE EDGE IS ALLOWED)
19 MAX
55.68
CHAMFER 0.3mm FOR PSU BOTTOM HOUSING
PLACE WARNING LABEL WITH SYMBOL 60417-1-IEC-5041 WITH EMBOSS LABEL MUST HAVE YELLOW BACKGROUND WITH BLACK TEXT EMBOSS LOCATION AND SIZE MUST MATCH DATABASE AND WARNING LABEL MUST FIT WITHIN EMBOSS (GAP=0.2MM REF. EMBOSS DEPTH=0.2MM) THE LABEL POSITION AND LABEL SIZE WILL BE BASED ON DESIGN OF EACH VENDOR AND NEED TO APPROVED
R1
8.5
7.6
2.75±0.2
DETAIL A SCALE 1.500
TOLERANCES (MM):
X.X ± 0.50
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_TA_73_5_185MM_TA_54V_2
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 09/05/2022
DRAWN BY C. TERRIQUEZ DATE 09/05/2022
CHECKED BY A. RODRIGUEZ DATE
APPROVED BY DATE
MATERIAL SEE NOTES FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS MECHANICAL SPEC PSU 73.5mm
SIZE A2 DRAWING NUMBER REV 8
SCALE: NONE DO NOT SCALE DRAWING SHEET 1 OF 5

SPEC
12V OUTPUT
REGULAR AIRFLOW
16.50±0.25
11.00±0.25
Ø5
2X 30°
14.34±0.25
55.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 2 OF 5

SPEC
12V OUTPUT
REVERSED AIRFLOW
16.50±0.25
11.00±0.25
Ø5
29.34±0.25
2X 30°
40.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 3 OF 5

SPEC
Ø5
2X 45°
25.00±0.25
11.00±0.2
Ø5
16.50±0.25
11.00±0.25
2X 30°
14.34±0.25
55.68
2X 5.20
54V OUTPUT
REGULAR AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 4 OF 5

SPEC
Ø5
2X 45°
25.00±0.2
11.00±0.2
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
54V OUTPUT
REVERSED AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 5 OF 5

Supplemental Material K. 185mm by 73.5mm -48VDC input M-CRPS mechanical drawing

3 INSULATOR TO BE APPLIED TO THE REAR SHEET METAL SURFACE WITH ADHESIVE AND COVER EXPOSED REAR SHEET METAL AS SHOWN.
A. MATERIAL: FORMEX GK-5 SERIES POLYPROPYLENE SHEET OR APPROVED EQUIVALENT.
B. COLOR: PATONE 877 SILVER.
C. PRIMARY SUBSTRATE MINIMUM THICKNESS TO BE 0.13MM (0.0005"). THIS DOES NOT INCLUDE ADDITIONAL LAMINATE.
D. THERMAL TRANSFER COEFFICIENT 1.0 OR LESS.
E. MATERIAL TO BE RATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS TEMPERATURE.
F. ADHESIVE TO BE TREATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS ENVIRONMENT ON SHEET METAL SURFACE.
G. MATERIAL AND ADHESIVE TO BE UL RECOGNIZED AND MEET THE REQUIREMENTS OF UL 94 V-0 OR 94 VTM-0 AND UL 746D.
REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 06/16/2022 CTA
- 2 DRAWING UPDATED ACORDING WITH THE REFERENCE OF THE VENDOR 03/06/2022 AURELIO R.
- 3 -THE THICKNESS OF THE BOARD WAS CHANGE FROM 1.60mm TO 1.57mm -NEW HANDLE AND EMBOSS IS INCLUDED IN THE DESIGN. 06/26/2023 CTA
- 4 DIMENSION AND NOTES ARE UPDATED ACORDING WITH LAST REVISION. 07/19/2023 CTA
- 5 MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC 08/18/2023 CTA
- 6 MODEL UPDATED ACORDING WITH THE M-CRPS 1.03 SPEC 10/04/2023 CTA
- 7 MODEL UPDATED ACORDING WITH THE M-CRPS 1.04 SPEC 02/09/2024 CTA
- 8 MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC 08/26/2024 CTA
40 FAN
WATTAGE LABEL SPEC
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
2.2 LATCH TO AC SOCKET
4.75 LED
2MM MAXIMUM CHASSIS PIN HEIGHT
KOZ BOARD RESTRICTION -BOTTOM-
SECTION A-A
185.0
33.5 (40.1mm TALL AREA)
30.1 [THE FAN LOCATION MUST NOT EXCEED THE DIMENSION INDICATED]
1.3
0.6
HOT SURFACE LABEL 60417-1-IEC-5041
40 FAN
SPEC
65.74±0.2
RING TERMINAL SUITABLE FOR 6AWG WIRE AND M6 SCREW
188.4±0.35
SEE DETAIL A
2X 0.800
2.16 EMI SPRING
40±0.5 RAMP
12.00
12.00
THUMB GRIP FEATURES
2.00
16.05±0.5
39±0.4
8.5±0.2
1.57±0.13
4.00
(31.99)
20.5
Ø5
16.50±0.25
11.00±0.25
14.34±0.25
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
7.1
2MM MAX CHASSIS PIN HEIGHT SECTION A-A
7 MIN
19 MAX
55.68
CONTINUOUS SHEARED EDGE (NO EMBOSSING OR OTHER FEATURE THAT DISTORTS THE EDGE IS ALLOWED)
34.66
LED PIPE HANDLE
CHAMFER 0.3mm FOR PSU BOTTOM HOUSING
73.5±0.4
1 FAN MUST BE EQUAL TO OR LOWER THAN THE SHEET METAL RAMP FORM AFTER ASSEMBLY
2. MATERIAL: 0.8mm MIN. THK +/- 0.08mm GALVANIZED STEEL. JIS G3302 SGCC Z08 SKIN PASSED MINIMUM OR NO SPANGLE. CHROMATE TREATED CHEM. TREAT DRY (NO OIL), 50-65 ROCKWELL B.
OR
JIS G3302 SGCC Z08, CHROMATE-FREE ANTI-FINGER PRINT TREATED. 50-65 ROCKWELL B, SMOOTH FINISH (SKIN PASS), NO OIL. CONDUCTIVITY - SURFACE RESISTANCE <1.0 MΩ AS MEASURED ACCORDING TO MITSUBISHI LORESTA MCP T350, ASP-PROBE.
PLACE WARNING LABEL WITH SYMBOL 60417-1-IEC-5041 WITH EMBOSS LABEL MUST HAVE YELLOW BACKGROUND WITH BLACK TEXT EMBOSS LOCATION AND SIZE MUST MATCH DATABASE AND WARNING LABEL MUST FIT WITHIN EMBOSS (GAP=0.2MM REF, EMBOSS DEPTH=0.2MM) THE LABEL POSITION AND LABEL SIZE WILL BE BASED ON DESIGN OF EACH VENDOR AND NEED TO APPROVED
R1
8.5
7.6
2.75±0.2
DETAIL A SCALE 1.800
TOLERANCES (MM):
X.X ± 0.50
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_TA_73_5_SPEC-48V M-CRPS MECHANICAL SPEC PSU 73.5mm -48V
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 06/16/2022
DRAWN BY C. TERRIQUEZ DATE 16/JUN/2022
CHECKED BY AURELIO R. DATE
APPROVED BY DATE
MATERIAL SEE NOTES FINISH SEE NOTES
DEPARTMENT
TITLE M-CRPS MECHANICAL SPEC PSU 73.5mm -48V
SIZE A2 DRAWING NUMBER REV 8
SCALE: NONE DO NOT SCALE DRAWING SHEET 1 OF 3

SPEC
12V OUTPUT
REGULAR AIRFLOW
16.50±0.25
11.00±0.25
Ø5
2X 30°
14.34±0.25
55.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 2 OF 3

SPEC
12V OUTPUT
REVERSED AIRFLOW
Ø5
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 3 OF 3

Supplemental Material L. 185mm by 60mm -48VDC input M-CRPS mechanical drawing

REVISION HISTORY
ZONE | REV | DESCRIPTION | DATE | APPR
- | 1 | INITIAL DRAWING RELEASE | 06/17/2022 | AURELIO R.
- | 2 | DRAWING UPDATED ACORDING WITH THE REFERENCE OF THE VENDOR | 03/06/2023 | AURELIO R.
- | 3 | -THE THICKNESS OF THE BOARD WAS CHANGE FROM 1.60mm TO 1.57mm -NEW HANDLE AND EMBOSS IS INCLUDED IN THE DESIGN. -DESIGN UPDATED FOR RELEASE SPEC 1.1 | 06/26/2023 | CTA
- | 4 | DIMENSION AND NOTES ARE UPDATED ACORDING WITH LAST REVISION. | 07/19/2023 | CTA
- | 5 | MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC | 08/18/2023 | CTA
- | 6 | MODEL UPDATED ACORDING WITH THE M-CRPS 1.03 SPEC | 11/28/2023 | CTA
- | 7 | MODEL UPDATED ACORDING WITH THE M-CRPS 1.04 SPEC | 02/09/2024 | CTA
- | 8 | MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC | 08/26/2024 | CTA
185.0
59.51 THE FAN LOCATION MUST NOT EXCEED THE DIMENSION INDICATED
33.86 (40.1mm TALL AREA)
0.60
HOT SURFACE LABEL 60417-1-IEC-5041
40 FAN
ALL VENT OPENINGS TO BE OPTIMIZED BY VENDOR
WATTAGE LABEL SPEC
RING TERMINAL SUITABLE FOR 6AWG WIRE AND M6 SCREW
3.31 LATCH TO SOCKET
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
8.6 LED
4.4 LED
SEE DETAIL A
SPEC
2.91±0.3
57.09±0.2
188.4±0.35
60±0.4
2.16 EMI SPRING
2X 0.800
121.86±0.3 HARD STOP
R0.5±0.2
11±0.3
39.9±0.25 HARD STOP
40.1±0.5 RAMP
12.00
39.9±0.25
100°±2°
2.00
39±0.4
16.05±0.5
8.5±0.2
2MM MAXIMUM CHASSIS PIN HEIGHT
KOZ BOARD RESTRICTION -BOTTOM-
SECTION A-A
THUMB GRIP FEATURES
(32.3)
20.5
16.50±0.25
11.00±0.25
1.57±0.13
Ø5
14.34±0.25
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
7.1
2MM MAX CHASSIS PIN HEIGHT SECTION A-A
CONTINUOUS SHEARED EDGE (NO EMBOSSING OR OTHER FEATURE THAT DISTORTS THE EDGE IS ALLOWED)
CHAMFER 0.3mm FOR PSU BOTTOM HOUSING
7 MIN
19 MAX
45.66
34.66
LED PIPE HANDLE
1 FAN MUST BE EQUAL TO OR LOWER THAN THE SHEET METAL RAMP FORM AFTER ASSEMBLY
2. MATERIAL: 0.8mm MIN. THK +/- 0.08mm GALVANIZED STEEL. JIS G3302 SGCC Z08 SKIN PASSED MINIMUM OR NO SPANGLE. CHROMATE TREATED CHEM. TREAT DRY (NO OIL), 50-65 ROCKWELL B.
OR
JIS G3302 SGCC Z08, CHROMATE-FREE ANTI-FINGER PRINT TREATED. 50-65 ROCKWELL B, SMOOTH FINISH (SKIN PASS), NO OIL. CONDUCTIVITY - SURFACE RESISTANCE <1.0 MΩ AS MEASURED ACCORDING TO MITSUBISHI LORESTA MCP T350, ASP-PROBE.
R1
8.5
7.6
2.75±0.2
DETAIL A SCALE 1.700
PLACE WARNING LABEL WITH SYMBOL 60417-1-IEC-5041 WITH EMBOSS LABEL MUST HAVE YELLOW BACKGROUND WITH BLACK TEXT EMBOSS LOCATION AND SIZE MUST MATCH DATABASE AND WARNING LABEL MUST FIT WITHIN EMBOSS (GAP=0.2MM REF. EMBOSS DEPTH=0.2MM) THE LABEL POSITION AND LABEL SIZE WILL BE BASED ON DESIGN OF EACH VENDOR AND NEED TO APPROVED
TOLERANCES (MM):
X.X ± 0.5
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5
QTY | ITEM NO | PART NUMBER | DESCRIPTION
TOP | M-CRPS_TA_60MM-48V_SPEC | M-CRPS MECHANICAL SPEC PSU 60mm -48V
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 06/17/2022
DRAWN BY C. TERRIQUEZ DATE 06/17/2022
CHECKED BY AURELIO R. DATE 06/17/2022
APPROVED BY DATE
MATERIAL SEE NOTES
FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS MECHANICAL SPEC PSU 60mm -48V
SIZE A2
DRAWING NUMBER
REV 8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 1 OF 3

SPEC
12V OUTPUT
REGULAR AIRFLOW
16.50±0.25
11.00±0.25
Ø5
2X 30°
14.34±0.25
45.66
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 2 OF 3

SPEC
12V OUTPUT
REVERSED AIRFLOW
ø5
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
30.66
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 3 OF 3

Supplemental Material M. Reference Distorted Waveforms

Please note the crest factor value listed below is calculated based on normalizing of the DST waveform under no load condition

Waveform A = DST01

N	%	D
5	9.80	0
7	15.80	0
8	2.16	0

DST01 (CF = 1.469)

Waveform A = DST02

N	%	D
3	1.50	0
7	1.50	0
19	2.00	0

DST02 (CF = 1.369)

Waveform A = DST03

N	%	D
3	2.00	0
5	1.40	0
7	2.00	0
23	1.40	0
31	1.00	0

DST03 (CF = 1.403)

Waveform A = DST04

N	%	D
3	2.50	0
5	1.90	0
7	2.50	0
23	1.90	0
25	1.10	0
31	1.50	0
33	1.10	0

DST04 (CF = 1.385)

Waveform A = DST05

N	%	D
3	1.10	0
5	2.80	0
7	1.40	0
9	2.30	0
11	1.50	0

DST05 (CF = 1.428)

Waveform A = DST06

N	%	D
3	1.65	0
5	4.20	0
7	3.45	0
15	1.05	0
19	3.00	0

DST06 (CF = 1.445)

Waveform A = DST07

N	%	D
3	2.20	0
5	5.60	0
7	2.80	0
9	4.60	0
11	3.00	0
15	1.40	0
21	1.00	0

DST07 (CF = 1.434)

Waveform A = DST08

N	%	D
3	4.90	0
5	1.60	0
7	2.70	0
11	1.40	0
15	2.00	0
17	1.10	0

DST08 (CF = 1.365)

Waveform A = DST09

N	%	D
3	7.35	0
5	2.40	0
7	4.05	0
11	2.10	0
13	1.05	0
15	3.00	0
17	1.65	0
19	1.05	0
21	1.05	0
23	1.20	0
25	1.05	0

DST09 (CF = 1.353)

Waveform A = DST10

N	%	D
3	9.80	0
5	3.20	0
7	5.40	0
9	1.20	0
11	2.80	0
13	1.40	0
15	4.00	0
17	2.20	0
19	1.40	0

N	%	D
21	1.40	0
23	1.60	0
25	1.40	0

DST10 (CF = 1.334)

Waveform A = DST11

N	%	D
3	17.75	0

DST11 (CF = 1.207)

Waveform A = DST12

N	%	D
3	21.25	0

DST12 (CF = 1.210)

Waveform A = DST13

N	%	D
3	24.50	0

DST13 (CF = 1.220)

Waveform A = DST14

N	%	D
2	2.30	0
5	9.80	0
7	15.80	0
8	2.50	0

DST14 (CF = 1.460)

Waveform A = DST15

N	%	D
2	1.15	0
5	4.90	0
7	7.90	0
8	1.25	0

DST15 (CF = 1.414)

Waveform A = DST16

N	%	D
5	2.45	0
7	3.95	0

DST16 (CF = 1.394)

Waveform A = DST17

N	%	D
3	11.11	180
5	4.00	0
7	2.04	180
9	1.23	0
11	0.83	180
13	0.59	0
15	0.44	180
17	0.35	0
19	0.28	180

N	%	D
21	0.23	0
23	0.19	180
25	0.16	0
27	0.14	180

DST17 (CF = 1.707)

Waveform A = DST18

N	%	D
3	7.17	0
5	3.42	180
9	0.80	0

DST18 (CF = 1.272)

Waveform A = DST19

N	%	D
3	8.07	0
5	3.55	180
9	0.96	0
13	0.92	180

DST19 (CF = 1.270)

Waveform A = DST20

N	%	D
3	9.38	0
5	3.44	180
9	1.12	0
13	0.50	180

DST20 (CF = 1.254)

Waveform A = DST21

N	%	D
3	2.06	180
5	1.77	0
7	1.62	180
9	1.23	0
11	0.91	180
13	0.54	0
23	0.51	0
25	0.53	180

DST21 (CF = 1.514)

Waveform A = DST22

N	%	D	N	%	D
3	3.08	180	27	0.69	0
5	2.72	0	29	0.56	180
7	2.43	180			
9	1.97	0			
11	1.41	180			
13	0.86	0			
21	0.62	180			
23	0.73	0			
25	0.77	180			

DST22 (CF = 1.574)

Waveform A = DST23

N	%	D	N	%	D
3	4.28	180	23	0.97	0
5	3.77	0	25	1.04	180
7	3.27	180	29	0.75	180
9	2.57	0			
11	1.93	180			
13	1.22	0			
15	0.55	180			
19	0.46	0			
21	0.83	180			

DST23 (CF = 1.624)

Waveform A = DST24

N	%	D	N	%	D
3	5.74	180	23	1.28	0
5	5.11	0	25	1.35	180
7	4.44	180	27	1.22	0
9	3.52	0	29	0.98	180
11	2.63	180			
13	1.65	0			
15	0.80	180			
19	0.61	0			
21	1.07	180			

DST24 (CF = 1.711)

Waveform A = DST25

N	%	D	N	%	D
3	7.35	180	23	1.64	0
5	6.60	0	25	1.73	180
7	5.74	180	27	1.56	0
9	4.57	0	29	1.24	180
11	3.41	180			
13	2.16	0			
15	1.04	180			
19	0.74	0			
21	1.35	180			

DST25 (CF = 1.793)

Waveform A = DST26

N	%	D	N	%	D
5	3.41	0	35	2.34	0
7	2.55	0	37	2.21	0
11	9.22	0			
13	7.68	0			
17	0.90	0			
19	0.90	0			
23	3.88	0			
25	3.56	0			
31	0.50	0			

DST26 (CF = 1.403)

Waveform A = DST27

N	%	D
21	1.24	0
23	4.91	0
25	2.21	0

DST27 (CF = 1.422)

Waveform A = DST28

N	%	D	N	%	D
3	33.39	0	21	4.52	0
5	20.01	0	23	4.00	0
7	13.76	0	25	3.49	0
9	10.70	0	27	2.91	0
11	8.39	0	29	2.45	0
13	7.06	0	31	1.94	0
15	5.85	0	33	1.95	0
17	4.86	0	35	1.91	0
19	4.86	0	37	1.89	0
			39	1.83	0

DST28 (CF = 1.088)

Waveform A = DST29

N	%	D	N	%	D
3	33.39	0	21	4.48	0
5	20.01	0	23	3.93	0
7	13.75	0	25	0.89	0
9	10.70	0	27	0.92	0
11	8.37	0	29	0.94	0
13	7.05	0	31	0.94	0
15	5.84	0	33	0.94	0
17	4.84	0	35	0.93	0
19	4.83	0	37	0.92	0
			39	0.91	0

DST29 (CF = 1.080)

Waveform A = DST30

N	%	D
3	33.39	0
5	20.01	0
7	13.75	0
9	10.70	0
11	8.33	0
13	6.99	0
15	5.26	0

DST30 (CF = 1.168)

Supplemental Material N. Luminosity Measurements

Measurement with light reader should be taken while looking straight at the rear of the system (not an angle). Both zone A and B defined *Figure N-1* should read an average of 500 +/- 100 L (cd/m² or nits) on a light meter with uniform light distribution (no hotspots or dead spots).

Figure N-1. Zones A and B in the handle

Example of acceptable reading on top segment, zone A:

Figure N-2. Zone A luminance Reading

Supplemental Material O. DC input impedance measurement procedure

Test Set-Up

The setup circuit is shown in *Figure L-1*, NMOS are used in parallel (number of devices in parallel depend on the maximum input current rating current of the PSU under test. Resistor R2 can be picked at 100kΩ, that capacitor could be 1uF (needs to >> MOSFET Cgs), R1 is 100Ω.

The NMOS selection depends on input voltage, if input is from 36VDC to 72VDC, this MOSFET needs to have a voltage rating of 100VDC typically. One example is IPB025N10N3, multiple NMOS transistors could be used in parallel. The power loss on these NMOS is significantly high, for example, if the DC operating point is 20A, and the voltage drop on those NMOS are same as V_{gs}, for example, 4V, this will give 80W loss. You need attach suitable heat-sink to these MOSFETs and recommend using a Fan to cool it.

For CH-B, you need check the probe attenuation (10:1 or 100:1) to make sure the signal is within the safe range of Analyzer, you can also use differential probe.

For CH-A, current probe can be used with a bandwidth at least 1MHz. Instead, use of suitable shunt resistor (with low ESL) can be made to measure the current.

Figure L-1. Input Impedance Measurement Setup

The excitation level should be set at 50mV ~100mV. The excitation level should be as small as possible while still being able to get a clean plot. The scanning frequency span should be from 10Hz to 100kHz typically.

Once the set-up is finalized, PSU under test is ready to be tested.
The test is to be performed at following Input and Load conditions:
Input Voltage – Minimum, Typical, Maximum

Typical Examples:

- 240Vdc Input PSUs – 192Vdc, 240Vdc, 288Vdc.
- -48Vdc Input PSUs - -40Vdc (or -36Vdc as the case may be), -48Vdc, -72Vdc.
- 400Vdc Input PSUs – 192Vdc, 240Vdc, 336Vdc, 400Vdc.

The output load shall be swept from no Load to 100% load in steps of 10%. Impedance and phase plots shall be from 10Hz to 100KHz. Typical plot looks like (recommended method is to have both plot impedance and phase data in one plot):

Figure L-2. Sample Impedance / Phase Plot

Once the plot is done, obtain value of f_{co}, the frequency at which the phase crosses -90° point. Then note the value of Z_{in} and after converting the value to Ohms, calculate the inductance at this point with:

$$L_{in} = \frac{Z_{in}}{2\pi F_{co}}$$

Value of L_{in} is to be calculated at each input and load conditions defined above. From the data, determine the lowest value of L_{in}, this value obtained should be ≥ minimum value called out in *Section 5.3.4 Input Impedance.* The data shall be submitted and be accompanied by raw Data from Analyzer and all plots. A sample is shown below:

Table J-1. -48VDC or 240V/380VDC input power supply input impedance

Load (%)	Frequency (Hz)	Impedance (Ω)	Lin(mH)
0%			
10%			
20%			
30%			
40%			
50%			
60%			
70%			

80%			
90%			
100%			

Note: One table per DC input condition shall be provided.

The main outputs of the power supply must turn off per Vin (turn-off) of the applicable line status range. Standby output shall turn on within the turn on thresholds of the lowest operational input voltage range and shall continue to operate at input voltages below minimum Vin (turn-off) threshold of lowest operational input voltage range.

Power supply design must assure no turn-on/off cycling occurs for DC line impedance defined in the Design Specification.

Supplemental Material P. Exhaust Temperature Measurement

Exhaust temperature of the M-CRPS shall be measured using four type T thermocouples positioned in the locations shown in *Figure O-1* and *Figure O-2* for forward airflow and *Figure O-3* and *Figure O-4* for reversed airflow.

Figure P-1. Thermocouple locations for the 185mm by 73.5mm and 265mm by 73.5mm form factors

Figure P-2. Thermocouple locations for the 185mm by 60mm form factor

Figure P-3. Thermocouple locations for the 185mm by 73.5mm and 265mm by 73.5mm form factors with reversed airflow

Figure P-4. Thermocouple locations for the 185mm by 60mm form factor with reversed airflow

The resulting exhaust temperature shall be calculated as the average of the four thermocouples for each form factor.

Note:

1. All tests shall be conducted using a thermal sleeve, refer to supplemental material for the mechanical drawings.
2. Normal Airflow (NAF) exhaust air thermocouple locations can be used as Reversed Air-Flow (RAF) inlet air locations & vice versa.

The surface temperature of the 185mm by 60mm M-CRPS shall be measured by six thermocouples attached in the locations shown in the figure below.

Figure P-4. Thermocouple locations to measure the surface temperature

Additionally, a scan with a thermal imaging camera of the top of the M-CRPS is needed to identify where the hot spot is located, once the hot spot has been located remove the label and attach a thermocouple to measure the temperature. The same process shall be conducted to identify and measure the hot spot temperature on the sides of the M-CRPS.

Supplemental Material Q. Additional Requirements on Input Line Transients

The PSU should be capable of riding through repetitive input line drops / brown outs as defined below: For Repetitive Brown-outs the repetition cycle can go on indefinitely. The design should be guaranteed with test by repeating 50 consecutive cycles at Design Verification test (DV); for Mass Production (MP) testing can be limited to one cycle.

Figure P-1. Input line transients for all PSUs except -48VDC input

Notes:

1. T6 (Tpwok_holdup) is fixed value as defined in design specification of individual PSU when is operating with dynamic bulk voltage.
2. T6 (Tpwok_holdup) will vary linearly with % load when PSU is operating with fixed bulk voltage.

Figure P-2. Input line transients for PSUs operating with AC input

Notes:

1. T6 (Tpwok_holdup) is fixed value as defined in design specification of individual PSU when is operating with dynamic bulk voltage.
2. T6 (Tpwok_holdup) will vary linearly with % load when the PSU is operating with fixed bulk voltage.
3. Any input voltage below 70% of nominal operating voltage (blue shaded area) is considered as total loss of input and the PSU will shut down if the duration of the drop is longer than T6.

Figure P-3. Input line transients for PSUs operating with high voltage DC input

Notes:

1. T6 (Tpwok_holdup) is fixed value as defined in design specification of individual PSU when is operating with dynamic bulk voltage.
2. T6 (Tpwok_holdup) will vary linearly with % load when the PSU is operating with fixed bulk voltage.
3. Any input voltage below 70% of nominal operating voltage (blue shaded area) is considered as total loss of input and the PSU will shut down if the duration of the drop is longer than T6.
4. For High voltage DC Input PSUs (192VDC-288VDC / 192VDC-400VDC), 200VDC is considered as nominal low.

Figure P-4. Additional requirements for PSUs with high voltage DC input capability

Figure P-5. Repetitive line disturbance

Notes:

1. The above timing sequence is just an example. Each PSU design is different, and so the timing should be adjusted to ensure the PSU will survive repeated input dropout / brownout.
2. This is the minimum value of input voltage marked on PSU Label for regulatory ratings. Vin min is the minimum value of the input voltage defined in the design specification of

the PSU. As an example, Vin nom min is marked as 100Vac or 100Vac / 200Vac on most of the PSUs. In case the PSU is single range, 100Vac -240Vac, the testing would be done based on Vin min = 100Vac, in case of split range, the testing needs to be done based on Vin min = 100Vac and then at 200Vac.

3. The dropout time of t1 = 200ms is based on presumption that internal bias of the PSU is still healthy 200ms after the input is lost. Minimum hold-up time of the internal bias should be calculated using WCEPTA to ensure it is > 200ms. The test should be repeated for individual designs by setting the time t1 equal to the 110% of calculated maximum hold up time of the internal bias supply of that design so that the PSU shuts down and all the data related to averaging of input current is lost.
4. The test is done at 100% rated capacity of the PSU.
5. If the PSU shuts down due to Over Temperature or Input current exceeding $I_{brownout}$ Current protection, it should self-restart once the condition for which it shut down does not exists and input voltage is in the specified range.
6. Note that this is ONLY a DV Test and should not be done on MP units.

Appropriate timers need to be set for riding through the transient events and also to limit the average value of input current below the maximum value of input current at Vin_turnoff threshold. Below is a timing diagram showing the timers for limiting the average value of the input current.

Figure P-6. Input current averaging windows and timers

Notes:

1. $I_{brownout}$ - value of $I_{brownout}$ should be taken from PSU parametric EE Specs based on the input voltage range.
2. The current averaging timer is set when the input current ≥ Ibrownout as defined above. This happens when the input voltage is at or below the minimum turn off value. The current average will reset only when Vin ≥ Vin turn on_max for 2s. If the input current drops below the $I_{brownout}$ value, the timer will hold the last value for 2s before resetting.
3. If Average Iin ≥ Ibrownout at end of 10s -12s window and if Vin < Vin turn on_max, the PSU shuts down, following the normal shut down sequences by de-asserting PWOK.
4. PSU can recover when the average values of Iin is less than Ibrownout and the averaging counter has reset and if the following conditions are satisfied:
    a. Input Voltage is ≥ Vin turn on min.
    b. OTP sensor if used is not indicating an over temperature condition preventing the PSU to turn on.
5. Iin reporting will follow the requirements as documented in the PMBus section for Sensor Reporting.

Supplemental Material R. 185mm by 73.5mm M-CRPS Mechanical Drawing with C22 connector

3 INSULATOR TO BE APPLIED TO THE REAR SHEET METAL SURFACE WITH ADHESIVE AND COVER EXPOSED REAR SHEET METAL AS SHOWN.
A. MATERIAL: FORMEX GK-5 SERIES POLYPROPYLENE SHEET OR APPROVED EQUIVALENT.
B. COLOR: PATONE 877 SILVER.
C. PRIMARY SUBSTRATE MINIMUM THICKNESS TO BE 0.13MM (0.0005"). THIS DOES NOT INCLUDE ADDITIONAL LAMINATE.
D. THERMAL TRANSFER COEFFICIENT 1.0 OR LESS.
E. MATERIAL TO BE RATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS TEMPERATURE.
F. ADHESIVE TO BE TREATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS ENVIRONMENT ON SHEET METAL SURFACE.
G. MATERIAL AND ADHESIVE TO BE UL RECOGNIZED AND MEET THE REQUIREMENTS OF UL 94 V-0 OR 94 VTM-0 AND UL 746D.
REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 09/05/2022 CTA
- 2 DRAWING UPDATED ACORDING WITH THE REFERENCE OF THE VENDOR 03/06/2023 AURELIO R.
- 3 -THE THICKNESS OF THE BOARD WAS CHANGE FROM 1.60mm TO 1.57mm -NEW HANDLE AND EMBOSS IS INCLUDED IN THE DESIGN. 06/26/2023 CTA
- 4 DIMENSION AND NOTES ARE UPDATED ACORDING WITH LAST REVISION. 07/19/2023 CTA
- 5 MODEL UPDATED ACORDING WITH THE M-CRPS 1.02 SPEC 08/18/2023 CTA
- 6 MODEL UPDATED ACORDING WITH THE M-CRPS 1.03 SPEC 10/02/2023 CTA
- 7 MODEL UPDATED ACORDING WITH THE M-CRPS 1.04 SPEC 02/09/2024 CTA
- 8 MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC 08/26/2024 CTA
40 FAN
WATTAGE LABEL SPEC
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE
1.6 LATCH TO AC SOCKET
HOT SURFACE LABEL 60417-1-IEC-5041
185.0
33.5 (40.1mm TALL AREA)
30.10 [THE FAN LOCATION MUST NOT EXCEED THE DIMENSION INDICATED]
0.60
40 FAN
SPEC
65.74±0.2
188.4±0.35
SEE DETAIL A
73.5±0.4
1 FAN MUST BE EQUAL TO OR LOWER THAN THE SHEET METAL RAMP FORM AFTER ASSEMBLY
2. MATERIAL: 0.8mm MIN. THK +/- 0.08mm GALVANIZED STEEL. JIS G3302 SGCC Z08 SKIN PASSED MINIMUM OR NO SPANGLE. CHROMATE TREATED CHEM. TREAT DRY (NO OIL), 50-65 ROCKWELL B.
OR
JIS G3302 SGCC Z08, CHROMATE-FREE ANTI-FINGER PRINT TREATED. 50-65 ROCKWELL B, SMOOTH FINISH (SKIN PASS), NO OIL. CONDUCTIVITY - SURFACE RESISTANCE <1.0 MΩ AS MEASURED ACCORDING TO MITSUBISHI LORESTA MCP T350, ASP-PROBE.
2X 0.800
2.16 EMI SPRING
40.001±0.5 RAMP
12
12
2.00
39±0.4
16.05±0.5
8.5±0.2
1.57±0.13
THUMB GRIP FEATURES
2 MM MAXIMUM CHASSIS PIN HEIGHT
KOZ BOARD RESTRICTION -BOTTOM-
SECTION A-A
4.00
(28.08)
20.5
Ø5
16.50±0.25
11.00±0.25
14.34±0.25
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
7.1
34.66
LED PIPE HANDLE
2MM MAX CHASSIS PIN HEIGHT
SECTION A-A
7 MIN
CONTINUOUS SHEARED EDGE (NO EMBOSSING OR OTHER FEATURE THAT DISTORTS THE EDGE IS ALLOWED)
CHAMFER 0.3mm FOR PSU BOTTOM HOUSING
55.68
19 MAX
PLACE WARNING LABEL WITH SYMBOL 60417-1-IEC-5041 WITH EMBOSS LABEL MUST HAVE YELLOW BACKGROUND WITH BLACK TEXT EMBOSS LOCATION AND SIZE MUST MATCH DATABASE AND WARNING LABEL MUST FIT WITHIN EMBOSS (GAP:0.2MM REF, EMBOSS DEPTH:0.2MM) THE LABEL POSITION AND LABEL SIZE WILL BE BASED ON DESIGN OF EACH VENDOR AND NEED TO APPROVED
R1
8.5
7.6
2.75±0.2
DETAIL A SCALE 1.500
TOLERANCES (MM):
X.X ± 0.50
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_TA_73_5_REP_TA_C22
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 09/05/2022
DRAWN BY C. TERRIQUEZ DATE 09/05/2022
CHECKED BY A. RODRIGUEZ DATE
APPROVED BY DATE
MATERIAL SEE NOTES FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS MECHANICAL SPEC PSU 73.5mm C22
SIZE A2 DRAWING NUMBER REV 8
SCALE: NONE DO NOT SCALE DRAWING SHEET 1 OF 5

SPEC
12V OUTPUT
REGULAR AIRFLOW
16.50±0.25
11.00±0.25
ø5
2X 30°
14.34±0.25
55.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 2 OF 5

SPEC
12V OUTPUT
REVERSED AIRFLOW
Ø5
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 3 OF 5

SPEC
Ø5
2X 45°
25.00±0.2
11.00±0.2
16.50±0.25
11.00±0.25
2X 30°
14.34±0.25
55.68
2X 5.20
54V OUTPUT
REGULAR AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 4 OF 5

SPEC
Ø5
2X 45°
25.00±0.2
11.00±0.2
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
54V OUTPUT
REVERSED AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
8
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 5 OF 5

Supplemental Material S. -48VDC Earth ground ring terminal

REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 10/04/2023 CTA
Ø9.24
Ø12.2
SCALE 2.000
1.27
8.64
RING TERMINAL SUITABLE
FOR 6AWG WIRE
QTY ITEM NO PART NUMBER DESCRIPTION
TOP M-CRPS_RING_TERMINAL-48V RING TERMINAL M-CRPS -48V
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY
DATE
DRAWN BY
C. TERRIQUEZ
DATE
02/OCT/2023
CHECKED BY
DATE
APPROVED BY
DATE
MATERIAL
SEE NOTES
FINISH
SEE NOTES
DEPARTMENT
TITLE
RING TERMINAL M-CRPS -48V
SIZE
A3
DRAWING NUMBER
REV
1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 1 OF 1

Supplemental Material T. -48VDC Earth ground screw

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	1	INITIAL DRAWING RELEASE	10/02/2023	CTA
-	2	MODEL UPDATED ACORDING WITH THE M-CRPS 1.04 SPEC	01/30/2024	CTA
-	3	MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC	08/28/2024	CTA

PARTS LIST

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	M-CRPS_SCREW_M6-48V	

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY	DATE	DEPARTMENT	
DRAWN BY C. TERRIQUEZ	DATE 10/02/2023	TITLE M-CRPS SCREW M6X10mm	
CHECKED BY	DATE		
APPROVED BY	DATE	SIZE A3	DRAWING NUMBER / REV 3
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE	DO NOT SCALE DRAWING / SHEET 1 OF 1

Supplemental Material U. 73.5mm by 185mm form factor thermal sleeve

REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 12/05/2023 CTA
161.86
2X 10.48
2X 2.5
12
15.55
2X 50.5
4X M3X0.5
1
40.6
51.6
74.5
77.45
178.2
TOP M-CRPS_HOUSING_185MM_X_60MM
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
TOLERANCES (MM):
X.X ± 0.5
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY DATE
DRAWN BY C. TERRIQUEZ DATE 12/05/2023
CHECKED BY DATE
APPROVED BY DATE
MATERIAL SEE NOTES
FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS HOUSING 185MM X 73.5MM
SIZE A2
DRAWING NUMBER
REV 1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 1 OF 1

Supplemental Material V. 73.5mm by 265mm form factor thermal sleeve

REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 12/05/2023 CTA
201.86
2X 10.48
2X 2.5
12
15.55
2X 50.5
1
40.6
51.6
74.5
77.45
258.2
TOLERANCES (MM):
X.X ± 0.5
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_HOUSING_265MM_X_60MM
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY DATE
DRAWN BY C. TERRIQUEZ DATE 12/05/2023
CHECKED BY DATE
APPROVED BY DATE
MATERIAL SEE NOTES
FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS HOUSING 265MM X 73.5MM
SIZE A2
DRAWING NUMBER
REV 1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 1 OF 1

Supplemental Material W. 60mm by 185mm form factor thermal sleeve

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	1	INITIAL DRAWING RELEASE	12/05/2023	CTA

TOLERANCES (MM):
X.X ± 0.5
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°

PARTS LIST

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	M-CRPS_HOUSING_185MM_X_60MM	

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY	DATE	DEPARTMENT
DRAWN BY C. TERRIQUEZ	DATE 12/05/2023	TITLE M-CRPS HOUSING 185MM X 60MM
CHECKED BY	DATE	
APPROVED BY	DATE	SIZE A2 / DRAWING NUMBER / REV 1
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE / DO NOT SCALE DRAWING / SHEET 1 OF 1

Supplemental Material X. 73.5mm in width thermal test plate

REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 12/05/2023 CTA
77.7
2X 50.5
52.65
3
41.6
2X 51.6
4X Ø4
1
13
TOLERANCES (MM):
X.X ± 0.5
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_PLATE_185MM_X_73-5MM
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY DATE
DRAWN BY DATE 05/DEC/2023
CHECKED BY DATE
APPROVED BY DATE
MATERIAL SEE NOTES
FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS PLATE 185MM X73-5MM
SIZE A2
DRAWING NUMBER
REV 1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 1 OF 1

Supplemental Material Y. 60mm in width thermal test plate

REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASE 12/05/2023 CTA
64.2
2X 37
3
39.15
41.6
2X 51.6
4X Ø4
1
13
TOLERANCES (MM):
X.X ± 0.5
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_PLATE_185MM_X_60MM
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY DATE
DRAWN BY C. TERRIQUEZ DATE 12/05/2023
CHECKED BY DATE
APPROVED BY DATE
MATERIAL SEE NOTES
FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS_PLATE_185MM X 60MM
SIZE A2
DRAWING NUMBER
REV 1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 1 OF 1

Supplemental Material Z.185mm by 73.5mm M-CRPS 277VAC input mechanical drawing

3 INSULATOR TO BE APPLIED TO THE REAR SHEET METAL SURFACE WITH ADHESIVE AND COVER EXPOSED REAR SHEET METAL AS SHOWN.
A. MATERIAL: FORMEX GK-5 SERIES POLYPROPYLENE SHEET OR APPROVED EQUIVALENT.
B. COLOR: PATONE 877 SILVER.
C. PRIMARY SUBSTRATE MINIMUM THICKNESS TO BE 0.13MM (0.0005"). THIS DOES NOT INCLUDE ADDITIONAL LAMINATE.
D. THERMAL TRANSFER COEFFICIENT 1.0 OR LESS.
E. MATERIAL TO BE RATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS TEMPERATURE.
F. ADHESIVE TO BE TREATED FOR A MINIMUM OF 95 DEGREE C CONTINUOUS ENVIRONMENT ON SHEET METAL SURFACE.
G. MATERIAL AND ADHESIVE TO BE UL RECOGNIZED AND MEET THE REQUIREMENTS OF UL 94 V-0 OR 94 VTM-0 AND UL 746D.
REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASED, MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC 08/26/2024 CTA
40 FAN
WATTAGE LABEL SPEC
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
2.28 LATCH TO AC SOCKET
4.8 LED
2MM MAXIMUM CHASSIS PIN HEIGHT
KOZ BOARD RESTRICTION -BOTTOM-
SECTION A-A
HOT SURFACE LABEL 60417-1-IEC-5041
1.3
0.60
185.0
33.5 (40.1mm TALL AREA)
30.1 [THE FAN LOCATION MUST NOT EXCEED THE DIMENSION INDICATED]
40 FAN
SPEC
65.74±0.2
188.4±0.35
SEE DETAIL A
2X 0.800
2.16 EMI SPRING
40.1±0.5 RAMP
12.00
12.00
THUMB GRIP FEATURES
2.00
39±0.4
16.05±0.5
8.5±0.2
1.57±0.13
4.00
(40.99)
20.5
Ø5
16.50±0.25
11.00±0.25
14.34±0.25
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
7.1
34.66
LED PIPE HANDLE
2MM MAX CHASSIS PIN HEIGHT
SECTION A-A
7 MIN
CONTINUOUS SHEARED EDGE
(NO EMBOSSING OR OTHER FEATURE THAT DISTORTS THE EDGE IS ALLOWED)
CHAMFER 0.3mm FOR PSU BOTTOM HOUSING
19 MAX
55.68
73.5±0.4
1 FAN MUST BE EQUAL TO OR LOWER THAN THE SHEET METAL RAMP FORM AFTER ASSEMBLY
2. MATERIAL: 0.8mm MIN. THK +/- 0.08mm GALVANIZED STEEL. JIS G3302 SGCC Z08 SKIN PASSED MINIMUM OR NO SPANGLE. CHROMATE TREATED CHEM. TREAT DRY (NO OIL), 50-65 ROCKWELL B.
OR
JIS G3302 SGCC Z08, CHROMATE-FREE ANTI-FINGER PRINT TREATED. 50-65 ROCKWELL B, SMOOTH FINISH (SKIN PASS), NO OIL, CONDUCTIVITY - SURFACE RESISTANCE <1.0 MΩ AS MEASURED ACCORDING TO MITSUBISHI LORESTA MCP T350, ASP-PROBE.
PLACE WARNING LABEL WITH SYMBOL 60417-1-IEC-5041 WITH EMBOSS
LABEL MUST HAVE YELLOW BACKGROUND WITH BLACK TEXT
EMBOSS LOCATION AND SIZE MUST MATCH DATABASE AND WARNING LABEL MUST FIT WITHIN EMBOSS (GAP=0.2MM REF, EMBOSS DEPTH=0.2MM)
THE LABEL POSITION AND LABEL SIZE WILL BE BASED ON DESIGN OF EACH VENDOR AND NEED TO APPROVED
R1
8.5
7.6
2.75±0.2
DETAIL A SCALE 1.500
TOLERANCES (MM):
X.X ± 0.50
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_TA_73_5_277V_TA
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 09/05/2022
DRAWN BY C. TERRIQUEZ DATE 04/24/2022
CHECKED BY A. RODRIGUEZ DATE
APPROVED BY DATE
MATERIAL SEE NOTES FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS MECHANICAL SPEC PSU 73.5mm 277V
SIZE A2 DRAWING NUMBER REV 1
SCALE: NONE DO NOT SCALE DRAWING SHEET 1 OF 5

SPEC
12V OUTPUT
REGULAR AIRFLOW
16.50±0.25
11.00±0.25
ø5
2X 30°
14.34±0.25
55.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 2 OF 5

SPEC
12V OUTPUT
REVERSED AIRFLOW
Ø5
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 3 OF 5

SPEC
Ø5
2X 45°
25.00±0.2
11.00±0.2
16.50±0.25
11.00±0.25
2X 30°
14.34±0.25
55.68
2X 5.20
54V OUTPUT
REGULAR AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 4 OF 5

SPEC
Ø5
2X 45°
25.00±0.2
11.00±0.2
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
40.68
2X 5.20
54V OUTPUT
REVERSED AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 5 OF 5

Supplemental Material AA. 185mm by 60mm M-CRPS 277VAC input mechanical drawing

REVISION HISTORY
ZONE REV DESCRIPTION DATE APPR
- 1 INITIAL DRAWING RELEASED, MODEL UPDATED ACORDING WITH THE M-CRPS 1.05 SPEC 09/17/2024 CTA
185.0
59.51 [THE FAN LOCATION MUST NOT EXCEED THE DIMENSION INDICATED]
33.86 (40.1mm TALL AREA)
0.6
2.91±0.3
HOT SURFACE LABEL 60417-1-IEC-5041
40 FAN
WATTAGE LABEL SPEC
ALL VENT OPENINGS TO BE OPTIMIZED BY VENDOR
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
10.36 LED
SPEC
57.09±0.2
60±0.4
188.4±0.35
5.3±0.2
2.65 LATCH TO AC SOCKET
4.75 LED
SEE DETAIL B
2.16 EMI SPRING
121.86±0.3 HARD STOP
R0.5±0.2
11±0.3
2X 0.800
39.9±0.25 HARD STOP
40.1±0.5 RAMP
12.00
39.9±0.25
100°±2°
2.00
39±0.4
16.05±0.5
8.5±0.2
1.57±0.13
SECTION A-A
2MM MAXIMUM CHASSIS PIN HEIGHT
KOZ BOARD RESTRICTION -BOTTOM-
THUMB GRIP FEATURES
1 FAN MUST BE EQUAL TO OR LOWER THAN THE SHEET METAL RAMP FORM AFTER ASSEMBLY
2. MATERIAL: 0.8mm MIN. THK +/- 0.08mm GALVANIZED STEEL. JIS G3302 SGCC Z08 SKIN PASSED MINIMUM OR NO SPANGLE. CHROMATE TREATED CHEM. TREAT DRY (NO OIL), 50-65 ROCKWELL B.
OR
JIS G3302 SGCC Z08, CHROMATE-FREE ANTI-FINGER PRINT TREATED. 50-65 ROCKWELL B, SMOOTH FINISH (SKIN PASS), NO OIL, CONDUCTIVITY - SURFACE RESISTANCE <1.0 MΩ AS MEASURED ACCORDING TO MITSUBISHI LORESTA MCP T350, ASP-PROBE.
4.00
(42.24)
20.5
Ø5
16.50±0.25
11.00±0.25
14.34±0.25
2MM MAX CHASSIS PIN HEIGHT
SECTION A-A
INPUT PLUG SHALL INSTALL WITHOUT INTERFERENCE WITH RELEASE LEVER AND HANDLE.
7.1
CONTINUOUS SHEARED EDGE (NO EMBOSSING OR OTHER FEATURE THAT DISTORTS THE EDGE IS ALLOWED)
CHAMFER 0.3mm FOR PSU BOTTOM HOUSING
7 MIN
19 MAX
45.66
34.66
LED PIPE HANDLE
PLACE WARNING LABEL WITH SYMBOL 60417-1-IEC-5041 WITH EMBOSS LABEL MUST HAVE YELLOW BACKGROUND WITH BLACK TEXT EMBOSS LOCATION AND SIZE MUST MATCH DATABASE AND WARNING LABEL MUST FIT WITHIN EMBOSS (GAP:0.2MM REF, EMBOSS DEPTH:0.2MM) THE LABEL POSITION AND LABEL SIZE WILL BE BASED ON DESIGN OF EACH VENDOR AND NEED TO APPROVED
R1
8.5
2.75±0.2
2.3
DETAIL B SCALE 1.800
TOLERANCES (MM):
X.X ± 0.50
X.XX ± 0.20
X.XXX ± 0.100
ANGLES ± 0.5°
TOP M-CRPS_REP_60MM
QTY ITEM NO PART NUMBER DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-2009. DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
DESIGNED BY C. TERRIQUEZ DATE 04/24/2024
DRAWN BY C. TERRIQUEZ DATE 04/24/2024
CHECKED BY AURELIO R. DATE
APPROVED BY DATE
MATERIAL SEE NOTES FINISH SEE NOTES
DEPARTMENT
TITLE
M-CRPS MECHANICAL 277V SPEC PSU 185mm X 60mm
SIZE A2 DRAWING NUMBER REV 1
SCALE: NONE DO NOT SCALE DRAWING SHEET 1 OF 5

SPEC
12V OUTPUT
REGULAR AIRFLOW
16.50±0.25
11.00±0.25
2X 30°
14.34±0.25
45.66
2X 5.20
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 2 OF 5

SPEC
12V OUTPUT
REVERSED AIRFLOW
16.50±0.25
11.00±0.25
Ø5
29.34±0.25
2X 30°
30.66
2X 5.2
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 3 OF 5

SPEC
11.00±0.20
Ø5
2X 45.2°
25±0.2
16.50±0.25
Ø5
11.00±0.25
14.34±0.25
45.66
2X 5.2
54V OUTPUT
REGULAR AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 4 OF 5

SPEC
11.00±0.20
Ø5
2X 45.2°
25±0.2
16.50±0.25
11.00±0.25
29.34±0.25
2X 30°
30.66
2X 5.2
54V OUTPUT
REVERSED AIRFLOW
DEPARTMENT
SIZE
A2
DRAWING NUMBER
REV
1
SCALE: NONE
DO NOT SCALE DRAWING
SHEET 5 OF 5

End of the document!!!