

數位系統實驗

作業十一

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數位系統實驗

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實驗一：累積時脈延時電路（以DFF為基礎設計電路）並觀察RTL

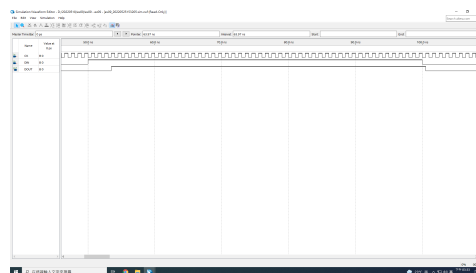
- 實驗結果照片：

```
1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3
4  ENTITY DEBOUNCING IS
5  PORT( DIN, CK : IN STD_LOGIC;
6        DOUT : OUT STD_LOGIC);
7  END DEBOUNCING;
8
9  ARCHITECTURE ARCH OF DEBOUNCING IS
10 COMPONENT DFF1
11 PORT( D, CK : IN STD_LOGIC;
12       Q : OUT STD_LOGIC);
13 END COMPONENT;
14
15 SIGNAL TMP : STD_LOGIC_VECTOR(4 DOWNTO 0);
16
17 BEGIN
18   TMP(0) <= DIN;
19   LP1 : FOR I IN 1 TO 4 GENERATE
20     U1 : DFF1 PORT MAP(TMP(I - 1), CK, TMP(I));
21   END GENERATE;
22   DOUT <= TMP(4) AND TMP(3) AND TMP(2) AND TMP(1);
23 END ARCH;
```

VHDL

```
1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3
4  ENTITY DFF1 IS
5  PORT( D, CK : IN STD_LOGIC;
6        Q : OUT STD_LOGIC);
7  END DFF1;
8
9  ARCHITECTURE ARCH OF DFF1 IS
10 BEGIN
11   PROCESS(CK)
12   BEGIN
13     IF RISING_EDGE(CK) THEN Q <= D;
14     END IF;
15   END PROCESS;
16 END ARCH;
```

DFF1



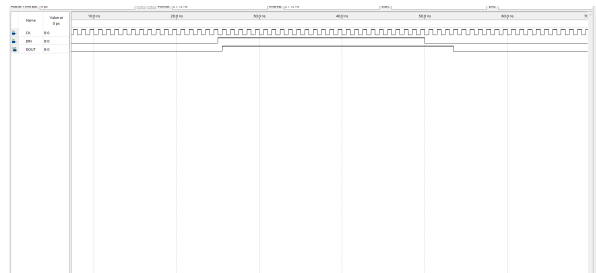
波形圖

實驗二：累積時脈延時電路（使用VHDL直接描述DFF電路）並觀察RTL

- 實驗結果照片：

```
8 | END DEBOUNCING2;  
9 |  
10 | ARCHITECTURE ARCH OF DEBOUNCING2 IS  
11 | BEGIN  
12 |     PROCESS(CK)  
13 |     VARIABLE TMP : INTEGER RANGE 0 TO 9;  
14 |     BEGIN  
15 |         IF RISING_EDGE(CK) THEN  
16 |             IF DIN = '1' THEN  
17 |                 TMP := 0;  
18 |                 DOUT <= '1';  
19 |             ELSE  
20 |                 TMP := TMP + 1;  
21 |                 IF TMP = 4 THEN  
22 |                     TMP := 0;
```

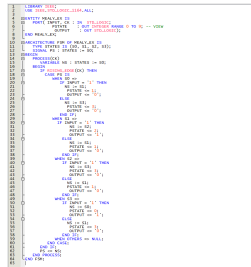
VHDL



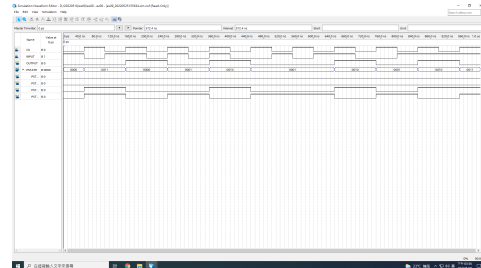
波形圖

實驗三：米利機電路設計

- 實驗結果照片：

A screenshot of a text editor showing VHDL code. The code is written in a dark background with light-colored text. It includes a library declaration, entity declaration, architecture, and logic for a Mealy machine. The code is color-coded with syntax highlighting.

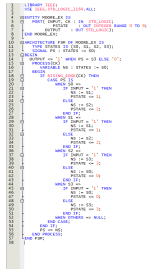
VHDL



波形圖

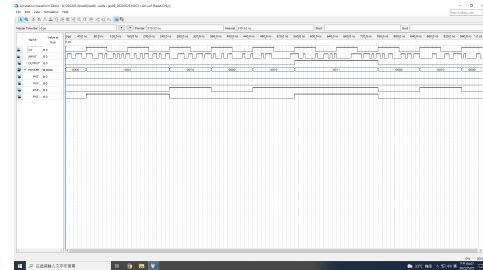
實驗四：莫爾機電路設計

- 實驗結果照片：



A screenshot of a VHDL code editor showing the implementation of a Moore machine. The code includes a clock signal definition, a process for state transitions, and output logic. The state transitions are defined by a case statement within a process sensitive to the clock. The outputs are determined by the current state.

VHDL



波形圖