數位系統實驗

作業十一

組員：

109601003 林群賀、109601005 謝文喨

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數位系統實驗

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實驗一：累積時脈延時電路（以DFF為基礎設計電路）並觀察RTL

- 實驗結果照片：

```vhdl
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY DEBOUNCING IS
   PORT( DIN, CK : IN  STD_LOGIC;
         DOUT    : OUT STD_LOGIC);
END DEBOUNCING;

ARCHITECTURE ARCH OF DEBOUNCING IS
   COMPONENT DFF1
      PORT( D, CK : IN  STD_LOGIC;
            Q     : OUT STD_LOGIC);
   END COMPONENT;

   SIGNAL TMP : STD_LOGIC_VECTOR(4 DOWNTO 0);
BEGIN
   TMP(0) <= DIN;
   LP1 : FOR I IN 1 TO 4 GENERATE
      U1 : DFF1 PORT MAP(TMP(I - 1), CK, TMP(I));
   END GENERATE;

   DOUT <= TMP(4) AND TMP(3) AND TMP(2) AND TMP(1);
END ARCH;
```

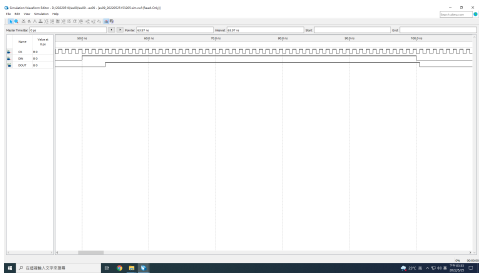
VHDL

```vhdl
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY DFF1 IS
   PORT( D, CK : IN  STD_LOGIC;
         Q     : OUT STD_LOGIC);
END DFF1;

ARCHITECTURE ARCH OF DFF1 IS
BEGIN
   PROCESS(CK)
   BEGIN
      IF RISING_EDGE(CK) THEN Q <= D;
      END IF;
   END PROCESS;
END ARCH;
```

DFF1



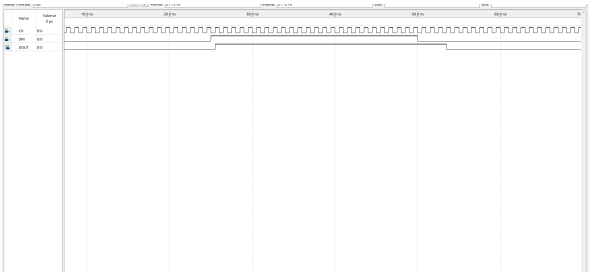
波形圖

實驗二：累積時脈延時電路（使用VHDL直接描述DFF電路）並觀察RTL

- 實驗結果照片：

```
 7   END DEBOUNCING2;
 8
 9   ARCHITECTURE ARCH OF DEBOUNCING2 IS
10   BEGIN
11      PROCESS(CK)
12         VARIABLE TMP : INTEGER RANGE 0 TO 9;
13      BEGIN
14         IF RISING_EDGE(CK) THEN
15           IF DIN = '1' THEN
16               TMP := 0;
17               DOUT <= '1';
18           ELSE
19               TMP := TMP + 1;
20               IF TMP = 4 THEN
21                  TMP := 0;
```

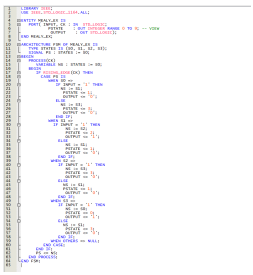
VHDL



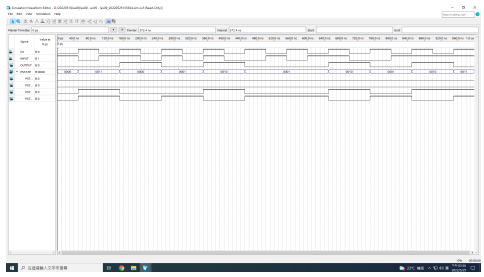
波形圖

實驗三：米利機電路設計

- 實驗結果照片：



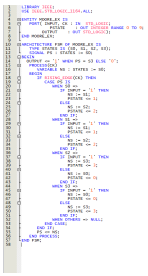
VHDL



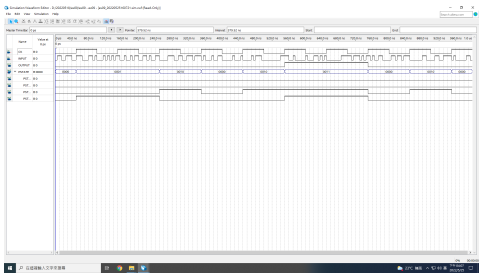
波形圖

實驗四：莫爾機電路設計

- 實驗結果照片：



VHDL



波形圖