

數位系統實驗

作業十二

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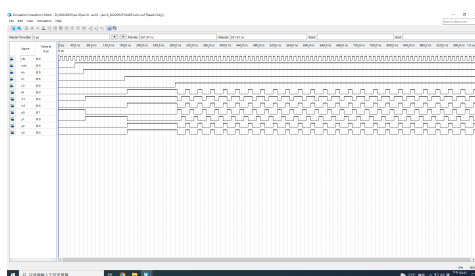
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實驗一：GRAFCET離散事件建模

- 實驗結果照片：

```
1 library ieee;
2
3 use IEEE.STD_LOGIC_1164.all;
4 use IEEE.STD_LOGIC_ARITH.all;
5 use IEEE.STD_LOGIC_UNSIGNED.all;
6
7 entity g0 is
8 port ( clk: in std_logic;
9       rstn: in std_logic;
10       en: in std_logic;
11       L1: in std_logic;
12       L2: in std_logic;
13       V1: out std_logic;
14       V2: out std_logic;
15       M: out std_logic;
16       y0, y1, y2, y3: out std_logic);
17 end g0;
18
19 architecture rtl of g0 is
20 signal x0, x1, x2, x3: std_logic;
21 signal w_v1: std_logic;
22 signal w_v2: std_logic;
23 signal w_M: std_logic;
24 begin
25 GRAFCET: process (clk, rstn)
26 begin
27 if rstn = '0' then
28 x0 <= '1'; x1 <= '0'; x2 <= '0'; x3 <= '0';
29 elsif clk'event and clk = '1' then
30 if x0 = '1' and en = '1' then
31 x0 <= '0'; x1 <= '1';
32 elsif x1 = '1' and L1 = '1' then
33 x1 <= '0'; x2 <= '1'; x3 <= '1';
34 elsif x2 = '1' and x3 = '1' and L2 = '1' then
35 x2 <= '0'; x3 <= '0'; x0 <= '1';
36 else null;
37 end if;
38 else null;
39 end if;
40 end process;
41
42 DATA_PATH: process (x0, x1, x2, x3)
43 begin
44 y0 <= x0; y1 <= x1; y2 <= x2; y3 <= x3;
45 if x0 = '1' then
46 w_v1 <= '0'; w_v2 <= '0'; w_M <= '0';
47 end if;
48 if x1 = '1' then
49 w_v1 <= '1';
50 end if;
51 if x2 = '1' then
52 w_M <= '1';
53 end if;
54 if x3 = '1' then
55 w_v2 <= '1';
56 end if;
57 V1 <= w_v1; V2 <= w_v2; M <= w_M;
58 end process;
59 END rtl;
60
61
```

VHDL



波形圖