

# 區塊圖形編輯設計

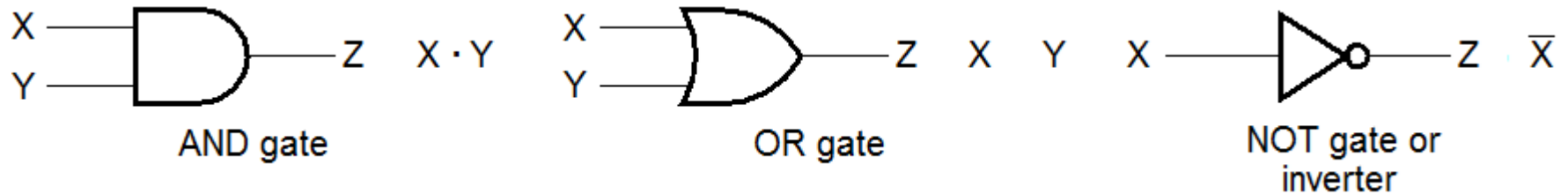
# Outline

- 基本概念複習
- 區塊圖形編輯設計
- Quartus Prime補充
- 課堂練習

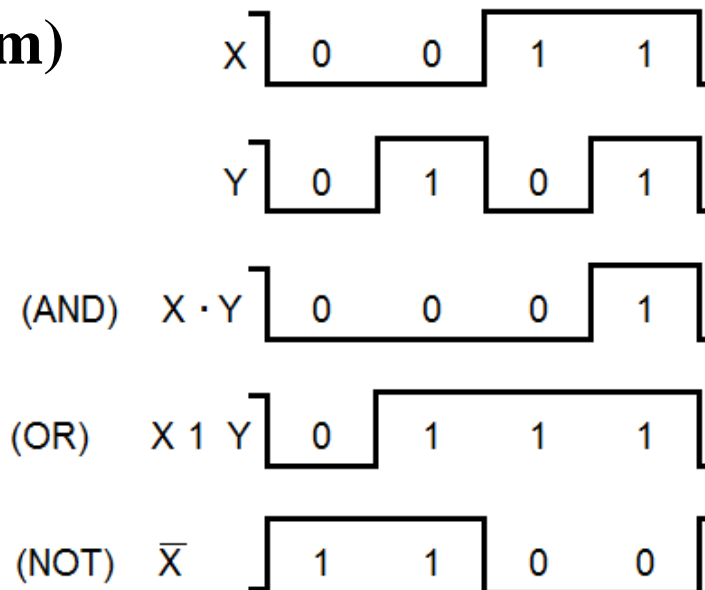
# 基本概念複習

# Logic Gate Symbols and Behavior



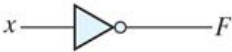

## Logic gates symbols:



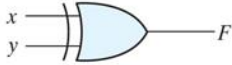
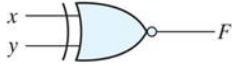


## Timing diagram(waveform)



# Logic Gates

Name	Graphic symbol	Algebraic function	Truth table															
AND		$F = x \cdot y$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	x	y	F	0	0	0	0	1	0	1	0	0	1	1	1
x	y	F																
0	0	0																
0	1	0																
1	0	0																
1	1	1																
OR		$F = x + y$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	1
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	1																
Inverter		$F = x'$	<table><tr><th>x</th><th>F</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	x	F	0	1	1	0									
x	F																	
0	1																	
1	0																	
Buffer		$F = x$	<table><tr><th>x</th><th>F</th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table>	x	F	0	0	1	1									
x	F																	
0	0																	
1	1																	

NAND		$F = (xy)'$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	x	y	F	0	0	1	0	1	1	1	0	1	1	1	0
x	y	F																
0	0	1																
0	1	1																
1	0	1																
1	1	0																
NOR		$F = (x + y)'$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	0
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	0																
Exclusive-OR (XOR)		$F = xy' + x'y$ $= x \oplus y$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	0
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	0																
Exclusive-NOR or equivalence		$F = xy + x'y'$ $= (x \oplus y)'$	<table><tr><th>x</th><th>y</th><th>F</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	1
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	1																

# Expressions of Logic Function

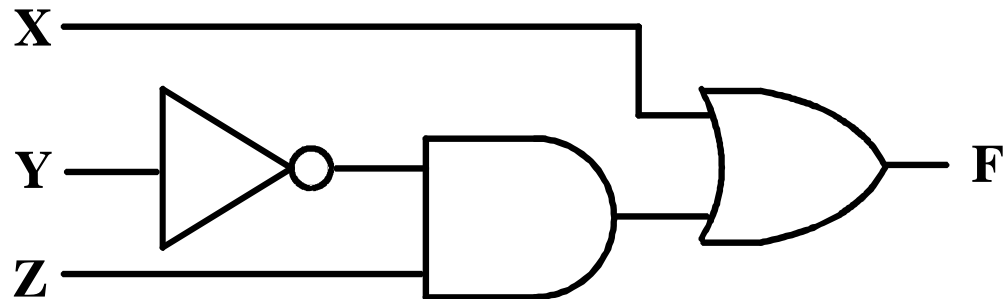
**Truth Table**

<b>X Y Z</b>	<b><math>F = X + \bar{Y} \times Z</math></b>
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

**Equation**

$$F = X + \bar{Y} Z$$

**Logic Diagram**



- Boolean equations, truth tables and logic diagrams describe the same function!
- Truth tables are unique; expressions and logic diagrams are not.

# Boolean Algebra

- An algebraic structure defined on a set of at least two elements,  $B$ , together with three binary operators (denoted  $+$ ,  $\cdot$  and  $\bar{\phantom{x}}$ ) that satisfies the following basic identities:

---

1.  $X + 0 = X$

2.  $X \cdot 1 = X$

3.  $X + 1 = 1$

4.  $X \cdot 0 = 0$

5.  $X + X = X$

6.  $X \cdot X = X$

7.  $X + \bar{X} = 1$

8.  $X \cdot \bar{X} = 0$

9.  $\overline{\overline{X}} = X$

---

10.  $X + Y = Y + X$

11.  $XY = YX$

Commutative

12.  $(X + Y) + Z = X + (Y + Z)$

13.  $(XY)Z = X(YZ)$

Associative

14.  $X(Y + Z) = XY + XZ$

15.  $X + YZ = (X + Y)(X + Z)$

Distributive

16.  $\overline{X + Y} = \bar{X} \cdot \bar{Y}$

17.  $\overline{X \cdot Y} = \bar{X} + \bar{Y}$

DeMorgan's

---

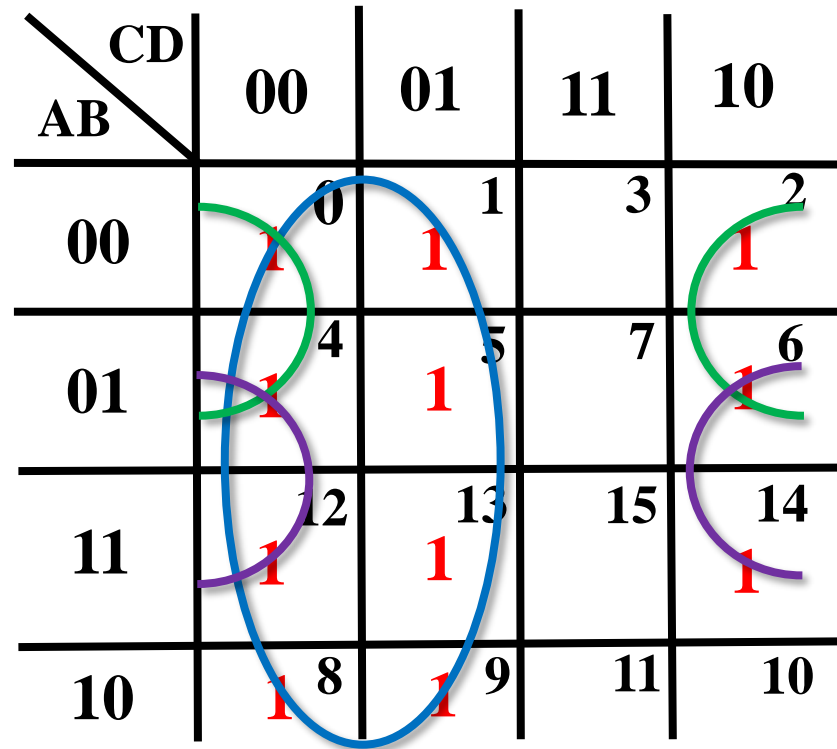
# Boolean Operator Precedence

- **The order of evaluation in a Boolean expression is:**
  1. Parentheses
  2. NOT
  3. AND
  4. OR
- **Consequence: Parentheses appear around OR expressions**
- **Example:  $F = A(B + C)(C + \overline{D})$**



# K-Map

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



$$F(w, x, y, z) = C' + A'D' + BD'$$

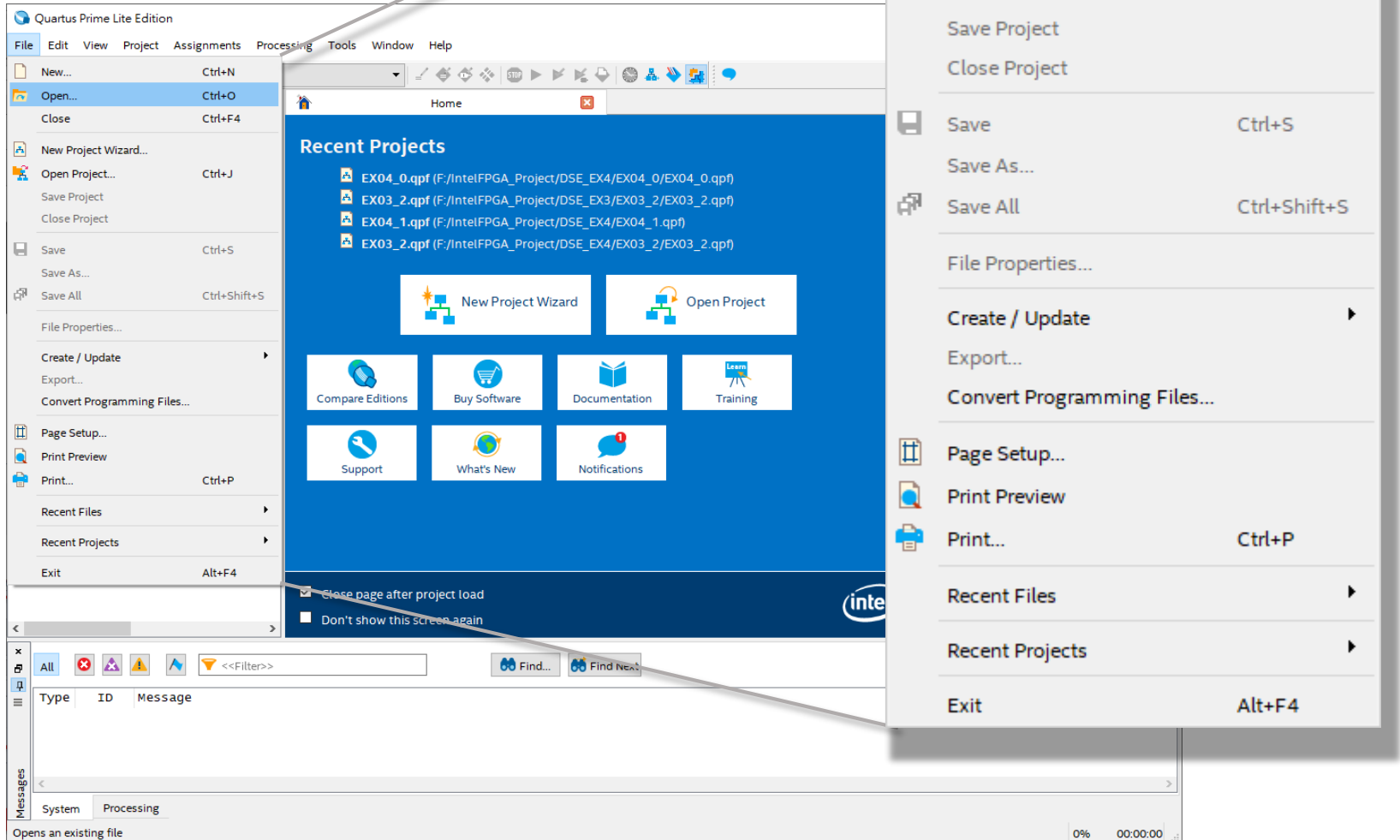
$$F(A, B, C, D) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$$

$$F(A, B, C, D) = A'B'C'D' + A'B'C'D + A'B'CD' + A'BC'D' + A'BC'D + A'BCD' + AB'C'D' + AB'C'D + ABC'D' + ABC'D + ABCD'$$

# 區塊圖形編輯設計

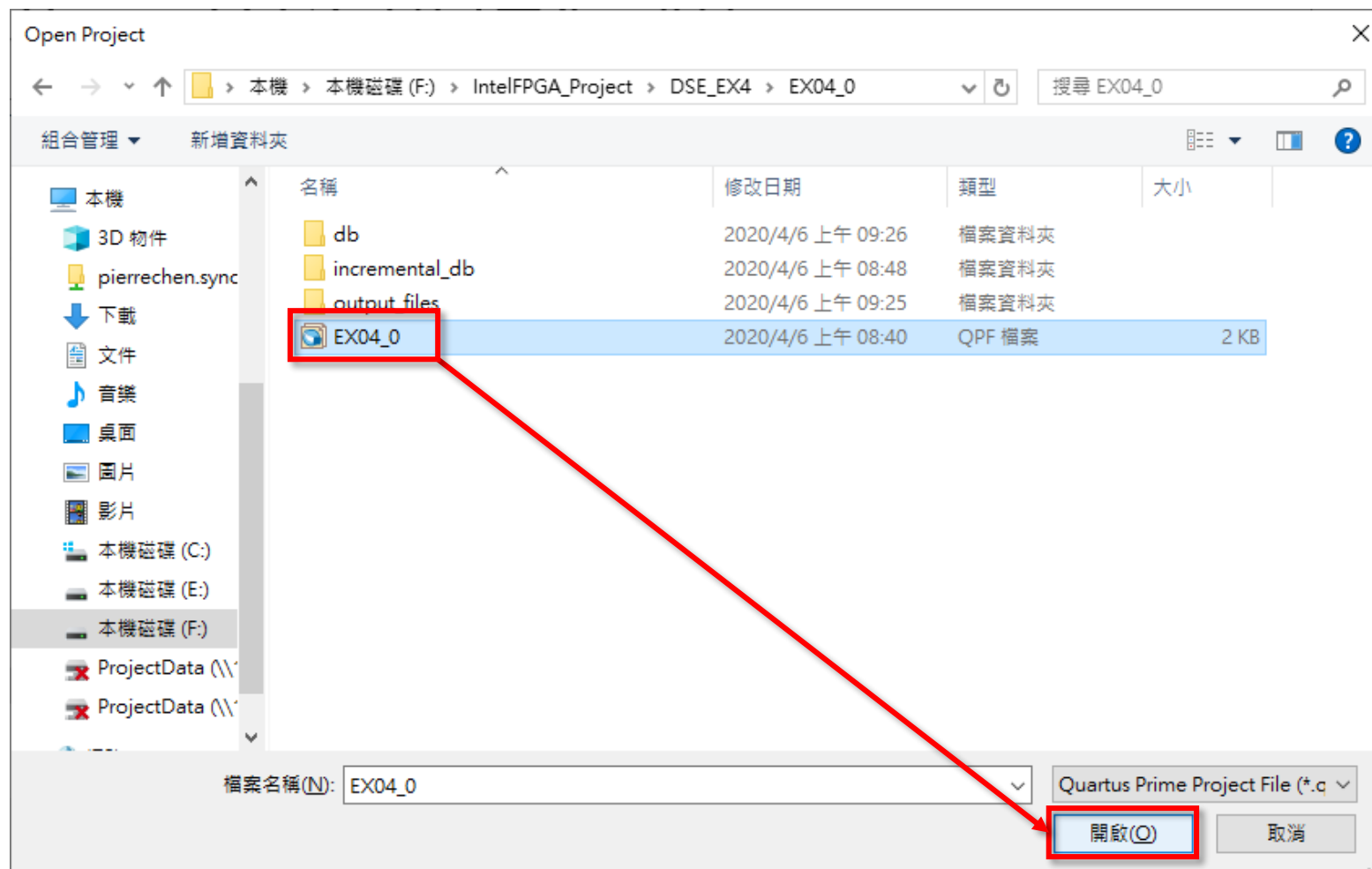
# Quartus Prime 區塊圖形編輯設計

- 開啟專案(1/3)



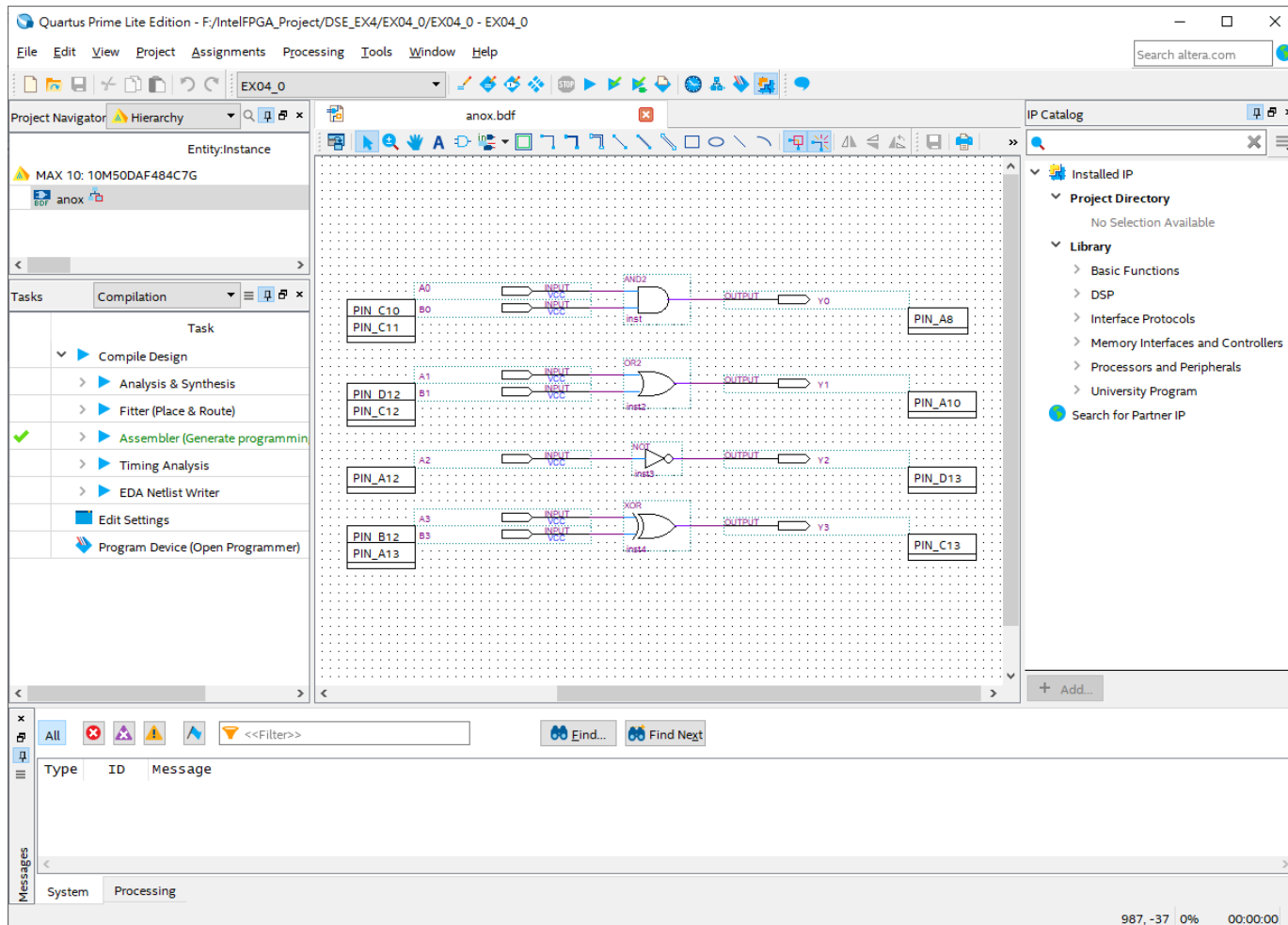
# Quartus Prime 區塊圖形編輯設計

- 開啟專案(2/3)



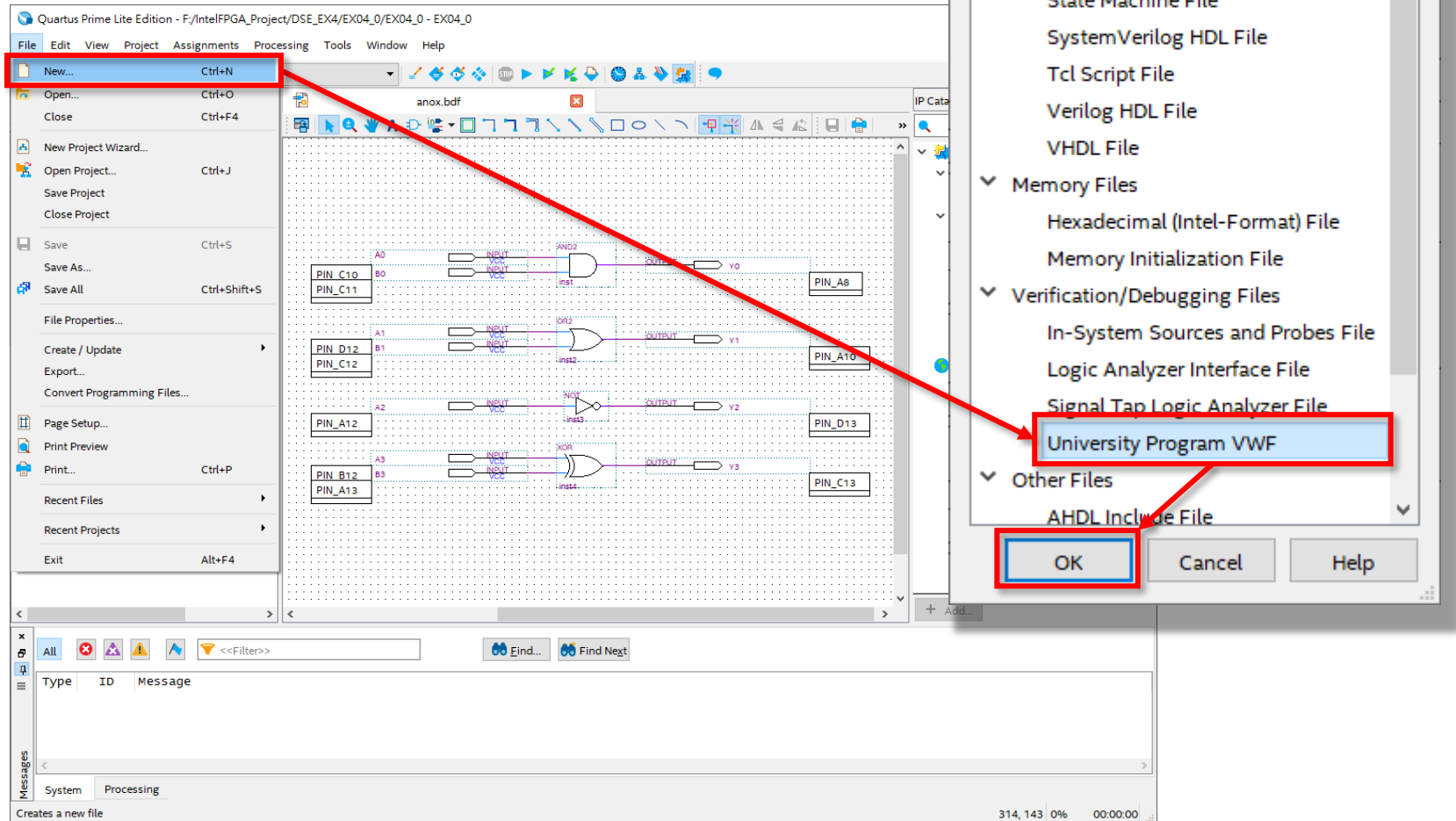
# Quartus Prime 區塊圖形編輯設計

- 開啟專案(3/3)



# Quartus Prime 電路功能模擬

- 新增Simulation Waveform Editor



# Quartus Prime 區塊圖形編輯設計

## • Insert Node(1/2)

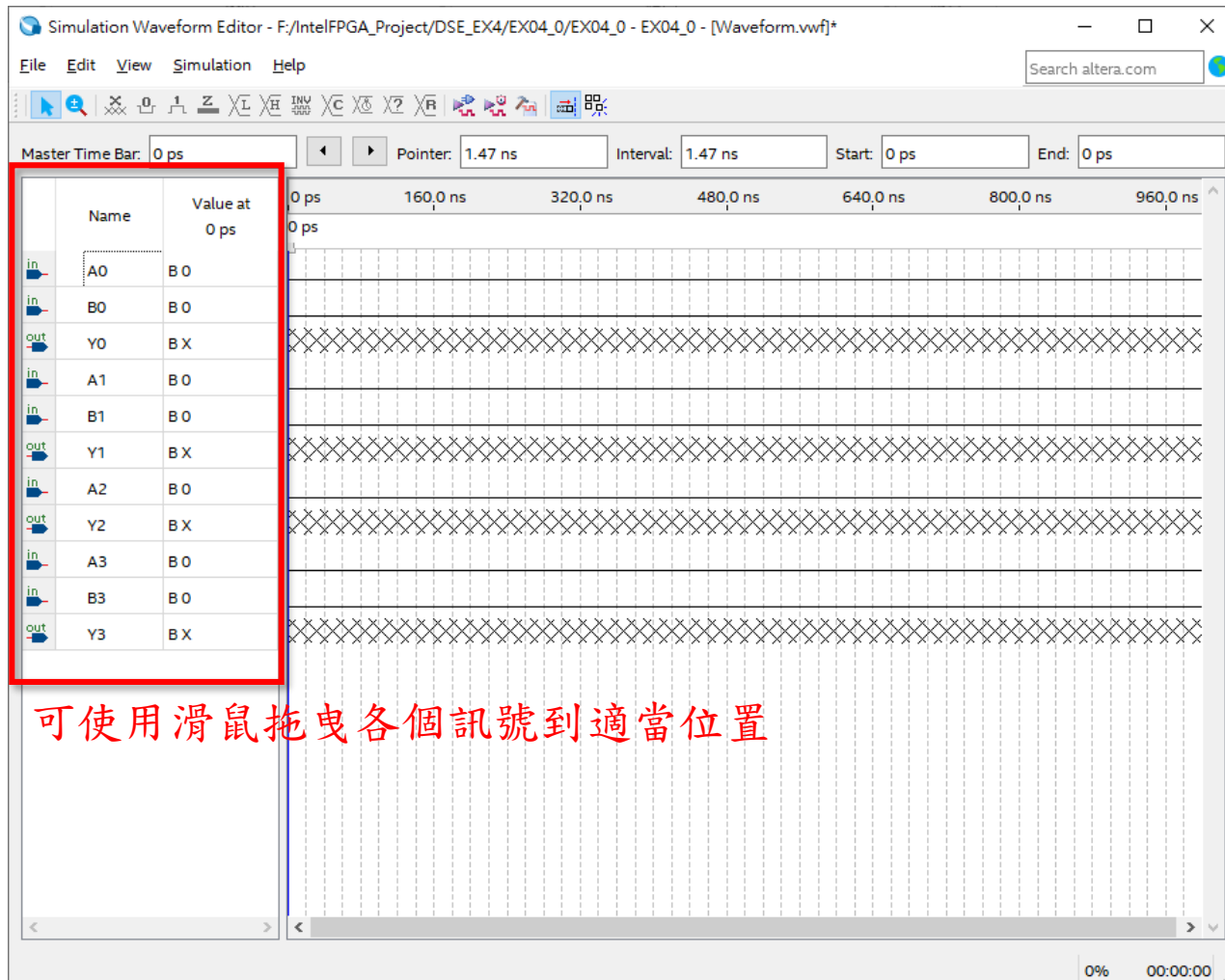
The screenshot illustrates the steps to insert a node in Quartus Prime. The main window is the Simulation Waveform Editor. The 'Edit' menu is open, and 'Insert Node or Bus...' is selected. This opens the 'Insert Node or Bus' dialog box. In this dialog, 'Name' is set to 'Use Node Finder to insert ...', 'Type' is 'INPUT', 'Value type' is '9-Level', 'Radix' is 'Binary', and 'Start index' is '0'. The 'Node Finder...' button is highlighted. Clicking it opens the 'Node Finder' dialog box. In the 'Node Finder' dialog, 'Named' is set to '\*' and 'Filter' is 'Pins: all'. The 'Look in' field is also set to '\*'. The 'List' button is highlighted. Clicking it displays a list of nodes found. The 'Nodes Found' table is as follows:

Name	Type
in A0	Input
in A1	Input
in A2	Input
in A3	Input
in B0	Input
in B1	Input
in B3	Input
out Y0	Output
out Y1	Output
out Y2	Output
out Y3	Output

The 'Selected Nodes' table is empty. The '>>' button is highlighted. Clicking it moves the selected nodes to the 'Selected Nodes' table. The 'OK' button in the 'Insert Node or Bus' dialog is highlighted, indicating the final step to insert the node.

# Quartus Prime 區塊圖形編輯設計

- Insert Node(2/2)





# Quartus Prime 區塊圖形編輯設計

- 設定所有 Input 訊號(1/3)

The screenshot shows the Quartus Prime Simulation Waveform Editor. The main window displays a list of signals on the left and a waveform editor on the right. The signals are:

Name	Value at 0 ps
in A0	B 0
in B0	B 0
out Y0	B X
in A1	B 0
in B1	B 0
out Y1	B X
in A2	B 0
out Y2	B X
in A3	B 0
in B3	B 0
out Y3	B X


The waveform editor shows a time axis from 0 ps to 640.0 ns. The signals are currently in a high-impedance state (X).

A red box highlights the 'Clock' button in the top toolbar. A red arrow points from this button to the 'Clock' dialog box. Another red arrow points from the 'Period' field in the dialog box to the 'A0' signal in the list. A third red arrow points from the 'Duty cycle (%)' field to the 'OK' button.

The 'Clock' dialog box is titled 'Clock' and has the following fields:

- Base waveform on time period
- Period: 100.0 ns
- Offset: 0.0 ns
- Duty cycle (%): 50
- OK button
- Cancel button

The 'OK' button is highlighted with a red box.

Name	Graphic symbol	Algebraic function	Truth table		
AND		$F = x \cdot y$	x	y	F
			0	0	0
			0	1	0
			1	0	0
			1	1	1

# Quartus Prime 區塊圖形編輯設計

- 設定所有 Input 訊號(1/3)

Simulation Waveform Editor - F:/IntelFPGA\_Project/DSE\_EX4/EX04\_0/EX04\_0 - EX04\_0 - [Waveform.vwf]\*

File Edit View Simulation Help

Master Time Bar: 0 ps Pointer: 27.97 ns Interval: 27.97 ns Start: 0

Base waveform on time period


Period: 100.0 ns

Offset: 25 ns

Duty cycle (%): 50

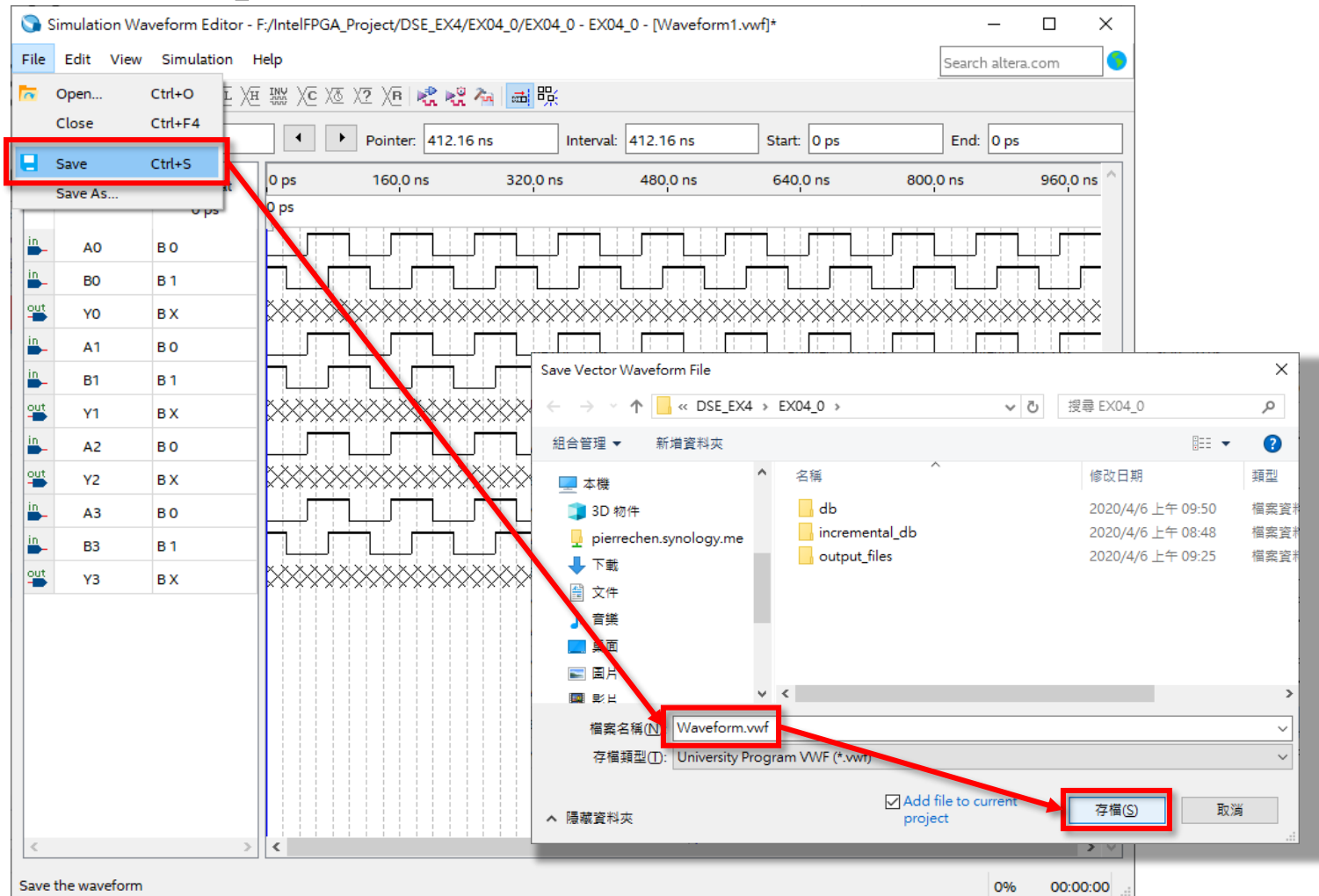
OK Cancel

依此類推，設定所有 Input 訊號

Name	Graphic symbol	Algebraic function	Truth table		
			x	y	F
AND		$F = x \cdot y$	0	0	0
			0	1	0
			1	0	0
			1	1	1

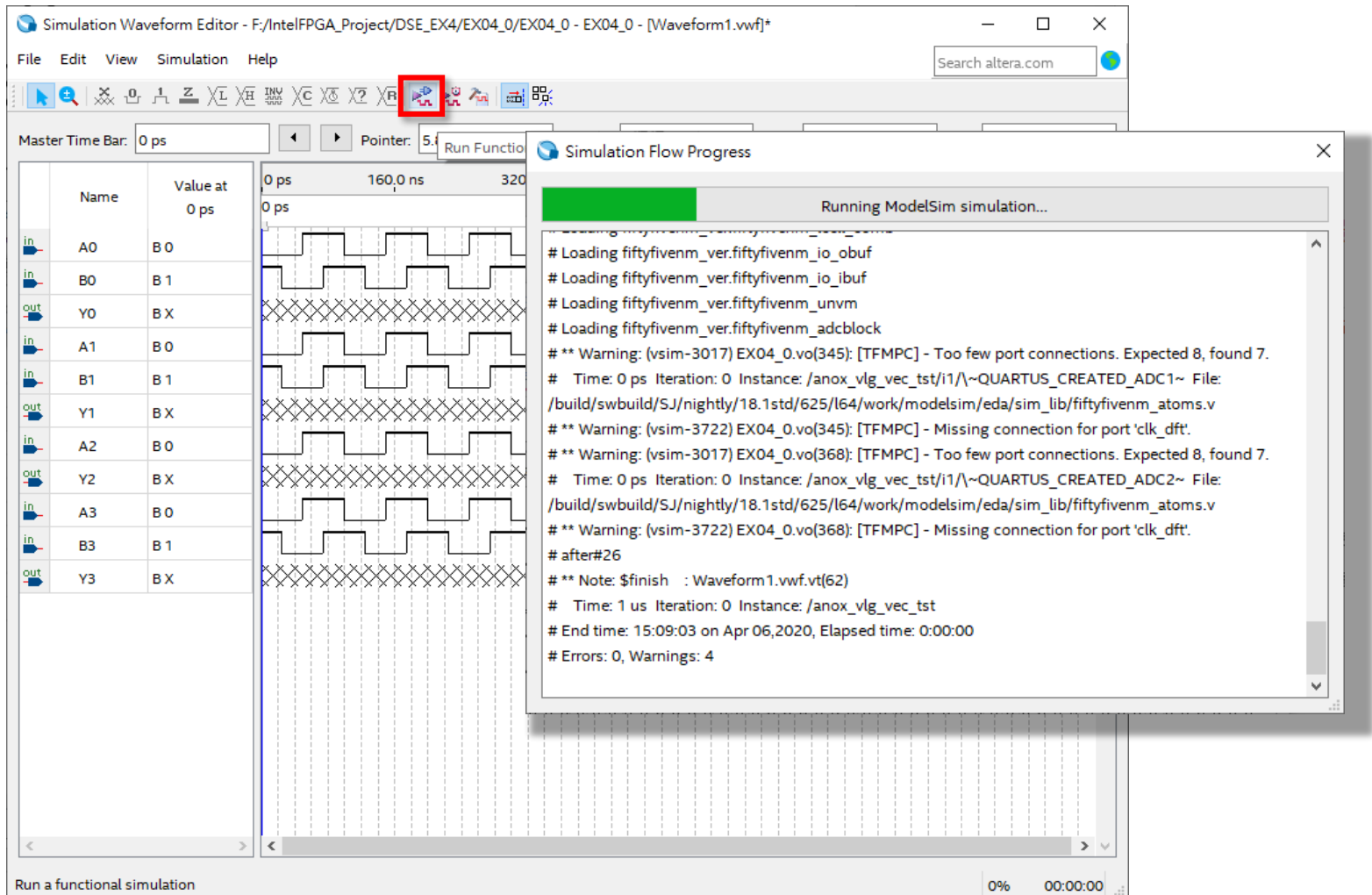
# Quartus Prime 區塊圖形編輯設計

- 設定所有 Input 訊號(3/3)



# Quartus Prime 區塊圖形編輯設計

- 開始模擬



Simulation Waveform Editor - F:/IntelFPGA\_Project/DSE\_EX4/EX04\_0/EX04\_0 - EX04\_0 - [Waveform1.vwf]\*

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: 5.4 Run Function

Name	Value at 0 ps
A0	B 0
B0	B 1
Y0	B X
A1	B 0
B1	B 1
Y1	B X
A2	B 0
Y2	B X
A3	B 0
B3	B 1
Y3	B X

Simulation Flow Progress

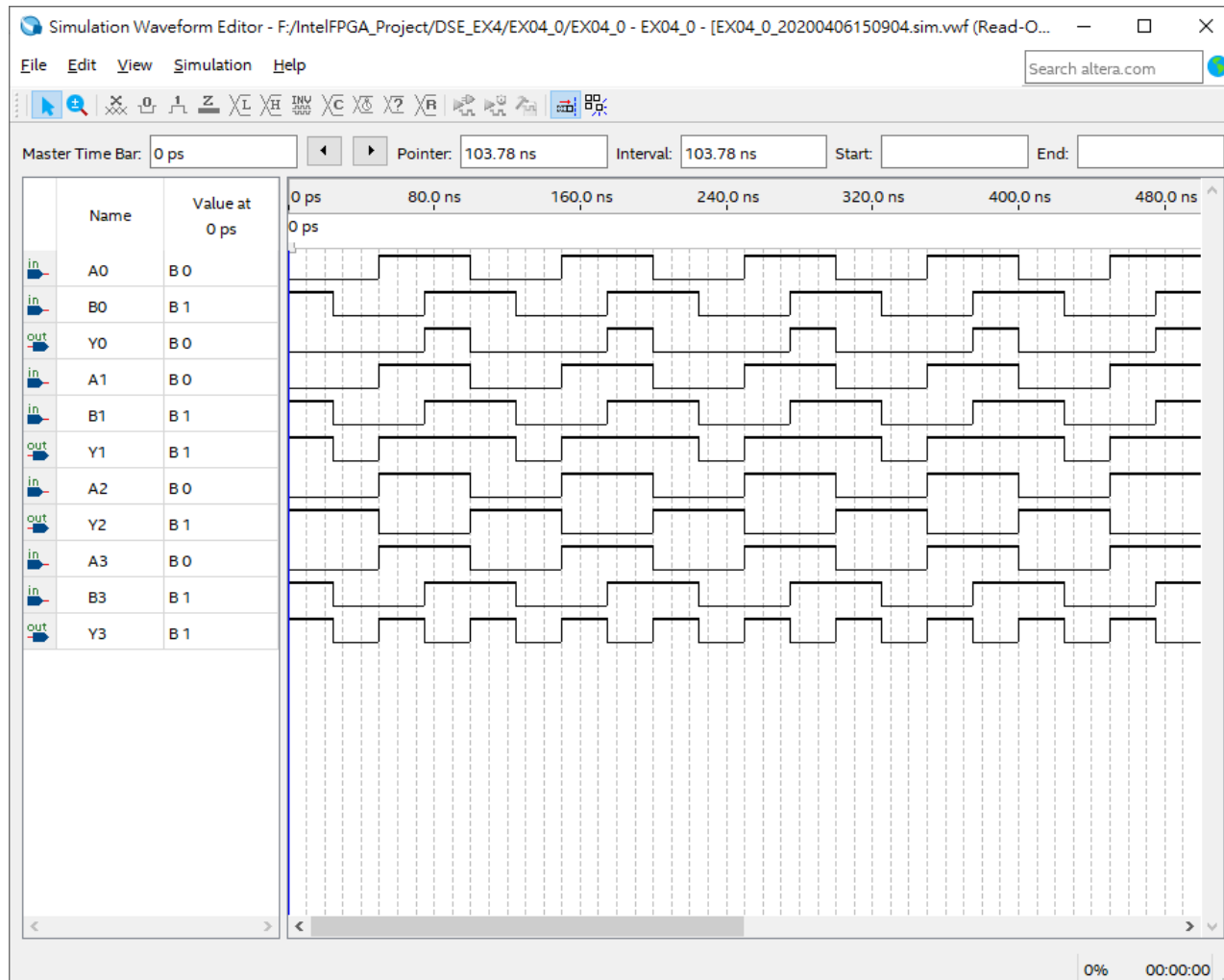
Running ModelSim simulation...

```
# Loading fiftyfivenm_ver.fiftyfivenm_io_obuf
# Loading fiftyfivenm_ver.fiftyfivenm_io_ibuf
# Loading fiftyfivenm_ver.fiftyfivenm_unvm
# Loading fiftyfivenm_ver.fiftyfivenm_adcblock
# ** Warning: (vsim-3017) EX04_0.vo(345): [TFMPC] - Too few port connections. Expected 8, found 7.
# Time: 0 ps Iteration: 0 Instance: /anox_vlg_vec_tst/i1/~QUARTUS_CREATED_ADC1~ File:
/build/swbuild/SJ/nightly/18.1std/625/l64/work/modelsim/eda/sim_lib/fiftyfivenm_atoms.v
# ** Warning: (vsim-3722) EX04_0.vo(345): [TFMPC] - Missing connection for port 'clk_dft'.
# ** Warning: (vsim-3017) EX04_0.vo(368): [TFMPC] - Too few port connections. Expected 8, found 7.
# Time: 0 ps Iteration: 0 Instance: /anox_vlg_vec_tst/i1/~QUARTUS_CREATED_ADC2~ File:
/build/swbuild/SJ/nightly/18.1std/625/l64/work/modelsim/eda/sim_lib/fiftyfivenm_atoms.v
# ** Warning: (vsim-3722) EX04_0.vo(368): [TFMPC] - Missing connection for port 'clk_dft'.
# after#26
# ** Note: $finish : Waveform1.vwf.vt(62)
# Time: 1 us Iteration: 0 Instance: /anox_vlg_vec_tst
# End time: 15:09:03 on Apr 06,2020, Elapsed time: 0:00:00
# Errors: 0, Warnings: 4
```

Run a functional simulation 0% 00:00:00

# Quartus Prime 區塊圖形編輯設計

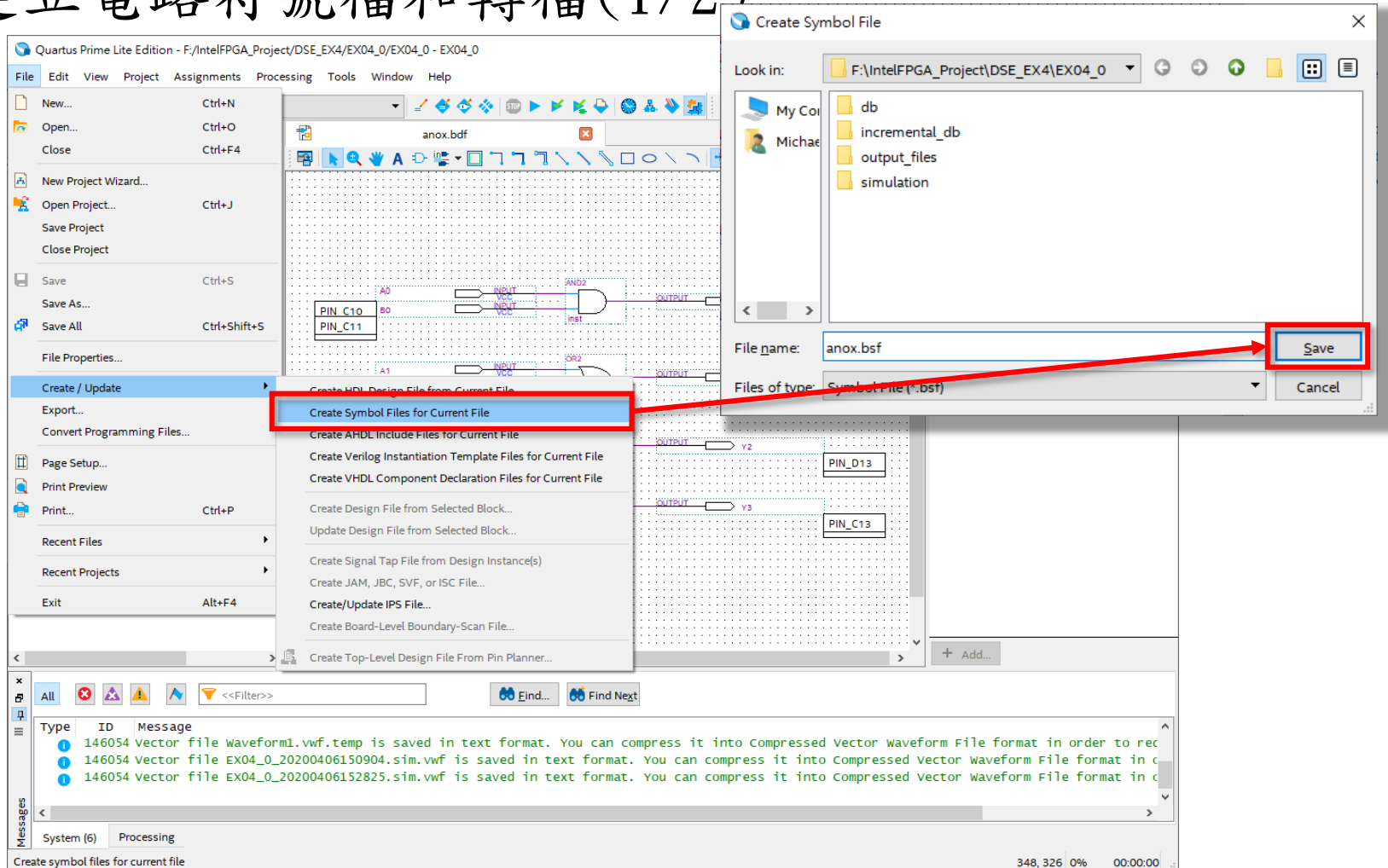
- 模擬結果



# Quartus Prime 補充

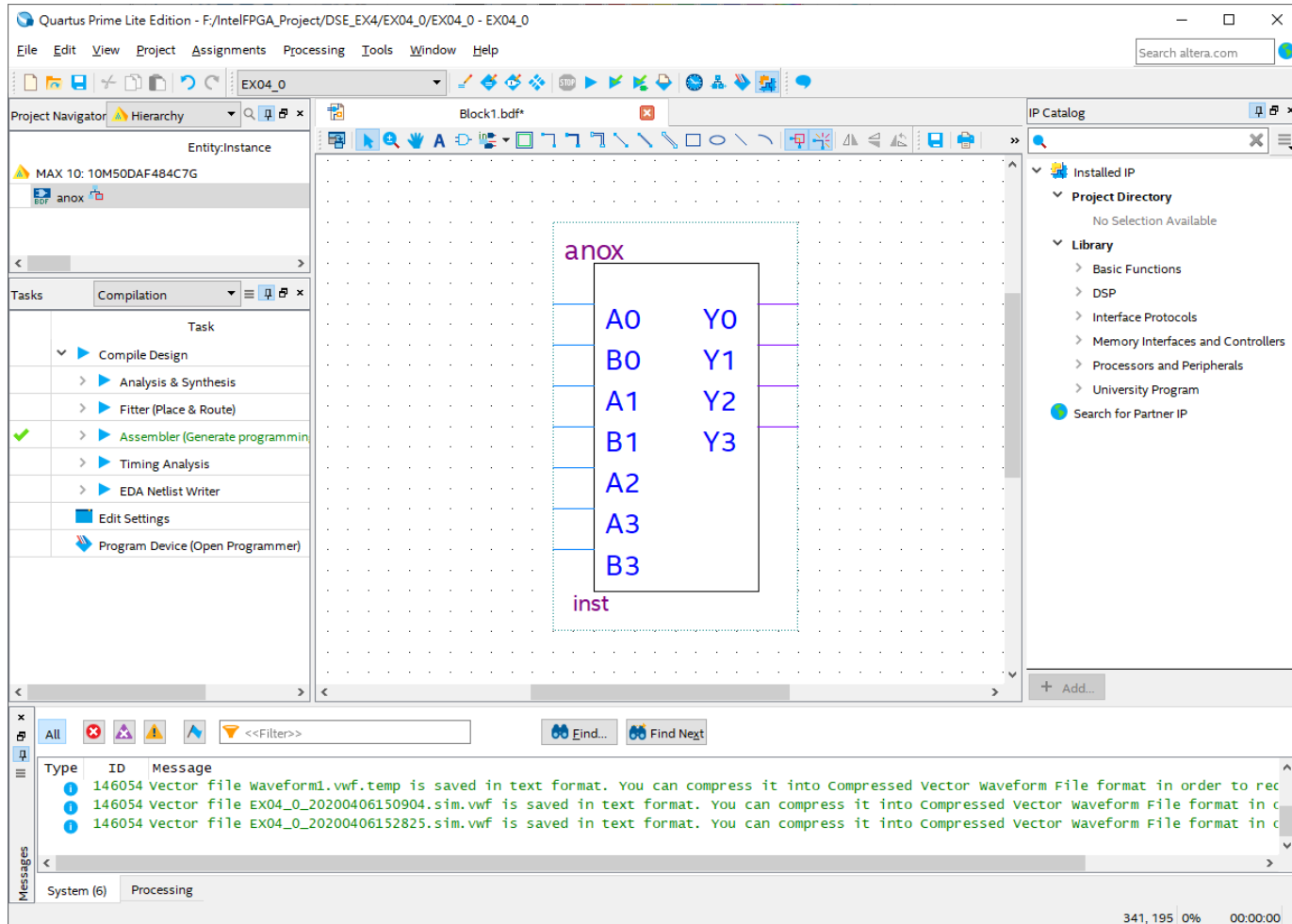
# Quartus Prime 補充(一)

- 建立電路符號檔和轉檔(1/2)



# Quartus Prime 補充(一)

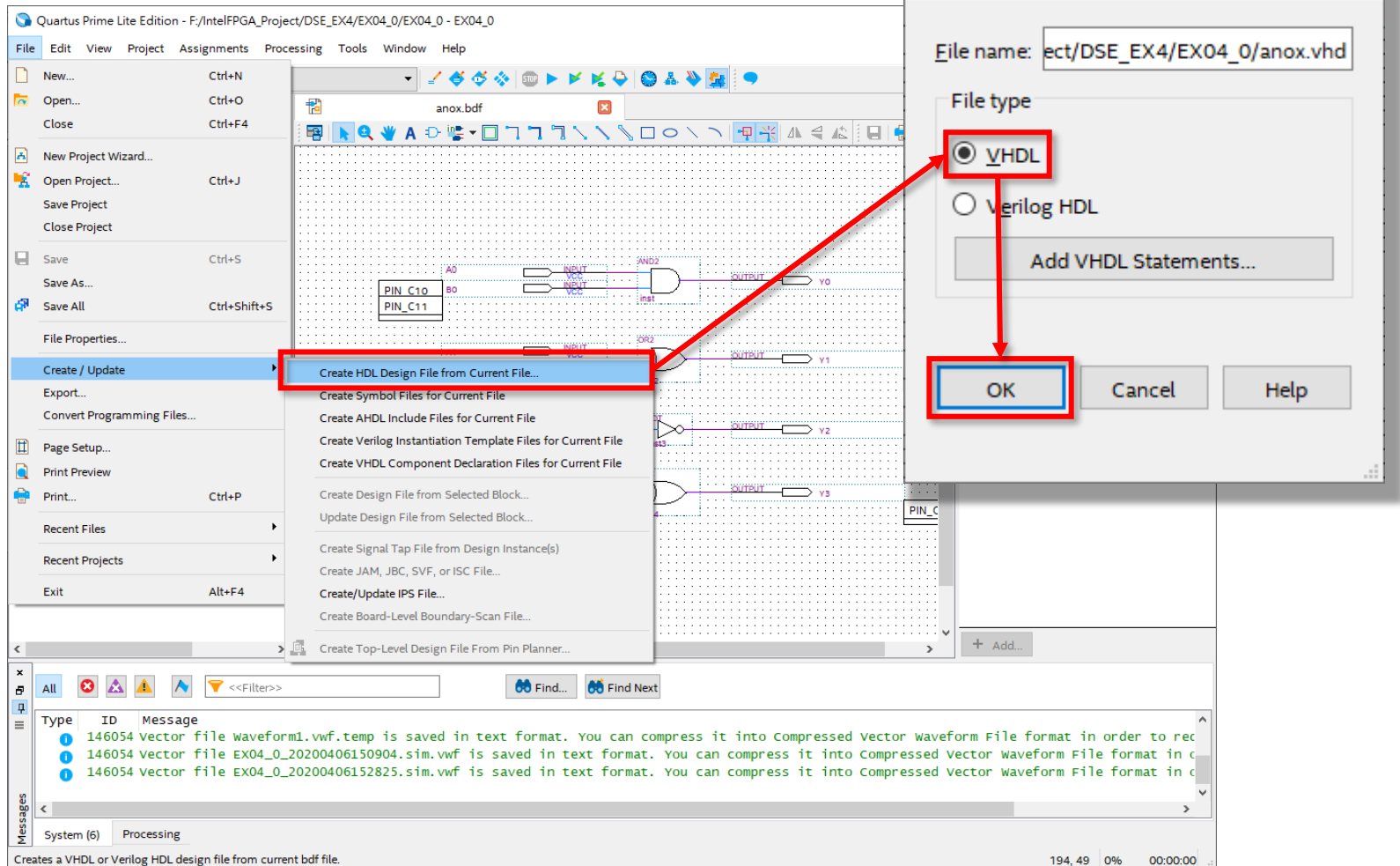
- 建立電路符號檔和轉檔(2/2)





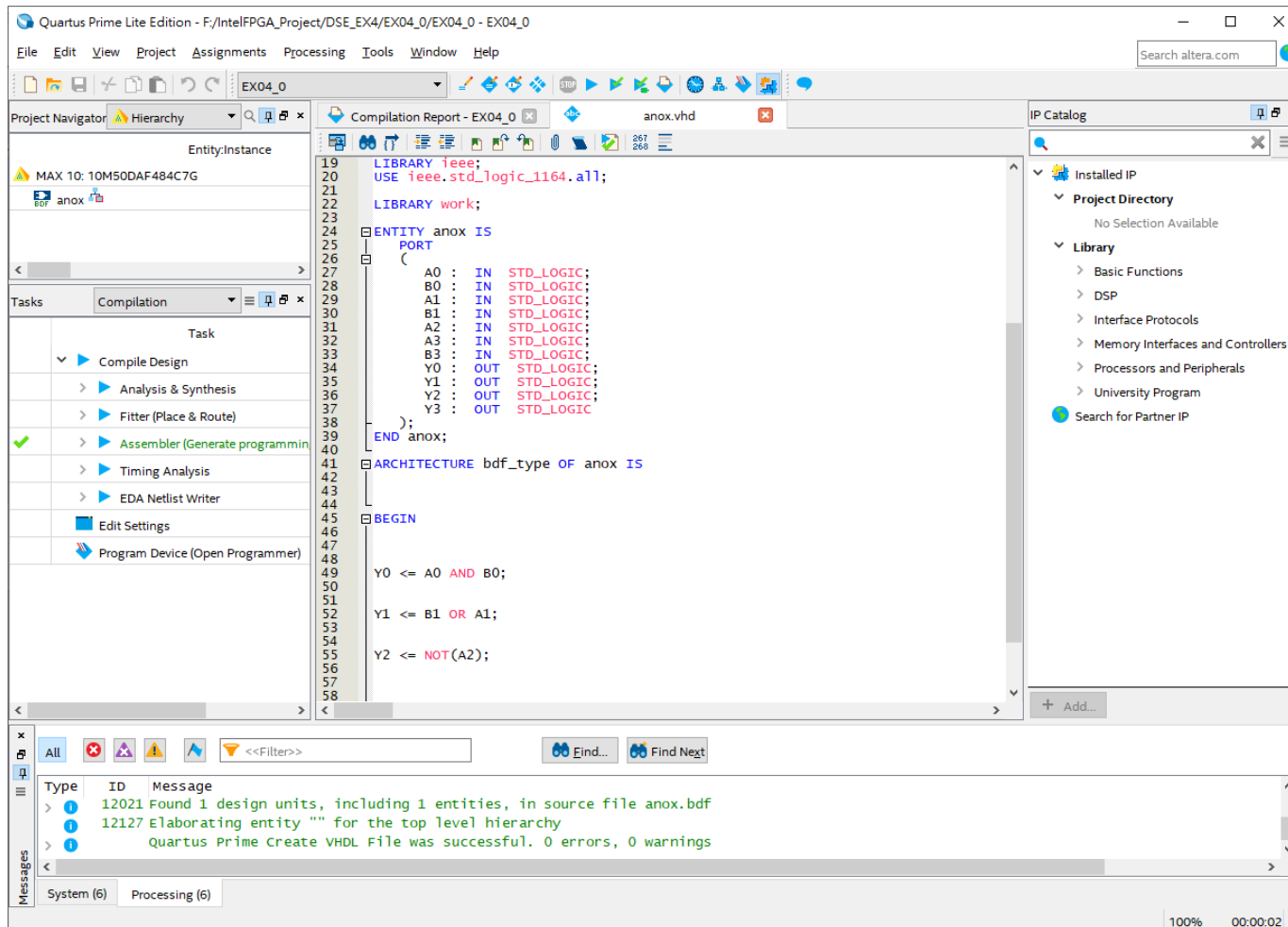
# Quartus Prime 補充(二)

- 轉檔(HDL)(1/2)



# Quartus Prime 補充(二)

- 轉檔(HDL)(2/2)



# 課堂練習

# 實驗一：Quartus操作練習

- 請完成下列邏輯表示式之：
  - a) 真值表
  - b) 最簡SOP
  - c) 電路設計並下載至DE10-Lite
  - d) 模擬波形圖

$$Y(A, B, C, D) = \sum(0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14)$$

- Pin Definition : A(C12) 、 B(D12) 、 C(C11) 、 D(C10) 、 Y(A8) 、
- 本次實驗需助教確認正確，並將專案跟文件資料(真值表、最簡SOP …)壓縮上傳EE-Class。
- Lecture4\_組別XX.ZIP