

數位系統實驗

作業九

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數位系統實驗

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實驗一：三對八解碼器（包含效能控制）

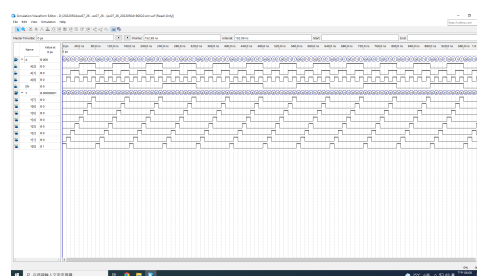
- 實驗結果照片：

```

1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3
4  ENTITY DECODER3_8 IS
5  PORT( EN :IN STD_LOGIC;
6        A :IN STD_LOGIC_VECTOR(2 DOWNTO 0);
7        Y :OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
8  END DECODER3_8;
9
10 ARCHITECTURE ARCH OF DECODER3_8 IS
11     SIGNAL TMP :STD_LOGIC_VECTOR(3 DOWNTO 0);
12 BEGIN
13     WITH A SELECT
14     Y <= "10000000" WHEN "111",
15          "01000000" WHEN "110",
16          "00100000" WHEN "101",
17          "00010000" WHEN "100",
18          "00001000" WHEN "011",
19          "00000100" WHEN "010",
20          "00000010" WHEN "001",
21          "00000001" WHEN "000";
22 END ARCH;

```

VHDL



波形圖

實驗二：八對三編碼器

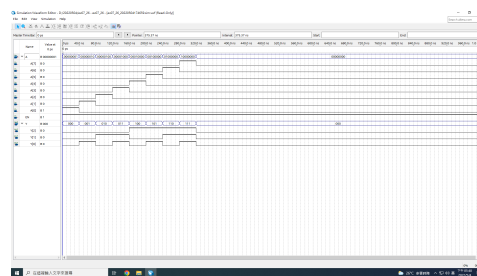
- 實驗結果照片：

```

1  Library IEEE;
2  Use IEEE.std_logic_1164.all;
3
4  Entity Encoder_8_to_3 is
5  Port(EN: in std_logic;
6        A: in std_logic_vector(7 downto 0);
7        Y: out std_logic_vector(2 downto 0));
8  End Encoder_8_to_3;
9
10 Architecture ARCH of Encoder_8_to_3 is
11 Begin
12 Process(EN, A)
13 Begin
14     if (EN='1') and (A="10000000") then Y <= "111";
15     elsif (EN='1') and (A="01000000") then Y <= "110";
16     elsif (EN='1') and (A="00100000") then Y <= "101";
17     elsif (EN='1') and (A="00010000") then Y <= "100";
18     elsif (EN='1') and (A="00001000") then Y <= "011";
19     elsif (EN='1') and (A="00000100") then Y <= "010";
20     elsif (EN='1') and (A="00000010") then Y <= "001";
21     else Y <= "000";
22     End if;
23 End Process;
24 End ARCH;
25
26

```

VHDL



波形圖

實驗三：八對一多工器

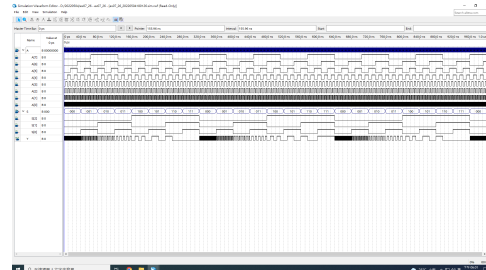
- 實驗結果照片：

```

1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3
4  ENTITY MUX8_1 IS
5      PORT (A :IN STD_LOGIC_VECTOR(7 DOWNTO 0);
6            S :IN STD_LOGIC_VECTOR(2 DOWNTO 0);
7            Y :OUT STD_LOGIC);
8  END MUX8_1;
9
10 ARCHITECTURE ARCH OF MUX8_1 IS
11 BEGIN
12     WITH S SELECT
13     Y <= A(0) WHEN "000",
14         A(1) WHEN "001",
15         A(2) WHEN "010",
16         A(3) WHEN "011",
17         A(4) WHEN "100",
18         A(5) WHEN "101",
19         A(6) WHEN "110",
20         A(7) WHEN OTHERS;
21 END ARCH;

```

VHDL



波形圖

實驗四：一對八解多工器

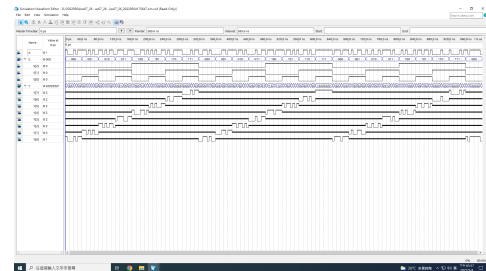
- 實驗結果照片：

```

1  Library IEEE;
2  Use IEEE.std_logic_1164.all;
3
4  Entity DeMUX1_8 is
5      Port ( A: in std_logic;
6            S: in std_logic_vector(2 downto 0);
7            Y: out std_logic_vector(7 downto 0) );
8  End DeMUX1_8;
9
10 Architecture ARCH of DeMUX1_8 is
11 Begin
12     Y(0) <= A when S="000" else 'Z';
13     Y(1) <= A when S="001" else 'Z';
14     Y(2) <= A when S="010" else 'Z';
15     Y(3) <= A when S="011" else 'Z';
16     Y(4) <= A when S="100" else 'Z';
17     Y(5) <= A when S="101" else 'Z';
18     Y(6) <= A when S="110" else 'Z';
19     Y(7) <= A when S="111" else 'Z';
20 End ARCH;
21
22

```

VHDL



波形圖