

數位系統實驗

作業十

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實驗一：二進位計數器設計

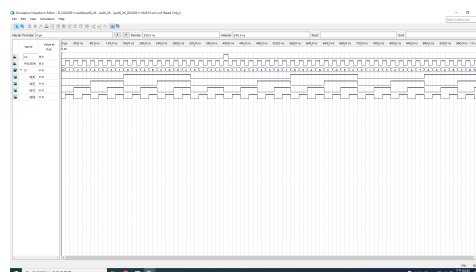
- 實驗結果照片：

```
1  LIBRARY IEEE;  
2  USE IEEE.STD_LOGIC_1164.ALL;  
3  
4  ENTITY DFF1 IS  
5  PORT ( CL,CK,T:IN STD_LOGIC;  
6        Q,QBAR:OUT STD_LOGIC );  
7  END DFF1;  
8  
9  ARCHITECTURE ARCH OF DFF1 IS  
10 BEGIN  
11   PROCESS(CL,CK)  
12     VARIABLE TMP:STD_LOGIC;  
13     BEGIN  
14       IF CL='1' THEN TMP := '0';  
15       ELIF RISING_EDGE(CK) THEN  
16         IF T='1' THEN TMP := NOT TMP;  
17         ELSE NULL;  
18       END IF;  
19     END IF;  
20     Q <= TMP;  
21     QBAR <= NOT TMP;  
22   END PROCESS;  
23 END ARCH;
```

VHDL

```
1  LIBRARY IEEE;  
2  USE IEEE.STD_LOGIC_1164.ALL;  
3  
4  ENTITY DFF1 IS  
5  PORT ( CL,CK,T:IN STD_LOGIC;  
6        Q,QBAR:OUT STD_LOGIC );  
7  END DFF1;  
8  
9  ARCHITECTURE ARCH OF DFF1 IS  
10 BEGIN  
11   PROCESS(CL,CK)  
12     VARIABLE TMP:STD_LOGIC;  
13     BEGIN  
14       IF CL='1' THEN TMP := '0';  
15       ELIF RISING_EDGE(CK) THEN  
16         IF T='1' THEN TMP := NOT TMP;  
17         ELSE NULL;  
18       END IF;  
19     END IF;  
20     Q <= TMP;  
21     QBAR <= NOT TMP;  
22   END PROCESS;  
23 END ARCH;
```

DFF1



波形圖

實驗二：二進位上/下計數器設計

- 實驗結果照片：

```

1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3  ENTITY UDC_4B IS
4  PORT( CL, UD, PULSEIN: IN STD_LOGIC;
5        Q: OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
6  END UDC_4B;
7
8  ARCHITECTURE ARCH OF UDC_4B IS
9  COMPONENT DFF1
10 PORT( CL, CK, T: IN STD_LOGIC;
11       Q, QBAR: OUT STD_LOGIC);
12 END COMPONENT;
13 SIGNAL TMP: STD_LOGIC_VECTOR(4 DOWNTO 0);
14 BEGIN
15   TMP(0) <= PULSEIN;
16   LP1:FOR I IN 0 TO 3 GENERATE
17     U: DFF1 PORT MAP (CL, TMP(I) XOR UD, '1', Q(I), TMP(I+1));
18   END GENERATE;
19 END ARCH;

```

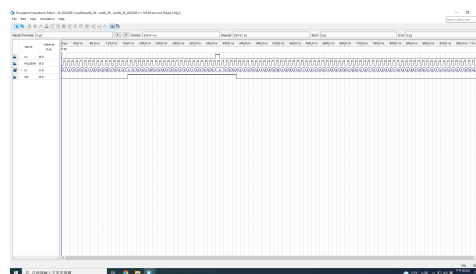
VHDL

```

1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3
4  ENTITY DFF1 IS
5  PORT( CL,CK,T:IN STD_LOGIC;
6        Q, QBAR:OUT STD_LOGIC );
7  END DFF1;
8
9  ARCHITECTURE ARCH OF DFF1 IS
10 BEGIN
11   PROCESS(CL,CK)
12   VARIABLE TMP:STD_LOGIC;
13   BEGIN
14     IF CL='1' THEN TMP := '0';
15     ELIF RISING_EDGE(CK) THEN
16       IF T='1' THEN TMP := NOT TMP;
17       ELSE NULL;
18     END IF;
19   END IF;
20   Q <= TMP;
21   QBAR <= NOT TMP;
22 END PROCESS;
23 END ARCH;

```

DFF1



波形圖

實驗三：除N計數器設計， $N = 12$

- 實驗結果照片：

```

1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3
4  ENTITY MOD12 IS
5  PORT( PULSEIN :IN STD_LOGIC;
6        Q :OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
7  END MOD12;
8
9  ARCHITECTURE ARCH OF MOD12 IS
10 COMPONENT DFF1
11 PORT( CL, CK, T:IN STD_LOGIC;
12       Q, QBAR :OUT STD_LOGIC);
13 END COMPONENT;
14
15 SIGNAL CL : STD_LOGIC;
16 SIGNAL TMP1 : STD_LOGIC_VECTOR(4 DOWNTO 0);
17 SIGNAL TMP2 : STD_LOGIC_VECTOR(3 DOWNTO 0);
18
19 BEGIN
20     TMP1(0) <= PULSEIN;
21     LP1: FOR I IN 0 TO 3 GENERATE
22     U: DFF1 PORT MAP (CL, TMP1(I), '1', TMP2(I), TMP1(I + 1));
23     END GENERATE;
24     CL <= TMP2(3) AND TMP2(2);
25     Q <= TMP2;
26 END ARCH;

```

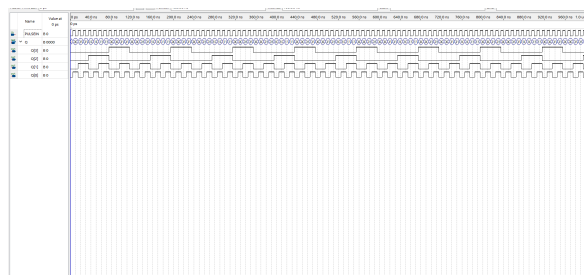
VHDL

```

1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3
4  ENTITY DFF1 IS
5  PORT( CL, CK, T:IN STD_LOGIC;
6        Q, QBAR:OUT STD_LOGIC );
7  END DFF1;
8
9  ARCHITECTURE ARCH OF DFF1 IS
10 BEGIN
11     PROCESS(CL, CK)
12     VARIABLE TMP:STD_LOGIC;
13     BEGIN
14         IF CL='1' THEN TMP := '0';
15         ELIF RISING_EDGE(CK) THEN
16             IF T='1' THEN TMP := NOT TMP;
17             ELSE NULL;
18         END IF;
19     END IF;
20     Q <= TMP;
21     QBAR <= NOT TMP;
22 END PROCESS;
23 END ARCH;

```

DFF1



波形圖

實驗四：BCD計數器設計

- 實驗結果照片：

```

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY BCD_COUNTER IS
    RESET : IN STD_LOGIC;
    CLOCK : IN STD_LOGIC;
    ZERO : OUT STD_LOGIC;
    NINE : OUT STD_LOGIC;
    BCD_OUT : OUT STD_LOGIC_VECTOR(3 DOWNTO 0);
END ENTITY BCD_COUNTER;

ARCHITECTURE ARCH OF BCD_COUNTER IS
    SIGNAL COUNT : STD_LOGIC_VECTOR(3 DOWNTO 0) := "0000";
    SIGNAL ZERO_FLAG : STD_LOGIC := '0';
    SIGNAL NINE_FLAG : STD_LOGIC := '0';
    SIGNAL BCD_OUT_SIGNAL : STD_LOGIC_VECTOR(3 DOWNTO 0);
    SIGNAL CARRY : STD_LOGIC := '0';

    -- Zero detection
    ZERO_FLAG <= COUNT(3) AND COUNT(2) AND COUNT(1) AND COUNT(0);

    -- Nine detection
    NINE_FLAG <= COUNT(3) AND COUNT(2) AND COUNT(1) AND NOT COUNT(0);

    -- BCD output
    BCD_OUT_SIGNAL <= COUNT;

    -- Counter logic
    PROCESS (CLOCK)
        BEGIN
            IF RISING_EDGE(CLOCK) THEN
                IF RESET = '1' THEN
                    COUNT <= "0000";
                ELSE
                    COUNT <= COUNT + 1;
                    IF COUNT = "1001" THEN
                        COUNT <= "0000";
                    END IF;
                END IF;
            END IF;
        END PROCESS;

        -- Zero output
        ZERO <= ZERO_FLAG;

        -- Nine output
        NINE <= NINE_FLAG;

        -- BCD output
        BCD_OUT <= BCD_OUT_SIGNAL;
    END ARCHITECTURE ARCH;

```

VHDL-1

```

-- VHDL-2: BCD Counter with 7-segment display output
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY BCD_COUNTER_2 IS
    RESET : IN STD_LOGIC;
    CLOCK : IN STD_LOGIC;
    ZERO : OUT STD_LOGIC;
    NINE : OUT STD_LOGIC;
    BCD_OUT : OUT STD_LOGIC_VECTOR(3 DOWNTO 0);
    SEGMENT_A : OUT STD_LOGIC;
    SEGMENT_B : OUT STD_LOGIC;
    SEGMENT_C : OUT STD_LOGIC;
    SEGMENT_D : OUT STD_LOGIC;
    SEGMENT_E : OUT STD_LOGIC;
    SEGMENT_F : OUT STD_LOGIC;
END ENTITY BCD_COUNTER_2;

ARCHITECTURE ARCH OF BCD_COUNTER_2 IS
    SIGNAL COUNT : STD_LOGIC_VECTOR(3 DOWNTO 0) := "0000";
    SIGNAL ZERO_FLAG : STD_LOGIC := '0';
    SIGNAL NINE_FLAG : STD_LOGIC := '0';
    SIGNAL BCD_OUT_SIGNAL : STD_LOGIC_VECTOR(3 DOWNTO 0);
    SIGNAL CARRY : STD_LOGIC := '0';

    -- Zero detection
    ZERO_FLAG <= COUNT(3) AND COUNT(2) AND COUNT(1) AND COUNT(0);

    -- Nine detection
    NINE_FLAG <= COUNT(3) AND COUNT(2) AND COUNT(1) AND NOT COUNT(0);

    -- BCD output
    BCD_OUT_SIGNAL <= COUNT;

    -- Counter logic
    PROCESS (CLOCK)
        BEGIN
            IF RISING_EDGE(CLOCK) THEN
                IF RESET = '1' THEN
                    COUNT <= "0000";
                ELSE
                    COUNT <= COUNT + 1;
                    IF COUNT = "1001" THEN
                        COUNT <= "0000";
                    END IF;
                END IF;
            END IF;
        END PROCESS;

        -- Zero output
        ZERO <= ZERO_FLAG;

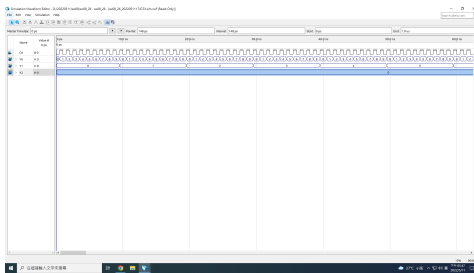
        -- Nine output
        NINE <= NINE_FLAG;

        -- BCD output
        BCD_OUT <= BCD_OUT_SIGNAL;

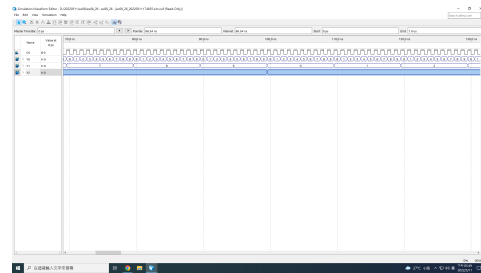
        -- 7-segment display outputs
        SEGMENT_A <= COUNT(3);
        SEGMENT_B <= COUNT(2);
        SEGMENT_C <= COUNT(1);
        SEGMENT_D <= COUNT(0);
        SEGMENT_E <= COUNT(3) XOR COUNT(2);
        SEGMENT_F <= COUNT(2) XOR COUNT(1);
    END ARCHITECTURE ARCH;

```

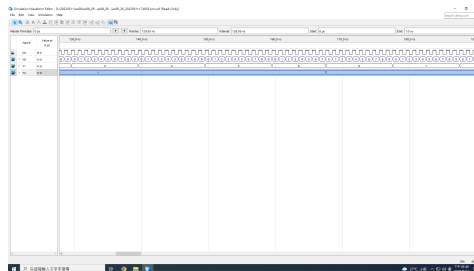
VHDL-2



波形圖-1



波形圖-2



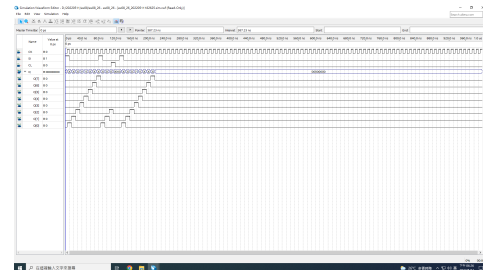
波形圖-3

實驗六：移位暫存器設計

- 實驗結果照片：

```
1  LIBRARY IEEE;  
2  USE IEEE.STD_LOGIC_1164.ALL;  
3  
4  ENTITY SREGISTER IS  
5  PORT ( SI, CK, CL: STD_LOGIC;  
6        Q:OUT STD_LOGIC_VECTOR(7 DOWNTO 0));  
7  END SREGISTER;  
8  
9  ARCHITECTURE ARCH OF SREGISTER IS  
10 BEGIN  
11   PROCESS(SI, CK, CL)  
12   VARIABLE REGT: STD_LOGIC_VECTOR(7 DOWNTO 0);  
13   BEGIN  
14     IF RISING_EDGE(CK) THEN  
15       IF CL='1' THEN  
16         REGT := "00000000";  
17       ELSE  
18         REGT := REGT(6 DOWNTO 0) & SI;  
19       END IF;  
20       Q <= REGT;  
21     END IF;  
22   END PROCESS;  
23 END ARCH;
```

VHDL



波形圖