數位系統實驗

作業十

組員：

109601003 林群賀、109601005 謝文喨

2022-0511

數位系統實驗

作業十

實驗一：二進位計數器設計

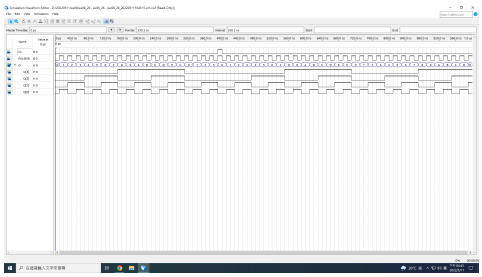
- 實驗結果照片：

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY DFF1 IS
   PORT( CL,CK,T:IN STD_LOGIC;
         Q, QBAR:OUT STD_LOGIC );
END DFF1;

ARCHITECTURE ARCH OF DFF1 IS
BEGIN
   PROCESS(CL,CK)
      VARIABLE TMP:STD_LOGIC;
      BEGIN
         IF CL='1' THEN TMP := '0';
         ELSIF RISING_EDGE(CK) THEN
            IF T='1' THEN TMP := NOT TMP;
            ELSE NULL;
         END IF;
      END IF;
      Q <= TMP;
      QBAR <= NOT TMP;
   END PROCESS;
END ARCH;
```

VHDL

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY DFF1 IS
   PORT( CL,CK,T:IN STD_LOGIC;
         Q, QBAR:OUT STD_LOGIC );
END DFF1;

ARCHITECTURE ARCH OF DFF1 IS
BEGIN
   PROCESS(CL,CK)
      VARIABLE TMP:STD_LOGIC;
      BEGIN
         IF CL='1' THEN TMP := '0';
         ELSIF RISING_EDGE(CK) THEN
            IF T='1' THEN TMP := NOT TMP;
            ELSE NULL;
         END IF;
      END IF;
      Q <= TMP;
      QBAR <= NOT TMP;
   END PROCESS;
END ARCH;
```

DFF1



波形圖

實驗二：二進位上/下計數器設計

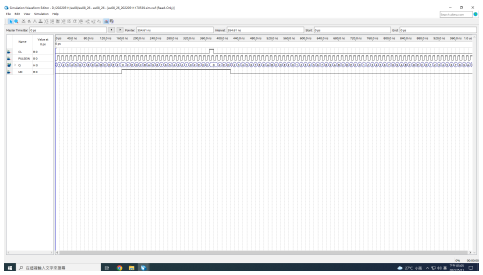
- 實驗結果照片：

```vhdl
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY UDC_4B IS
   PORT( CL, UD, PULSEIN: IN STD_LOGIC;
                          Q: OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
END UDC_4B;

ARCHITECTURE ARCH OF UDC_4B IS
   COMPONENT DFF1
      PORT( CL, CK, T: IN STD_LOGIC;
                Q, QBAR : OUT STD_LOGIC);
   END COMPONENT ;
   SIGNAL TMP: STD_LOGIC_VECTOR(4 DOWNTO 0);
BEGIN
   TMP(0) <= PULSEIN;
   LP1:FOR I IN 0 TO 3 GENERATE
      U: DFF1 PORT MAP (CL, TMP(I) XOR UD, '1', Q(I), TMP(I+1));
   END GENERATE;
END ARCH;
```

VHDL

```vhdl
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY DFF1 IS
   PORT( CL,CK,T:IN STD_LOGIC;
         Q, QBAR:OUT STD_LOGIC );
END DFF1;

ARCHITECTURE ARCH OF DFF1 IS
BEGIN
   PROCESS(CL,CK)
      VARIABLE TMP:STD_LOGIC;
      BEGIN
         IF CL='1' THEN TMP := '0';
         ELSIF RISING_EDGE(CK) THEN
            IF T='1' THEN TMP := NOT TMP;
            ELSE NULL;
         END IF;
      END IF;
      Q <= TMP;
      QBAR <= NOT TMP;
   END PROCESS;
END ARCH;
```

DFF1



波形圖

實驗三：除N計數器設計，N = 12

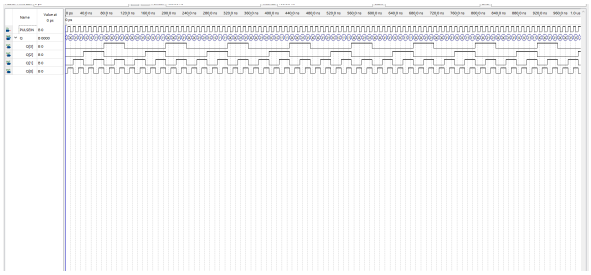
- 實驗結果照片：

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY MOD12 IS
   PORT( PULSEIN :IN STD_LOGIC;
         Q :OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
END MOD12;

ARCHITECTURE ARCH OF MOD12 IS
   COMPONENT DFF1
      PORT(CL, CK, T:IN STD_LOGIC;
           Q , QBAR :OUT STD_LOGIC);
   END COMPONENT;

   SIGNAL CL : STD_LOGIC;
   SIGNAL TMP1 : STD_LOGIC_VECTOR(4 DOWNTO 0);
   SIGNAL TMP2 : STD_LOGIC_VECTOR(3 DOWNTO 0);

BEGIN
      TMP1(0) <= PULSEIN;
      LP1: FOR I IN 0 TO 3 GENERATE
         U: DFF1 PORT MAP (CL, TMP1(I), '1', TMP2(I), TMP1(I + 1));
      END GENERATE;
      CL <= TMP2(3) AND TMP2(2);
      Q <= TMP2;
END ARCH;
```

VHDL

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY DFF1 IS
   PORT( CL,CK,T:IN STD_LOGIC;
         Q, QBAR:OUT STD_LOGIC );
END DFF1;

ARCHITECTURE ARCH OF DFF1 IS
BEGIN
   PROCESS(CL,CK)
      VARIABLE TMP:STD_LOGIC;
      BEGIN
         IF CL='1' THEN TMP := '0';
         ELSIF RISING_EDGE(CK) THEN
            IF T='1' THEN TMP := NOT TMP;
            ELSE NULL;
         END IF;
      END IF;
      Q <= TMP;
      QBAR <= NOT TMP;
   END PROCESS;
END ARCH;
```

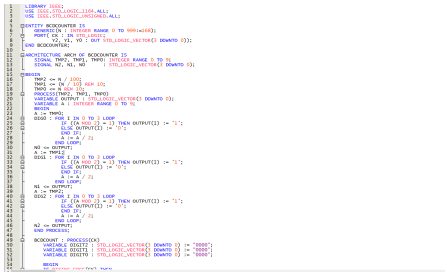
DFF1



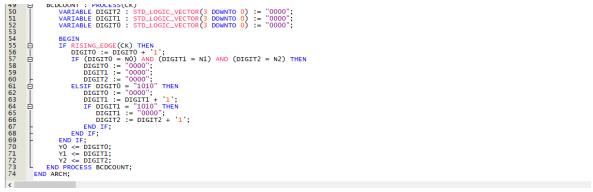
波形圖

實驗四：BCD計數器設計

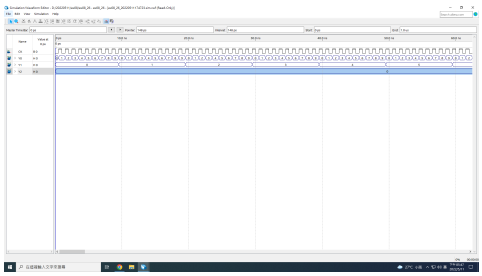
- 實驗結果照片：



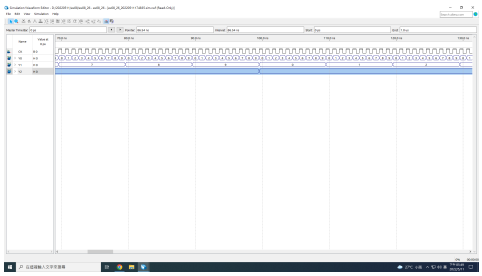
VHDL-1



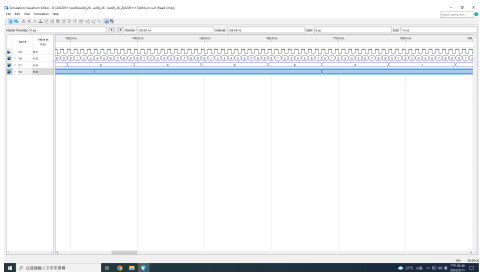
VHDL-2



波形圖-1



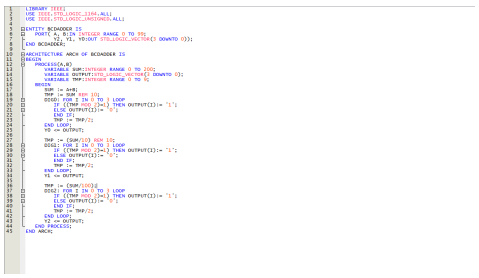
波形圖-2



波形圖-3

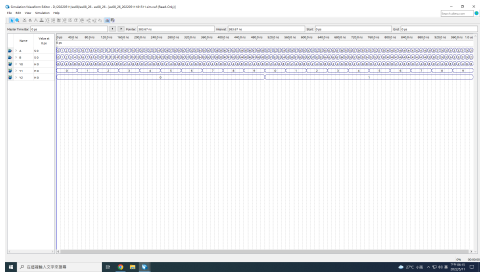
實驗五：BCD加法器設計

- 實驗結果照片：



```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY BCDADDER IS
    PORT( X, Y: IN INTEGER RANGE 0 TO 99;
          Z: OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
END BCDADDER;

ARCHITECTURE ARCH OF BCDADDER IS
BEGIN
    PROCESS(A,B)
        VARIABLE SUM:INTEGER RANGE 0 TO 200;
        VARIABLE OUTPUT:STD_LOGIC_VECTOR(7 DOWNTO 0);
        VARIABLE TMP:INTEGER RANGE 0 TO 9;
    BEGIN
        SUM := X+Y;
        TMP := SUM MOD 10;
        DIG0: FOR I IN 7 TO 7 LOOP
            IF ((TMP MOD 2)=1) THEN OUTPUT(I):= '1';
            ELSE OUTPUT(I):= '0';
            END IF;
            TMP:= TMP/2;
        END LOOP;
        Y0 <= OUTPUT;

        TMP := (SUM/10) MOD 10;
        DIG1: FOR I IN 7 TO 7 LOOP
            IF ((TMP MOD 2)=1) THEN OUTPUT(I):= '1';
            ELSE OUTPUT(I):= '0';
            END IF;
            TMP:= TMP/2;
        END LOOP;
        Y1 <= OUTPUT;

        TMP := (SUM/100);
        DIG2: FOR I IN 7 TO 7 LOOP
            IF ((TMP MOD 2)=1) THEN OUTPUT(I):= '1';
            ELSE OUTPUT(I):= '0';
            END IF;
            TMP:= TMP/2;
        END LOOP;
        Y2 <= OUTPUT;
    END PROCESS;
END ARCH;
```

VHDL



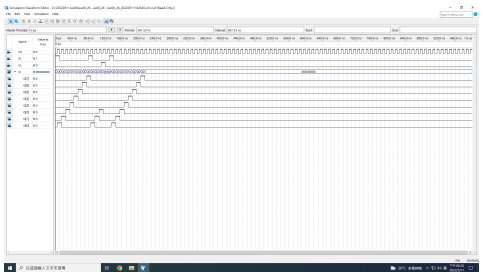
波形圖

實驗六：移位暫存器設計

- 實驗結果照片：

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY SREGISTER IS
   PORT( SI, CK, CL: STD_LOGIC;
         Q:OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
END  SREGISTER;

ARCHITECTURE ARCH OF SREGISTER IS
BEGIN
   PROCESS(SI, CK, CL)
      VARIABLE REGT: STD_LOGIC_VECTOR(7 DOWNTO 0);
   BEGIN
      IF RISING_EDGE(CK) THEN
         IF CL='1' THEN
            REGT := "00000000";
         ELSE
            REGT := REGT(6 DOWNTO 0) & SI;
         END IF;
         Q <= REGT;
      END IF;
   END PROCESS;
END ARCH;
```

VHDL



波形圖