TECHNISCHE UNIVERSITÄT WIEN

Institut für Computertechnik
Institute of Computer Technology

Dynamic Partial Reconfiguration in FPGAs

A Tutorial

- By Andreas Dejmek

Supervised by Nima TaheriNejad

Outline

- Basic principles
- Types of configuration interfaces
- Design flow
- Application

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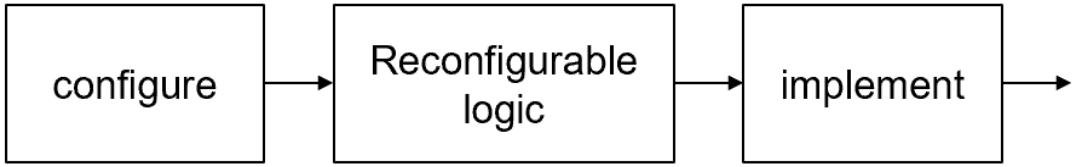
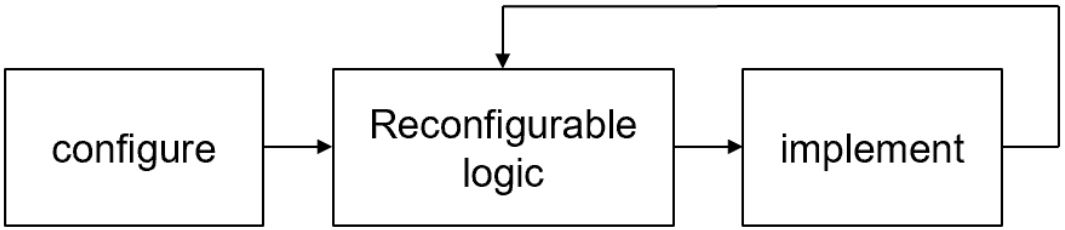
Partial reconfiguration

- Static: FPGA is stopped during reconfiguration



- Dynamic: reconfiguration during run-time
  - Only parts of a system might be updated



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Motivation

- Why is DPR useful?
- What can it be used for?

- Efficient resource utilization
- Save reconfiguration time
- Save memory

- In-field updates
- Fault-redundant systems

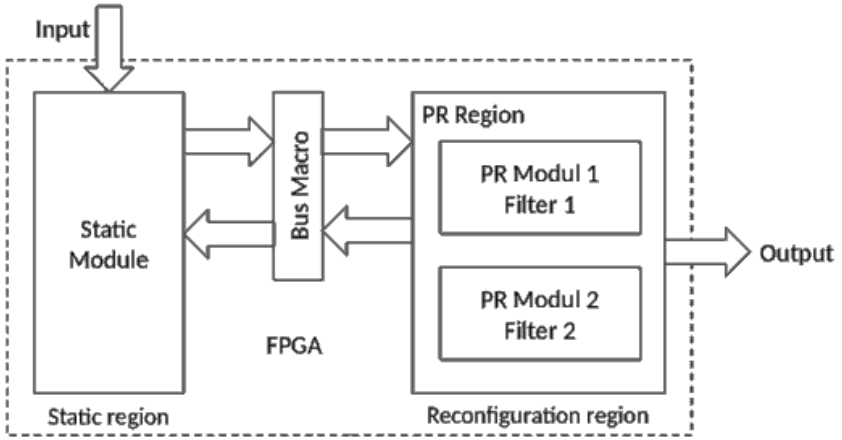
Basic methods

Difference-based

- Allow small design changes
  - LUTs equations
  - I/O standards
  - RAM content
- Bitstreams only contain differences

Module-based

- FPGA area is split into regions:
  - Static region
  - Partial reconfiguration regions



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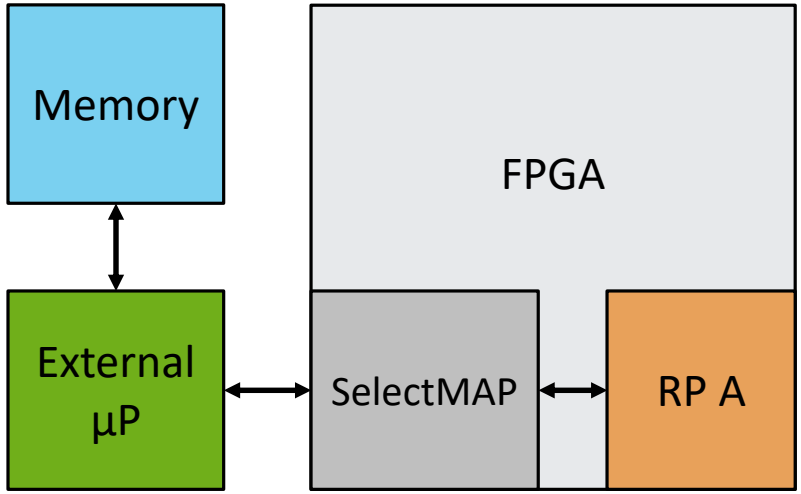
Types of configuration interfaces

- Joint Test Action Group *(JTAG)*
- Serial mode
- SelectMAP
- Internal configuration access port *(ICAP)*
- Processor configuration access port *(PCAP)*
- Media configuration access port *(MCAP)*

SelectMAP

- Slave/master modes



- Bus width: 8-bit, 16-bit or 32-bit bidirectional
  - Auto detection
  - Defined during design phase

- set_property CONFIG_MODE <value> [current_design]

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SelectMAP – reconfiguration

- BitGen *persist* option must be set
  - Otherwise, data pins → user I/Os
- set_property BITSTREAM.CONFIG.PERSIST <value> [current_design]

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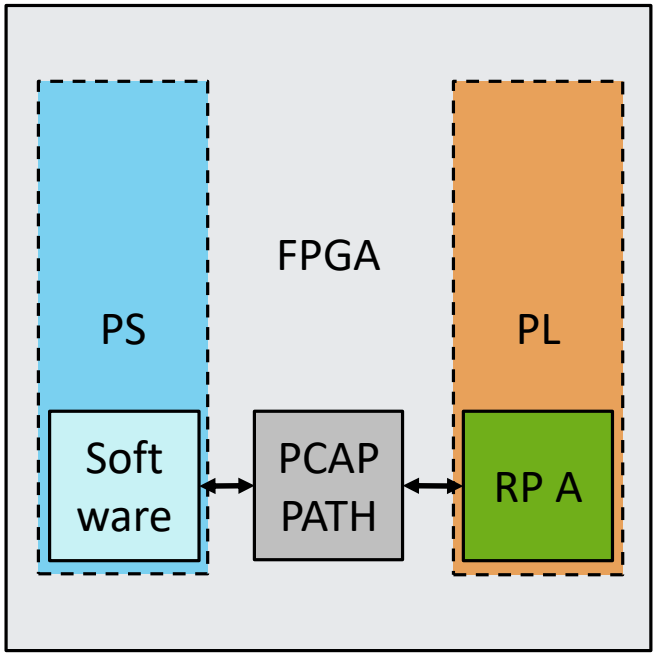
ICAP

- Internal version of SelectMAP
  - Except ICAP has dedicated data I/Os
- Is a primitive
  - ICAPE2 for Xilinx® 7 Series / Zynq-7000 SoC
  - ICAPE3 for UltraScale / UltraScale+
- Initial configuration not possible
  - Instantiation of primitive

PCAP

- Configure PL from PS
- Uses DMA controller
- Xilinx® provides device drivers
  - Linux OS
- Initial configuration possible
  - Boots from PS



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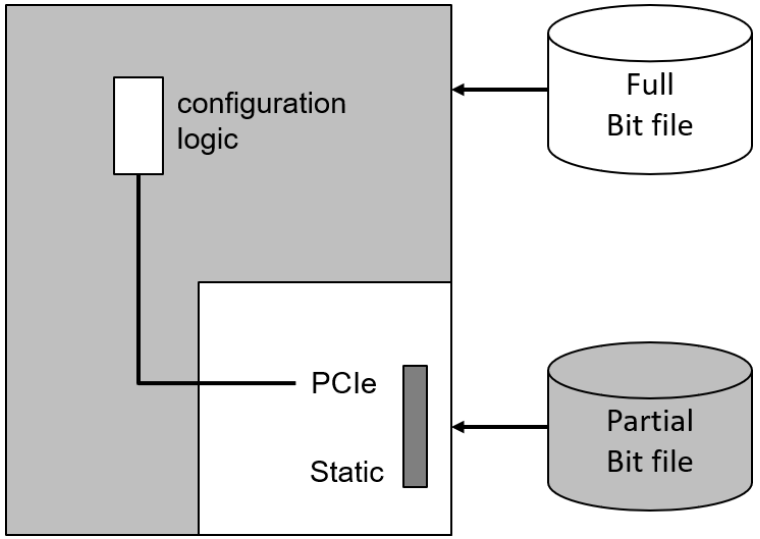
MCAP

- Configuration through PCIe block
- Tandem PCIe configuration
- Reconfiguration
  - PCIe link remains active
- Initial configuration not possible



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Supported configuration interfaces

Configuration Mode	7 Series	Zynq-7000	UltraScale	UltraScale+	Zynq UltraScale+ MPSoC
external:					
JTAG	Yes	Yes	Yes	Yes	Yes
Serial mode	Yes	N/A	Yes	Yes	N/A
SelectMAP	Yes	N/A	Yes	Yes	N/A
internal:					
ICAP	Yes	Yes	Yes	Yes	Yes
PCAP	N/A	Yes	N/A	N/A	Yes
MCAP	N/A	N/A	Yes	Yes	Yes

Source: [4]

Performance throughput

configuration mode	max. clock rate	data width	max. bandwidth
Serial mode	100 MHz	1-bit	12.5 MB/s
JTAG	66 MHz	1-bit	8.25 MB/s
SelectMAP **ICAP** **PCAP**	100 MHz	32-bit	400 MB/s
MCAP	200 MHz	32-bit	800 MB/s

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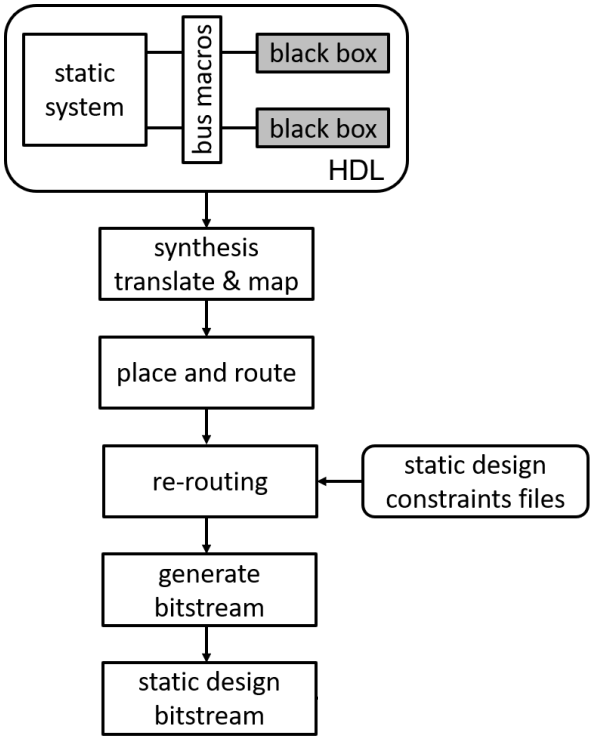
Design flow



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Design restrictions

- Restrictions for Pblocks

Affects architectures before UltraScale:

- No clock or clock modifying logic
  - PLLs
  - Clock buffers
- I/Os and I/O related components

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Application – Image processing

- Using dynamic partial reconfiguration to:

- Implement two morphological functions
  - Erosion
  - Dilation

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Application – Image processing

Original

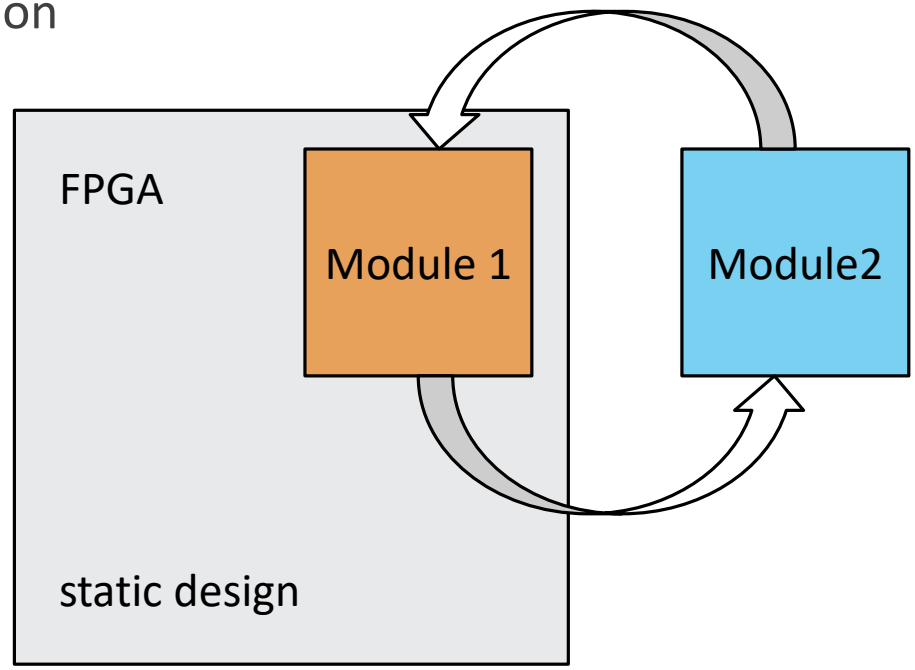
Eroded

Dilated

Source: [19]

Application – Image processing

- Using ICAP for reconfiguration
- Module
  - Erosion
  - Dilation



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Application – Conclusion

bitstream	size (bytes)	configuration time (µs)
full	250.680	627,2
partial	35.840	92,3
Savings	**85,7%**	**85,3%**

$$t[\mu s] = \frac{bitstream\_size * 8}{32 * 100}$$

$$\begin{cases} 32\ bit \ldots bus\ width\ of\ ICAP \\ 100\ MHz \ldots clock\ frequency\ of\ ICAP \end{cases}$$

Source: [19]

Sources

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Questions?

THANK YOU FOR YOUR ATTENTION!