Report generated on 2023-01-02 06:18 GMT by riscof v

Environment

Riscof Version	1.25.1
Riscv-arch-test Version/Commit Id	-
ISA	RV32IMAFDCZicsr_Zifencei
User Spec Version	2.3
Privilege Spec Version	1.10

Yaml

Show all details / Hide all details

Name
/home/user3/tools/test/riscof_work/spike_simple_isa_checked.yaml *(show details)*
/home/user3/tools/test/riscof_work/spike_simple_platform_checked.yaml *(show details)*

Please visit YAML specifications for more information.

Test Stats

Test Name	Mem Footprint (Bytes)	Code size (Bytes)	Data size (Bytes)	Sign size (Bytes)
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/mstatus.S	19740	880	4	1536
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/misa.S	18884	56	4	1536
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/mip.S	19112	212	4	1536
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/minstret.S	18976	92	4	1536
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/mie.S	19416	544	4	1536
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/mideleg.S	19536	656	4	1536
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/mepc.S	19048	148	4	1536
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/medeleg.S	19156	276	4	1536
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/mcycle.S	18936	68	4	1536
/home/user3/tools/riscv-arch-test/riscv-test-suite/rv32i_m/testing/mcause.S	19456	624	4	1536

Coverage Report (Total Coverpoints: 199)

Show all details / Hide all details

Coverage Label	(Covered-points)/(Total-points)	Percentage
ebreak	0/1 *(show details)*	0.00%
ecall	0/1 *(show details)*	0.00%
mcause	3/4 *(hide details)*	75.00%

```
config:
   - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*);
csr_comb:
     (mcause >> 31) & 1 == 0: 23
     (mcause >> 31) & 1 == 1: 0
     coverage: 1/2
mnemonics:
     csrrs: 15
     csrrw: 8
     coverage: 2/2
total_coverage: 3/4
```

mcycle	2/3 *(hide details)*	66.67%

```
config:
   - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*);
csr_comb:
     mcycle == 0x0: 2
     coverage: 1/1
mnemonics:
     csrrs: 2
     csrrw: 0
     coverage: 1/2
total_coverage: 2/3
```

medeleg	3/15 *(hide details)*	20.00%

Coverage Label	(Covered-points)/(Total-points)	Percentage

```
config:
   - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*);
csr_comb:
     (medeleg >> 0) & 0x01 == 0x01: 10
     (medeleg >> 1) & 0x01 == 0x01: 0
     (medeleg >> 12) & 0x01 == 0x01: 0
     (medeleg >> 13) & 0x01 == 0x01: 0
     (medeleg >> 15) & 0x01 == 0x01: 0
     (medeleg >> 2) & 0x01 == 0x01: 0
     (medeleg >> 3) & 0x01 == 0x01: 0
     (medeleg >> 4) & 0x01 == 0x01: 0
     (medeleg >> 5) & 0x01 == 0x01: 0
     (medeleg >> 6) & 0x01 == 0x01: 0
     (medeleg >> 7) & 0x01 == 0x01: 0
     (medeleg >> 8) & 0x01 == 0x01: 0
     (medeleg >> 9) & 0x01 == 0x01: 0
     coverage: 1/13
```

mepc	4/9 *(hide details)*	44.44%

```
config:
   - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*);
csr_comb:
     (mepc & 0x3) == 0x00: 6
     (mepc & 0x3) == 0x01: 0
     (mepc & 0x3) == 0x02: 0
     (mepc & 0x3) == 0x03: 0
     (mepc >> 3) & 0x07 == 0x00: 2
     (mepc >> 3) & 0x07 == 0x01: 0
     (mepc >> 3) & 0x07 == 0x02: 4
     coverage: 3/7
mnemonics:
     csrrs: 6
     csrrw: 0
     coverage: 1/2
total_coverage: 4/9
```

mideleg	2/8 *(hide details)*	25.00%

```
config:
   - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*);
csr_comb:
     (mideleg >> 1) & 0x01 == 0x01: 0
     (mideleg >> 11) & 0x1 == 0x01: 0
     (mideleg >> 3) & 0x01 == 0x01: 0
     (mideleg >> 5) & 0x01 == 0x01: 0
     (mideleg >> 7) & 0x01 == 0x01: 0
     (mideleg >> 9) & 0x01 == 0x01: 0
     coverage: 0/6
mnemonics:
     csrrs: 17
     csrrw: 20
     coverage: 2/2
total_coverage: 2/8
```

mie	4/10 *(hide details)*	40.00%

```
config:
   - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*);
csr_comb:
     ((mie >> 0) & 0x01) == 0x00: 25
     ((mie >> 0) & 0x01) == 0x01: 0
     ((mie >> 1) & 0x01) == 0x01: 0
     ((mie >> 11) & 0x01) == 0x01: 0
     ((mie >> 3) & 0x01) == 0x01: 22
     ((mie >> 5) & 0x01) == 0x01: 0
     ((mie >> 7) & 0x01) == 0x01: 0
     ((mie >> 9) & 0x01) == 0x01: 0
     coverage: 2/8
mnemonics:
     csrrs: 11
     csrrw: 14
     coverage: 2/2
total_coverage: 4/10
```

minstret	1/3 *(hide details)*	33.33%

```
config:
   - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*);
csr_comb:
     minstret > 1: 0
     coverage: 0/1
mnemonics:
     csrrs: 4
     csrrw: 0
     coverage: 1/2
total_coverage: 1/3
```

mip	4/10 *(hide details)*	40.00%

Coverage Label	(Covered-points)/(Total-points)	Percentage
config: - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*); csr_comb: ((mip >> 1) & 0x01) == 0x01: 0 ((mip >> 11) & 0x01) == 0x01: 0 ((mip >> 3) & 0x01) == 0x01: 0 ((mip >> 5) & 0x01) == 0x01: 0 ((mip >> 7) & 0x01) == 0x01: 14 ((mip >> 9) & 0x01) == 0x01: 0 mip & 0x00007fff == 0x00000000: 1 mip & 0x00007fff == 0x00007fff: 0 coverage: 2/8 mnemonics: csrrs: 9 csrrw: 6 coverage: 2/2 total_coverage: 4/10		
misa	3/6 *(hide details)*	50.00%
config: - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*); csr_comb: ((misa >> 3) & 0x01) == 0 & ((misa >> 5) & 0x01) == 0: 2 misa >> (xlen-2) == 0x01: 2 misa >> (xlen-2) == 0x02: 0 misa >> (xlen-2) == 0x03: 0 coverage: 2/4 mnemonics: csrrs: 2 csrrw: 0 coverage: 1/2 total_coverage: 3/6		
misalign-beq	0/2 *(show details)*	0.00%
misalign-bge	0/2 *(show details)*	0.00%
misalign-bgeu	0/2 *(show details)*	0.00%
misalign-blt	0/2 *(show details)*	0.00%
misalign-bltu	0/2 *(show details)*	0.00%
misalign-bne	0/2 *(show details)*	0.00%
misalign-jal	0/2 *(show details)*	0.00%
misalign-lh	0/2 *(show details)*	0.00%
misalign-lhu	0/2 *(show details)*	0.00%
misalign-lw	0/4 *(show details)*	0.00%
misalign-sh	0/2 *(show details)*	0.00%
misalign-sw	0/4 *(show details)*	0.00%
misalign1-jalr	0/2 *(show details)*	0.00%
misalign2-jalr	0/2 *(show details)*	0.00%
mstatus	12/20 *(hide details)*	60.00%
config: - check ISA:=regex(.*32.*); regex(.*I.*Zicsr.*); csr_comb: (mstatus >> 1) & 0x01 == 0x01: 2 (mstatus >> 10) & 0x3 == 0x01: 0 (mstatus >> 10) & 0x3 == 0x02: 2 (mstatus >> 10) & 0x3 == 0x3: 0 (mstatus >> 17) & 0x1 == 0x01: 7 (mstatus >> 18) & 0x1 == 0x01: 8 (mstatus >> 19) & 0x1 == 0x01: 0 (mstatus >> 20) & 0x1 == 0x01: 8 (mstatus >> 21) & 0x1 == 0x01: 8 (mstatus >> 22) & 0x1 == 0x01: 0 (mstatus >> 3) & 0x01 == 0x01: 13 (mstatus >> 37) & 0x1 == 0x01: 0 (mstatus >> 5) & 0x01 == 0x01: 8 (mstatus >> 6) & 0x1 == 0x01: 0		
pmpcfg	0/50 *(show details)*	0.00%
pmpna4	0/9 *(show details)*	0.00%
pmpnapot	0/9 *(show details)*	0.00%
pmptor	0/9 *(show details)*	0.00%