

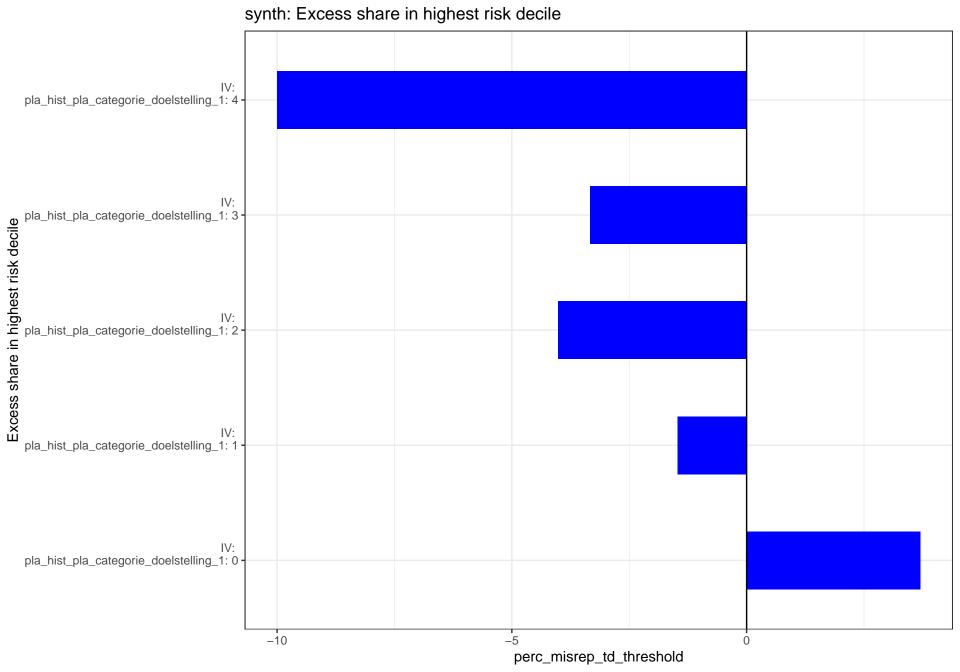
real\_conditional: Excess share in highest risk decile IV: pla\_hist\_pla\_categorie\_doelstelling\_1: 6 IV: pla\_hist\_pla\_categorie\_doelstelling\_1: 5 pla\_hist\_pla\_categorie\_doelstelling\_1: 4
yst

pla\_hist\_pla\_categorie\_doelstelling\_1: 3
IV:

pla\_hist\_pla\_categorie\_doelstelling\_1: 3
IV:

pla\_hist\_pla\_categorie\_doelstelling\_1: 2
IV:

pla\_hist\_pla\_categorie\_doelstelling\_1: 2pla\_hist\_pla\_categorie\_doelstelling\_1: 1 pla\_hist\_pla\_categorie\_doelstelling\_1: 0 0.0 0.1 0.3 perc\_misrep\_td\_threshold



synth\_conditional: Excess share in highest risk decile IV: pla\_hist\_pla\_categorie\_doelstelling\_1: 6 IV: pla\_hist\_pla\_categorie\_doelstelling\_1: 5 pla\_hist\_pla\_categorie\_doelstelling\_1: 4
yst

pla\_hist\_pla\_categorie\_doelstelling\_1: 3
IV:

pla\_hist\_pla\_categorie\_doelstelling\_1: 3
IV:

pla\_hist\_pla\_categorie\_doelstelling\_1: 2
IV:

pla\_hist\_pla\_categorie\_doelstelling\_1: 2pla\_hist\_pla\_categorie\_doelstelling\_1: 1 pla\_hist\_pla\_categorie\_doelstelling\_1: 0 0.0 0.2 0.4 perc\_misrep\_td\_threshold