HDMI Input/Output FMC Module
Hardware Guide

AVNET electronics marketing

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1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the HDMI Input/Output FMC Module from Avnet Electronics Marketing. This document includes descriptions of the hardware features.

1.1 Description

The HDMI Input/Output FMC Module is not a stand-alone module, but rather a plug-in module designed to interface with FMC compatible baseboards. In that role, the FMC adapter provides a number of video interfaces to its host via a LPC FMC connector. The HDMI Input/Output FMC Module is shown in Figure 1.

1.2 Features

The HDMI Input/Output FMC Module provides the following features.

Video Input
- — Single interface for ON Semiconductor's VITA family of image sensors
- — HDMI input interface

Video Output
- — HDMI output interface

Clock Source
- — Video clock synthesizer

I2C Configuration
- — IPMI Identification EEPROM
- — Peripheral configuration

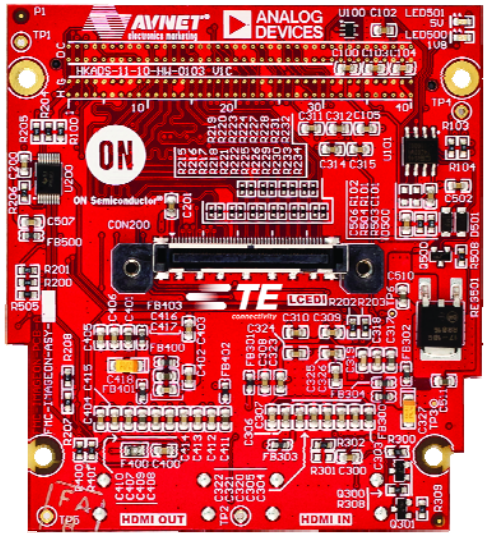

Figure 1 – HDMI Input/Output FMC Module

NOTE :
Spread Spectrum Clocking (SSC) is used on the FMC-IMAGEON module's HDMI output interface (HDMIO_CLK) to reduce radiated emissions to industry approved levels.
This can be implemented using the SSC feature of the on-board TI CDCE913 video clock synthesizer.
Refer to section 3.1 for more information.

1.3 Ordering Information

The following table lists the evaluation kit part numbers and available software options.

Part Number	Hardware
AES-FMC-IMAGEON-G (www.em.avnet.com/fmc-imageon)	HDMI Input/output FMC Module (image sensor not included)
AES-FMC-IMAGEON-VITA2000C-G (www.em.avnet.com/fmc-imageon-v2000c)	ON Semiconductor Image Sensor (VITA-2000, color) with HDMI Input/Output FMC Bundle

Table 1 - Ordering Information

The ON Semiconductor Image Sensor with HDMI Input/Output FMC bundle includes the FMC module, and an image sensor head board with lens, tripod and cable.

Figure 2 – ON Semiconductor Image Sensor with HDMI Input/Output FMC bundle

1.4 References

Analog Devices Engineering Zone : ADV7611 HDMI Receiver resources
http://ez.analog.com/docs/DOC-1745

Analog Devices Engineering Zone : ADV7511 HDMI Receiver resources
http://ez.analog.com/docs/DOC-1740

On Semiconductor VITA-2000 image sensor
http://www.onsemi.com/PowerSolutions/product.do?id=VITA2000

Texas Instruments CDCE913 datasheet: Programmable 2-PLL VCXO Clock Synthesizer
http://focus.ti.com/docs/prod/folders/print/cdce913.html

FMC Specification
http://www.vita.com/fmc.html

Platform Management FRU Information Storage Definition V1.0
http://download.intel.com/design/servers/ipmi/FRU1011.pdf

2.0 Functional Description

The HDMI Input/Output FMC Module is a low pin count (LPC) FMC module containing interfaces intended for video processing. This module contains no processing intelligence and requires that it be plugged into a compatible baseboard for power, control and data processing. The FMC module has a single interface that can be used to connect one of OnSemi's VITA family of image sensors (VITA-1300, VITA-2000, VITA-5000).

Figure 3 depicts the architecture of the HDMI Input/Output FMC Module and ON Semiconductor Image Sensor head board.

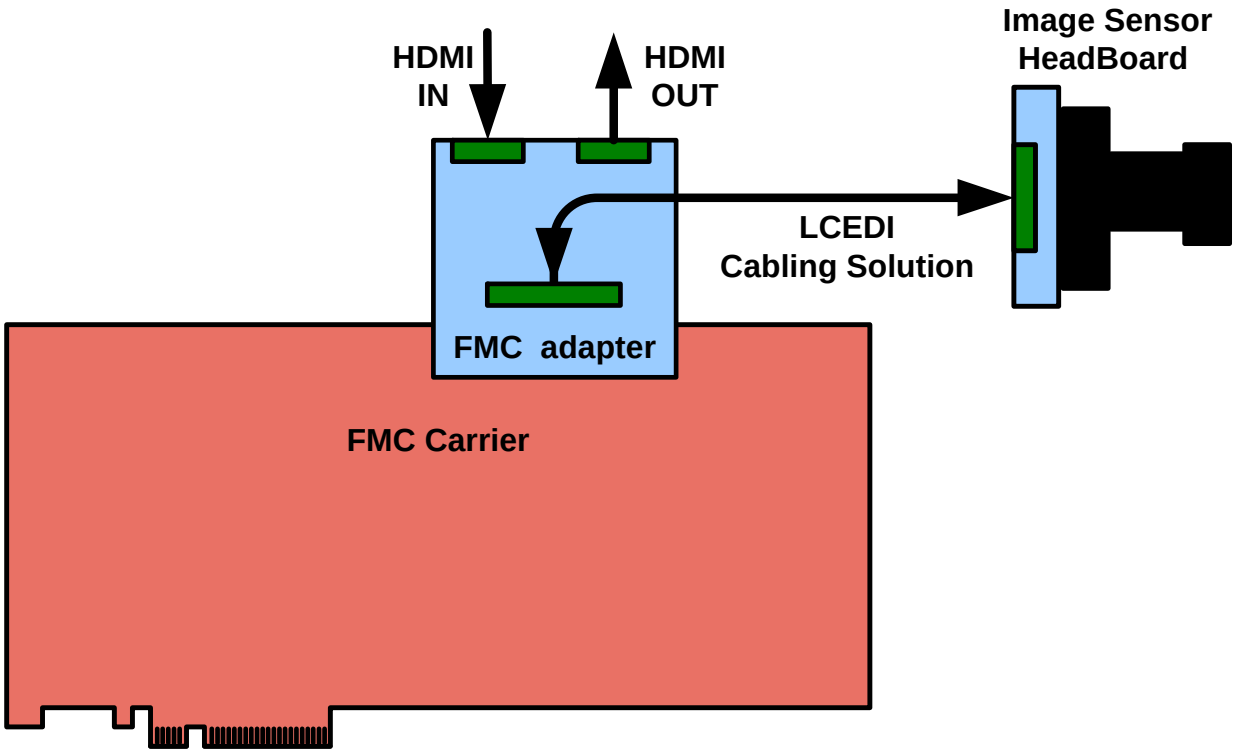

Figure 3 – ON Semiconductor Image Sensor with HDMI Input/Output FMC bundle - System Diagram

Figure 4 illustrates the block diagram of the HDMI Input/Output FMC Module and ON Semiconductor Image Sensor head board.

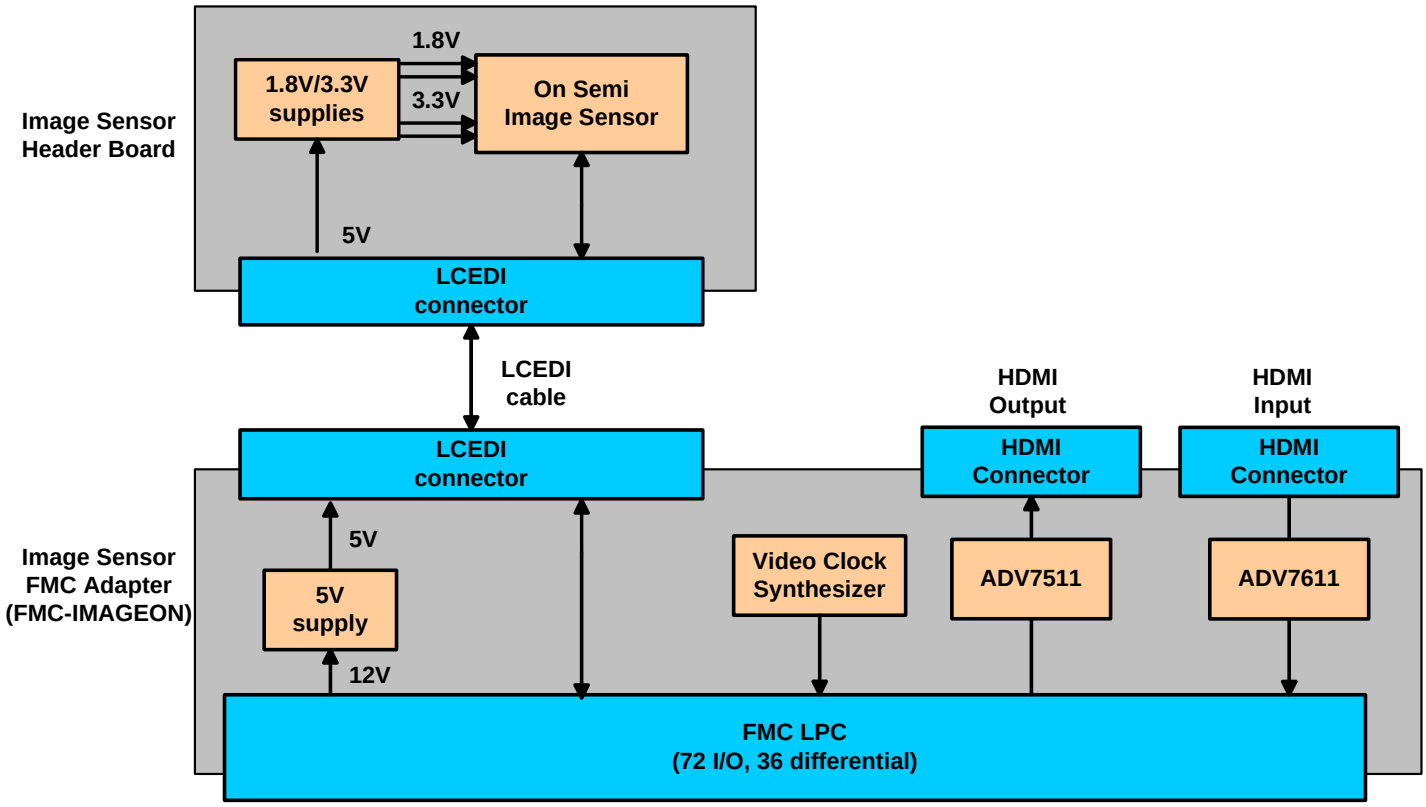

Figure 4 – ON Semiconductor Image Sensor with HDMI Input/Output FMC bundle - Block Diagram

2.1 FMC Connector

The FMC LPC connector provides 68 single-ended I/O or 34 differential I/O as defined in Table 2.

	H	G	D	C
1	VREF_A_M2C	GND	PG_C2M	GND
2	PRSNT_M2C_L	CLK1_M2C_P	GND	DP0_C2M_P
3	GND	CLK1_M2C_N	GND	DP0_C2M_N
4	CLK0_M2C_P	GND	GBTCLK0_M2C_P	GND
5	CLK0_M2C_N	GND	GBTCLK0_M2C_N	GND
6	GND	LA00_P_CC	GND	DP0_M2C_P
7	LA02_P	LA00_N_CC	GND	DP0_M2C_N
8	LA02_N	GND	LA01_P_CC	GND
9	GND	LA03_P	LA01_N_CC	GND
10	LA04_P	LA03_N	GND	LA06_P
11	LA04_N	GND	LA05_P	LA06_N
12	GND	LA08_P	LA05_N	GND
13	LA07_P	LA08_N	GND	GND
14	LA07_N	GND	LA09_P	LA10_P
15	GND	LA12_P	LA09_N	LA10_N
16	LA11_P	LA12_N	GND	GND
17	LA11_N	GND	LA13_P	GND
18	GND	LA16_P	LA13_N	LA14_P
19	LA15_P	LA16_N	GND	LA14_N
20	LA15_N	GND	LA17_P_CC	GND
21	GND	LA20_P	LA17_N_CC	GND
22	LA19_P	LA20_N	GND	LA18_P_CC
23	LA19_N	GND	LA23_P	LA18_N_CC
24	GND	LA22_P	LA23_N	GND
25	LA21_P	LA22_N	GND	GND
26	LA21_N	GND	LA26_P	LA27_P
27	GND	LA25_P	LA26_N	LA27_N
28	LA24_P	LA25_N	GND	GND
29	LA24_N	GND	TCK	GND
30	GND	LA29_P	TDI	SCL
31	LA28_P	LA29_N	TDO	SDA
32	LA28_N	GND	3P3VAUX	GND
33	GND	LA31_P	TMS	GND
34	LA30_P	LA31_N	TRST_L	GA0
35	LA30_N	GND	GA1	12P0V
36	GND	LA33_P	3P3V	GND
37	LA32_P	LA33_N	GND	12P0V
38	LA32_N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND
	LPC Connector	LPC Connector	LPC Connector	LPC Connector

Table 2 – FMC LPC Connector Pinout

Note: For the FMC LPC, the connector columns K, J, F, E, B, and A are not used and not shown in the above table.

The FMC pin allocation for the FMC-IMAGEON FMC Module is defined in Table 3.

	H	G		D	C	
1	-	GND	1	PG_C2M	GND	1
2	PRSNT_M2C_L	HDMII_CLK (in)	2	GND	-	2
3	GND	HDMIO_CLK (out)	3	GND	-	3
4	VCLK1 (in)	GND	4	-	GND	4
5	CAM_RESET_N	GND	5	-	GND	5
6	GND	CLK_OUT_P (in)	6	GND	-	6
7	CAM_D[7]_P	CLK_OUT_N (in)	7	GND	-	7
8	CAM_D[7]_N	GND	8	HDMIIO_INT#	GND	8
9	GND	CAM_D[6]_P	9	I2C_MUX_RESET_N	GND	9
10	CAM_D[4]_P	CAM_D[6]_N	10	GND	CAM_D[5]_P	10
11	CAM_D[4]_N	GND	11	CAM_D[3]_P	CAM_D[5]_N	11
12	GND	CAM_D[2]_P	12	CAM_D[3]_N	GND	12
13	CAM_D[1]_P	CAM_D[2]_N	13	GND	GND	13
14	CAM_D[1]_N	GND	14	CAM_D[0]_P	SYNC_P	14
15	GND	SPI_SCLK	15	CAM_D[0]_N	SYNC_N	15
16	SPI_MOSI	SPI_SSEL_N	16	GND	GND	16
17	SPI_MISO	GND	17	CLK_PLL (out)	GND	17
18	GND	I2C_MUX_SCL	18	TRIGGER[2]	TRIGGER[1]	18
19	MONITOR[0]	I2C_MUX_SDA	19	GND	TRIGGER[0]	19
20	MONITOR[1]	GND	20	HDMIO_CBCR[6]	GND	20
21	GND	HDMIO_CBCR[7]	21	HDMIO_CBCR[3]	GND	21
22	HDMIO_CBCR[4]	HDMIO_CBCR[5]	22	GND	HDMIO_CBCR[2]	22
23	HDMIO_CBCR[1]	GND	23	HDMIO_Y[7]	HDMIO_Y[6]	23
24	GND	HDMIO_CBCR[0]	24	HDMIO_Y[3]	GND	24
25	HDMIO_Y[4]	HDMII_Y[5]	25	GND	GND	25
26	HDMIO_Y[2]	GND	26	HDMII_Y[7]	HDMII_Y[6]	26
27	GND	HDMIO_Y[1]	27	HDMII_Y[4]	HDMII_Y[3]	27
28	HDMIO_SPDIF	HDMIO_Y[0]	28	GND	GND	28
29	HDMII_SPDIF	GND	29	-	GND	29
30	GND	HDMII_Y[5]	30	TDI	SCL	30
31	HDMII_Y[1]	HDMII_Y[2]	31	TDO[1]	SDA	31
32	HDMII_Y[0]	GND	32	3P3VAUX	GND	32
33	GND	HDMII_CBCR[7]	33	-	GND	33
34	HDMII_CBCR[5]	HDMII_CBCR[6]	34	-	GA0	34
35	HDMII_CBCR[4]	GND	35	GA1	12P0V	35
36	GND	HDMII_CBCR[3]	36	3P3V	GND	36
37	HDMII_CBCR[1]	HDMII_CBCR[2]	37	GND	12P0V	37
38	HDMII_CBCR[0]	GND	38	3P3V	GND	38
39	GND	VADJ	39	GND	3P3V	39
40	VADJ	GND	40	3P3V	GND	40

Table 3 –FMC LPC Pinout

[1] TDO is connected to TDI in order not to break the JTAG chain

2.2 Voltage Sources

The following table lists all the voltage sources available on the Image Sensor with HDMI I/O FMC solution.

Voltage Name	Voltage	Current	Description
supplied by **FMC connector**			
3V3AUX	3.3 V		Used by IPMI Identification prior to module power-up.
3V3	3.3 V		Used by ADV7611, ADV7511, CDCE913, and level translators
VADJ	2.5 V or 3.3 V		Used for all single-ended signals connected to FMC connector.
12V	12.0 V		
supplied by the FMC-IMAGEON **FMC module**			
REG_5V	5V	1A	Over-designed for VITA-5000 image sensor module
REG_1V8	1.8V	TBD	Used by ADV7611, ADV7511, CDCE913
supplied by the Image Sensor **Head Board**			
VDD_18	1.8V	240 mA	Reference AN65465 – VITA 5000 HSMC Ref Board
VDD_33	3.3V	260 mA	Reference AN65465 – VITA 5000 HSMC Ref Board
VDD_PIX	3.3V	1 mA	Reference AN65465 – VITA 5000 HSMC Ref Board
VDD_PIX_LOW	1.8V	26 mA (sinking)	Reference AN65465 – VITA 5000 HSMC Ref Board

Table 4 –Voltage Sources

2.3 I2C Chain 1 – IPMI Identification EEPROM

The following I2C section implements the IPMI identification for the FMC module.

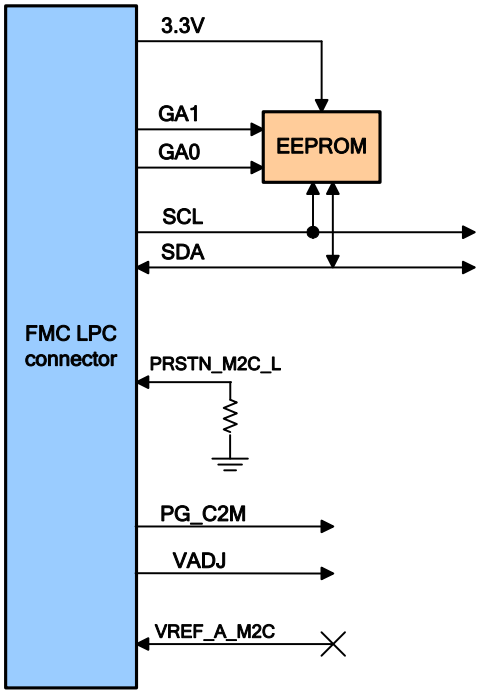

Figure 5 – IPMI Identification, Block Diagram

When the VADJ voltage is valid, the PG_C2M (ie. power good) will be asserted high. An inverted version of this signal is used to enable all the voltage level translators connected to VADJ.

The address of the I2C EEPROM will be determined by the GA[0:1] signals driven by the carrier.

Table 5 describes the EEPROM address for the FMC module.

GA[0:1]	FMC-IMAGEON I2C EEPROM Address
00	0xA0
01	0xA2
10	0xA4
11	0xA6

Table 5 – IPMI Identification, I2C EEPROM Address

The EEPROM content is defined by the Platform Management FRU Information Storage Definition V1.0.
http://download.intel.com/design/servers/ipmi/FRU1011.pdf

For the FMC-IMAGEON module, the content is described in Table 6.

Content	FMC-IMAGEON
Board Information	
- Manufacturer Date/Time	-
- Manufacturer	Avnet / On Semiconductor
- Product	FMC-IMAGEON
- Serial	-

- Part Number	AES-FMC-IMAGEON-G
- FRU File ID	-

Table 6 – IPMI Identification, EEPROM Content

2.4 I2C Chain 2 – Peripheral Configuration

The FMC-IMAGEON Module implements two I2C chains. The second I2C chain is used to configure the FMC-IMGEON module's peripherals.

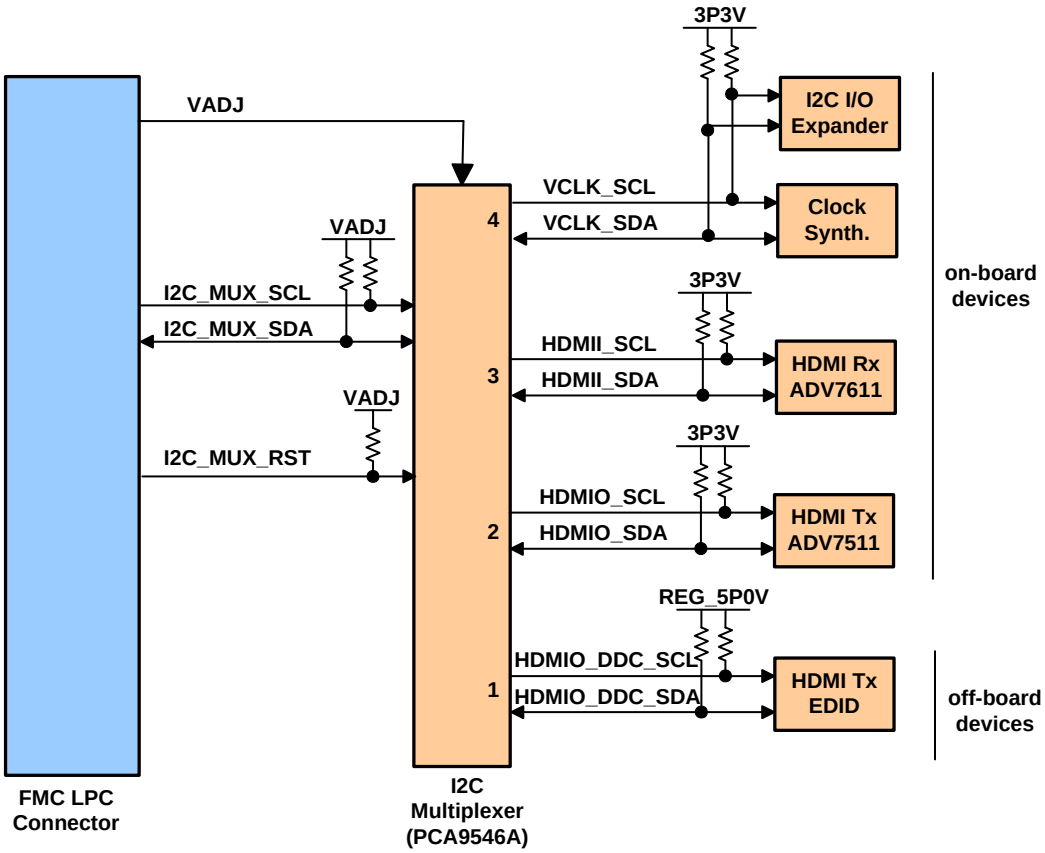

Figure 6 – I2C Peripheral Configuration, Block Diagram

The Texas Instruments PCA9546A I2C Multiplexer performs two purposes:

- Voltage level translation (2.5 V, 3.3 V, 5.0 V)
- I2C address conflict resolution

The following table lists the I2C addresses that may be present on each of the I2C Multiplexer's ports. Notice that the I2C Multiplexer's address is always visible regardless of which port is enabled.

Device	I2C Address
I2C Multiplexer	0xE0 (PCA9546)
Mux Port 1	
HDMI Output DDC EDID	0xA0
Mux Port 2	
HDMI Output	0x72 (ADV7511)
Mux Port 3	
HDMI Input	0x98 (ADV7611)
Mux Port 4	
Video Clock Synth.	0xCA (CDCE913)
I2C I/O Expander	0x40 (PCA9555)

Table 7 – I2C Peripheral Configuration, Device Summary

2.5 Video Clock Synthesizer

A Video Clock Generator is included on the FMC module in order to provide a clock for all video applications.

The following block diagram illustrates the connections for the Video Clock Generator.

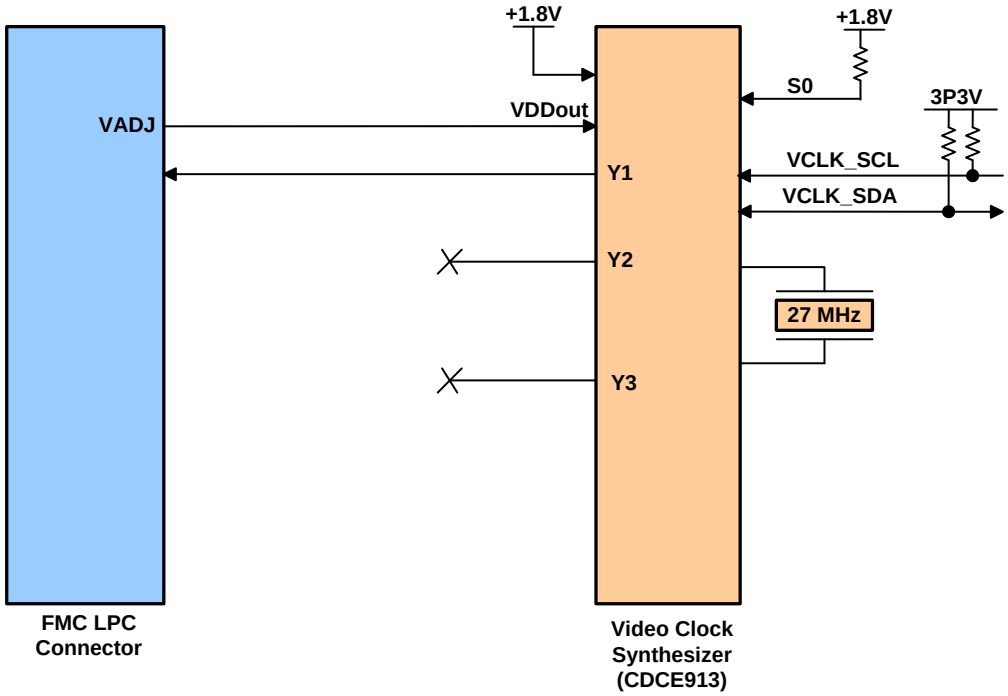

Figure 7 – Video Clock Synthesizer, Block Diagram

The Texas Instruments CDCE913 clock synthesizer has three clock outputs which are used as follows.

Clock	PLL	Description
Y1	PLL1	Can be used for any application
Y2	PLL1	Can be used for any application
Y3	-	Unused

Table 8 – Video Clock Generator, Clock Output Usage

The Y1 and Y2 clock outputs can be used for any application. One of these applications could be the 62MHz reference clock for the image sensor, another could be the clock source for the HDMI output. The Y3 clock output is not used.

The default mode of the CDCE913 is to output a 27 MHz clock on all of its outputs.

Configuration is performed via I2C. The SDA/SCL pins of the CDCE913 device are 3.3 V tolerant.
The settings of the CDCE913 video clock synthesizer can be calculated automatically using the TI Pro-Clock™ software.

2.6 HDMI Input

The HDMI input interface is implemented using the Analog Devices ADV7611 device. This device's output video interface supports YCbCr mode with embedded syncs, which significantly reduce the number of I/O required for the FMC side interface.

By using the YCbCr 4:2:2 mode, the pixels are 16 bits instead of 24 bits. This is acceptable since the Xilinx video reference designs use YCbCr 4:2:2 video format.

The following block diagram illustrates the connections between the FMC connector and the HDMI Receiver.

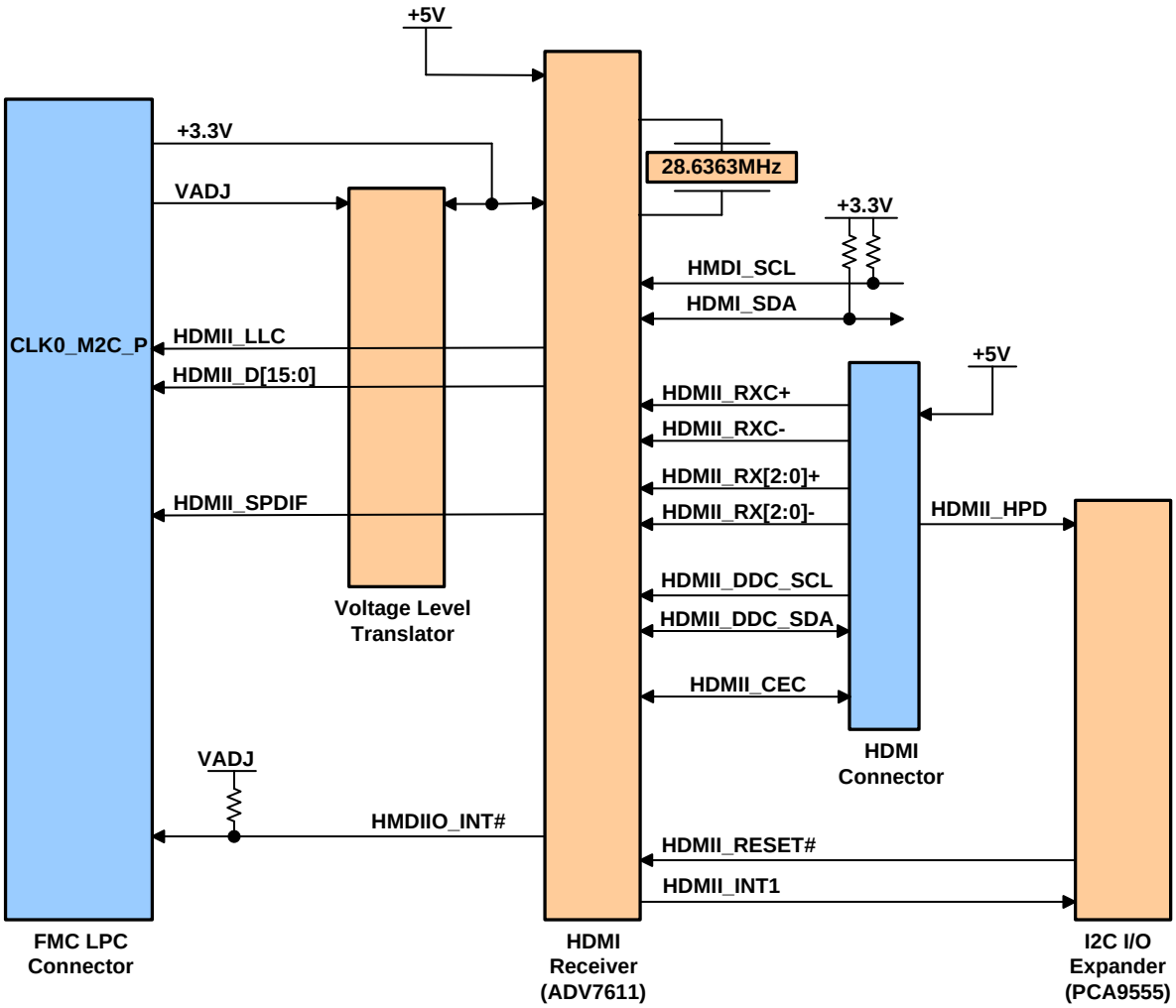

Figure 8 – HDMI Input, Block Diagram

The HDMII_SCL/SDA signals are connected to the I2C MUX device

More detailed information on the ADV7611, including a hardware user guide and recommended schematic/layout/bom, can be found on the Analog Devices EngineerZone:
http://ez.analog.com/docs/DOC-1745

2.7 HDMI Output

The HDMI output interface is implemented using the Analog Devices ADV7511 device. This device's input video interface supports YCbCr mode with embedded syncs, which significantly reduce the number of I/O required for the FMC side interface.

By using the YCbCr 4:2:2 mode, the pixels are 16 bits instead of 24 bits. This is acceptable since the Xilinx video reference designs use YCbCr 4:2:2 video format.

The following block diagram illustrates the connections between the FMC connector and the HDMI Transmitter.

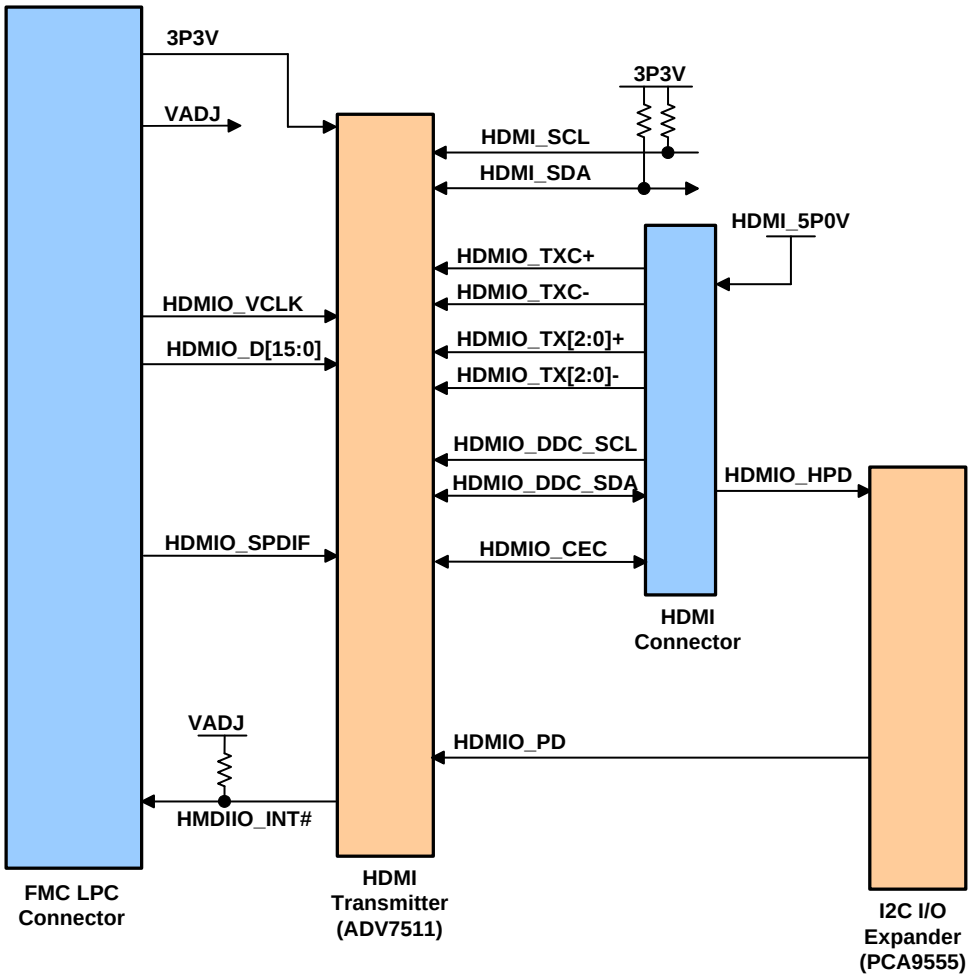

Figure 9 – HDMI Output, Block Diagram

The HDMIO_SCL/SDA signals are connected to the I2C MUX device.

More detailed information on the ADV7511, including a hardware user guide and example schematics/layout, can be found on the Analog Devices EngineerZone:
http://ez.analog.com/docs/DOC-1740

2.8 VITA Image Sensor Interface

The FMC-IMAGEON module supports the following image sensors from On Semiconductor:
- VITA-1300 => 1280x1024 @ 150 frames/sec, 4 LVDS output data pairs @ 620Mbps
- VITA-2000 => 1900x1200 @ 100 frames/sec, 4 LVDS output data pairs @ 620Mbps
- VITA-5000 => 2592x2048 @ 75 frames/sec, 8 LVDS output data pairs @ 620Mbps

The following block diagram illustrates the details of the interface to the On Semiconductor Image Sensor Head Board.

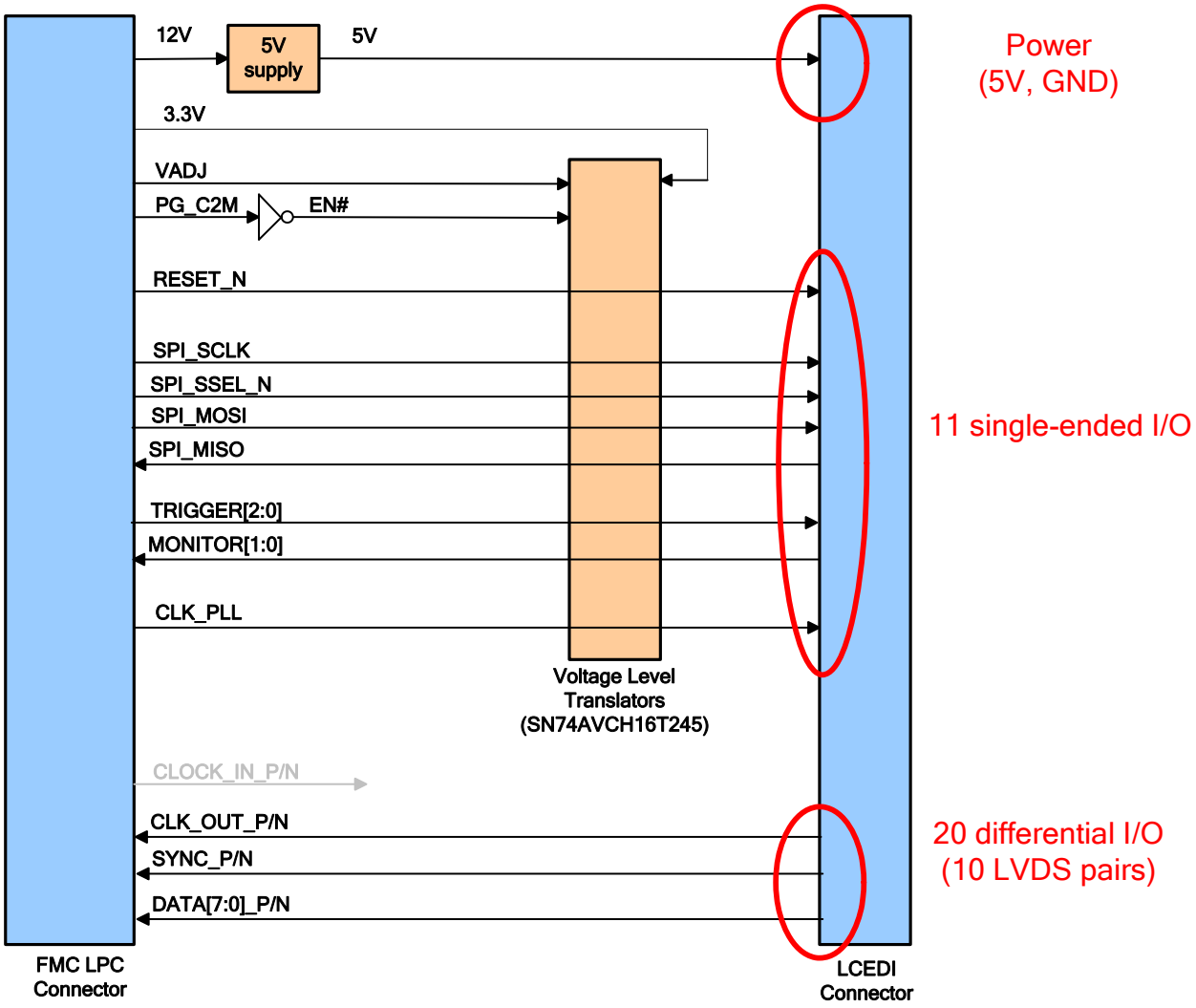

Figure 10 – VITA Image Sensor Interface, Block Diagram

The single-ended signals (RESET_N, CLK_PLL, SPI_*, MONITOR[1:0], TRIGGER[2:0]) need to be voltage translated to the FMC carrier's VADJ voltage. The image sensor must supply its internally generated 3.3V for the purpose of voltage level translation. An inverted version of PG_C2M can be used to enable the voltage level translators only when VADJ is valid.

The differential signals (CLK_OUT_P/N, SYNC_P/N, DATA[7:0]_P/N) are connected directly to the image sensor connector.

2.9 LCEDI Image Sensor Cable

The Image Sensor Head Board is connected to the FMC-IMAGEON module with an LCEDI cable from TE Connectivity.

The LCEDI cable is being adopted for LCD panels and for eDP (embedded DisplayPort, supporting data rates of 2.7Gbps).

The LCEDI cable is grouped into two consisting of a digital section, and an LVDS section.
- the digital section uses AWG#32 of Teflon Discrete wire
- the LVDS section uses AWG#40 of Micro Coax. or AWG#34 of Teflon Discrete wire

The current rating for LCEDI is:
- Discrete AWG#32: 1.0A AC/DC(per a contact)
- SGC AWG#32: 1.0 A AC/DC(per a contact)
- SGC AWG#40: 0.3A AC/DC(per a contact)

The following image illustrates the two sections, as well as the different wires used.

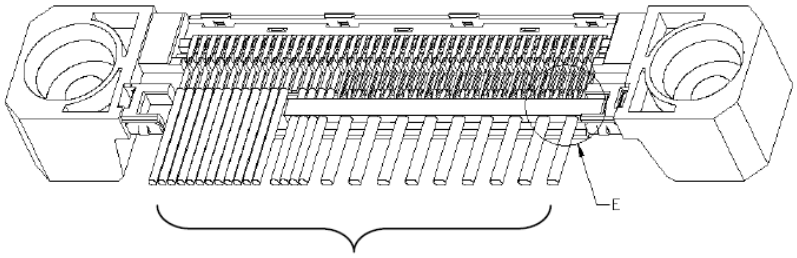

Figure 11 – LCEDI – Customer Defined Cable Definition

Avnet has defined a custom implementation of the cable for this image sensor application.
The following table describes the pinout of the Avnet LCEDI cable used for the FMC-IMAGEON module.

	SECTION	SIGNAL
1	Digital	5V (1A capable)
2	Digital	GND
3	Digital	CLK_PLL
4	Digital	RESET_N
5	Digital	SPI_SCLK
6	Digital	SPI_SSEL_N
7	Digital	SPI_MOSI
8	Digital	SPI_MISO
9	Digital	TRIGGER[2]
10	Digital	TRIGGER[1]
11	Digital	TRIGGER[0]
12	Digital	MONITOR[1]
13	Digital	MONITOR[0]
14		
15	LVDS	GND
16	LVDS	DATA[7]_P
17	LVDS	DATA[7]_N
18	LVDS	GND
19	LVDS	DATA[6]_P
20	LVDS	DATA[6]_N
21	LVDS	GND
22	LVDS	DATA[5]_P
23	LVDS	DATA[5]_N

24	LVDS	GND
25	LVDS	DATA[4]_P
26	LVDS	DATA[4]_N
27	LVDS	GND
28	LVDS	DATA[3]_P
29	LVDS	DATA[3]_N
30	LVDS	GND
31	LVDS	DATA[2]_P
32	LVDS	DATA[2]_N
33	LVDS	GND
34	LVDS	DATA[1]_P
35	LVDS	DATA[1]_N
36	LVDS	GND
37	LVDS	DATA[0]_P
38	LVDS	DATA[0]_N
39	LVDS	GND
40	LVDS	SYNC_P
41	LVDS	SYNC_N
42	LVDS	GND
43	LVDS	CLK_OUT_P
44	LVDS	CLK_OUT_N

Table 9 – Avnet LCEDI Cable – Pinout Definition

3.0 Known Issues & Limitations

This section describes the known issues and limitations for the FMC Module.

3.1 HDMI Output – HDMIO_CLK – reducing radiated emissions

Spread Spectrum Clocking (SSC) is used on the FMC-IMAGEON module's HDMI output interface (HDMIO_CLK) to reduce radiated emissions to industry approved levels. This can be implemented using the SSC feature of the on-board TI CDCE913 video clock synthesizer.

The recommended setting is to modulate the clock using down-spread clocking by an amount of -0.75%. This technique significantly lowers the radiated emissions, while maintaining functionality on the HDMI output interface.

The following I2C registers settings will program the CDCE913 for down-spread clocking of -0.75%.

Setting	Register	Value	Description
SSC1DC	0x16[7]	0	PLL1 SSC down/center selection = **down**
SSC1	0x10[2:0]	011	PLL1 SSC Selection (Modulation Amount) = **-0.75%**

Table 10 – CECE913 I2C Register Settings for SSC

4.0 Revisions

V0.1	Initial release for prototype board (AES-FMC-IMAGEON-G Revision A)	November 30, 2011
V0.2	Normalize FMC module name, update FMC pinout table, update I2C mux description	December 13, 2011
V0.3	Update pictures of FMC module, Add picture of OnSemi FMC bundle	December 21, 2011
V1.0	Update for CE compliant production hardware: - new product naming, new images - FMC connector changes : remove VCLK2, add HDMIIO_INT# - mention SSC clocking for HDMIO_CLK net	September 7, 2012