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https://github.com/1mimhe/16bit-CPU

Instruction format(16-bit):

Every Instruction is 16-bit so they are basically one format but the bits could have different meanings.

R-type:

| Opcode(4-bit) | Rs(4-bit) | Rt(4-bit) | Rd(4-bit) |
|---------------|-----------|-----------|--------------------------------|
| I-type: | | | |
| Opcode(4-bit) | Rs(4-bit) | Rt(4-bit) | Imm/Address/Off set (4-bit) |

Instructions and Opcodes:

| Instruction | Op Code | Format |
|-------------|---------|--------|
| add | 0000 | R |
| sub | 0001 | R |
| mul | 0010 | R |
| div | 0011 | R |
| ori | 0100 | Ι |
| nor | 0101 | R |
| nand | 0110 | R |
| sw | 0111 | Ι |
| lw | 1000 | Ι |
| blt | 1001 | Ι |

Control Unit Truth Table:

| | R-format | ori | SW | lw | blt |
|----------|----------|---------|-----|---------|---------|
| RegDst | 1 | 0 | X | 0 | X |
| Alusrc | 0 | 1 | 1 | 1 | 0 |
| MemToReg | 0 | 0 | X | 1 | X |
| RegWrite | 1 | 1 | 0 | 1 | 0 |
| MemWrite | 0 | 0 | 1 | 0 | 0 |
| MemRead | 0 | 0 | 0 | 1 | 0 |
| Branch | 0 | 0 | 0 | 0 | 1 |
| ExtOp | X | 0 | 1 | 1 | 1 |
| Aluctr | Op[2:0] | Op[2:0] | 000 | Op[2:0] | Op[2:0] |

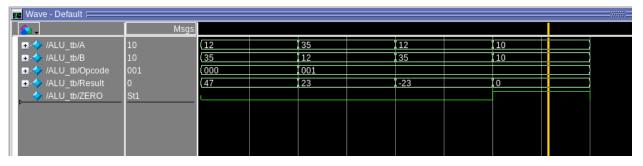
add, sub, mul, div, nor and nand are the same but with different Opcodes.

Control Unit test results:

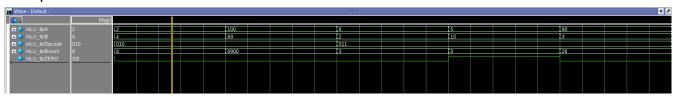
| List - Default | |
|--|---|
| ps⊸, delta⊸, | /ControlUnit_tb/Opcode—,/ControlUnit_tb/MemWrite—, /ControlUnit_tb/RegDst—, /ControlUnit_tb/Branch—, /ControlUnit_tb/ALUsrc—, /ControlUnit_tb/ExtOp—, /ControlUnit_tb/MemtoReg—, /ControlUnit_tb/ALUctr—, /ControlUnit_tb/RegWrite—, |
| 0 +0 0 +2 100 +0 100 +2 200 +0 200 +2 300 +0 300 +2 400 +2 500 +0 600 +2 700 +2 800 +0 800 +2 900 +2 | 0000 StX StX StX StX StX StX StX StX xxx 0000 St1 St0 St0 St1 St0 St0 St0 000 0001 St1 St0 St0 St1 St0 St0 St0 000 0001 St1 St0 St0 St1 St0 St0 St0 000 0001 St1 St0 St0 St1 St0 St0 St0 001 0010 St1 St0 St0 St1 St0 St0 St0 001 0010 St1 St0 St0 St1 St0 St0 St0 010 0011 St1 St0 St0 St1 St0 St0 St0 010 0011 St1 St0 St0 St1 St0 St0 St0 010 0011 St1 St0 St0 St1 St0 St0 St0 011 0101 St1 St0 St0 St1 St0 St0 St0 011 0101 St1 St0 St0 St1 St0 St0 St0 011 0110 St1 St0 St0 St1 St0 St0 St0 101 0110 St1 St0 St0 St1 St0 St0 St0 101 0110 St1 St0 St0 St1 St0 St0 St0 101 0110 St1 St0 St0 St1 St0 St0 St0 100 0111 St1 St0 St0 St1 St0 St0 St0 110 0100 St0 St1 St0 St1 St0 St0 St0 100 0111 St0 St1 St0 St0 St1 St0 St0 St0 100 0111 St0 St1 St0 St0 St1 St0 St0 St0 100 0111 St0 St1 St0 St0 St1 St0 St0 St0 100 0111 St0 St1 St0 St0 St1 St0 St1 St0 St0 100 0100 St0 St1 St0 St0 St1 St0 St1 St0 St1 000 1000 St0 St1 St1 St1 St0 St0 St1 St0 St1 000 1000 St0 St1 St1 St1 St0 St0 St1 St0 St1 000 1000 St0 St1 St1 St1 St1 St0 St0 St1 St0 001 |

ALU test results:

Adder and subtractor tests:



Multiplier and Subtractor tests:



OR, NOR and NAND tests:

