# Instruction forma(16-bit):

## R-type:

Opcode(4-bit)	Rs(4-bit)	Rt(4-bit)	Rd(4-bit)
I-type:			

Opcode(4-bit)	Rs(4-bit)	Rt(4-bit)	Imm/Address/Offset (4-bit)
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# Instructions and Opcodes:

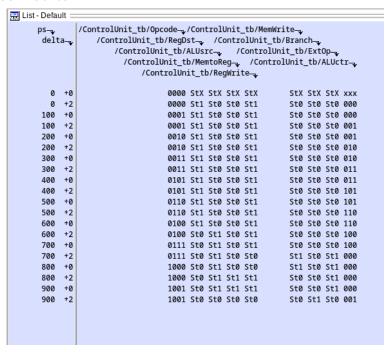
Instruction	Op Code	format
add	0000	R
sub	0001	R
mul	0010	R
div	0011	R
ori	0100	I
nor	0101	R
nand	0110	R
sw	0111	I
lw	1000	I
blt	1001	I

## Control Unit Truth Table:

	R-format	ori	sw	lw	blt
RegDst	1	0	X	0	X
Alusrc	0	1	1	1	0
MemToReg	0	0	X	1	X
RegWrite	1	1	0	1	0
MemWrite	0	0	1	0	0
Branch	0	0	0	0	1
ExtOp	X	0	1	1	0
Aluctr	Op[2:0]	Op[2:0]	000	Op[2:0]	Op[2:0]

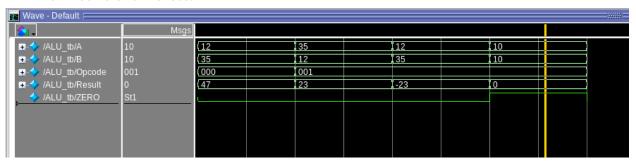
add, sub, mul, div, nor and nand are the same but with different Opcodes.

### **Control Unit test results:**

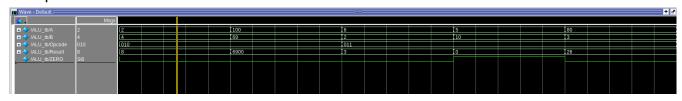


### **ALU test results:**

Adder and subtractor tests:



## Multiplier and Subtractor tests:



## OR, NOR and NAND tests:

