Digital Logic:

Question 1:

‘#’ is a tennary connective (three-input gate). ‘#pqr’ is true precisely if a majority of p,q, and r are true. A nice sum-of-products form for ‘#pqr’ is ‘pq + pr + qr’.

#pqr agrees with the majority of the truth values.

p	q	r	#pqr
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Suppose you have 2-input ‘AND’ gates that settle in 125 ps, 2-input ‘OR’ gates that settle in 135 pz, and infinitely fast wires, At time 0, all inputs are asserted.

a- How fast can you compute ‘#pqr’? show work.

b- 2-input AND gates settle in 125 ps. 2-input OR gates settle in 150 ps. How long does it take this circuit to settle? (p \/ q \/ r) \/ (s /\ t)

Answer ___ ps

c- ‘4#’ is a 12-ary connective. Its 12 inputs are divided into groups of 3. Each group of 3 inputs is fed into a separate ‘#’ gate. ‘4#’ is true precisely if all 4 ‘#’ circuits report true. At time 0, all 12 inputs are asserted. How fast can you compute ‘4#’? Show work.

d- Both {~,/\} and {~,\/} are complete. ‘→’ is a binary connective (“Conditional”). ‘p→q’ (if p, then q) is false is ‘p’ is true and ‘q’ is false, and true otherwise.
We have ‘p→q’ |==| ~p\/q’.
Show that {~,→} is complete. Derive an equivalent for ‘p/\q’ using only ‘~’ and ‘→’.

p/\q |==| _____

Question2:

$pqr is true if and only if an odd number of p,q and r is true. Fill in the missing values of $pqr

p	q	r	$pqr
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Consider implementing the logic formula 'signal 1' below as a hardware circuit without any implementation. You have 2-input 'OR' gates that settle in 150 ps, 2-input 'XOR' gates ('+') that settle in 175 ps, and infinitely fast wires. After all original inputs have been asserted, how long it takes the circuit to settle. Show numerical calculations.

Signal 1 = $((p \vee q) \vee (r \vee s)) \vee (t + u + v)$

Answer ___ ps

Question 3: Amdahl's Law

On a uniprocessor, perfectly serial portion 'A' of program 'P' consumes 10 s, while perfectly parallel portion 'B' consumes 90 s.

a- When run on a quad-core processor, the run time of P decreases to how many seconds?
b- To get at least twice the quad-core speedup requires that you have how many cores?
c- To get at least 3 times the quad-core speedup requires that you have how many cores?

Question:

In a 100-watt sequential circuit, the combinational logic dissipates20 watts independently of the clock frequency. A (clocked) state element dissipates the remaining 80 watts. In the state element, power is proportional to the square of the clock frequency.

a- The designers propose to reduce the clock frequency by a factor of 10. After the change, how much power is dissipated by the circuit?

Answer ___ watts.

b- New plan. Starting from the original circuit, the designers now propose to reduce the clock frequency by a factor of 15. After the change, how much power is dissipated by the circuit?

Answer ___ watts.

Question 3: Data Dependences between Boxes.

For each part below, list any '.a' boxes that are producers of values consumed by '.b' boxes, and also any '.b' boxes that are consumers of values produced by '.a' boxes.

Write 'none' otherwise.

a-
```
ADD   r1, r2, r3          f.a  d.a  x.a  m.a  w.a
BNE   r2, r3, loop             f.b  d.b  x.b  m.b  w.b
```

Producer (s) ----------- consumer (s) ----------------

b-
```
l.d      f6, 0(r1)        f.a  d.a  x.a  m.a  w.a
mul.d    f8, f4, f6            f.b  d.b  x.b  m.b  w.b
```

Producer (s) ----------- consumer (s) ----------------

c-
```
mul.d    f4, f2, f0       f.a  d.a  x.a  m.a  w.a
s.d      f4, 0(r1)             f.b  d.b  x.b  m.b  w.b
```

Producer (s) ----------- consumer (s) ----------------

d-
```
add   r1,r1,r1            f.a  d.a  x.a  m.a  w.a
sw    r1,8(r1)                 f.b  d.b  x.b  m.b  w.b
```

Producer (s) ----------- consumer (s) ----------------

Hex Table:

0	0000	4	0100	8	1000	c	1100
1	0001	5	0101	9	1001	d	1101
2	0010	6	0110	a	1010	e	1110
3	0011	7	0111	b	1011	f	1111

Question 4: Instruction Formats

A small computer has 16-bit registers. The instruction format for a conditional branch is

Opcode	rs	rt	immediate
2 bits	3 bits	3 bits	8 bits

a- Consider the program fragment:

```
Loop: l.d f6, 0(r2)        <at byte address 3,962>
…
…
bne r1, r2, loop           <at byte address 4,096>
```

Show the hexadecimal representation of the low-order 8 bits of the 'bne' instruction.

Answer __ __

b- Consider 'l.d f6, -65(r1)'. Show the hexadecimal representation of the fully processed, 8-bit immediate just before it is added to the base register 'r1'.

Answer __ __ __ __

c- Consider 'l.d f6, 120(r2)'. Show the hexadecimal representation of the fully processed, 8-bit immediate just before it is added to the base register 'r1'.

Answer __ __ __ __

d- Consider 'l.d f6, -120(r2)'. Show the hexadecimal representation of the fully processed, 8-bit immediate just before it is added to the base register 'r1'.

Answer __ __ __ __

Question 4: Fixed-Point and Floating-Point Formats

A small computer has 16-bit registers. All numbers are positive, so no sign bit is necessary.

a- What is the hexadecimal representation of the (8+8)-bit binary fixed-point format for 13.4? Do not round. Show work.

Answer __ __ __ __

b- The floating point format is: First four bits for the exponent, and the next 12 bits for the fractional part of the significand. What is the hexadecimal representation of the floating-point format for 13.4? Do not round. Show work.

Answer __ | __ __ __

A small computer has 16-bit registers. All floating-point numbers are positive, so no sign bit is necessary. The floating-point format is: First four bits for the exponent, and the next 12 bits for the fractional part of the significand.

a- What is the hexadecimal representation of the floating-point format for 12.125? Do not round. Show work.

Answer __ | __ __ __

b- What is the hexadecimal representation of the floating-point format for .2? Do not round. Show work.

Answer __ | __ __ __