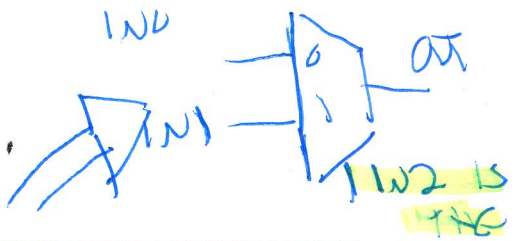
SOLUTION : PROBLEM 4



Problem 4)
An unknown component has the following truth table.

SEL

IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

The unknown component (the rectangular box in the circuit below) is part of a combinational logic circuit shown in Figure 1 which consists of one instance of this "mystery component" and a two input AND gate. The circuit has four inputs: MICK, KEITH, CHARLIE and BILL and one output STONES. (Shown below)

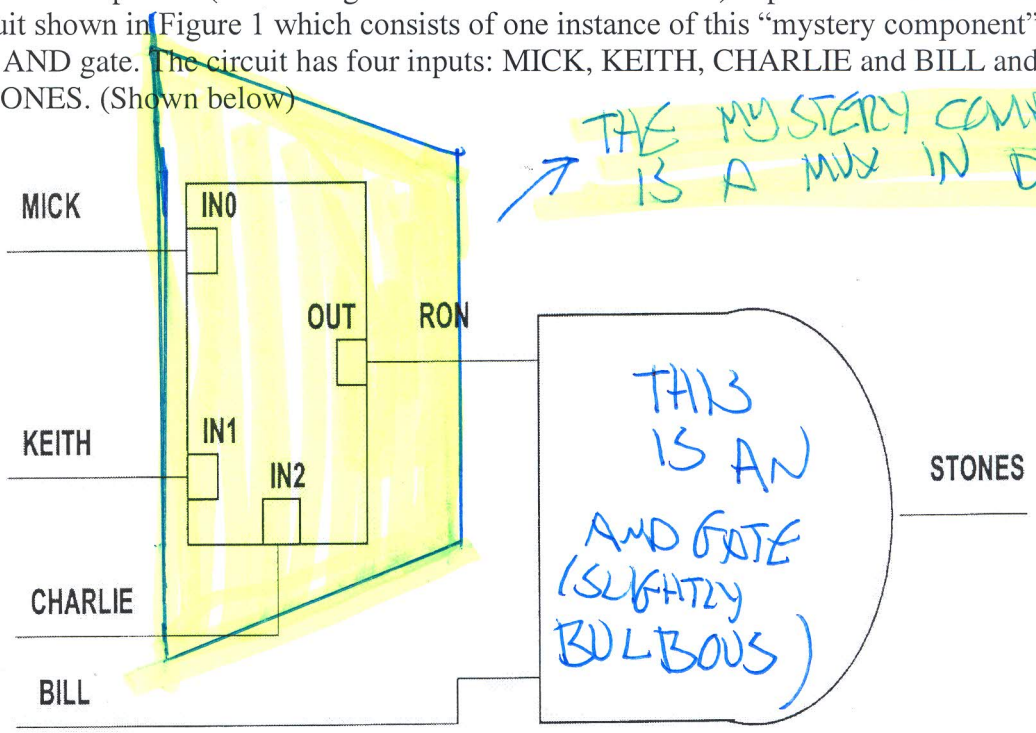
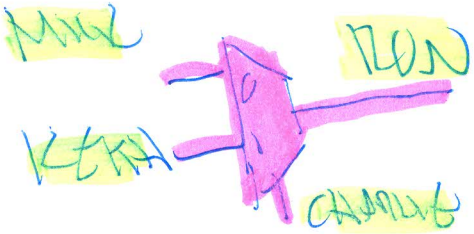


Figure 1: A circuit consisting of a "mystery component" with an AND gate.

You are to fill out the truth table below, where the response is based on the circuit in figure 1.



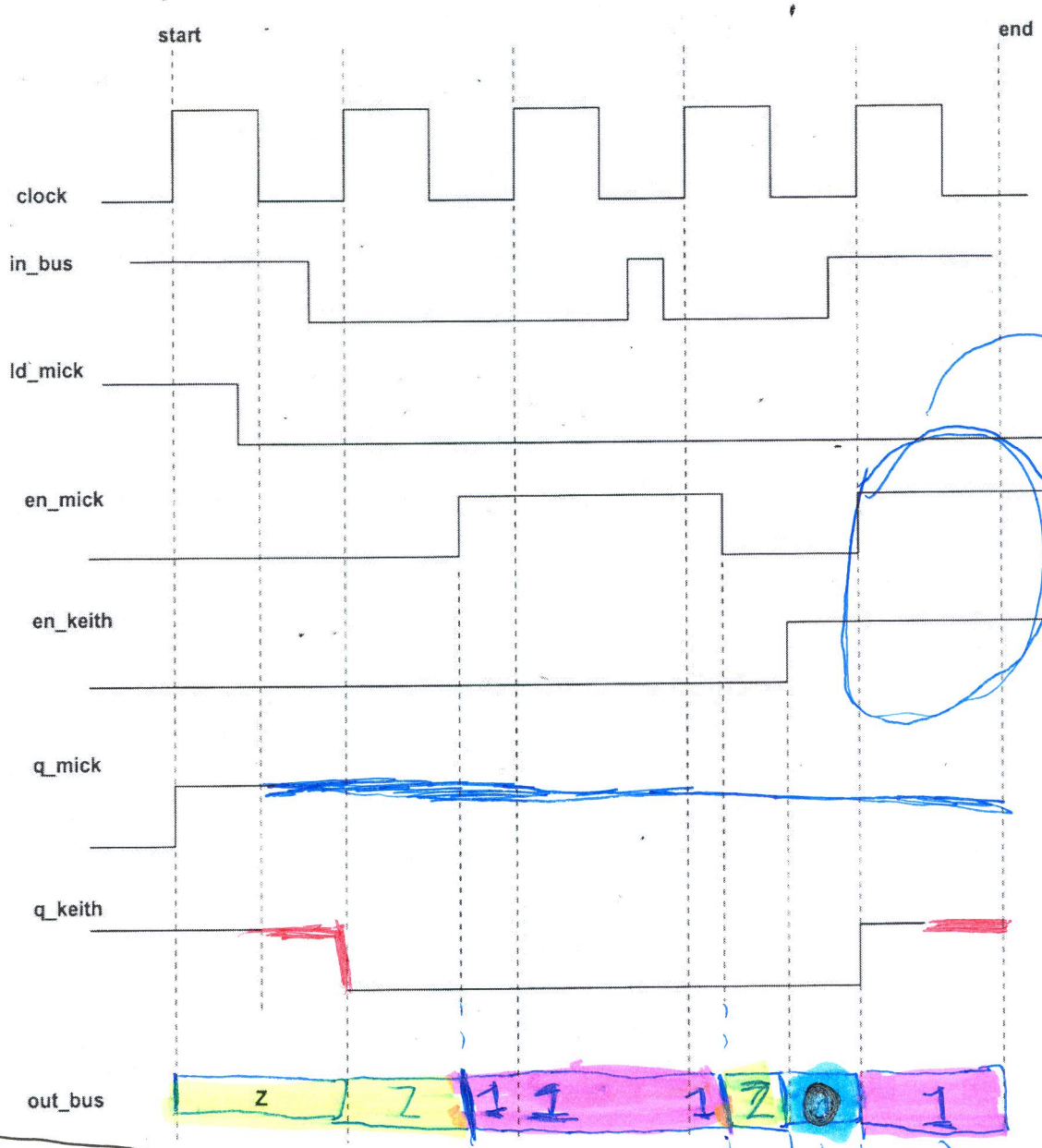
Truth Table for circuit in figure 1

MICK	KEITH	CHARLIE	BILL	RON	STONES
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	1	1

Problem 5)

Consider the circuit shown in the figure below which consists of a **positive edge triggered** flip-flop with selective load capability (identified as MICK) and a **level sensitive D-type latch** (labelled as KEITH). There is an input bus (consisting of a single wire) , an output bus, and two tri-state buffers. Complete the timing diagram which is included at the end of this question. Indicate in the provided timing diagram the behavior of the output of the flip-flop and the latch (q_mick and q_keith) as well as the behavior of the output bus between the indicated "start" and "end" times. Use the symbol "Z" to denote the state of the output bus when it is in the high-impedance (tri-state value). In the given diagram, it is assumed that the initial value of q_mick is logic '0' and that the initial value of q_keith is logic '1'. Note also that the timing diagram intentionally contains a fatal design error. You are to explain in words the nature of this design

SOLUTION: PROBLEM 5



DESIGN CONTROL. BOTH ENABLES ARE ACTIVE AT SAME TIME. THIS IS BAD.

BUS = Q_MICK

BUS = Q_KEITH

BUS DRIVEN TO LOGIC 1 SINCE BOTH Q_MICK AND Q_KEITH ARE 1. BUT THERE WOULD BE FIRE IF Q_MICK and Q_KEITH ARE OPPOSITE LOGIC VALUES.

LEGEND

Z = Z (TRI-STATE)

1 = LOGIC '1'

0 = LOGIC '0'