

3-D ORGANIZATION OF A 32 x 1 bit RAM

(USING CHIPS OF SIZE 4 LOCATIONS x 1 BIT)

A 3-D organization employs three address decoders and consists of two "slices" of a 2-D Memory system. The high-order address bit (A_4 in this example) decodes between the two slices. The MEMORY MAP is:

	Slice	Row	Column	LOCATION IN A CHIP	
	A_4	A_3	A_2	A_1	A_0
BANK 0	0	0	0	0	0
	0	0	0	0	1
	0	0	0	1	0
	0	0	0	1	1
BANK 1	0	0	1	0	0
	0	0	1	0	1
	0	0	1	1	0
	0	0	1	1	1
BANK 2	0	1	0	0	0
	0	1	0	0	1
	0	1	0	1	0
	0	1	0	1	1
BANK 3	0	1	1	0	0
	0	1	1	0	1
	0	1	1	1	0
	0	1	1	1	1
BANK 4	1	0	0	0	0
	1	0	0	0	1
	1	0	0	1	0
	1	0	0	1	1
BANK 5	1	0	1	0	0
	1	0	1	0	1
	1	0	1	1	0
	1	0	1	1	1
BANK 6	1	1	0	0	0
	1	1	0	0	1
	1	1	0	1	0
	1	1	0	1	1
BANK 7	1	1	1	0	0
	1	1	1	0	1
	1	1	1	1	0
	1	1	1	1	1

$A_4 A_3 A_2 =$
BANK NUMBER

