Date: Wednesday, April 21, 2004
Time: 14:00-17:00
Course Instructor: Tadeusz S. Obuchowicz
Location: H611

Material Allowed: Course textbooks, course lecture notes, electronic calculators, pencils, pens, rulers, erasers.

Instructions: Answer all **5** questions. If you make any assumptions, clearly state so in your anwer booklet.

Question 1: [20 points]

Consider the following floating point number format:

Sign	Exponent	Mantissa
1 bit	3 bits	4 bits

The exponent is stored in **excess-4** notation. The mantissa is **normalized** (meaning the first bit of the mantissa is always 1). There is no "hidden" 1 bit. The **base** is 2.

(a) What are the possible decimal values for the exponent field?

(b) The largest positive decimal number in this representation is +7.5. The smallest positive number we can represent in this notation is +0.03125 Give the 8-bit binary representations using the above floating-point format for the **next three largest** positive numbers and the **next three smallest** numbers. In other words, give the representations for the numbers L1, L2, L3, S1,S2, and S3 as illustrated in the following figure:

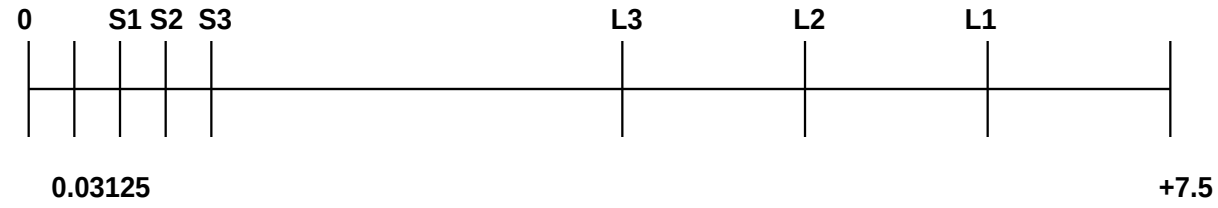

Figure 1: Number line.

(c) How many different positive numbers can be represented using this format?

(d) How will the number of different representable positive real numbers change if we change the base from 2 to 4 and keep the rest of the format identical ?

Question 2: [20 points]

Consider a CPU which has 20 bit wide instructions interfaced to a memory in which each location is 40 bits wide (see Figure 2 next page). This means every location in main memory contains 2 separate program instructions. If we have 4 words in main memory, a total of 8 instructions may be stored in this memory. A 3-bit Program Counter is necessary to access each of these 8 instructions. A 2-bit wide Memory Address Register will suffice to address the 4 words. A 20-bit wide Instruction Register is needed to store an instruction. Give the details of the "mystery component" hardware which is needed so that the Instruction Register is loaded with the appropriate instruction. Formulate a procedure which may be used to FETCH and EXECUTE instructions on this organization. Express your procedure similar to what we have done in class, i.e.:

T0: load MAR with PC
T1: read from memory and load instruction into IR
T2: "execute" the instruction
...

Of course, this is only meant as an example, your solution will be different. You may assume that the "execute" phase of an instruction may be done in one clock cycle, you do not have to show the details of the "execute" phase. We are interested in the procedure used to successively load the Instruction Register with the low-order and high-order 20-bit instructions stored in a given 40-bit word stored in one location of the memory.

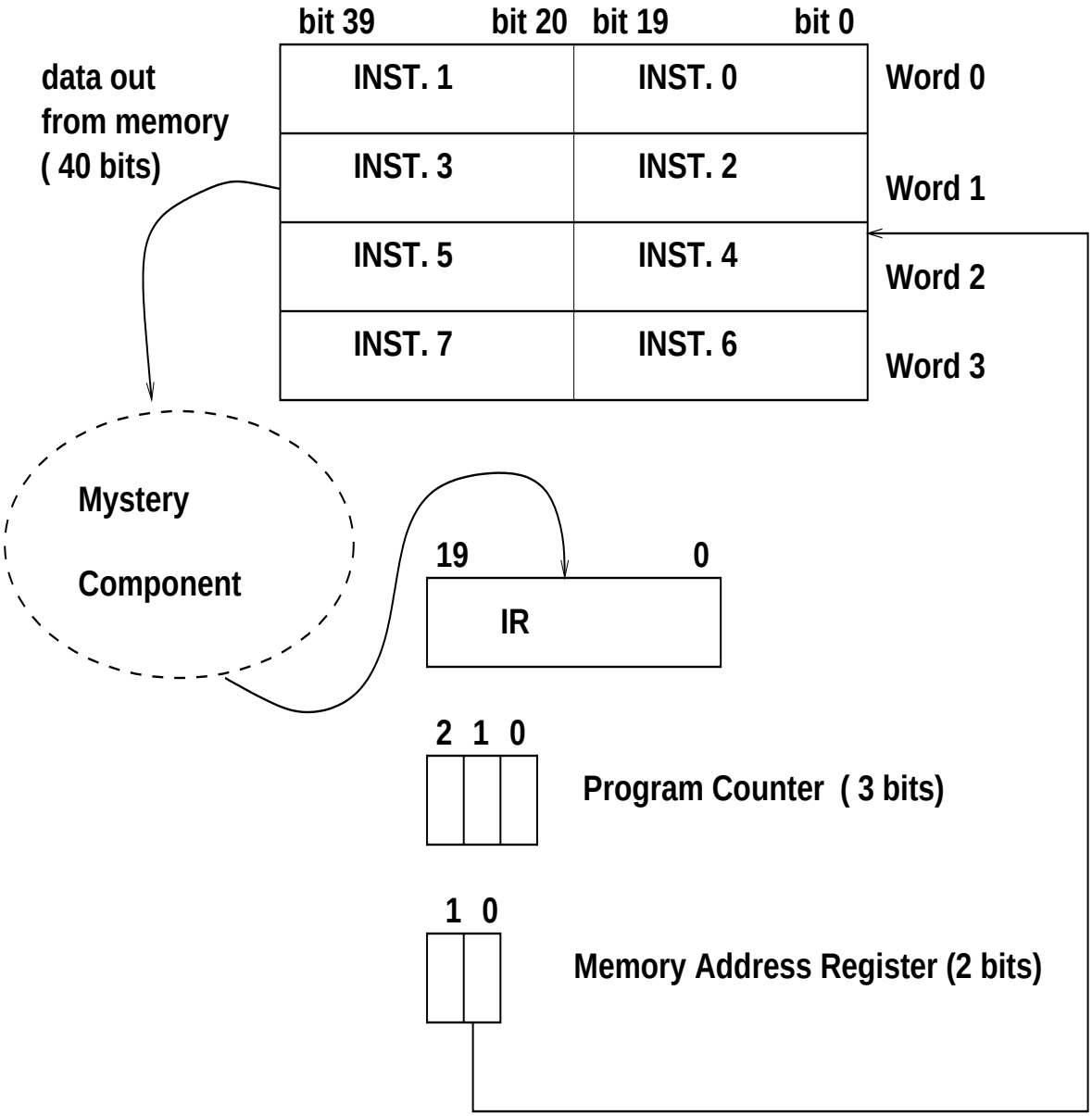

Figure 2: A "wide" memory interfaced to a "narrow" CPU.

Question 3: [20 points]

Consider a small, **direct-mapped** cache which consists of 8 blocks with 4 bytes per block. Main memory consists of 256 bytes.

(a) Give the format of a main memory address in terms of the Word, Block, and Tag fields.

(b) How many different main memory blocks map onto a given cache block?

(c) When a program is executed, the processor reads the following sequence of main memory locations:

00, 04, 08, 0C, F4, F0, 00, 04, 18, 1C, 4C, F4 (addresses are given in hexadecimal).

This pattern of reads is repeated a total of **4 times**. Assuming that the cache is **initially empty**, **show the contents of the cache** at the end of every pass through the loop. **Compute the hit rate**. Use the style shown in Figure 3 when showing the contents of the cache at the end of each pass. In this figure, the [00] means the main memory block which contains the byte stored at address 00 is stored in cache block 0.

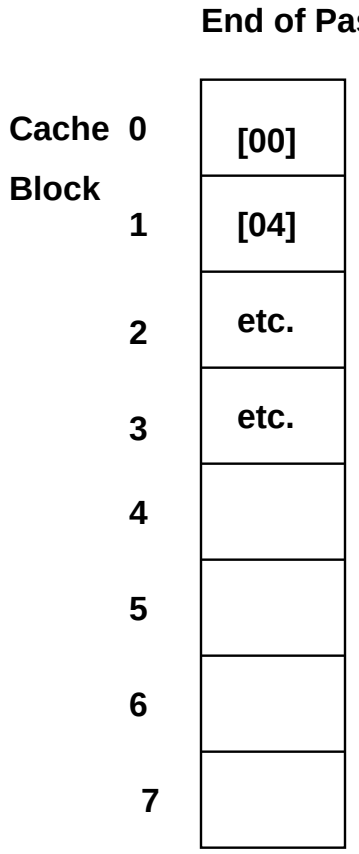

Figure 3: How to show contents of cache at end of each pass.

Question 4: [20 points]

Consider a main memory system consisting of 24 different locations, each location is 8 bits wide. Thus, the range of addresses in this main memory is 00000 through to 10111 (in binary). Design the memory system using RAM chips of size 4 locations with 8 bits per location. Show your memory map. Draw a NEAT diagram showing the organization of the chips and the address, data, and control line connections to and from the CPU/memory.

Question 5: [20 points]

Answer TRUE or FALSE for the following:

(a) It requires less time to read or write into a CPU register than it does to read or write into a main memory location.

(b) The access time for a cache memory is longer than the access time for main memory.

(c) The contents of secondary storage (magnetic tape, magnetic hard drives, optical disks) are lost when power is removed from the storage device.

(d) An interrupt service routine is a specialized type of subroutine.

(e) A daisy chain structure is used to determine which device has raised an interrupt and requires servicing when a CPU has a single INTERRUPT line and a single INTERRUPT ACKNOWL-EDGE line.

(f) Programmed I/O is an inefficient means of performing input/output with slow devices.

(g) "Busy waiting" occurs with interrupt I/O.

(h) In an I/O mapped system, a device may share an address with a main memory location.

(i) Overflow can never occur in n-bit two's complement notation whenever we add two numbers of opposite sign.

(j) Cache memory systems make use of the fact that a program at run-time exhibits a property known as the "locality of reference".