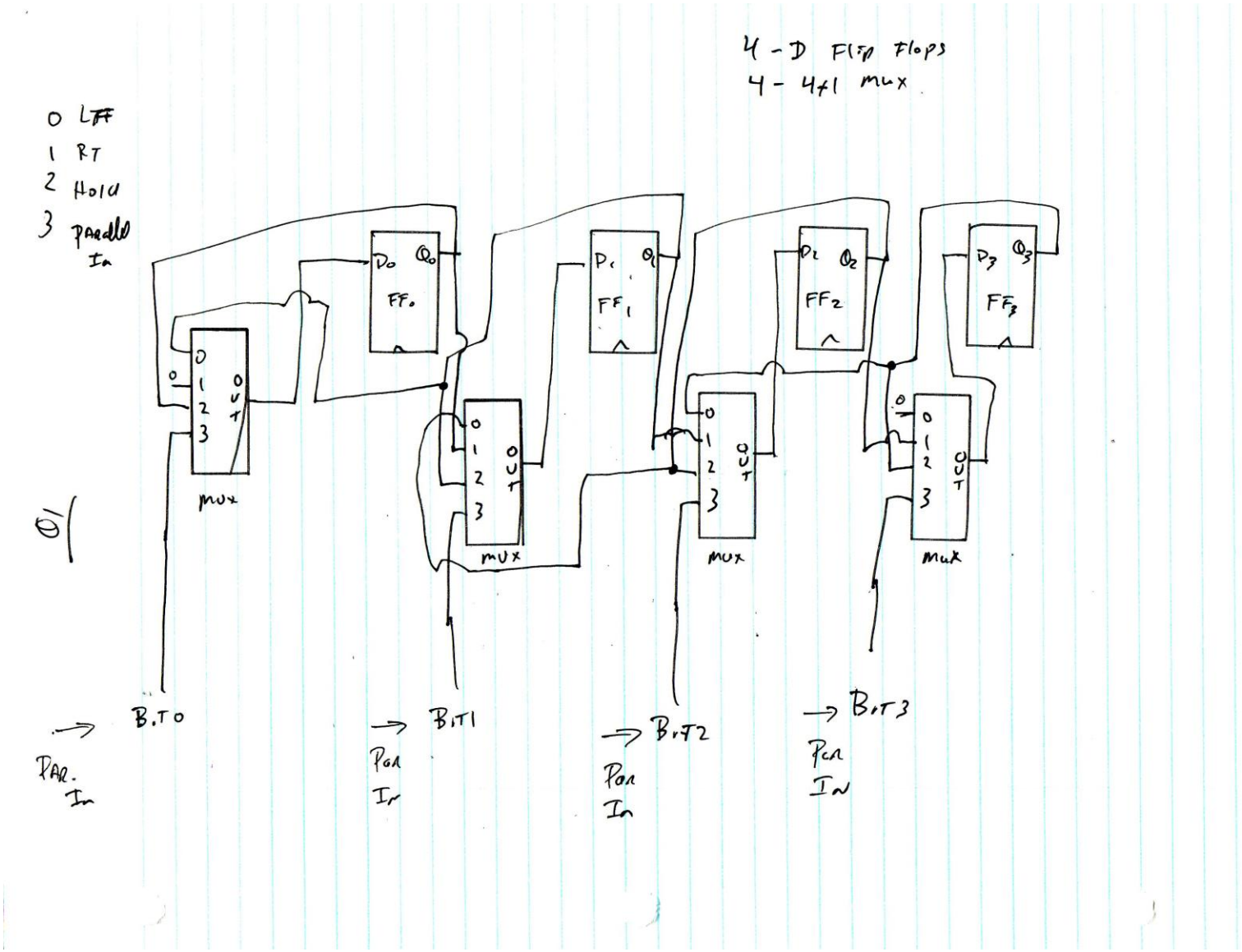
61)

~~Dsgn~~ Design a 4 Bit Register
has the following features
That ~~with~~ i) Parallel Read 4 Bits
from Another device.
ii) Hold Bit Values
iii) Shift left
iv) Shift Right


4 - D Flip Flops
4 - 4x1 mux
0 LFF
1 RT
2 Hold
3 parallel In
FF0
FF1
FF2
FF3
mux
mux
mux
mux
Bit 0
Bit 1
Bit 2
Bit 3
Par. In
Par In
Par In
Par In

Q2/

For each of the Below cases

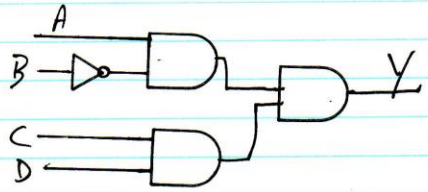
Design A Circuit To detect A PATTERN 1011 And Produce AN Output of 1 When The Bits ARE Read

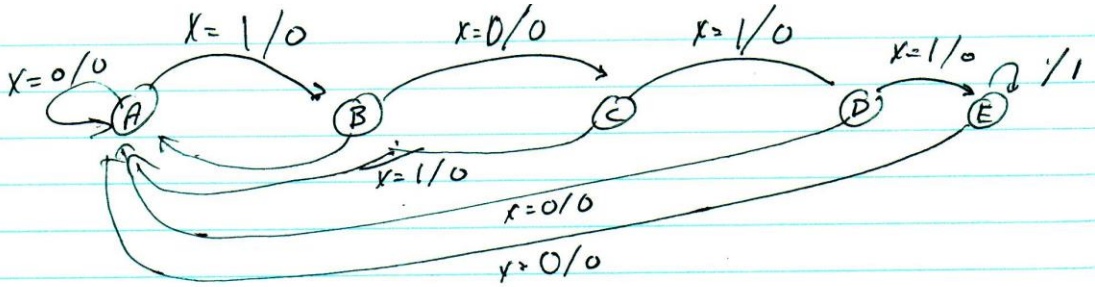
1) In Parallel
2) in Series

Q2 i) 1/

Parallel Using 3- 2 input AND Gate
1- Inverter.

$Y = A\bar{B}CD$




FORMAT X input / output

Output Zero Until STATE E

So Out = $Q_0\bar{Q}_1\bar{Q}_2$

| $Q_0$ | $Q_1$ | $Q_2$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |

Q2 ii

5 STATES
→ 3 Flip Flops (Allows for 8 STATES

| | $Q_0$ $Q_1$ $Q_2$ |
|---|---|
| A | 0 0 0 |
| B | 0 0 1 |
| C | 0 1 0 |
| D | 0 1 1 |
| E | 1 0 0 |
| F | 1 0 1 |
| G | 1 1 0 |
| H | 1 1 1 |

F, G, H: extra states

$Y = Q_0 \bar{Q}_1 \bar{Q}_2$

one input line A I
one output line O/P

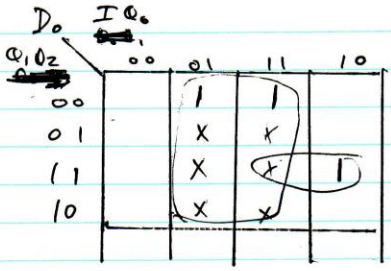
| | Present | | | Next | | |
|---|---|---|---|---|---|---|
| I | $Q_0$ | $Q_1$ | $Q_2$ | $Q_0^+$ | $Q_1^+$ | $Q_2^+$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | x | x | x |
| 0 | 1 | 1 | 0 | x | x | x |
| 0 | 1 | 1 | 1 | x | x | x |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | x | x | x |
| 1 | 1 | 1 | 0 | x | x | x |
| 1 | 1 | 1 | 1 | x | x | x |

x → don't care does not happen

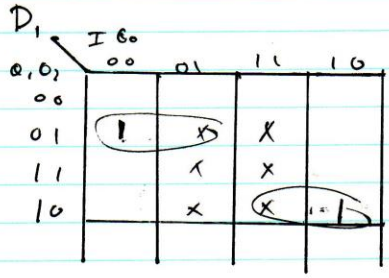
Q2 ii)



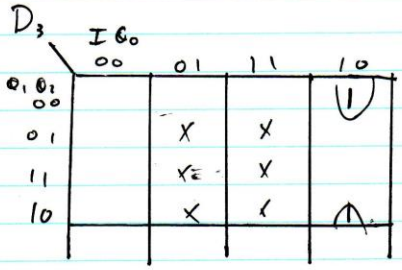
Flip Flop inputs And Transition



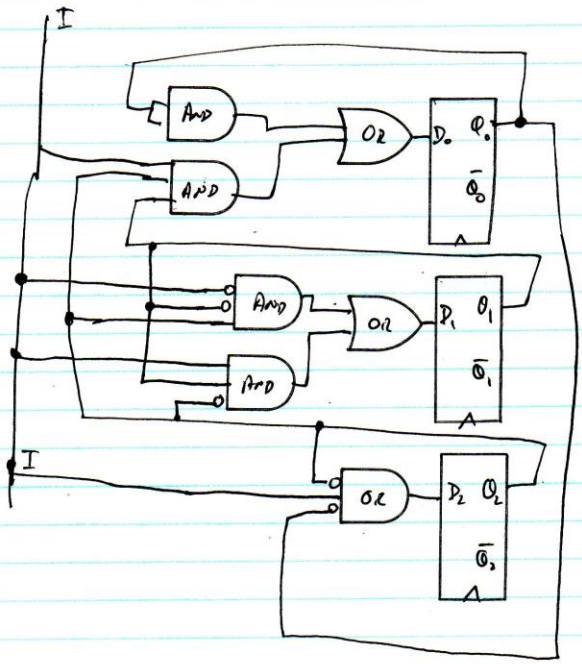

$$D_0 = Q_0 + I Q_1 Q_2$$




$$D_1 = \bar{I} \bar{Q}_1 Q_2 + I Q_1 \bar{Q}_2$$




$$D_3 = I \bar{Q}_0 \bar{Q}_2$$




$D_0 = Q_0 + I Q_1 Q_2$

$D_1 = \bar{I} \bar{Q}_1 Q_2 + I Q_1 \bar{Q}_2$

$D_2 = I \bar{Q}_0 \bar{Q}_2$

Clock NOT shown.

o → Denotes

1) Could have used $\bar{Q}_0$, $Q_1$ $\bar{Q}_2$ inputs But MAKE this using Inverters

Bad design choice

03)

Simply the following Boolean expressions to a minimum Number of literals

1) $\overline{AB}\,(AB + CD)$

2) $(A+\overline{B})\,(A+\overline{B})$

3) $AB + \overline{A}C + BC$

4) $(A+B)\,(\overline{A}+C)\,(B+C)$

5) $A + \overline{A}B$

Q3) Solution 1/

1) $\bar{A}\bar{B}(AB + CD)$

$= (\bar{A}\bar{B})(AB) + \bar{A}\bar{B}CD$

$= 0 + \bar{A}\bar{B}CD$

$= \boxed{\bar{A}\bar{B}CD}$

2) $(A+B)(A+\bar{B})$

$= AA + A\bar{B} + AB + B\bar{B}$

$= A + A\bar{B} + AB + 0$

$= A + A(B + \bar{B})$

$= A + A(1)$

$= A + \bar{A} = \boxed{A}$

3) $AB + \bar{A}C + BC$ ← This is 1

$AB + \bar{A}C + BC(A + \bar{A})$

$AB + \bar{A}C + ABC + \bar{A}BC$

$AB(1 + C) + \bar{A}C(1 + B)$

$= \cancel{AB + AC}$ $AB(1) + \bar{A}C(1)$

$= \boxed{AB + \bar{A}C}$

4) $(A+B)(\bar{A}+C)(B+C)$

By duality This is ~~Example~~ the dual of Problem 3

dual of $AB + \bar{A}C$ is $(A+B)(\bar{A}+C)$

so $(A+B)(\bar{A}+C)(B+C) = \boxed{(A+B)(\bar{A}+C)}$

Q3) Solution

~~$A(\bar{A}+B)$~~ $A + \bar{A}B$

$= (A + \bar{A})(A + B)$

$= 1(A + B) = A + B$

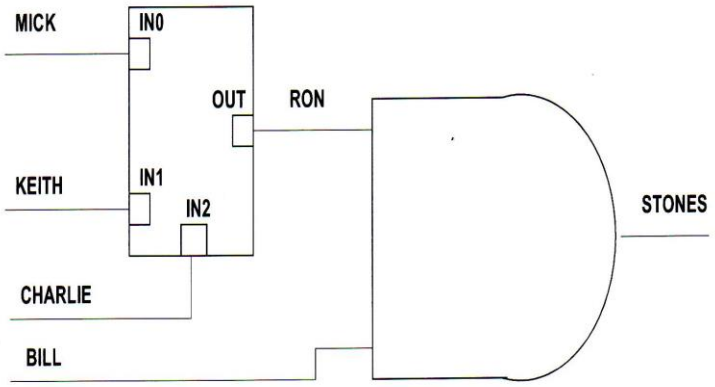
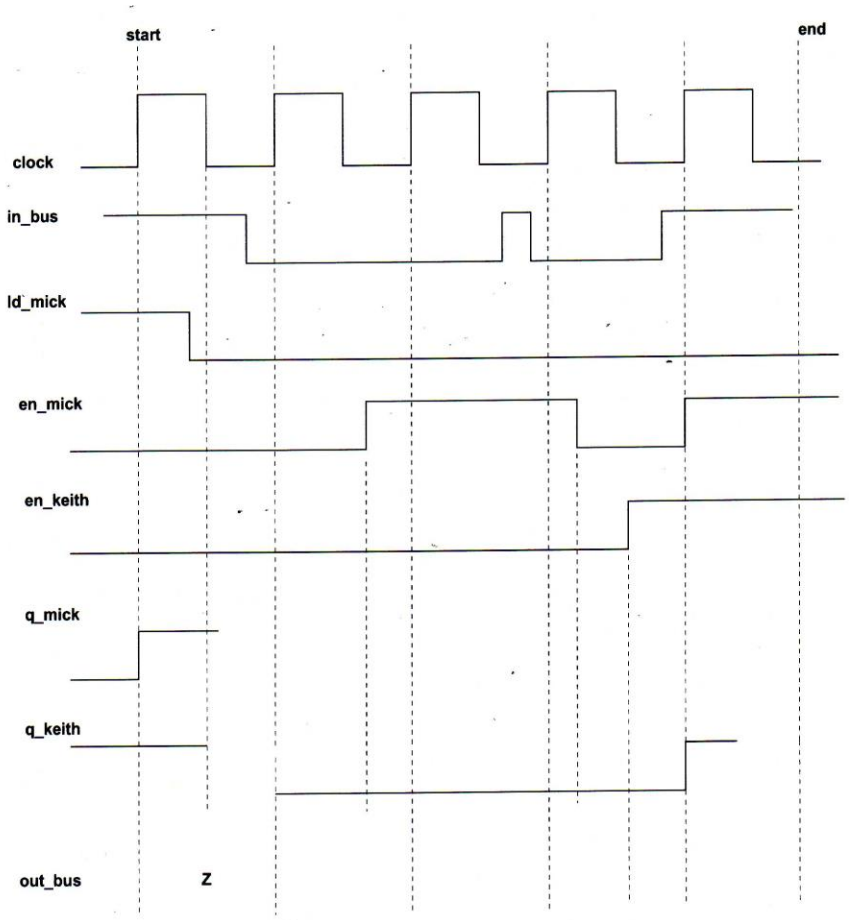
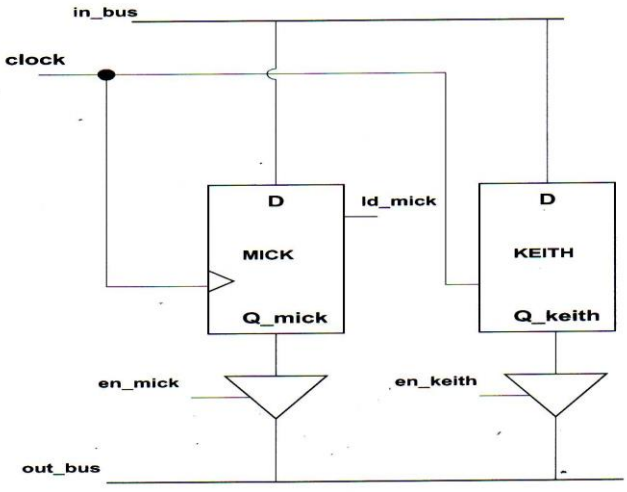



Figure 1: A circuit consisting of a "mystery component" with an AND gate.

**Table 2: Partially Completed Truth Table for the circuit in Figure 1**

| MICK | KEITH | CHARLIE | BILL | RON | STONES |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | | |
| 0 | 0 | 1 | 1 | | |
| 0 | 1 | 0 | 0 | 0 | |
| 0 | 1 | 0 | 1 | 0 | |
| 0 | 1 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | | |
| 1 | 0 | 0 | 1 | | |
| 1 | 0 | 1 | 0 | | |
| 1 | 0 | 1 | 1 | | |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | | |
| 1 | 1 | 1 | 1 | | |


start
end
clock
in_bus
ld_mick
en_mick
en_keith
q_mick
q_keith
out_bus
Z


in_bus
clock
D
MICK
Q_mick
ld_mick
D
KEITH
Q_keith
en_mick
en_keith
out_bus