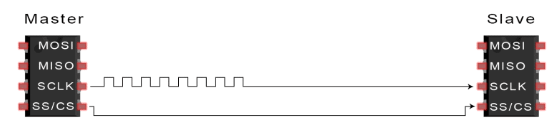
**Practical 4: RPI-3B SPI and Interrupt**

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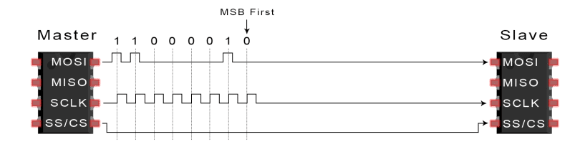
Ciaran McKey – MCKDAV12

**Question 1:**

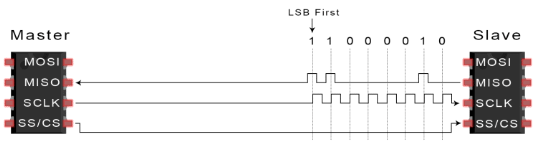
1. SPI communication protocol works in a synchronous system where both devices (slave and master) share a common clock signal. The clock signal synchronizes the master output data bits to the sampling bits of the slave. One bit of data is transferred per clock cycle therefore the speed of data transfer is determined by the frequency of the clock. SPI communication is initiated by the master as the master configures and generates the clock signal. The clock signal can be modified using “clock polarity” and “clock phase”. These properties determine when the data bits are output and sampled. “Clock polarity” sets whether the bits are output/sampled on rising/falling edges of the clock cycle. “Clock phase” sets whether the bits are output/sampled on the first/second edge of the clock cycle; regardless of rising/falling state. A timing diagram is shown below:
   1. The master outputs a clock signal to the slave via the SCLK channel and sets SS LOW, to enable the slave.
   2. The master outputs data bits, one at a time on the rising edge of the clock cycle from the MOSI channel and is sampled by the slave simultaneously.
   3. If there is a response required, the slave replies with data bits, one at a time on the rising edge of the clock cycle. This can occur while data is being transmitted from the master to slave.



a



b



c