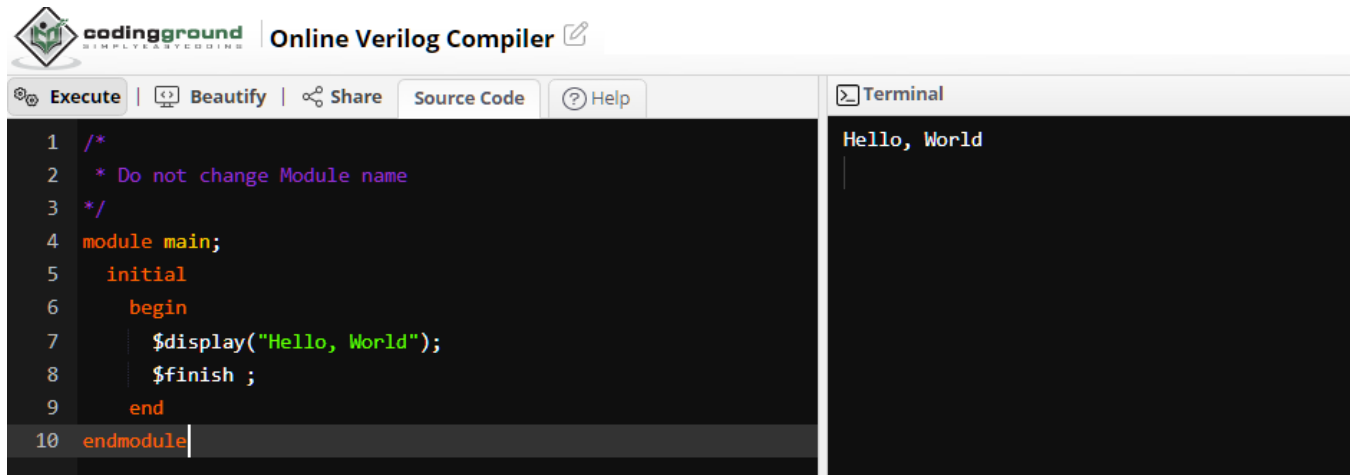


In Class Assignment #1 (9/18)

- **Design a 4-bit ripple carry counter and a stimulus**
 - Please see the textbook
 - Submit a zip file (DD01_StudentID.zip) that includes Verilog source and screen capture for the result to LMS
- **Please use AMD/Xilinx Vivado or an online Verilog compiler**
 - https://www.tutorialspoint.com/compile_verilog_online.php



The screenshot shows a web-based Verilog compiler interface. The top bar includes the 'codingground' logo and the title 'Online Verilog Compiler'. Below the bar are tabs for 'Execute', 'Beautify', 'Share', 'Source Code', and 'Help'. The main area is split into two panes. The left pane contains Verilog code:

```
1 /*
2  * Do not change Module name
3  */
4 module main;
5     initial
6     begin
7         $display("Hello, World");
8         $finish ;
9     end
10 endmodule
```

 The right pane, titled 'Terminal', shows the output:

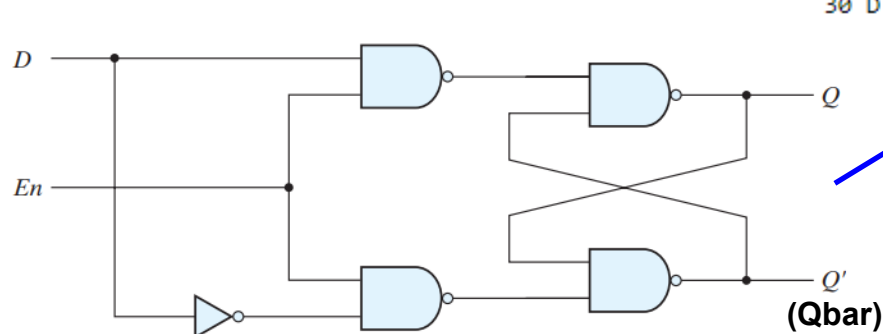
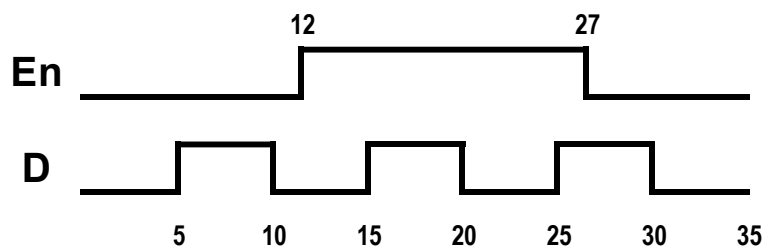
```
Hello, World
```

- <https://www.jdoodle.com/execute-verilog-online/>
- <https://coderpad.io/languages/verilog/>

- **Please everybody completes the installation of Xilinx Vivado**

In Class Assignment #2 (9/18)

- **Design a D-latch based on a NAND-based SR latch**
 - Please see the SR latch implementation at the textbook
 - Module name: D_latch, Input: D, En, Output: Q, Qbar
 - Stimulus name: Top, Please use **named mapping** to instantiate D_latch and apply the following waveform to the latch
 - Submit DD02_StudentID.zip that includes source and screen capture to LMS



(a) Logic diagram

0 D = 0, En = 0, Q = x, Qbar = x
 5 D = 1, En = 0, Q = x, Qbar = x
 10 D = 0, En = 0, Q = x, Qbar = x
 12 D = 0, En = 1, Q = 0, Qbar = 1
 15 D = 1, En = 1, Q = 1, Qbar = 0
 20 D = 0, En = 1, Q = 0, Qbar = 1
 25 D = 1, En = 1, Q = 1, Qbar = 0
 27 D = 1, En = 0, Q = 1, Qbar = 0
 30 D = 0, En = 0, Q = 1, Qbar = 0

En	D	Next state of Q
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table