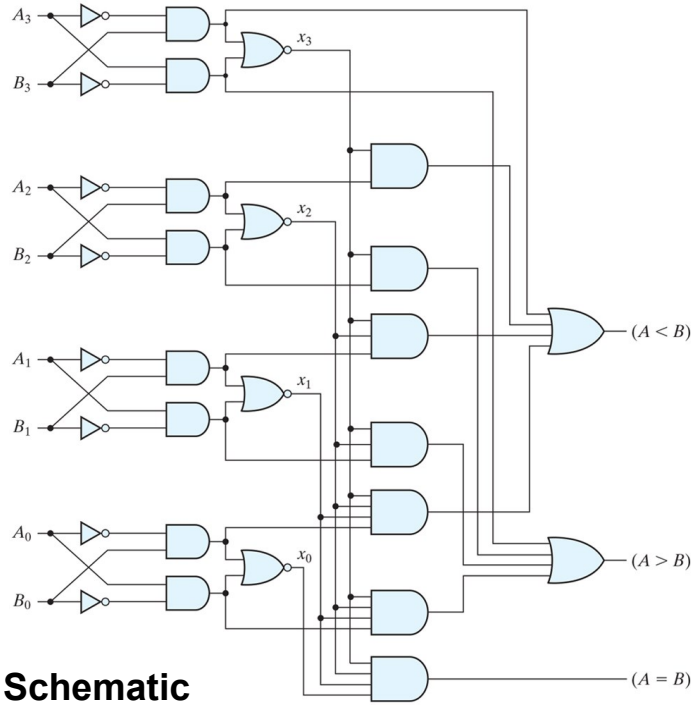
In Class Assignment #3 (9/25)

- **Design a 4-bit comparator using gate-level modeling**
  - Module: MyComparatorGate, Stimulus: Top, Please use named mapping
  - Input: A, B (4-bits), Output: A_lt_B, A_gt_B, A_eq_B (1-bit)
  - Apply the input pairs (A, B) = (4'h0, 4h'1), (4'hf, 4'h3), (4'ha, 4'hb), (4'h0, 4'h0), (4'h7, 4'hd), (4'h9, 4'h9) with a delay of 10
  - Submit DD03_StudentID.zip that includes source and screen capture to LMS



Schematic

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 0 A = 0, B = 1, A_lt_B = 1, A_gt_B = 0, A_eq_B = 0
10 A = f, B = 3, A_lt_B = 0, A_gt_B = 1, A_eq_B = 0
20 A = a, B = b, A_lt_B = 1, A_gt_B = 0, A_eq_B = 0
30 A = 0, B = 0, A_lt_B = 0, A_gt_B = 0, A_eq_B = 1
40 A = 7, B = d, A_lt_B = 1, A_gt_B = 0, A_eq_B = 0
50 A = 9, B = 9, A_lt_B = 0, A_gt_B = 0, A_eq_B = 1
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Expected Outputs