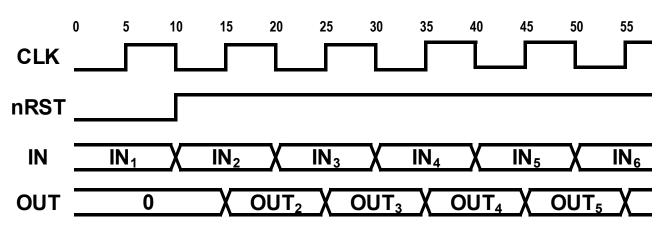
## In Class Assignment #5 (1) (10/16)

- Design a 4-bit comparator and a BCD to decimal decoder using behavioral modeling
  - Make each output to be captured by a positive edge D flipflop with negative edge triggered asynchronous reset (CLK, nRST)
  - Use at least two always statements for comb/seg circuit each
  - Set the clock period of 10
  - Use the named mapping to instantiate each design
  - Input stimulus and the expected output timing diagram



Submit zip files that contain the source code and screen capture to LMS

## In Class Assignment #5 (2) (10/16)

- 4-bit comparator (DD05-1\_StudentID.v)
  - Module: MyComparatorBeh, Stimulus: Top
  - Input: A, B (4-bits), CLK, nRST, Output: A\_lt\_B, A\_gt\_B, A\_eq\_B (1-bit)

Apply the input pairs (A, B) = (4'h0, 4h'1), (4'hf, 4'h3), (4'ha, 4'hb), (4'h0, 4'h0),

(4'h7, 4'hd), (4'h9, 4'h9)

```
0 A = 0, B = 1, A_lt_B = 0, A_gt_B = 0, A_eq_B = 0
10 A = f, B = 3, A_lt_B = 0, A_gt_B = 0, A_eq_B = 0
15 A = f, B = 3, A_lt_B = 0, A_gt_B = 1, A_eq_B = 0
20 A = a, B = b, A_lt_B = 0, A_gt_B = 1, A_eq_B = 0
25 A = a, B = b, A_lt_B = 1, A_gt_B = 0, A_eq_B = 0
30 A = 0, B = 0, A_lt_B = 1, A_gt_B = 0, A_eq_B = 0
35 A = 0, B = 0, A_lt_B = 0, A_gt_B = 0, A_eq_B = 1
40 A = 7, B = d, A_lt_B = 0, A_gt_B = 0, A_eq_B = 1
45 A = 7, B = d, A_lt_B = 1, A_gt_B = 0, A_eq_B = 0
50 A = 9, B = 9, A_lt_B = 1, A_gt_B = 0, A_eq_B = 0
55 A = 9, B = 9, A_lt_B = 0, A_gt_B = 0, A_eq_B = 1
```

## BCD to decimal decoder (DD05-2\_StudentID.v)

- Module: BCDtoDecimalBeh, Stimulus: Top
- Input: BCDIn (4-bits), CLK, nRST
- Output: DECOut (10-bits)
- Apply the input from 0 to 15 and 0 again

```
0 --> DECOut = 0000000000
              --> DECOut = 0000000000
55 BCDIn = 5 --> DECOut = 0000100000
            9 --> DECOut = 0100000000
            9 --> DECOut = 1000000000
100 BCDIn = 10 --> DECOut = 1000000000
           0 --> DECOut = 0000000000
165 BCDIn = 0 --> DECOut = 0000000000
```