# Introduction

In this demo we will demonstrate that the specification vs verification package can handle running of multiple testcases as separate simulator runs. The output from each of the simulation runs will be stored to individual files, and the run\_spec\_vs\_verif.py script will combine the output from all the test runs when evaluating the requirements.

# Background Information

This example of the Specification vs Verification concept is slightly more advanced than the example located in the basic\_usage folder. This example will demonstrate the multiple output files and sub-requirements feature of the Specification vs Verification concept. Similar to the basic\_usage example, the testbench is based on a simplified version of the testbench available in the bitvis\_uart example. The UART DUT is located under *bitvis\_uart/src/*.

For this example, the following requirements are used as requirements from the “customer”.

|  |  |
| --- | --- |
| **Requirement** | **Description** |
| FPGA\_SPEC\_1 | The default register values of the module shall be as follows:   * RX\_DATA: 0x00 * TX\_READY: 0x01 * RX\_DATA\_VALID: 0x00 |
| FPGA\_SPEC\_2 | Data written to the TX\_DATA register shall be transmitted by the UART TX interface |
| FPGA\_SPEC\_3 | Data received by the UART RX interface shall be made available in the RX\_DATA register, accessible over SPI |
| FPGA\_SPEC\_4 | The module shall handle simultaneous operation of UART transmit and receive. |

The first requirement, FPGA\_SPEC\_1, is broader than it should be. As it is now, it contains three individual, testable requirements. In order to get the desired configuration where one requirement is tested by one testcase, we divide the requirement into three sub-requirements:

**FPGA\_SPEC\_1.a** – The default register value of RX\_DATA shall be 0x00

**FPGA\_SPEC\_1.b** – The default register value of TX\_READY shall be 0x01

**FPGA\_SPEC\_1.c** – The default register value of RX\_DATA\_VALID shall be 0x00

In addition, the customer follows a strict development procedure where all testcases must be defined before implementation, and it must be demonstrated that all requirements will be covered by the verification. In these cases, it is common to create a testcase to requirement mapping. For this example, the testcase to requirement mapping can be seen in the table below.

|  |  |  |
| --- | --- | --- |
| **Testcase** | **Verifies Requirement** | **Description** |
| TC\_DUT\_DEFAULTS\_0 | FPGA\_SPEC\_1.a | The default register value of RX\_DATA shall be 0x00. |
| TC\_DUT\_DEFAULTS\_1 | FPGA\_SPEC\_1.b | The default register value of TX\_READY shall be 0x01. |
| TC\_DUT\_DEFAULTS\_2 | FPGA\_SPEC\_1.c | The default register value of RX\_DATA\_VALID shall be 0x00. |
| TC\_UART\_TX | FPGA\_SPEC\_2 | Data written to the TX\_DATA register shall be transmitted by the UART TX interface. |
| TC\_UART\_RX | FPGA\_SPEC\_3 | Data received by the UART RX interface shall be made available in the RX\_DATA register, accessible over SPI. |
| TC\_UART\_SIMULTANEOUS | FPGA\_SPEC\_4 | The module shall handle simultaneous operation of UART transmit and receive. |

The information in this table is added to the req\_to\_test\_map.csv file.

# Running the demo

The demo can be run by running the python script *run\_advanced\_demo.py* from the script/ directory:

>>python run\_advanced\_demo.py

Or from the sim/ directory:

>>python ../script/run\_advanced\_demo.py

Note that Python 3.x is required to run this demo-script. The script will compile all the VHDL sources and execute each testcase as a separate run in the simulator. Since some simulators are locked to a fixed number of licenses, the simulations will not be started in parallel. However, this could be efficient if there are multiple available simulation licenses.

Once all the VHDL testcases have completed, the *run\_advanced\_demo.py* script will call the *run\_spec\_vs\_verif.py* script automatically. The input to the script is read from the file */demo/advanced\_usage/resultlistfile.txt.* The script will parse the output files from the VHDL simulations, now located under:

* */sim/advanced\_demo\_req\_output\_file\_TC0.csv*
* */sim/advanced\_demo\_req\_output\_file\_TC1.csv*
* */sim/advanced\_demo\_req\_output\_file\_TC2.csv*
* */sim/advanced\_demo\_req\_output\_file\_TC3.csv*

The script will also read the requirement to sub-requirement configuration that is located in the CSV file */demo/advanced\_usage/req\_to\_sub\_req\_map.csv*, and the requirement to testcase map that is located in the CSV file */demo/advanced\_usage/req\_to\_test\_map.csv*.

After reading all the input files, the script will go through the data and evaluate each requirement as compliant or non-compliant. The results of this evaluation is written to the output file, which is stored under /*sim/advanced\_usage\_requirement\_results.csv*.