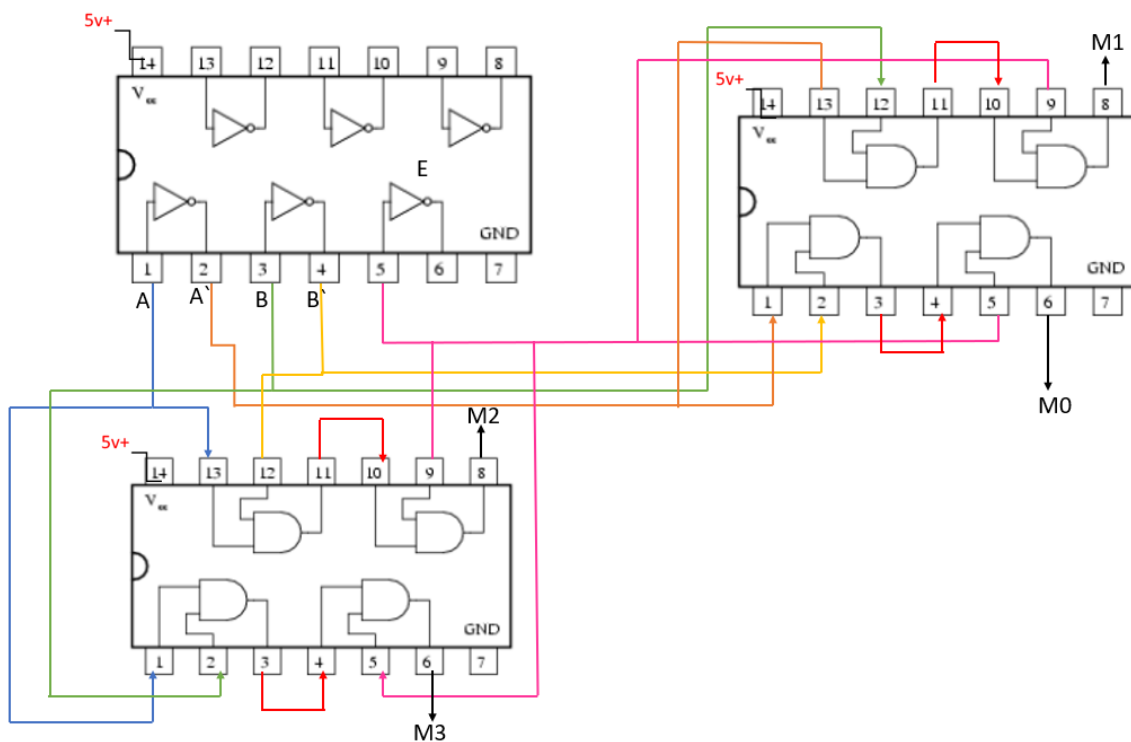Name: Rasha Mansour

ID:1210773

4.6 Post Lab

1. How do you go about adding an Enable (E) signal to the decoder in Figure 4.7? Modify the

implementation to show that. (Design Only using chips in Figure 1).
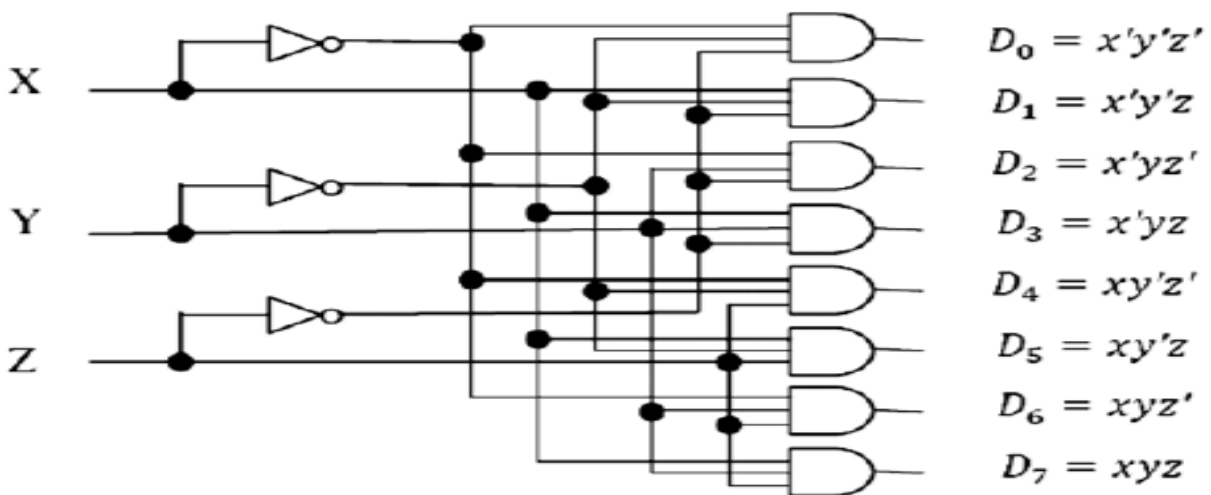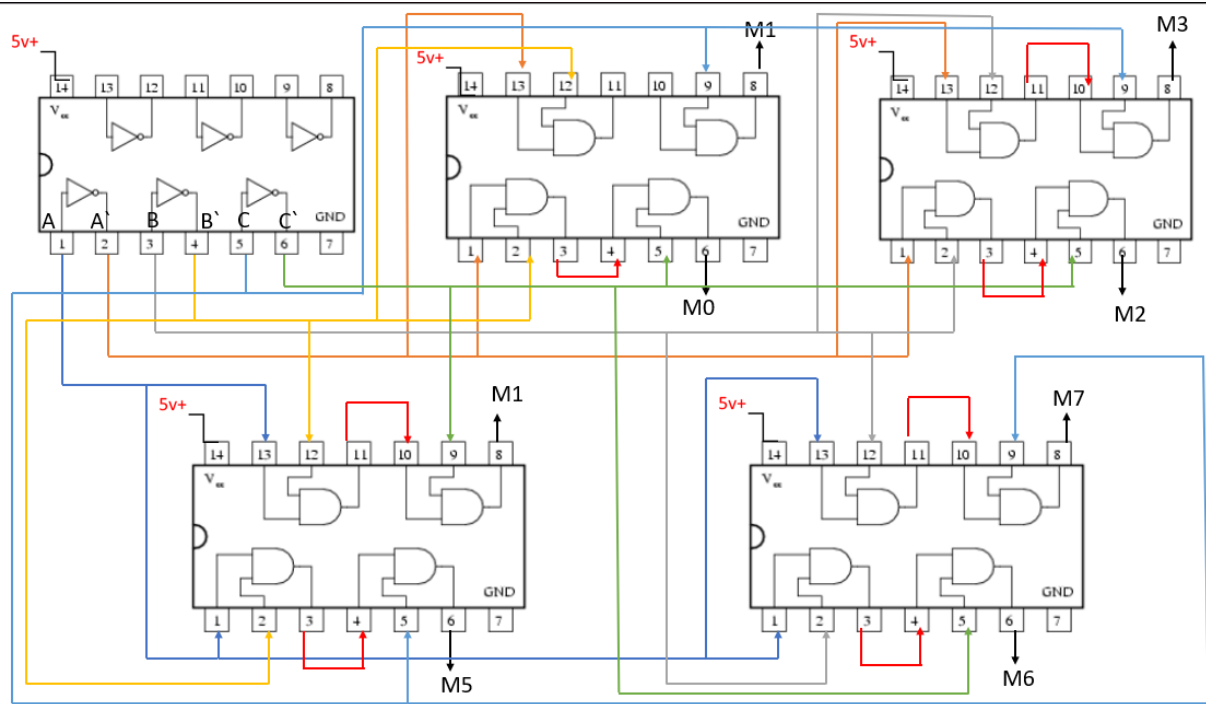
Decoder 2x4 with Enable:

E	A	B	M0	M1	M2	M3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

2. How to use that to implement a 3x8 decoder using chips in Figure 1.

A	B	C	M0	M1	M2	M3	M4	M5	M6	M7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

$$D_0 = x'y'z'$$
$$D_1 = x'y'z$$
$$D_2 = x'yz'$$
$$D_3 = x'yz$$
$$D_4 = xy'z'$$
$$D_5 = xy'z$$
$$D_6 = xyz'$$
$$D_7 = xyz$$

3. Use the just constructed 4x1 multiplexer to design a three inputs network that gives 1 if the majority of its inputs are 1 and outputs a zero otherwise (Design Only using chips in Figure

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1
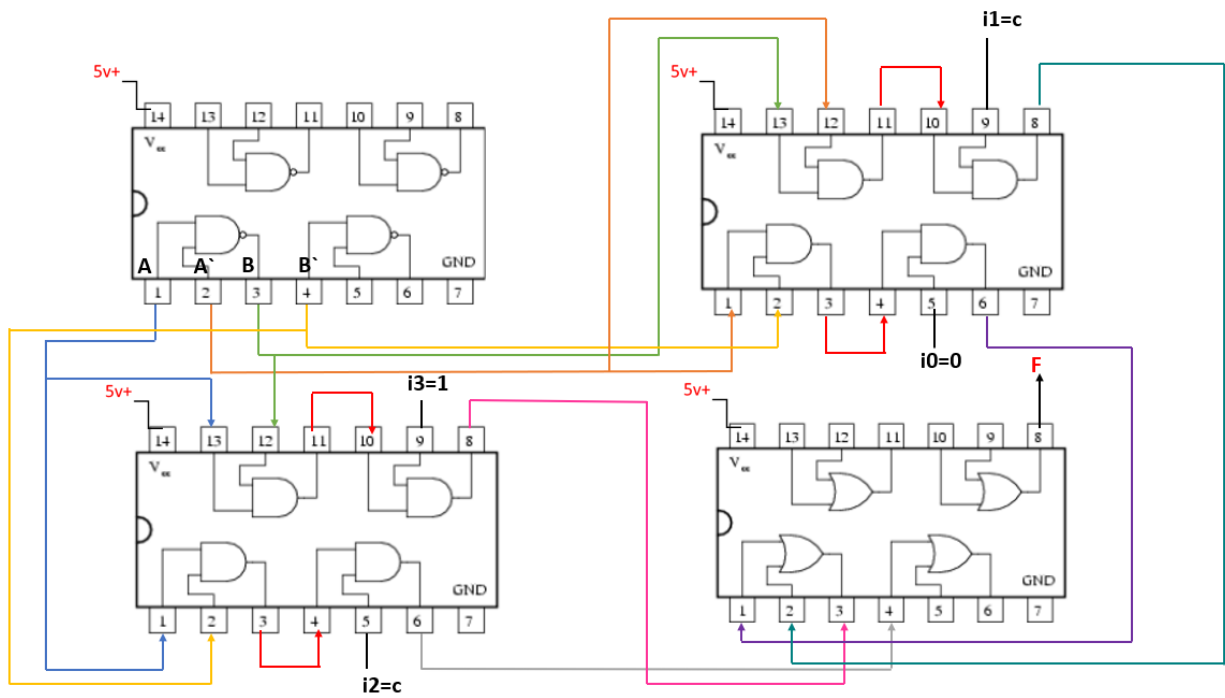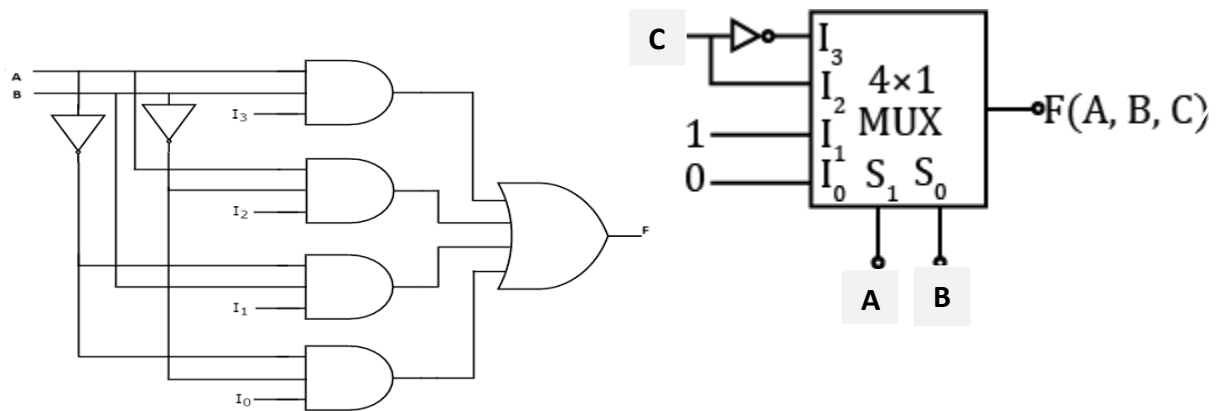
4. Implement f(x, y, z) = m(0, 1, 4, 6, 7), using 4x1 MUX using chips in Figure 1.

$F(x,y,z)=m(0,1,4,6,7)$

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

4x1 Multiplexer

I0
I1
I2
I3

Output

S1   S0

5v+

V_{cc}

E

A   A`    B    B`   GND

14 13 12 11 10 9 8

1 2 3 4 5 6 7

i1=0

5v+

V_{cc}

GND

14 13 12 11 10 9 8

1 2 3 4 5 6 7

i0=1

5v+

i3=1

V_{cc}

GND

14 13 12 11 10 9 8

1 2 3 4 5 6 7

i2=c`

F

5v+

V_{cc}

GND

14 13 12 11 10 9 8

1 2 3 4 5 6 7