Faculty of Engineering and Technology
Electrical and Computer Engineering Department

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION LABORATORY
ENCS2110

Experiment No.5 –
Sequential Logic Circuits

Prepared by:
Rasha Mansour 1210773.

Partners:
Fatima Azazmah 1200400
Mariam Awwad 1213069

Instructor: Dr.Khader Mohammad
Teaching assistant: Haleema Hmedan

Section:7
Date: 20/12/2023

Abstract

The aim of this experiment, to review our knowledge of Sequential Circuits such as, Latches, Flip-Flops, Registers and Counters. we will also recognize about their operations, types of each one, how to implement each one using the basic gates and the flip-flops. To be able to know the difference between combinational and sequential circuits. At the end of experiment my theoretical background will be proved practically so; I will be able to construct a counter using JK flip-flops.

Table of Contents:

Table of Figures

List of Tables

1. Theory

1.1 Equipment Required

- IT-3000 Basic Electricity Circuit Lab.
- IT-3007 J-K Flip-Flop Circuits.
- IT-3008 Flip-Flop Circuits.

1.2 Theory

1.2.1 Sequential Circuits

The sequential circuit is a special type of circuit that has a series of inputs and outputs. The outputs of the sequential circuits depend on both the combination of present inputs and previous outputs. The previous output is treated as the present state. So, the sequential circuit contains the combinational circuit and its memory storage elements. A sequential circuit doesn't need to always contain a combinational circuit. So, the sequential circuit can contain only the memory element.[1]

1.2.2 Latches:

“The latch is a basic memory element that storing one bit of information. The latch circuit consists of two inverters; with the output of one connected to the input of the other.it has two outputs, one for the stored value (Q) and one for its complement (Q'). The problem with the latch formed by NOT gates is that we can't change the stored value. For example, if the output of inverter B has logic 1, then it will be latched forever; and there is no way to change this value”.[1]

1.2.2.1 The SR (SET-RESET) Latch:

a) SR latch with NAND gates:

The figure below shows how the SR latch with NAND work.

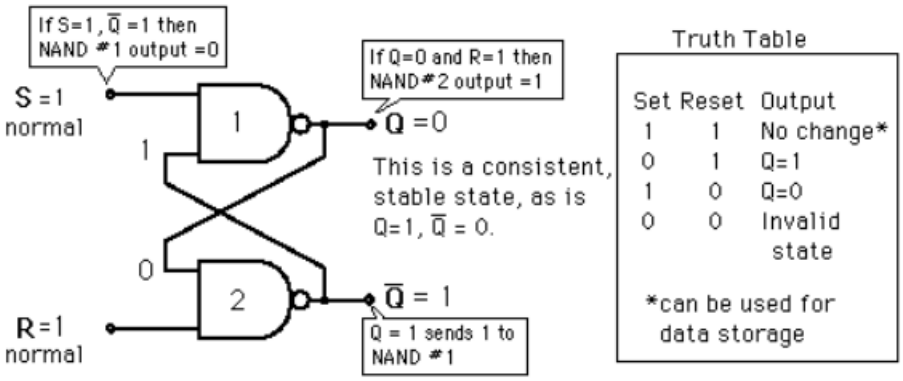


Figure 1:SR latch with NAND gate and truth table.

b) SR latch with NOR gates:

The figure below explains how the SR latch with NOR gate work.

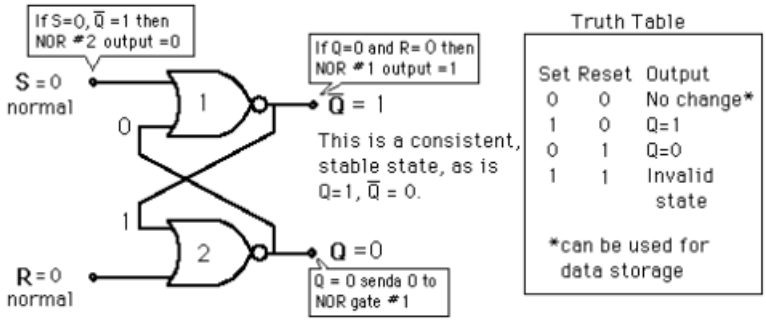


Figure 2:SR latch with NOR gate and the truth table.

c) SR latch with control input:

The figure below shows how the SR latch with control work.

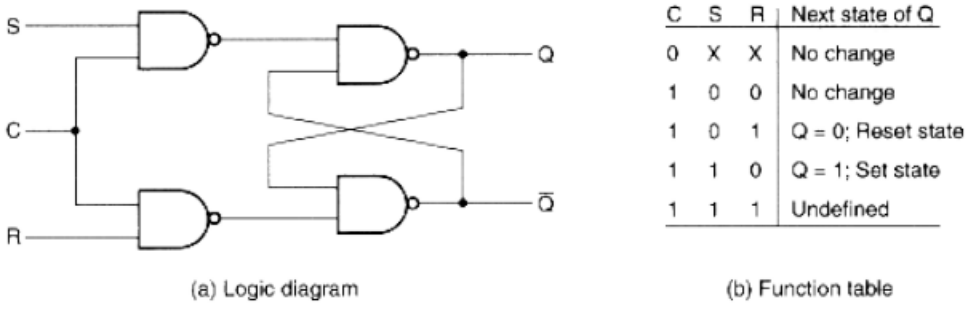


Figure 3: RS latch with control input and the truth table.

1.2.2.2 The D latch.

The figure below shows how the D latch with control work:

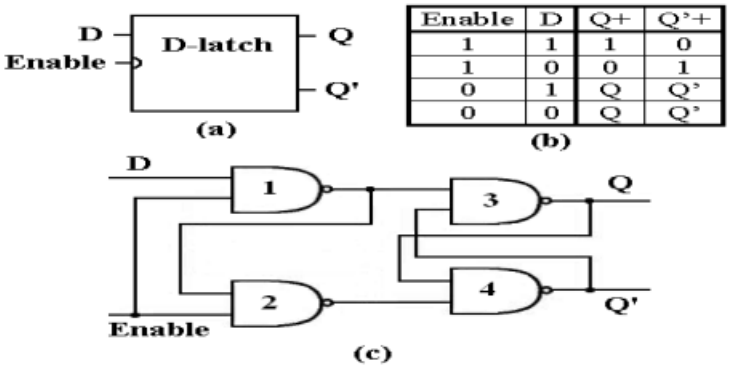


Figure 4:: D latch and the truth table.

1.2.3 Flip-Flops:

The flip flops in sequential circuits are the memory elements. Mainly used in clocked sequential circuits. They store one bit information. It is a circuit with two outputs, one is the normal value and other its complement value. We can know them by few more names as latches. Ther are many types of flip flops the common ones are D, T, JK flip flops.[2]

The figure below shows the types of Flip-Flops:

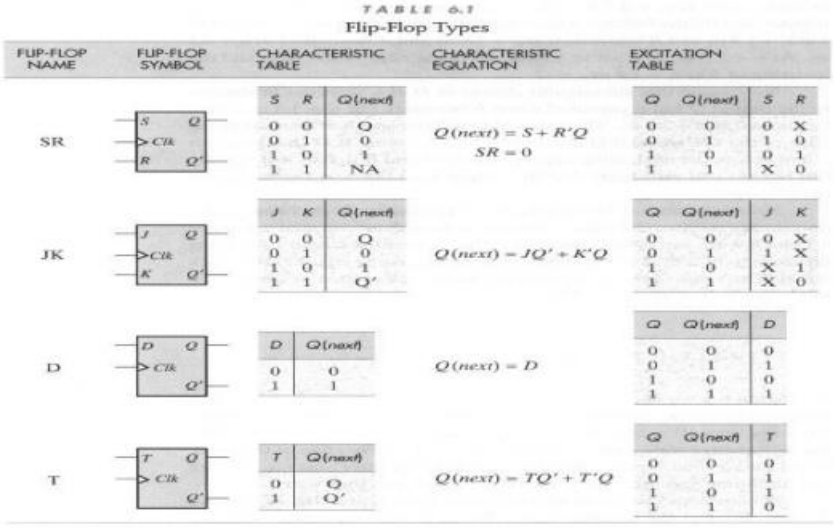


Figure 5: types of Flip- Flops .

1.2.4 Registers:

A Register is a fast memory used to accept, store, and transfer data and instructions. A Register can also be considered as a group of flip-flops with each flip-flop capable of storing one bit of information. A register with n flip-flops is capable of storing binary information of n-bits. There are many types of registers, the common ones are shift right and shift left registers.

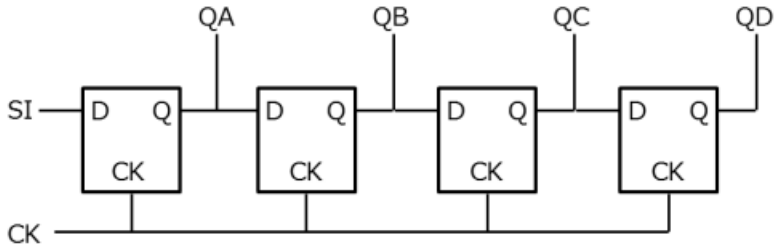


Figure 6: 4-bits shift right registers

1.2.5 Counters:

A special type of sequential circuit used to count the pulse is known as a counter, or a collection of flip flops where the clock signal is applied is known as counters. The counter is one of the widest applications of the flip flop. Based on the clock pulse, the output of the counter contains a predefined state. The number of the pulse can be counted using the output of the counter. The counters are classified into two categories: Ripple and Synchronous. In ripple counters there is no common clock. In Synchronous counters, all flip flop receives a common clock. [1]

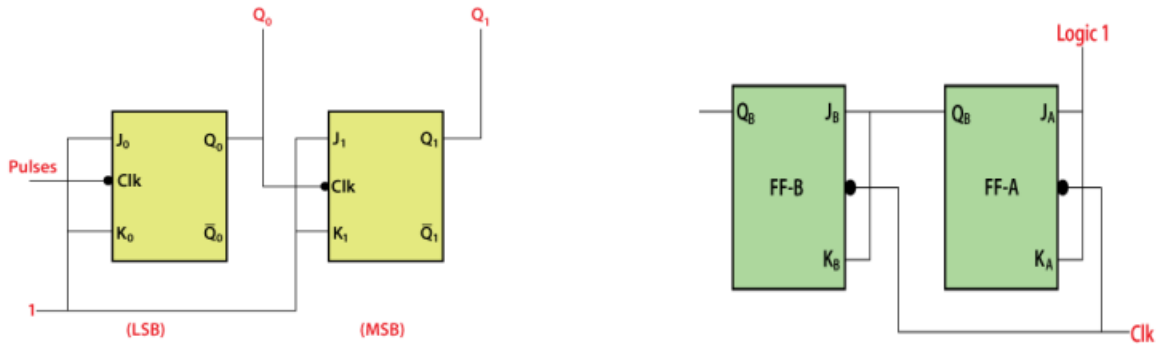


Figure 7: (a) 2-bits ripple counter.(b) 2-bit Synchronous counter.

1.3 Procedure

1.3.1 Latches and Flip flops:

a) Constructing RS latch with basic logic gates:

Use IT-3008 module to construct the circuit. Connect +5V of module IT-3008 to the +5V output of fixed power supply and GND of module IT-3008 to GND output of fixed power supply 2. Connect inputs A3, A4 to Switches SW1, SW2. 4. Connect outputs F6 and F7 to Logic Indicators L1, L2.

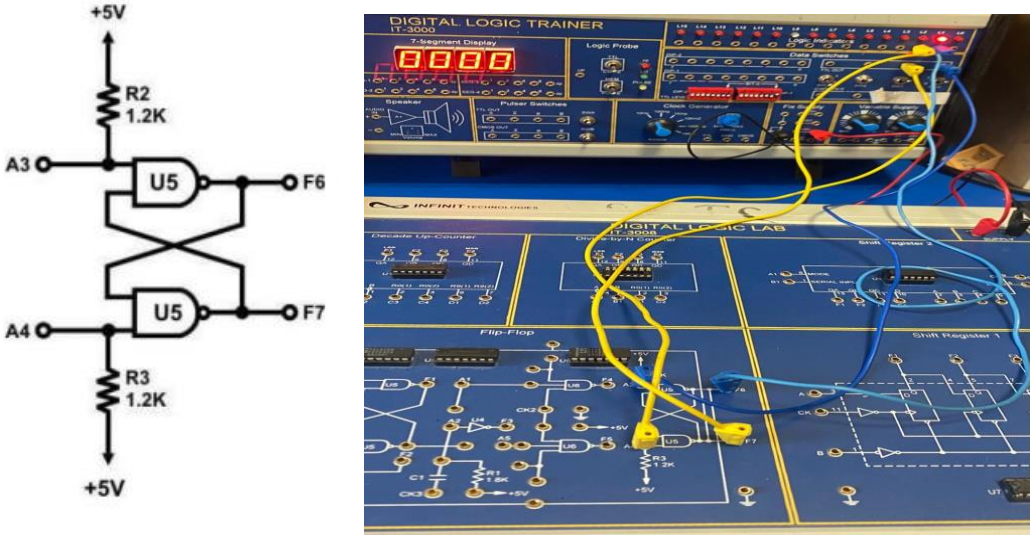


Figure 8:RS latch with gates

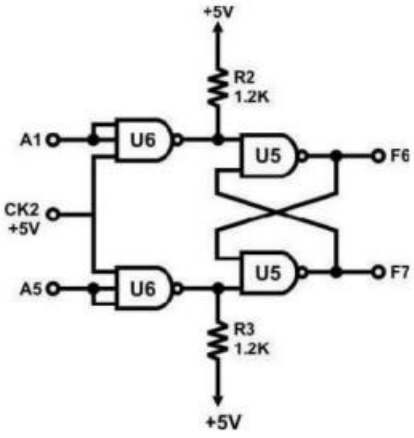
A3	A4	F6	F7
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	1

Table 1: Truth table for RS latch.

When both A3 and A4 are equal to zero, then Q and Q' will be 1(undefined since it is impossible that Q and its complement have the same value). When A3=0 and A4=1 (SET) then Q will be one with a complement of zero. Then if A3=1 and A4=0 (RESET) Q will be zero with a complement of one. Now when both A3 and A4 are 1 then we have NO CHANGE, that means Q and its complement will be the same as the previous state (if its 0 it will be Q=0, Q'=1, but if its 1 it will be Q=1, Q'=0).

b) Constructing RS latch with control input:

Use IT-3008 module to connect the circuit. Connect inputs A1, A5 to Switches SW1.



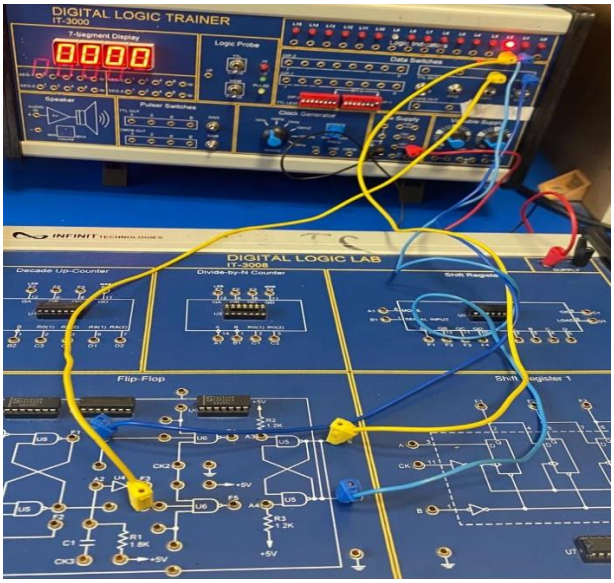


Figure 9:RS latch with control

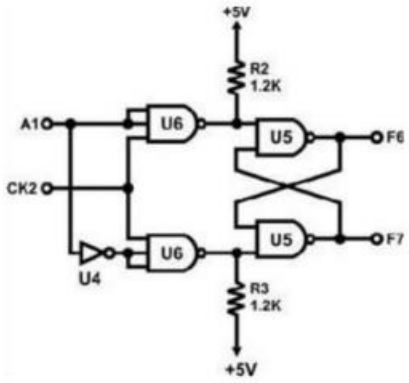
A1	A5	F6	F7
0	0	0	1
0	1	0	1
1	0	1	0
1	1	1	1

Table 2: The truth table for RS latch with control input.

If A1=0 and A2=1 then the output (RESET), when A1=1 and A2=0 the output (SET), when both A1 and A5 are equal to 1 it will be undefined since both Q and its complement are equal to 1 which is impossible, Now when both A3 and A4 are 0 then we have NO CHANGE, that means Q and its complement will be the same as the previous state (if its 0 it will be Q=0, Q'=1, but if its 1 it will be Q=1, Q'=0).

C) Constructing D latch with RS latch:

Use IT-3008 module to construct the circuit. Connect A1 to SW1; CK2 to SWA A and F6 to L1.



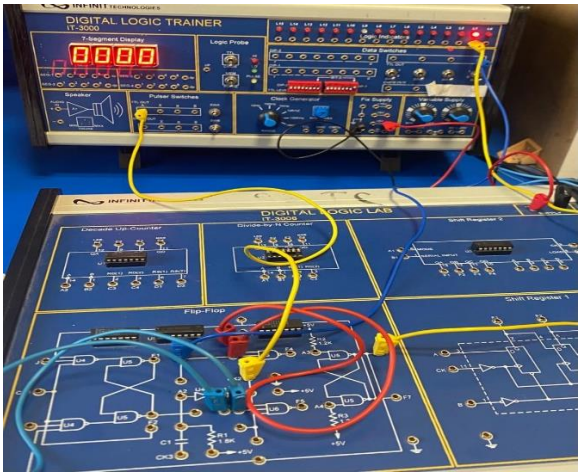


Figure 10: D latch

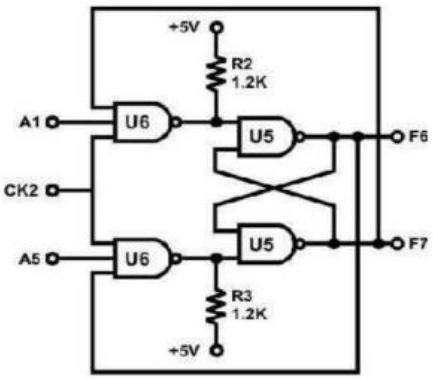
CK2	A1	F6
0	0	0
0	1	0
∏	0	0
∏	1	1

Table 3: Truth table for D latch .

if the clock signal is zero, then the value of D (A1) is X (don't care) then the output will be zero, then if we set the clock to ⎍ (the positive edge of the clock) then if D equal to 1 the output will be 1, if D=0 then the output will be 0" the output(Q+1) = D".

D) Constructing JK latch with RS latch:

Use IT-3008 module to construct the circuit. Connect CK2 to SWB B output; A1 to SW0; A5 to SW1; F6 to L1.



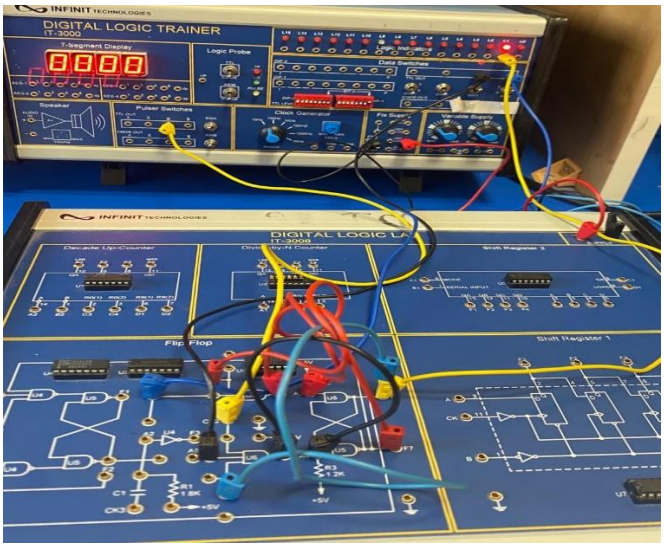


Figure 11: JK latch

CK2	A1	A5	F6	STATUS
∏	1	0	1	
∏	0	0	1	memory
∏	1	1	0	
∏	1	0	1	
∏	0	0	1	memory
∏	0	1	0	
∏	1	1	1	

Table 4Table 5.4 : truth table for JK latch

If both inputs A1 and A5 are set to 0 that means J and K set to 0, the JK flip flop will work as a memory(NO CHANGE), when A1 and A5 are set to 1(J and K set to 1), then the next state will be the complement of the last value on the memory(Q+1 = Q', if Q = 0 it will be 1, and if it is 1 it will be 0), if J = 1 and K = 0, (SET) then the output F6 = 1, if J = 0 and K = 1, (RESET) then the output F6 =0.

E) Constructing JK Flip-flop with master- slave RS latches:

Use IT-3008 module to construct the circuit shown in Figure. Connect CK1 to SWA A output; J to SW1; K to SW0; F1, F2, F6, F7 to L3, L2, L1 and L0, respectively.

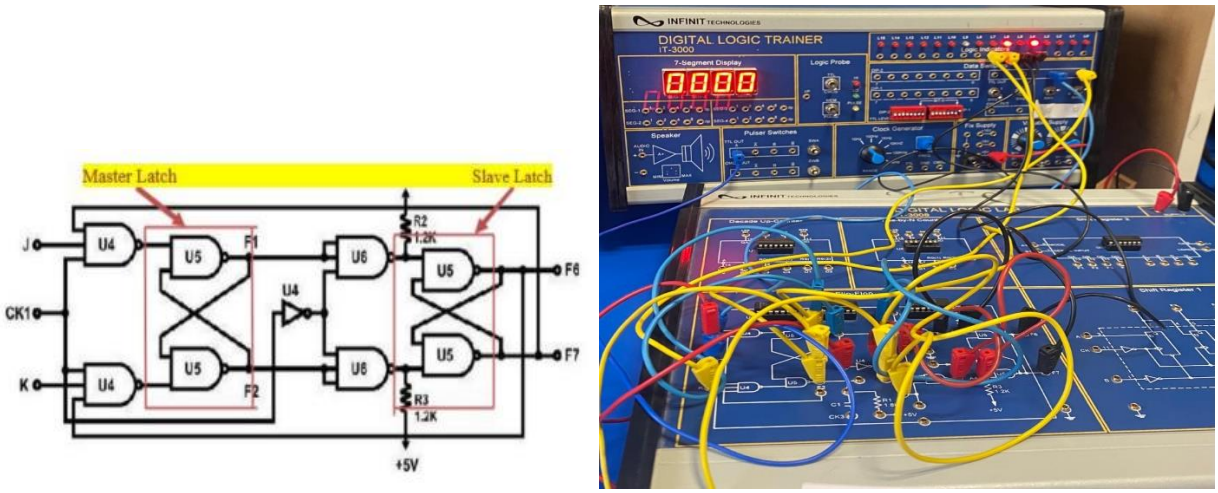


Figure 12:JK flip –flops.

CK2	K	J	F1	F2	F6	F7
∏	0	0	0	1	0	1
∏	0	1	1	0	1	0
∏	1	0	0	1	0	1
∏	1	1	1	0	1	0
∏	1	1	0	1	0	1

Table 5Table 5.5: truth table for JK flip flop with master .

If both inputs J and K set to 0, the JK flip flop will work as a memory(NO CHANGE), when J and K set to 1, then the next state will be the complement of the last value on the memory(Q+1 = Q', if Q = 0 it will be 1, and if it is 1 it will be 0), if J = 1 and K = 0, (SET) then the output F6 = 1, if J = 0 and K = 1, (RESET) then the output F6 =0.

1.3.2 Registers:

a) Constructing Shift Register with D Flip-Flops:

Block Shift Register 1 of module IT-3008 will be used to construct the circuit. Connect B (clear) to SW0; A (I/P) to SW1; CK to SWA A output; F1, F2, F3, F4 to L1, L2, L3, L4 respectively. 3. Set SW0 to "0" to clear B and then set SW0 to "1".

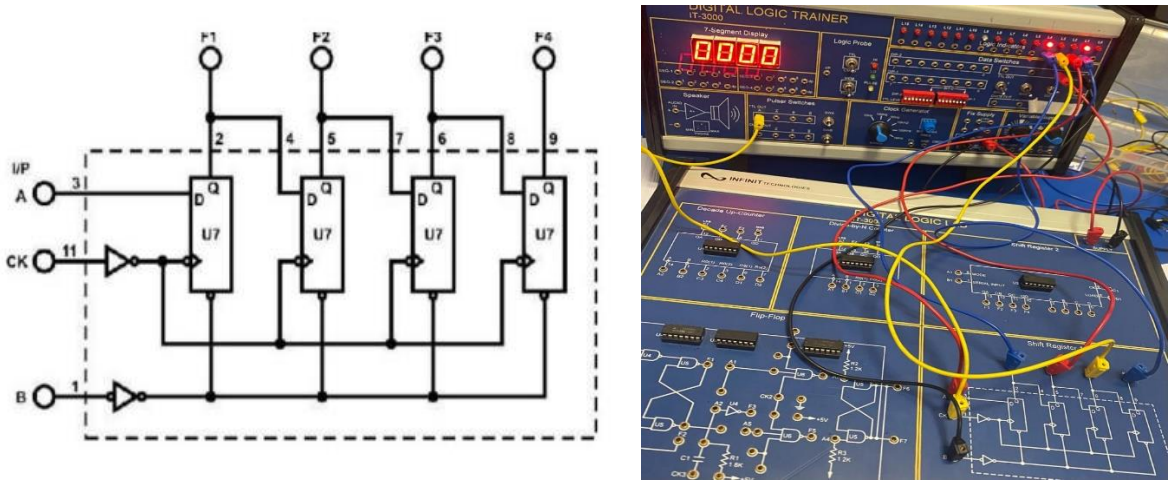


Figure 13: shift D register

When clear (B) set to 0.

A	CK	F1	F2	F3	F4
1	∏	0	0	0	0
0	∏	0	0	0	0
0	∏	0	0	0	0
1	∏	0	0	0	0

(a)

When clear (B) Set to 1.

A	CK	F1	F2	F3	F4
1	∏	1	0	0	0
0	∏	0	1	0	0
0	∏	0	0	1	0
1	∏	1	0	0	0

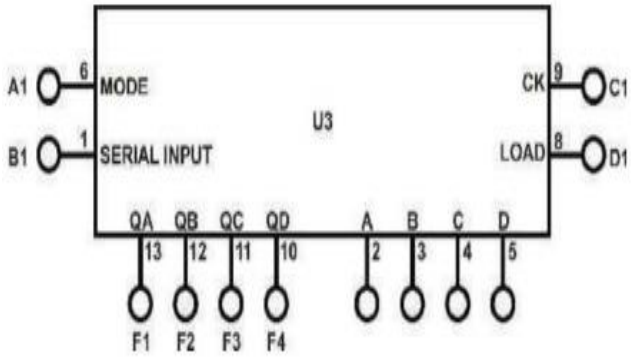
(b)

Table 6Table 5.6: (a) and (b) truth table for shift right register .

This register shifts the digit 1 in the input 1-bit to the right.

b) 4-Bit Shift Register with serial and parallel load:

Use Shift Register 2 module in IT-3008 which is 4-Bit Shift Register with serial and parallel synchronous operating modes. Connect Inputs A, B, C, D to SW0, SW1, SW2, SW3 Outputs F1, F2, F3, F4 to L0, L1, L2, L3, respectively. B1 (I/P) to DIP2.0. A1 (MODE) to DIP2.1. Connect CK (C1) to the clock generator TTL level output at 1Hz and change data at B1 with DIP2.0.



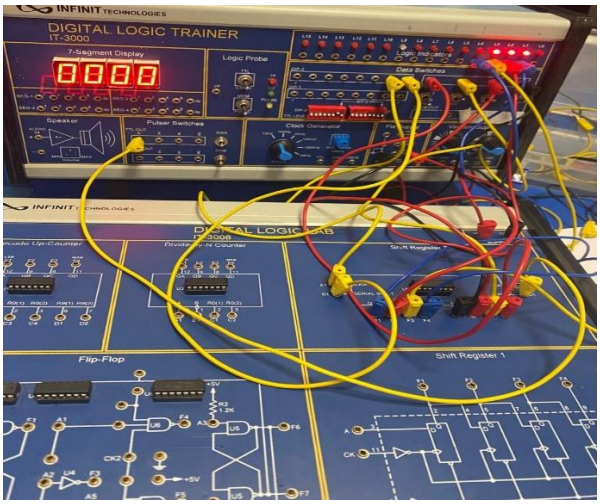


Figure 14: shift register with serial and load

A1	C1	L3	L2	L1	L0
0	∏	1	1	1	1
0	∏	1	1	1	0
0	∏	1	1	0	0
1	∏	1	0	0	0

(a)

D1	D	C	B	A	L3	L2	L1	L0
∏	0	0	1	0	0	0	1	0
∏	1	0	1	0	1	0	1	0
∏	1	1	1	0	1	1	1	0
∏	0	1	1	1	0	1	1	1
∏	0	1	1	0	0	1	1	0

(b)

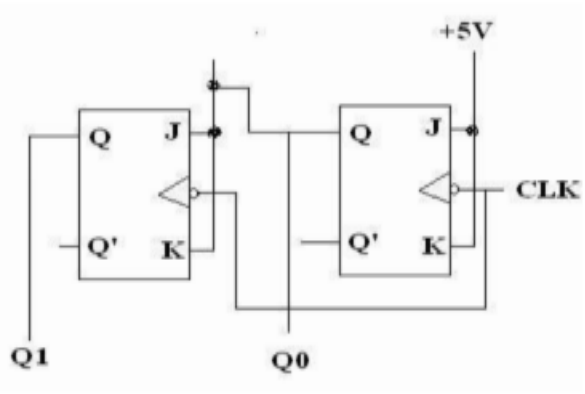
Table 7: (a) and (b) truth table for shirt register with serial and load

a) When A = 0, that's mean it is will work with shifting, so in first and third cases it is become like that as: 1000, 1100, 1110, 1111, but in the second case it is become like that as: 0111, 0011, 0001, 0000. Now when A = 1, that's mean it will work without shifting.
b) This circuits lode the data by let the output equaled to the input and after that store it in the register.

1.3.3 Counters:

a) 2-bit Synchronous Counter:

Use IT-3007 module to implement the 2-bit synchronous counter. Connect +5V of module IT-3007 to the +5V output of fixed power supply and GND of module IT-3007to GND output of fixed power supply. Connect CLK input to pulser switch SWA. Connect counter outputs Q1 and Q0 to indication lamps L1, L2, respectively. Apply clock pulses to CLK input.



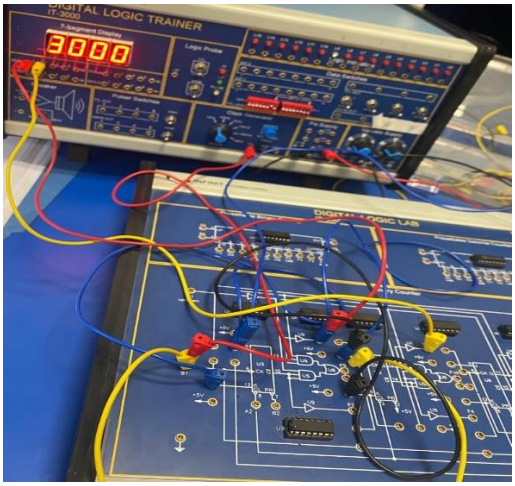


Figure 15: Synchronous counter

CLK	Q1	Q0	D
∏	1	0	2
∏	1	1	3
∏	0	0	0
∏	0	1	1
∏	1	0	2
∏	1	1	3
∏	0	0	0
∏	0	1	1

Table 8Table 5.8: truth table for synchronous counter.

In this circuit we connect J and K together with +5v so we make a T flip flop. This counter starts from 00 to 11 (0 to 3) two-bit counter, for each clock the counter will increment.

b) 3-bit (divide-by-eight) Ripple Counter:

Use the IT-3007 module to implement the 3-bit (divide by eight) Ripple counter. Connect CLK input to pulser switch. Connect counter outputs Q2, Q1 and Q0 to indication lamps. Apply clock pulses to CLK input.

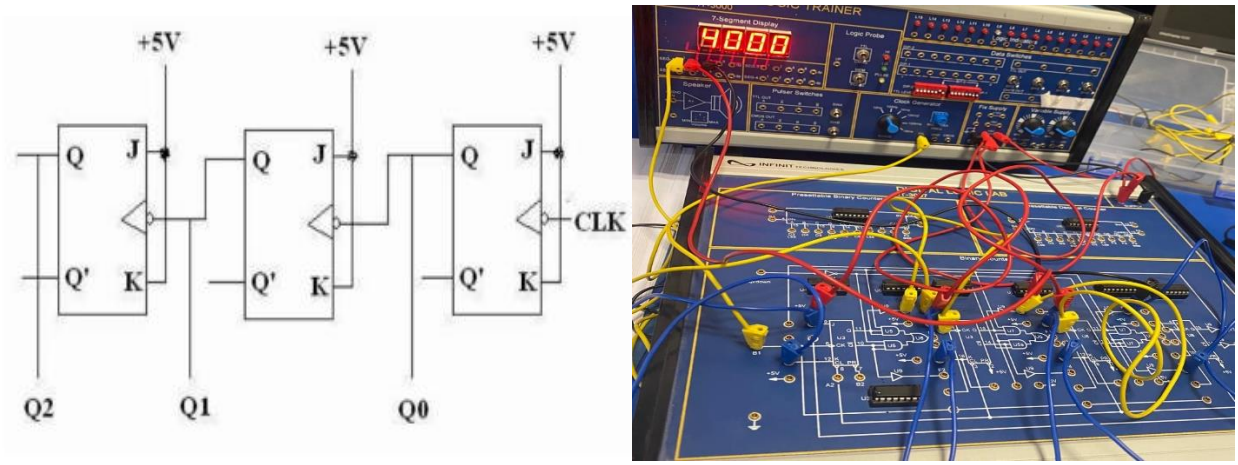


Figure 16:rippel counter

CLK	Q2	Q1	Q0	D
∏	0	0	0	0
∏	0	0	1	1
∏	0	1	0	2
∏	0	1	1	3
∏	1	0	0	4
∏	1	0	1	5
∏	1	1	0	6
∏	1	1	1	7
∏	0	0	0	0
∏	0	0	1	1

Table 9Table 5.9: truth table for ripple counter.

apply counter outputs Q2, Q1 and Q0 to seven segment display D.

The 3-bit ripple counter used in the; circuit above has eight different states, each one of which represents a count value. The sequence of counting usually gets repeated after a limit. When counting up, for the n-bit counter the count sequence goes from 000, 001, 010, … 110, 111, 000, 001, … etc. When counting down the count sequence goes in the opposite manner: 111, 110, … 010, 001, 000, 111, 110, … etc.

c) BCD Counter:

Connect +5V of module IT-3008 to the +5V output of fixed power supply and GND of module IT-3008 to GND output of fixed power supply. Connect C3, C4 to SW0 and SW1; D1, D2 to SW2 and SW3; F1~F4 to L1~L4, A2 to SWA A output. Connect F1 to B2, set C3, C4, D1 and D2 to ground and A2 to SWA A pulse. Measure and record the outputs F1, F2, F3, F4. 4. Set SW2 and SW3 to 0.

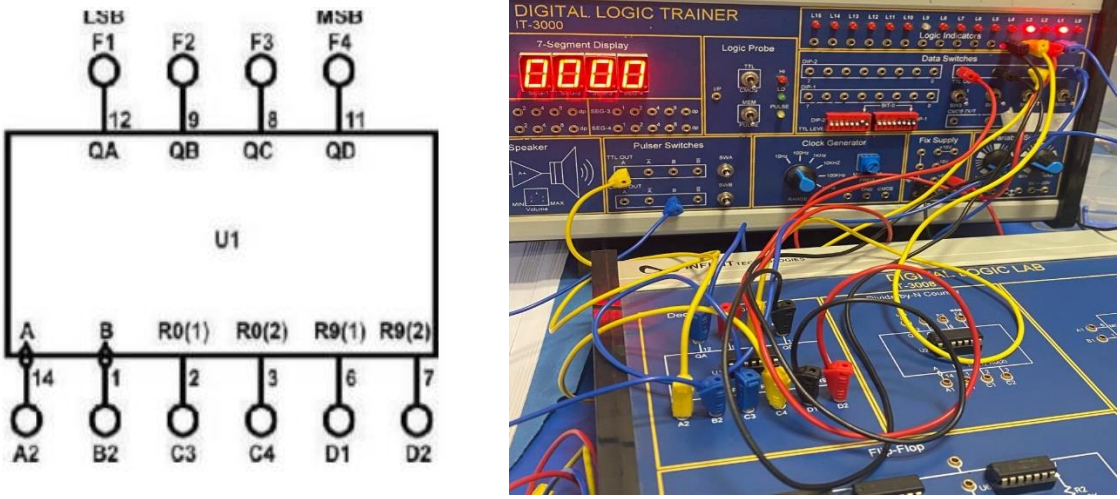


Figure 17: (a) and (b) BCD counter

Input	Output			
A	F4	F3	F2	F1
⎍	0	0	0	0
⎍	0	0	0	1
⎍	0	0	1	0
⎍	0	0	1	1
⎍	0	1	0	0
⎍	0	1	0	1
⎍	0	1	1	0
⎍	0	1	1	1
⎍	1	0	0	0
⎍	1	0	0	1

Table 10: truth table for BCD counter.

A BCD counter is one of the 4-bit binary counters. When the count reaches the last value, it resets all the flip-flops and starts to count again from 0.

d) Divide-by-8 counter using BCD chip counter:

on the same circuit just modify some changes: change R0(2) to 5V+ R0(1) to QD output and this will make the counter reset 111. Connect clock A2 to pulser switch. Connect the output A,B,C and D to lamp. Apply clock pulses to A2 and observe the count sequence.

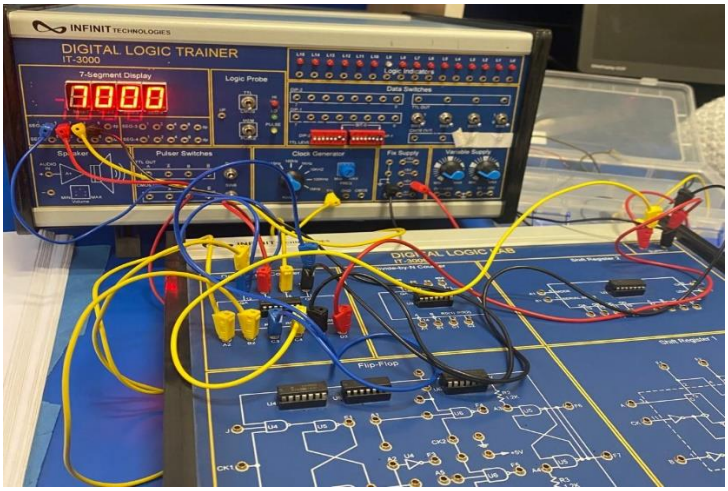


Figure18: Divide-by-8 counter using BCD chip counter.

In the Divide-by-8 counter using a BCD chip counter, the BCD counter is likely configured to count in binary-coded decimal (BCD) up to the number 7 (which is represented as '0111' in binary). When the count reaches 7, the next clock pulse will reset the counter to 0, completing the divide-by-8 operation.

2. Discussion:

1.Although latches are useful for storing binary information, they are rarely used in sequential circuit design, why? [3]

It's right that the latches are faster than the flip-flops since the flip-flops consist of several latches, and they consume less power but the latches tend to make glitches which are not appreciated in the designing, also the latches are level triggered as mentioned before while the flip-flops are edge-triggered, so the change in the flip-flop will happen only at the triggering edge.

2. What is the disadvantage of the RS flip flops?

The major disadvantage is when both inputs are 1 (S=R=1) in this case the output and its complement will be 1 which is not allowed.

3. What is the difference between “synchronous” and “ripple” counters?

At the ripple-counters, each flip-flop is triggered with its clock, while at the synchronous counter all flipflops are triggered with the same clock so the synchronous counter should be faster than the ripple counter.

3. Conclusion

In conclusion, this experiments we see the deference's between combinational and sequential logic circuits. Then we learn about sequential logic circuits who has memory units to store data, how this circuits work and their operating principles, starting with latches such as SR latch and D latch then flip flops as D flip flop and JK flip flop then we see who to use them to implement registers and counters.

4. References

- [1] Manual for Digital Electronics and Computer Organization Lab, 2023, Birzeit University.

https://ritaj.birzeit.edu/bzu-msgs/attach/2375682/Digital+lab+manual+2023.pdf