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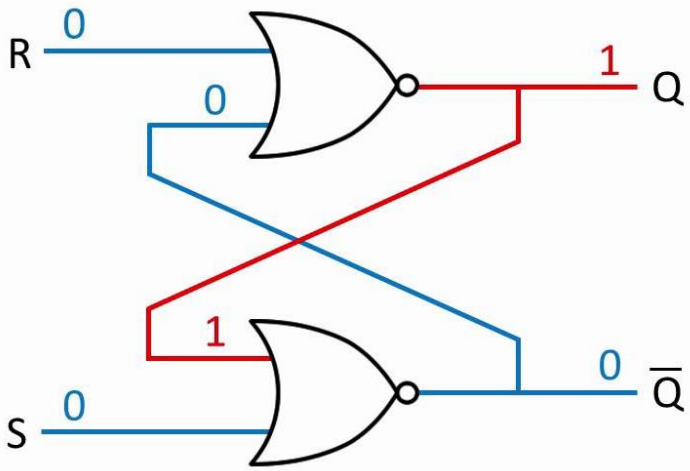
5.3 Pre Lab

1)Design the Logic Diagram, function table of the SR latch using NOR gates, and explain how it works.

S	R	Q	$\overline{Q}$
0	0	1 0	0 1
0	1	0	1
1	0	1	0
1	1	0	0



How It works: SR latches (set/rest) is an asynchronous circuit, the SR latch is a key circuit in digital storage units, when both S and R equals to 0, the output Q remains the same. This is a memory function of the SR latch, it has two inputs, namely set(s) and reset (r) and two output namely Q and Q`. the SR latch operates by storing a bit (either 0 or 1) and then latching onto it until it receives a new input.

-case1: when R=0 and S=0

Suppose initially the value of a Q is 0, then both of the lower Nor gate becomes 0 and the output of the gate become 1 (example Q `= 1 now in the upper gate will be zero and 1 so the output Q=0, it's called memory condition\ hold state.

-case2: when R=1 and S=0

At the upper Nor gate we will receive output as 0 ,(example Q =1 now at the lower nor gate we have both inputs 0 ,Q`=1),it is called rest condition.

-case3: when R=0 and S=1

In this case output at of the second Nor gate will be 0 (example, Q`=0, Q=1), it is called set condition.

-case2: when R=1 and S=1

at both gates, the gate out about Q and Q` =0, which is absurd and doesn't follow the basic. It is called invalid state or forbidden state.