Name: Rasha Mansour

ID:1210773

8.7 Post Lab

1-4-bit-adder

four_bit_adder.v | Compilation Report - Flow Summ... | four_bit_and_array.v

```
module four_bit_adder (
  input [3:0] x,
  input [3:0] y,
  input c_in,
  output c_out,
  output [3:0] sum
);

  wire [3:0] carry;


  assign {carry[3], sum[3:0]} = x + y + c_in;

  assign c_out = carry[3];

endmodule
```

2-4-bit-and-array:

four_bit_adder.v | Compilation Report - Flow Summ... | four_b

```
module four_bit_and_array(
    input [3:0] a,
    input [3:0] b,
    output [3:0] c);

assign c[0] = a[0] & b[0];
assign c[1] = a[1] & b[1];
assign c[2] = a[2] & b[2];
assign c[3] = a[3] & b[3];

endmodule
```

3-4-bit-or array:

four_bit_adder.v | Compilation Report - Flow Summ...

```
module four_bit_or_array(
    input [3:0] a,
    input [3:0] b,
    output [3:0] c
);

assign c[0] = a[0] | b[0];
assign c[1] = a[1] | b[1];
assign c[2] = a[2] | b[2];
assign c[3] = a[3] | b[3];

endmodule
```

4-quad-mux2x1:

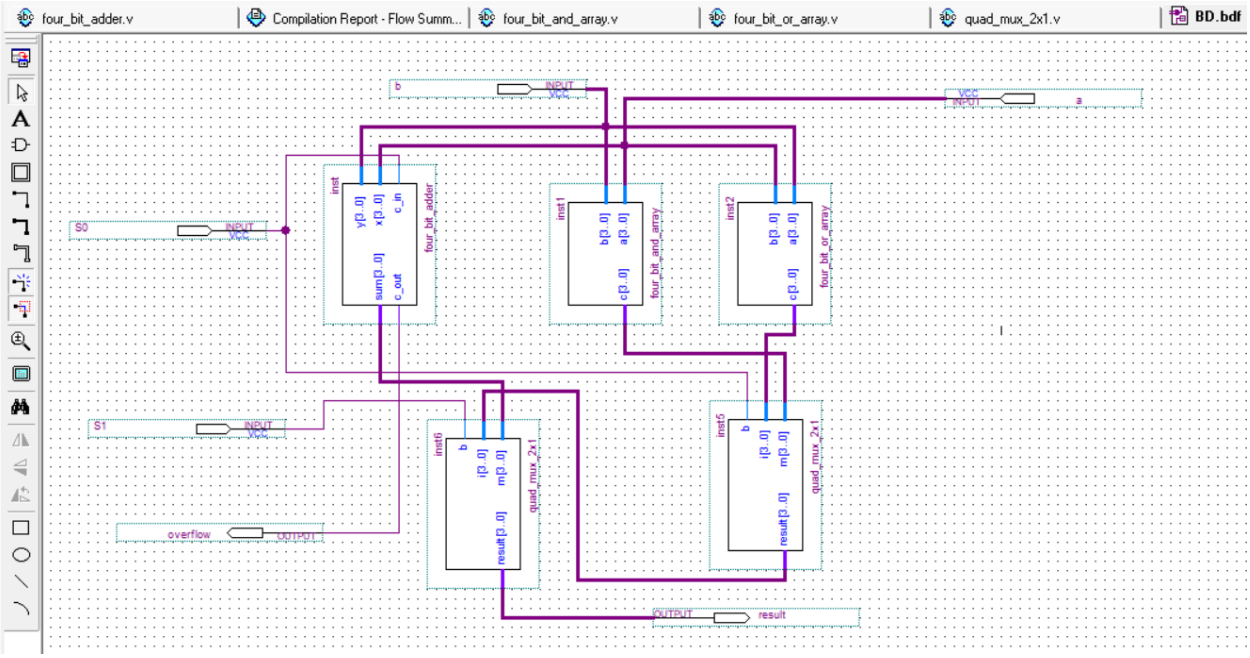
four_bit_adder.v | Compilation Report - Flow Summ... | four_bit_and_array.v | four_bit_or_array.v | quad_mux_2x

```
module quad_mux_2x1 (
    input [3:0] m,
    input [3:0] i,
    input b,
    output [3:0] result
);

assign result = (b & m[0] & i[0]) | (b & m[1] & i[1]) | (~b & m[2] & i[2]) | (~b & m[3] & i[3]);

endmodule
```

The circuit:


four_bit_adder.v
Compilation Report - Flow Summ...
four_bit_and_array.v
four_bit_or_array.v
quad_mux_2x1.v
BD.bdf
b
INPUT
VCC
VCC
INPUT
a
S0
INPUT
VCC
inst
y[3..0]
x[3..0]
c_in
sum[3..0]
c_out
four_bit_adder
inst1
b[3..0]
a[3..0]
c[3..0]
four_bit_and_array
inst2
b[3..0]
a[3..0]
c[3..0]
four_bit_or_array
S1
INPUT
VCC
inst6
b
i[3..0]
m[3..0]
result[3..0]
quad_mux_2x1
inst5
b
i[3..0]
m[3..0]
result[3..0]
quad_mux_2x1
overflow
OUTPUT
OUTPUT
result