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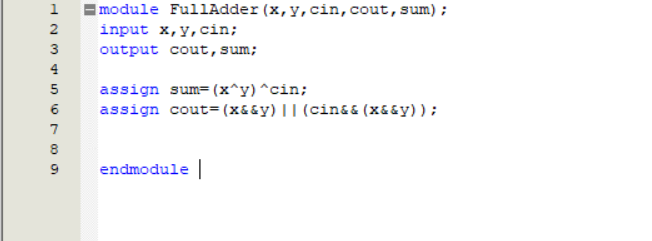
**8.6 Task in lab**

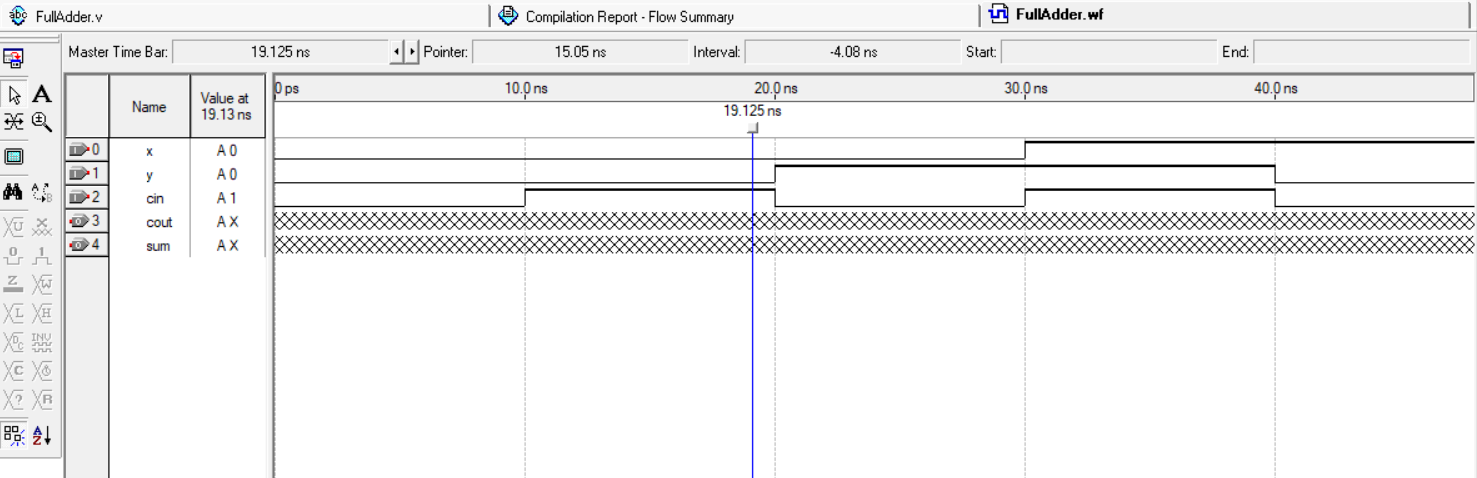
1. Create schematic symbols as shown in the figure, Use: Y3Y2Y1Y0 = 0111. What does this circuit do?

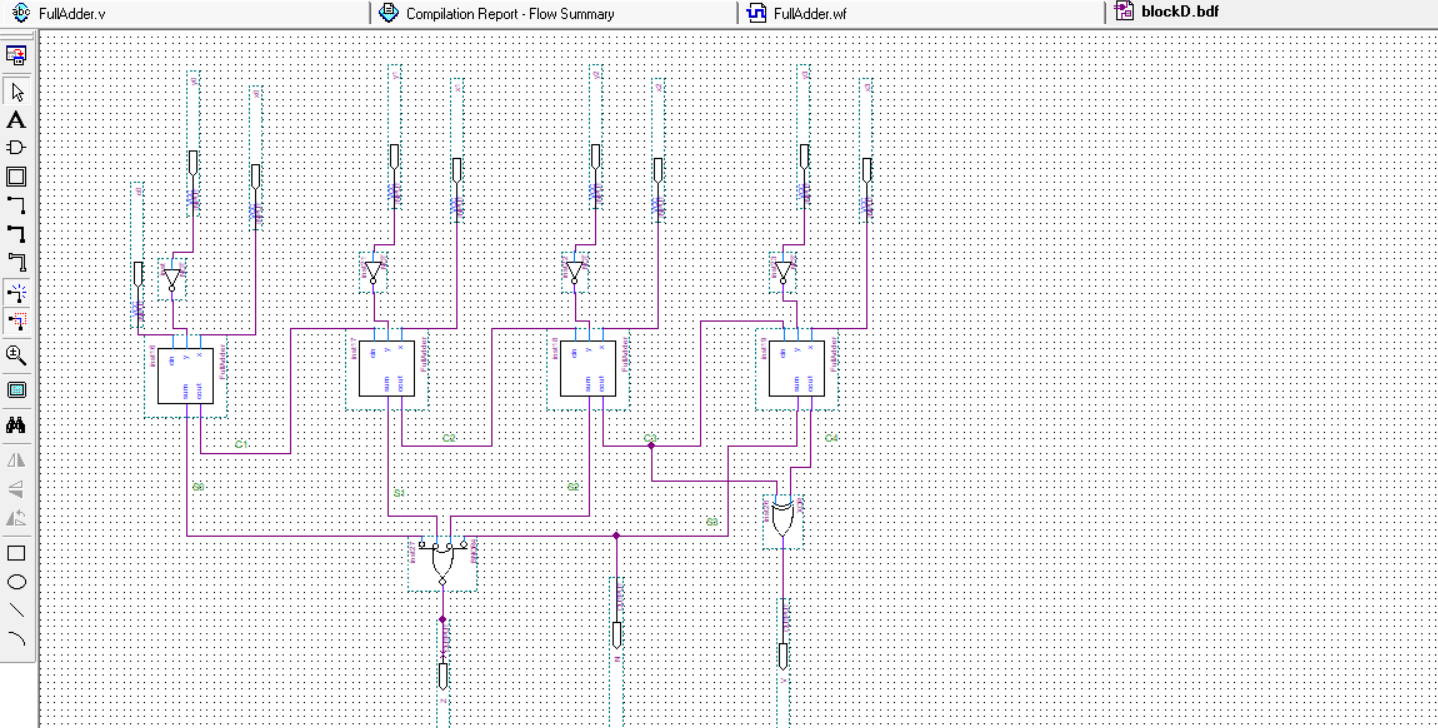
Use Verilog to implement the circuit and run a meaningful simulation for this circuit.

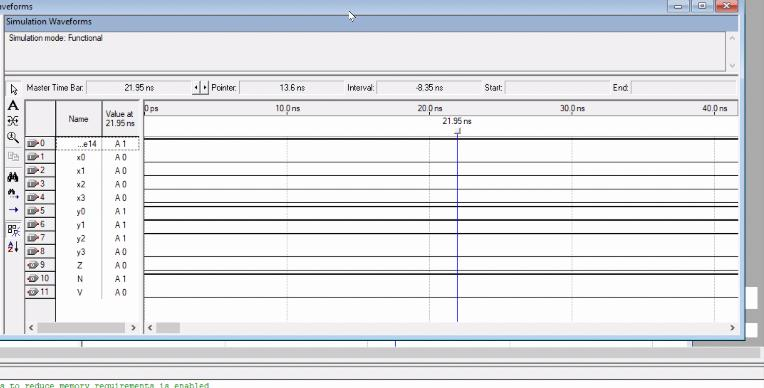
x+2s Complement y

x-y





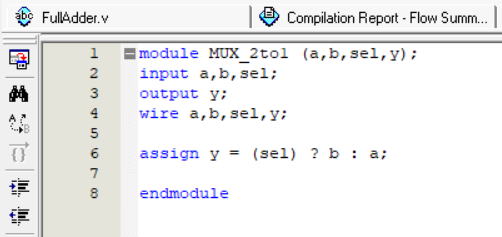


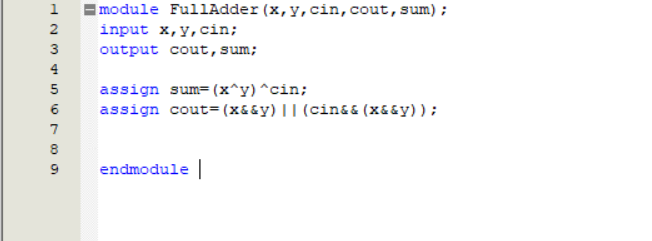


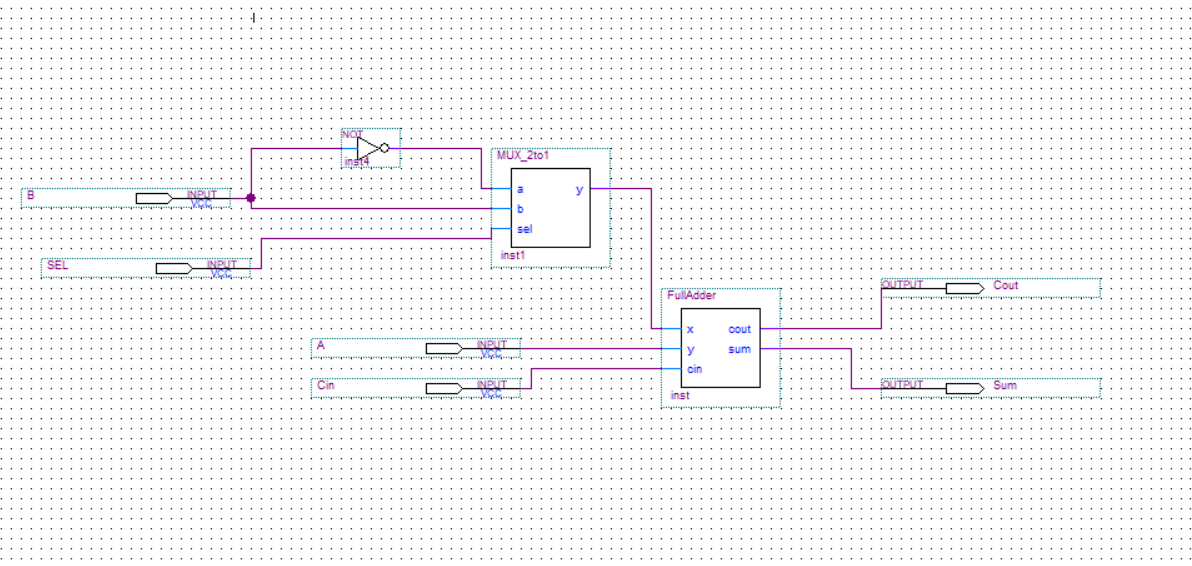
2. Use Verilog HDL to implement a 2-to-1 MUX. Use Verilog HDL to implement a Full Adder. Create

schematic symbols for both the MUX and the Full adder, then connect them as shown in the figure. Run

a meaningful simulation for this circuit.







3. Use Verilog HDL to implement a 2-bit counter with direct reset input (RESET). Use Verilog HDL to

implement a 2-to-4 Decoder. Create schematic symbols for both the counter and the decoder, then

connect them as shown in figure below. Run a meaningful simulation for this circuit

