Aditya T

LinkedIn : Aditya T
Github : 1sand0s (For hardware design files)
YouTube : Audi tt (For software demonstration)

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Education

- **University of Texas at Austin** — Austin, TX
  PhD in Electrical and Computer Engineering; GPA: 3.87/4.0 — *Dec. 2021 – Present*
  Track : Software Engineering and Systems
  Research Area : JIT Compiler Optimization, Regression Test Selection
- **University of Texas at Austin** — Austin, TX
  Master of Science in Electrical and Computer Engineering; GPA: 3.87/4.0 — *Aug. 2019 – Dec. 2021*
  Track : Electromagnetics and Acoustics
  Research Area : EM Side-Channel Vulnerability Modeling
- **PES Institute of Technology** — Bangalore, India
  Bachelor of Engineering in Electronics and Communication Engineering; GPA: 9.52/10.00 — *Aug. 2013 – July. 2017*
  Thesis : Through Wall Imaging Using Micro-Doppler Features

Work Experience

- **University of Texas at Austin** — Austin, TX
  Graduate Research Assistant — *Aug 2019 - Dec 2021*
  Programming Languages - C, C++, MATLAB, Python, Powershell, Bash
  Tags - Keil, ucSim, PyTMCL, PyVISA, HFSS, LTspice, COMSOL, KiCad, RReliefF, ANOVA

  1. Developed a cycle level electromagnetic(EM) field simulator for the C-51 ISA of AT89S51 using *ucSim* which **predicts firmware vulnerability to EM side channel attacks at compile time** with up to 88% accuracy based on the Dalton Benchmark programs
  2. Developed a cycle level instruction disassembler for the AT89S51 which is capable of **reverse engineering firmware using the radiated EM fields** with up to 98% accuracy
  3. Designed and fabricated an 8051 (AT89S51) board for characterizing EM field radiations
  4. Automated end-to-end measurement flow (Oscilloscope to Desktop) using NI VISA, PyTMCL, MATLAB and Powershell
  5. Served as the Corporate Relations Officer for GREECE (UT Graduate ECE Student Organization)

- **SimYog** — Bangalore, India
  R&D Engineer — *Feb 2018 - June 2019*
  Programming Languages - C++, Python, Powershell, MATLAB
  Tags - FreeCAD, Dassault Spatial, ODB++, QT, Unreal Engine, LTspice, KiCad, Altium

  1. Headed the formulation and development of Harmonic and Sample Balance based methods to accurately predict EMI/EMC compliance of automotive circuitry using 3D Field Solvers (Method of Moments)
  2. Headed and developed the Integrated Circuit Immunity Model (ICIM) and Integrated Circuit Emission Model (ICEM) integration into *Compliance Scope* which helps in accurate prediction of an integrated circuits effect on *Bulk Current Injection*(BCI) and *Radiated Emission*(RE) tests.
  3. Headed and Optimized algorithms for **CAD Boolean operations using Dassault's Spatial suite which showed a 10× improvement** in speed relative to competitors
  4. Designed circuit boards for testing Bulk Current Injection (BCI) compliance which was used to validate *Compliance Scope's* simulation result with measurement
  5. Designed the UI for the product using QT
  6. Designed a concept Virtual Reality(VR) UI (*link*) for the product using Unreal Engine and Oculus rift

- **Indian Institute of Science (IISc)** — Bangalore, India
  Undergraduate Research Assistant — *Aug 2016 - Feb 2018*
  Programming Languages - Java, MATLAB
  Tags - LTspice, HFSS, CST MWS, Antenna Magus, KiCad

1. Designed and fabricated a radar board for through wall imaging (TWIR) that detected movement behind a 4cm thick plywood board. Designed and fabricated a Vivaldi antenna for TWIR
2. Worked on a hybrid 2D/3D solver based on artificial neural networks and Quasi TEM assumptions to improve simulation time of a 3D EM field solver

- **Google Summer of Code** Bangalore, India
  Summer Intern *May 2015 - Aug 2015*
  Programming Languages - Java

1. Developed a Java based simulator for modeling Rayleigh-Sommerfeld diffraction
2. The simulator helps in computing phase delays in excitation of individual elements in an ultrasonic transducer array to create specific patterns of constructive and destructive interference
3. These patterns can be used to augment interactive spaces with tactile feedback

Publications (Recent)

- Aditya T, Vishnuvardhan Iyer, Andreas Gerstlauer and Michael Orshansky, *"Prediction of Software Vulnerability to EM-Side Channel Attacks"*, **Under Review**, November 2021
- Meizhi Wang, Shanshan Xie, Ping Na Li, Aseem Sayal, Ge Li, Vishnuvardhan Iyer, Aditya T, Michael Orshansky, Ali E. Yilmaz, and Jaydeep P. Kulkarni, *"Galvanically Isolated, Power and Electromagnetic Side-Channel Attack Resilient Secure AES Core with Integrated Charge Pump based Power Management"*, **IEEE Custom Integrated Circuits Conference (CICC)**, April 2021
- Vishnuvardhan Iyer, Aditya T and Ali Yilmaz, *"Testing the Resilience of Cryptographic Modules Against Fine-Grained Time-and Frequency-Domain EM Side-Channel Analysis Attacks"*, **2021 International Conference on Electromagnetics in Advanced Applications (ICEAA)**, Hawaii, USA, August 2021
- Aditya T, BP Nayak, Anant Devi and Dipanjan Gope, *"MoM-HB Algorithm for prediction of High Voltage Interference in Automotive Active Circuitry "*, **27th IEEE International Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)**, San Jose, California, 2018 (**Top conference for Numerical Electromagnetics**)
- Aditya T, Nikhil S, Dipanjan Gope, V Mahadevan, *"Through Wall Imaging Radar based on Micro-Doppler Features"*, **11th IEEE International Radar Symposium**, Bangalore, India, 2017 (Acceptance Rate : 35%)

Academic Projects/Awards/Open Source Contributions

- **Most Efficient Inverter Design, 2021**: My H-Bridge Inverter placed second in EE462L/EE394-7 with an efficiency of 94.8%. The competition involved choosing appropriate MOSFETs to improve efficiency while minimizing expenses and also the design of the boostrap circuitry to drive the high-side MOSFETs. I modeled the circuit in the **Laplace Domain** and computed its step response in MATLAB to choose the components. I also a built a **Diode Bridge Rectifier, Buck, Boost and SEPIC converters** as a part of this course
- **LC3b Cycle Level Simulator, 2020**: As part of my Computer Architecture course, I built an LC3b Cycle Level Simulator using C. The simulator also includes an assembler designed using **Finite Automata Theory**.
- **Synchronous Serial Port and Wishbone Interface, 2019**: I designed a Synchronous Serial Port in Verilog using the **Xilinx ISE Design Suite**. The project also invovled the design of a **Wishbone Bus** to interface the serial port with an ARM core and the design of a clock management module to manage all the clocks and interrupts. All the modules were optimized for clocking frequency and reduction in area.
- **Java Based stand alone FEM 2D solver**: I developed a stand alone **FEM 2D solver inclusive of the meshing routines** in Java (*link*)
- **GTP Stack for Pcap4J 2016**: I developed and committed the GTP(GPRS Tunneling Protocol) stack to the Java open-source packet library Pcap4J.
- **National Robotics Competition, Wipro 2015**: My project Driverless car using Machine Learning was awarded First place in the two regional rounds and Second place in the national round. I used **OpenCV** to generate 10×10 bitmaps of binary images obtained from a camera mounted on the car. These were fed to a neural network to decide on the direction of the car. The project was based on **Texas Instrument's OMAP** processors.
- **Project Interhaptics to Google's Interactive Spaces 2015**: Project Interhaptics which was developed during the course of Google Summer of Code was committed to Google's Interactive Spaces.
- **Microsoft Hackathon 2014**: My project based on Pranav Mistry's *Sixth Sense* was awarded the **Audience Best Project** award and **Top five best projects** award. I used **OpenCV** and colored markers on my fingers to interactively navigate through applications and perform tasks such as snapping pictures based on certain gestures.
- **Android App for Multinational Company DSC 2014**: I designed an Android App for Quan Zhou Dong Shan Machine CO.,LTD.
- **Academic Honors**: Placed first in the university across all branches of engineering for the academic years 2013-2015.