PROPOSAL FOR OPEN ENDED EXPERIMENT

LINEAR INTEGRATED CIRCUITS LAB

SIXTH SENSE INTERFACED TELEPHONE

ADITYA T **1PI13EC126 'A' section**

TITLE: Sixth sense interfaced telephone**.**

OBJECTIVE: To design and program a sixth sense interfaced telephone

EXPECTED OUTCOME: DTMF tone generated at the output

DETAILS:

Why this project?

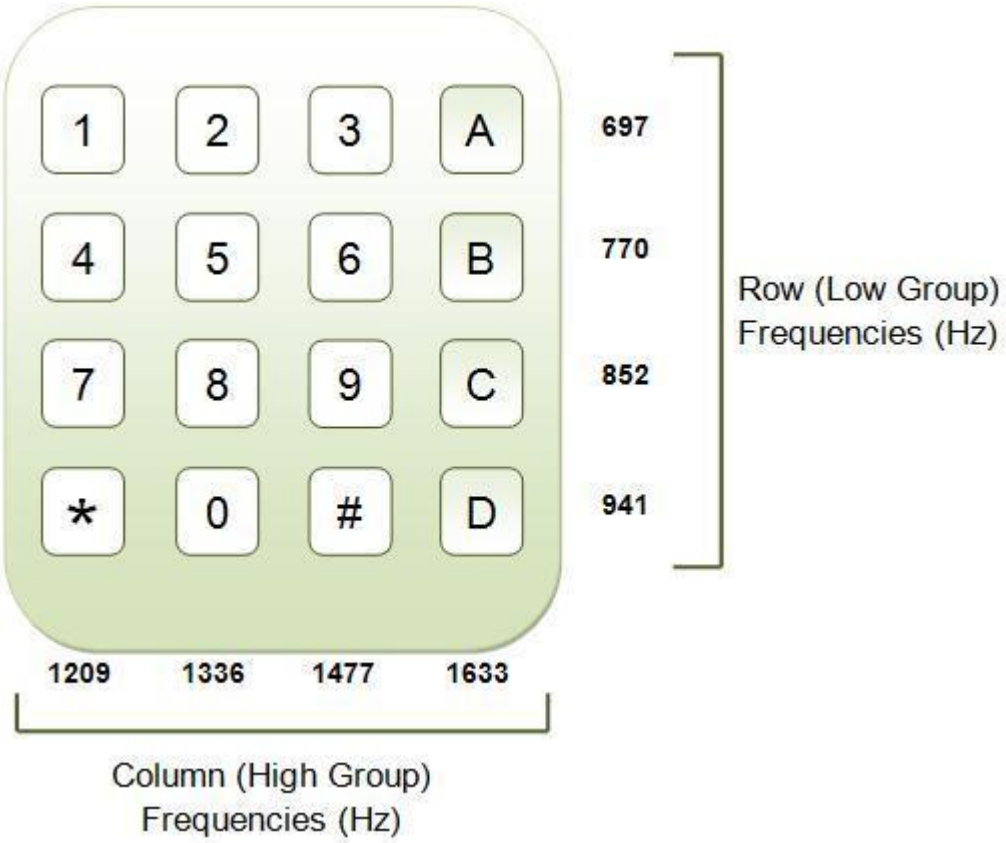
It's the beginning of a new era of technology where engineering will reach new peaks. Just like, in the science fiction movies where display of computer screen appears on walls, commands are given by gestures. Sixth Sense is a wearable gestural interface that enhances the physical world around us with digital information and lets us use natural hand gestures to interact with that information. It is based on the concepts of augmented reality and has well implemented the perceptions of it. Sixth sense technology has integrated the real world objects with the digital world. To get along with the new technology, there is a need for something new in the field of telephones. So this concept of using 6^{th} sense for giving input for the system would be an additional feature to the much developed field of telephones. So ultimately the prospect of interacting directly with the device thereby augmenting our experience with the digital world furthered our purpose to develop this device.

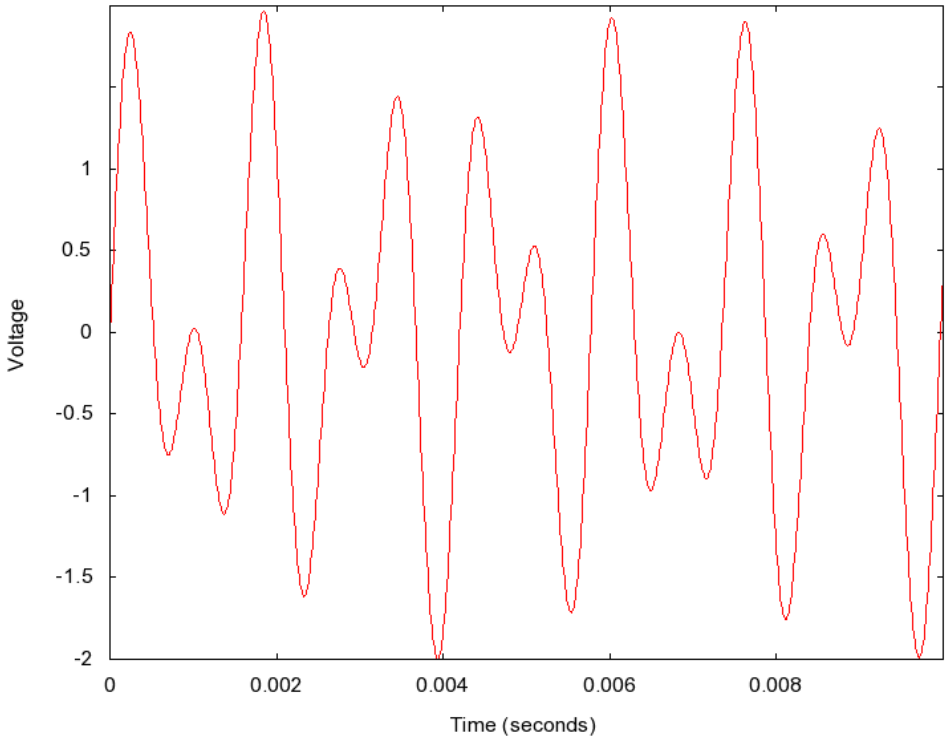
Are there any systems similar to this?

No, right now there is no device that serves the purpose of calling someone through a sixth sense interface apart from the one developed by Pranav Mistry which is exclusively for cellphones.

Circuit Details

The circuit basically consists of an 8051 microcontroller for the purpose of converting the incoming user event(either pressing keypad or through sixth sense) into the corresponding DTMF(Dual Tone Multi-Frequency) signals. The basic principle behind DTMF is that the keypad matrix is made up of a 3x3 matrix therefore each row and each column is allotted a unique frequency such that no two frequencies form harmonic pairs to avoid resonance and hence standing waves in the circuit. So evidently every keypad event or key press generates sine waves of two frequencies one belonging to low group(corresponding to rows) and the other belonging to high group(corresponding to columns).These waves get superimposed to form a resultant wave which corresponds to the DTMF tone for that key.





The above diagram shows the superimposition of 697Hz and 1209Hz generating a DTMF tone for the key ‘1’.

A Brief History into telephones

The first telephones used pulse mode dialling which basically involved cutting and Joining the circuit the number of times which corresponded to the key pressed.For Example dialling 1 meant breaking and joining the circuit once and so on, however this posed a problem during long distance communication wherein the signals suffer severe attenuation . This concept can be found in the old rotary dial telephones, where the characteristic clicking sound corresponded to the circuit break and join.

The new system on the other hand uses DTMF which encodes the ac signal in the phone line with the superimposed sine waves of the keypresses which is then decoded at the local telephone exchange and directed appropriately.

The key event is got from either the sixth sense device or the keypad interface, these are fed into the DC input pins P1(0 to 7) and P2(0 to 1) which hence correspond to the numbers 1 to 8 , 0 and 9 respectively, these are then processed by the assembly code(yet to be written) with appropriate delays generating two independent square waves of one high group frequency(columns) and one low group frequency(rows) .These are then fed to a LC series circuit which converts the square waves into sine waves ,these sine waves are then fed into op-amp multiplier two superimpose them. The resultant is a DTMF tone.

The P3(3) pin also known as INT1 is a non-maskable interrupt to which a basic receiver circuit is connected to receive signals from the sixth sense device as to which key was pressed. An active low on the non-maskable interrupt suspends the processing of all other functions and delivers the flow of control to the programmed vector address where the signals are again converted in the above manner.The receiver circuit basically consists of an antenna coupled with an inductor in parallel with a variable capacitor , the capacitor can be tuned to select the resonant frequency of the antenna to accept only the valid signals, this arrangement is then fed into a diode for rectification followed by an op-amp amplifier stage and hence input to the non-maskable interrupt P3(3) of the IC 8051.

Sixth Sense Device

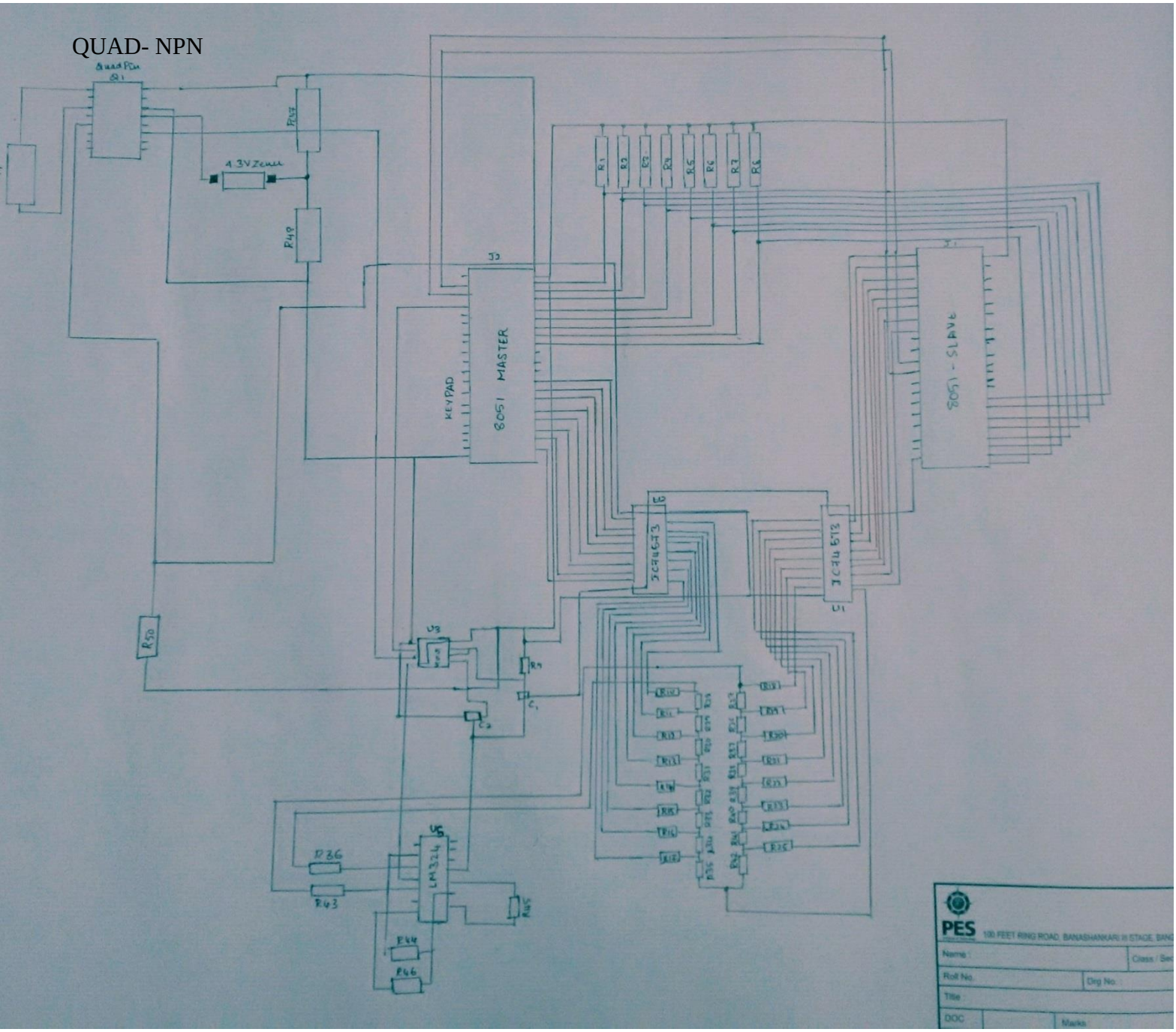
The sixth sense device is basically consists of a rasberrypi connected to a camera And a transmitter, using image processing it is capable of extracting the touch event From a projected keypad and then send the same to the receiver on the IC 8051.

List of components

SLNO	NAME	QUANTITY	COST(Rs)
1	AT89C51	2	120
2	IC74573	2	14
3	NE555	1	7
4	LM324	1	7
5	2n2222(npn)	3	21
6	Resistors –	As per requirement	10

	10k,1k,100k,20k,100,363k		
7	Capacitors- 0.1 micro farad,0.33 micro farad	Asper requirement	10
8	Zener diode (4.3 Vz)	1	2
9	Crystal oscillators(12Mhz)	2	18

Circuit Diagram



Explanation for choice of Components

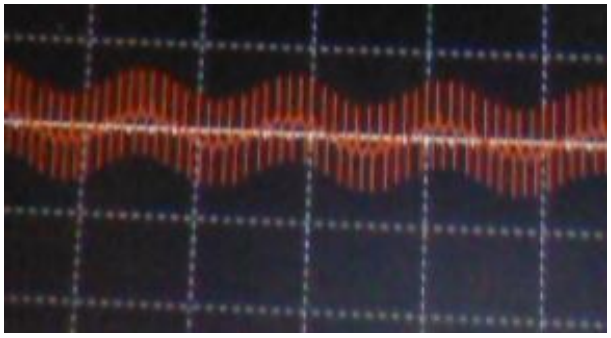
AT89C51

The **Intel MCS-51** (commonly referred to as **8051**) is a Harvard architecture, CISC instruction set, single chip microcontroller (µC) series which was developed by Intel in 1980 for use in embedded systems. Intel's original versions were popular in the 1980s and early 1990s and enhanced binary compatible derivatives remain popular today.

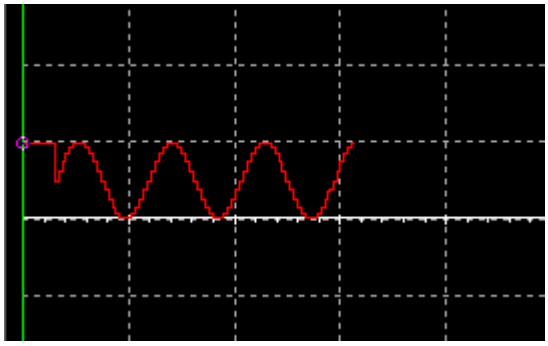
The IC-8051 was preferred above all the other IC's cause for generating two independent square waves simultaneously we required two timers and 8051 offers two timers and besides this it was the most inexpensive option for achieving this goal.

IC74573(Octal D-type Latch)

On moving the data from the accumulator to the output ports , there is a finite delay involved as a result of this the voltage intermittently drops to 0v just before rising to its new potential



(Before using IC74573)



(After using IC74573)

Therefore the value assigned to the ports during the previous cycle is latched by the IC followed by which it is disabled until the port acquires new value during the next cycle , therefore until the cycle elapses the values being latched by the IC prevents an abrupt drop to zero during the transition from one cycle to another.

NE555(timer)

The dtmf protocol as stated under the ETSI standard ETSI ES 201 235-4 V1.3.1 (2006-03) states that for a telephone exchange to identify and hence decode the received dtmf signal ,it must exist for a period of atleast 40ms , for this purpose we have used a 555 timer to accurately time the signal and restrict it to just above 40ms. The output of the 555 timer connects to the OE(active low) pin of IC74573. This pin when turned high transitions the output to a high impedance off state . The output of the timer when the trigger is above 1/3vcc , is low this causes the voltage drop across R50 to be negligibly low, therefore the input to OE will be Vcc or high ,therefore during the non key press time , OE is clamped to Vcc ,therefore the output of IC74573 is disabled and hence no output, but when any key is pressed , the trigger goes falls below 1/3Vcc to 0, thereby causing the 555 timer to start counting and hence producing an output of about equal to Vcc , this is then fed to the base of the transistor , thereby clamping R50 to ground due to the short on emitter, this inturn clamps OE to 0 thereby enabling the outputs of IC74573 and hence sending bits to the DAC.

LM324(quad-opamp)

The op-amp serves two purposes.

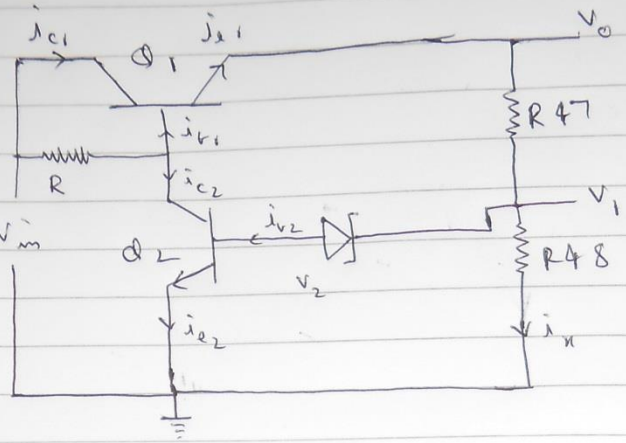
1. Firstly it acts as a summing amplifier , superposing the sine waves belonging namely to the low group and high group , hence producing the resultant DTMF tone.
2. Secondly , since the circuit is connected to the phone line, any interference in the output due to feedback can interrupt or hamper the working of the circuit, therefore to isolate the input from the output, before passing the generated sinusoids to the summing amplifier ,they are passed through voltage followers , which provide the necessary isolation.

DAC(R-2R Ladder)

The digital stream of bits generated by 8051 for the appropriate sinusoid wave value is sent to the DAC and depending on the bits which are on and off , the voltage divider network outputs a voltage corresponding to the sinusoid value at that instant.

Design Of The Circuit

1.Voltage regulator stage (For providing DC regulated voltage of 5-6.15V)



$V_o = 5 - 6.5\ V.$

$V_1 = \dfrac{V_o\ R_{48}}{R_{48} + R_{47}}$, $V_1 = V_2 + 0.7.$

$\therefore V_2 + 0.7 = \dfrac{5\ R_{48}}{R_{48} + R_{47}}$, $R_{48} = 100k$, $R_{47} = 1k.$

$V_2 = 4.25V$, $\therefore$ choosing.

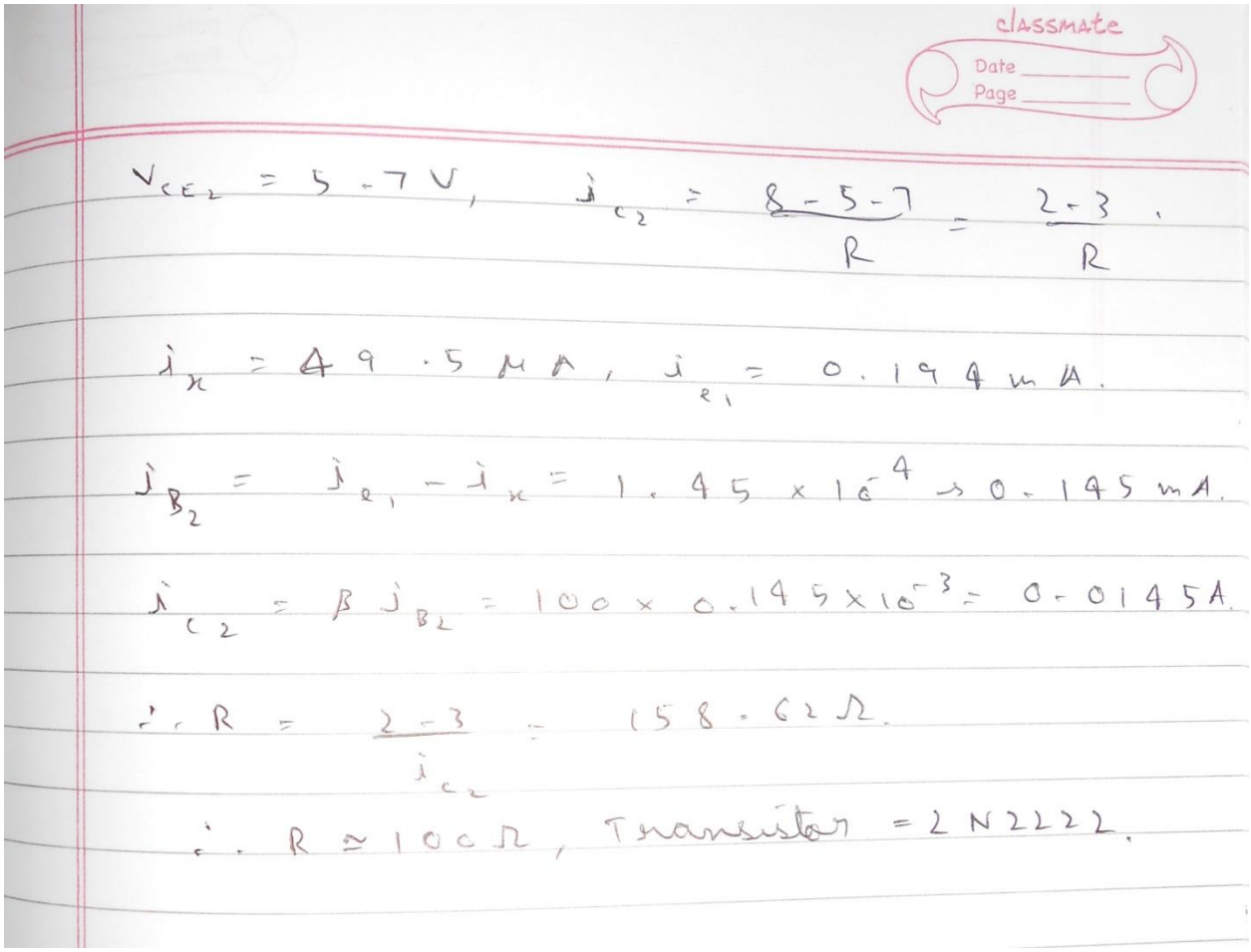
IN 4731 with $V_z = 4.3V.$

For $V_{in} = 8V.$ (max tolerance).

$\dfrac{V_{in} - V_{CE2}}{R} = i_{C2} + i_{B1}$, but $i_{C2} \gg i_{B1}$

$\therefore \dfrac{V_{in} - V_{CE2}}{R} = i_{C2}$, ~~$V_{CE_2} = 0.7 + \dfrac{V_o R_1}{R_1 + R_2} + 4.3 +$~~

$V_{CE_2} = 0.7 + \dfrac{V_o R_1}{R_1 + R_2} + 4.3 + 0.7$ (KVL).



2.Timer for 40ms delay

The time period of the count is given by

T=1.1RC, therefore T=40ms, and choosing C= 0.1 micro farad

R= 363k, therefore R is chosen as 370k

Assembly Code

8051-Master

```
org 0000h
mov r5,#1h
loop:mov p3,#0ffh
        mov p1,#0ffh
        mov tcon,#0h
       check1:          mov p3,#0ffh
```

```
                    cjne r5,#1h,pr
               pr:nop
                    cpl p3.0
                    jb p3.4,check2
                    jmp key1
          check2:   mov p3,#0ffh
                    cpl p3.0
                    jb p3.5,check3
                    jmp key2
          check3:   mov p3,#0ffh
                    cpl p3.0
                    jb p3.6,check4
                    jmp key3
          check4:   mov p3,#0ffh
                    cpl p3.1
                    jb p3.4,check5
                    jmp key4
          check5:   mov p3,#0ffh
                    cpl p3.1
                    jb p3.5,check6
                    jmp key5
          check6:   mov p3,#0ffh
                    cpl p3.1
                    jb p3.6,check7
                    jmp key6
          check7:   mov p3,#0ffh
                    cpl p3.2
                    jb p3.4,check8
                    jmp key7
          check8:   mov p3,#0ffh
                    cpl p3.2
                    jb p3.5,check9
                    jmp key8
          check9:   mov p3,#0ffh
                    cpl p3.2
                    jb p3.6,check0
                    jmp key9
          check0:   mov p3,#0ffh
                    cpl p3.3
                    jb p3.5,loop
                    jmp key0


key1:   mov r3,#0dbh  ;low
              mov r4,#0f4h  ;high
              jmp trans

key2:   mov r3,#0dbh  ;low
```

```
                mov r4,#0f7h  ;high
                jmp trans

key3:   mov r3,#0dbh  ;low
                mov r4,#0fah  ;high
                jmp trans

key4:   mov r3,#0e2h  ;low
                mov r4,#0f4h  ;high
                jmp trans

key5:   mov r3,#0e2h  ;low
                mov r4,#0f7h  ;high
                jmp trans

key6:   mov r3,#0e2h  ;low
                mov r4,#0fah  ;high
                jmp trans

key7:   mov r3,#0e6h  ;low
                mov r4,#0f4h  ;high
                jmp trans

key8:   mov r3,#0e6h  ;low
                mov r4,#0f7h  ;high
                jmp trans

key9:   mov r3,#0e6h  ;low
                mov r4,#0fah  ;high
                jmp trans

key0:   mov r3,#0ebh  ;low
                mov r4,#0f7h  ;high
                jmp trans

trans:  mov p0,r4
                mov r5,#0h
                mov p1,#0ffh
                cpl p1.1
                synchronize:    jnb p1.2,synchronize

proc:   mov dptr,#sine
                mov tmod,#12h
                mov b,r3
                mov r0,#18h
RTP:    mov tl1,#0c0h
                mov th1,#063h
                clr p1.3
```

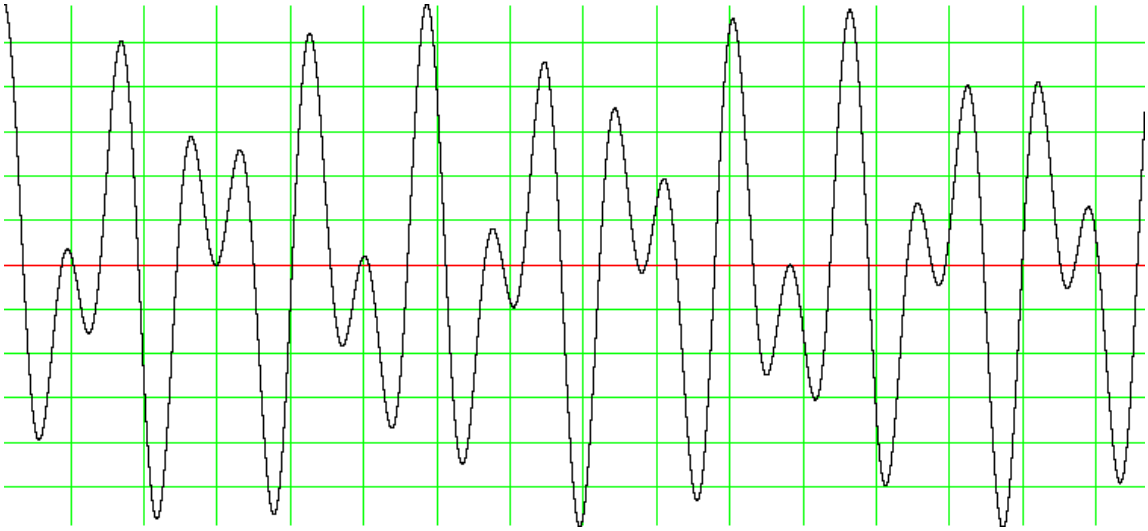
```
                setb tr1
crtp:   jnb tf1,proc1
                jmp loop
proc1:  mov tl0,b
                mov th0,#0ffh
                setb tr0
proc2:  jnb tf0,proc2
                cpl tr0
                cpl tf0
                clr a
                movc a,@a+dptr
                mov p2,a
                setb p1.0
                clr p1.0
                inc dptr
                djnz r0,crtp
proc3:  mov dptr,#sine
                mov r0,#18h
                jmp crtp
sine:   db
127,160,191,217,237,250,255,250,237,217,191,160,127,94,63,37,17,4,0,4,17,37,63,94,12
7
END
```

8051-Slave

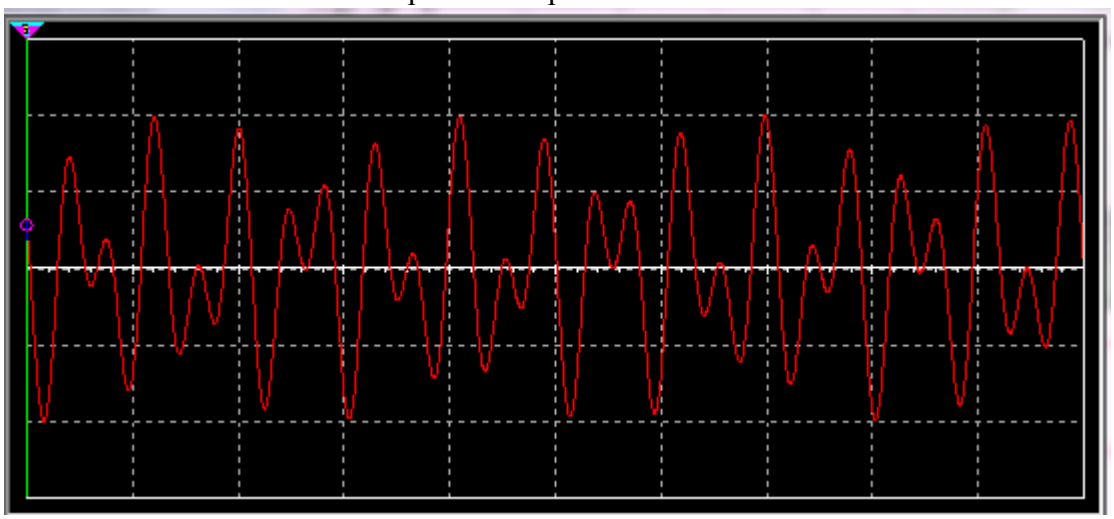
```
        org 0000h
init:   mov p2,#0ffh
                mov p3,#0ffh
                mov tcon,#0h
synchronize:    jb p3.1,synchronize
                                cpl p3.2

                mov dptr,#sine
                mov b,p2
                mov tmod,#21h
                mov r0,#18h
rtp:    mov tl0,#0c0h
                mov th0,#063h
                setb tr0
rtpch:  jnb tf0,proc1
                jmp init
proc1:  mov tl1,b
                mov th1,#0f0h
                setb tr1
proc2:  jnb tf1,proc2
                cpl tr1
                cpl tf1
                clr a
```

```
                movc a,@a+dptr
                mov p0,#00h
                mov p1,a
                mov p0,#1h
                mov p0,#0h
                inc dptr
                djnz r0,rtpch
proc3:  mov dptr,#sine
                mov r0,#18h
                jmp rtpch
sine:   db
127,160,191,217,237,250,255,250,237,217,191,160,127,94,63,37,17,4,0,4,17,37,63,94,12
7
END
```

Expected Waveforms and Graphs



Expected output for '1'



Output for key press 1 from the circuit

References

Wikipedia for the DTMF concept and waveform and courtesy of wolfram for being able to plot our output wave and hence derive the appropriate results. The entire circuit ,its designing and the assembly, C-code was designed and developed by me.