

# Final Exam S2

## Computer Architecture

Duration: 1 hr 30 min

Answer on the answer sheet only.

Do not show any calculation unless you are explicitly asked.

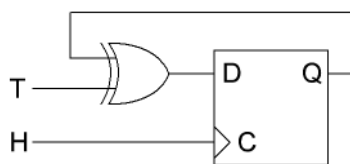
Do not use red ink.

**Exercise 1 (5 points)**

- Convert the numbers given on the [answer sheet](#) into their **single-precision** IEEE-754 representations. Write down the final result in its **binary form** and specify the three fields.
- Convert the **double-precision** IEEE-754 words given on the [answer sheet](#) into their associated representations. If a representation is a number, use the base-10 following form:  $k \times 2^n$  where  $k$  and  $n$  are integers (either positive or negative).

**Exercise 2 (5 points)**Answer the questions on the [answer sheet](#).**Exercise 3 (5 points)**

- Wire the flip-flops ([figure 1](#)) in order to design a **modulo-14 asynchronous up counter**.
- Wire the flip-flops ([figure 2](#)) in order to design a **modulo-14 asynchronous down counter**.
- Complete the timing diagrams shown on the [answer sheet](#) (up to the last vertical dotted line) for the following circuit.

**Exercise 4 (6 points)**

The table shown on the [answer sheet](#) gives the sequence of a counter we want to design. This counter should be made up of JK flip-flops.

- Complete the table shown on the [answer sheet](#).
- Write down the most simplified expressions of  $J$  and  $K$  for each flip-flop on the [answer sheet](#). **Complete the Karnaugh maps for the solutions that are not obvious.** An obvious solution does not have any logical operations apart from the complement (for instance:  $J_0 = 1$ ,  $K_1 = \overline{Q_2}$ ).



Last name: ..... First name: ..... Group: .....

**ANSWER SHEET****Exercise 1**

1.

Number	S	E	M
217.25			
0.21875			

2.

IEEE-754 Representation	Associated Representation
423E 0000 0000 0000 <sub>16</sub>	
8003 8000 0000 0000 <sub>16</sub>	
7FF0 0000 0000 0000 <sub>16</sub>	

**Exercise 2**

Question	Answer
A memory has a depth of 64 Ki words. How many address lines does this memory have?	
A memory has an 8-bit data bus and a 16-bit address bus. In a power of two, what is the capacity in bits of this memory?	
An <b>M1</b> memory has a 16-bit data bus and a 32-bit address bus. Two <b>M1</b> memories are connected in series to build an <b>M2</b> memory. What is the size of the address bus of the <b>M2</b> memory?	
A microprocessor has a 20-bit address bus. Three address lines are used for selecting the devices. With the linear address decoding, what is the maximum number of address lines that a device connected to this microprocessor can have?	
A microprocessor has a 24-bit address bus. Using the linear address decoding, we connect this microprocessor to the following devices. <ul style="list-style-type: none"> <li>• a ROM device (20 address lines)</li> <li>• a RAM device (15 address lines)</li> <li>• a peripheral device (10 address lines)</li> </ul> How many bits are unused in the case of the RAM device?	

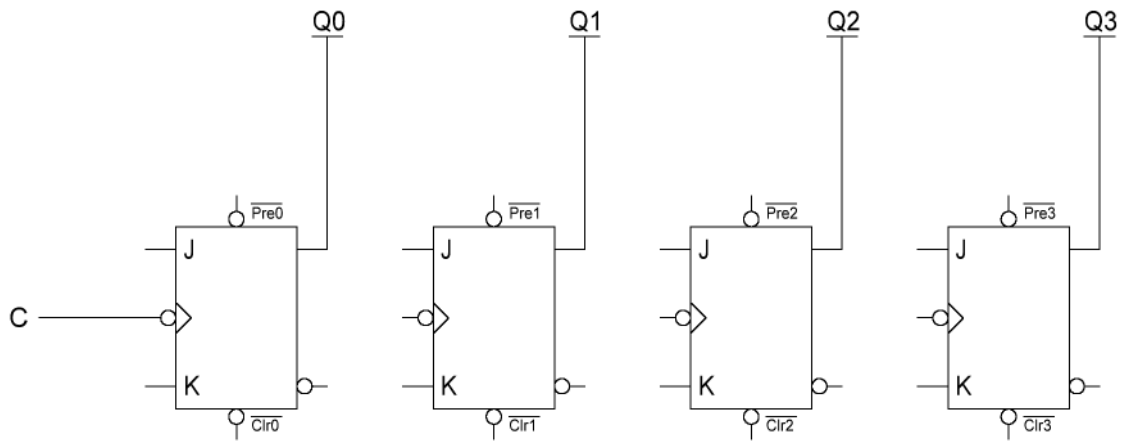
**Exercise 3**

Figure 1

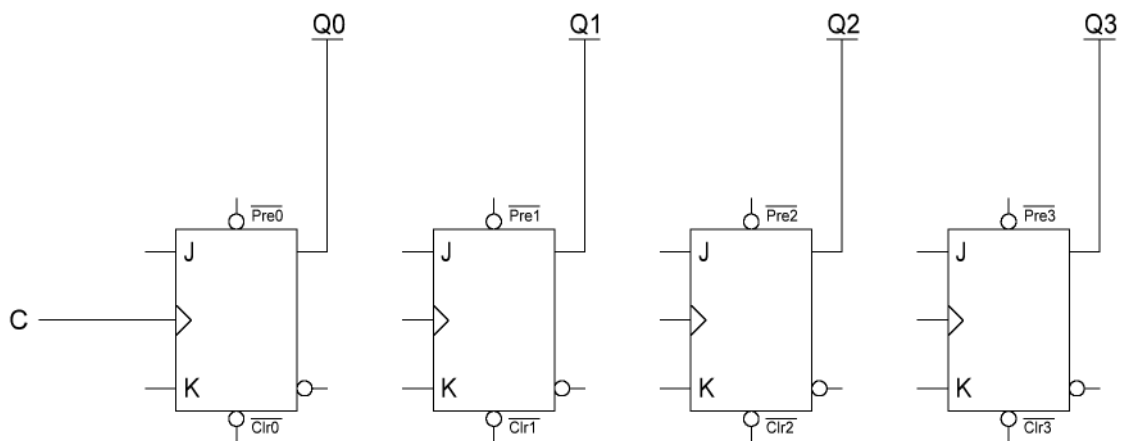
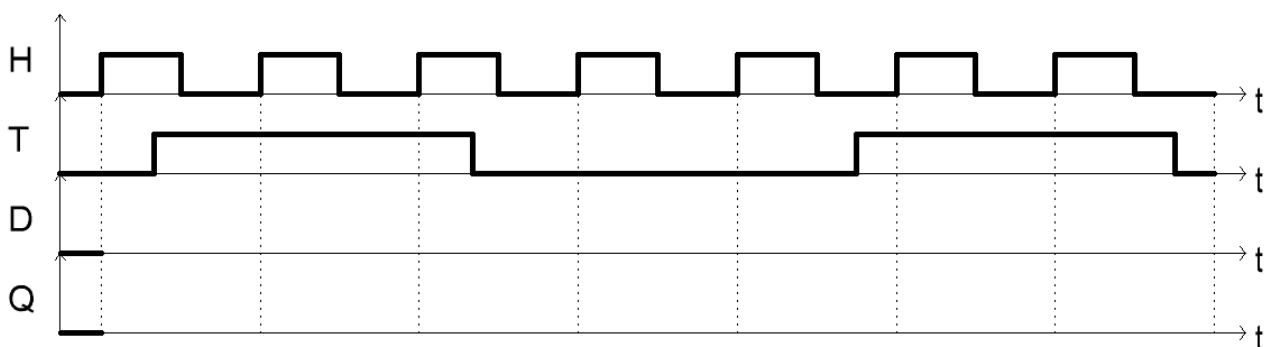


Figure 2



**Exercise 4**

Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
1	1	1						
1	0	0						
1	0	1						
1	1	0						
0	1	0						
0	0	1						
0	0	0						

**Do not use Karnaugh maps for obvious solutions.**

		Q1 Q0				
		J0	00	01	11	10
Q2	0					
	1					

**J0 =**

		Q1 Q0				
		K0	00	01	11	10
Q2	0					
	1					

**K0 =**

		Q1 Q0				
		J1	00	01	11	10
Q2	0					
	1					

**J1 =**

		Q1 Q0				
		K1	00	01	11	10
Q2	0					
	1					

**K1 =**

		Q1 Q0				
		J2	00	01	11	10
Q2	0					
	1					

**J2 =**

		Q1 Q0				
		K2	00	01	11	10
Q2	0					
	1					

**K2 =**

Feel free to use the blank space below if you need to: