

Contrôle S3

Architecture des ordinateurs

Durée : 1 h 30

Répondre exclusivement sur le document réponse.

Exercice 1 (5 points)

Remplir le tableau présent sur le document réponse. Donnez le nouveau contenu des registres (sauf le PC) et/ou de la mémoire modifiés par les instructions. **Vous utiliserez la représentation hexadécimale. La mémoire et les registres sont réinitialisés à chaque nouvelle instruction.**

Valeurs initiales : D0 = \$FFFF0010 A0 = \$00005000 PC = \$00006000
 D1 = \$10000002 A1 = \$00005008
 D2 = \$FFFFFFF0 A2 = \$00005010

\$005000	54 AF 18 B9 E7 21 48 C0
\$005008	C9 10 11 C8 D4 36 1F 88
\$005010	13 79 01 80 42 1A 2D 49

Exercice 2 (4 points)

Remplissez le tableau présent sur le document réponse. Donnez le résultat des additions ainsi que le contenu des bits N, Z, V et C du registre d'état.

Exercice 3 (2 points)

Soit les programmes ci-dessous. Complétez le tableau présent sur le document réponse.

```

move.l  #$76543210,d1
ror.l   #8,d1
ror.b   #4,d1
swap    d1
ror.b   #4,d1
  
```

```

move.l  #$76543210,d2
ror.b   #4,d2
ror.w   #8,d2
ror.b   #4,d2
ror.w   #8,d2
  
```

Exercice 4 (3 points)

Répondez aux questions sur le document réponse.

Exercice 5 (6 points)

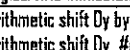

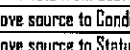
Soit le programme ci-dessous. Complétez le tableau présent sur le document réponse.

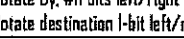
Main	move.l #158f,d7	
next1	moveq.l #1,d1 tst.b d7 bpl next2 moveq.l #2,d1	
next2	moveq.l #1,d2 tst.l d7 bmi next3 moveq.l #2,d2	
next3	clr.l d3 move.l #87654321,d0	
loop3	addq.l #1,d3 subq.w #1,d0 bne loop3	
next4	clr.l d4 move.w #5aa,d0	
loop4	addq.l #1,d4 dbra d0,loop4 ; DBRA = DBF	
next5	moveq.l #1,d5 cmp.b #542,d7 bgt next6 moveq.l #2,d5	
next6	moveq.l #1,d6 cmp.b #542,d7 bls quit moveq.l #2,d6	
quit	illegal	

EASy68K Quick Reference v1.8

<http://www.wowgweb.com/EASy68K.htm>

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Opcode	Size	Operand	CCR	Effective Address s=source, d=destination, e=either, i=displacement													Operation	Description
		BWL	s,d	XNZVC	Dn	An	(An)	(An)+	-(An)	(i,An)	(i,An,Rn)	abs.W	abs.L	(i,PC)	(i,PC,Rn)	#n		
ABCD	B	Dy,Dx -(Ay),-(Ax)	*U*U*	e	-	-	-	-	-	-	-	-	-	-	-	-	$Dy + Dx_{10} + X \rightarrow Dx_{10}$ $-(Ay)_{10} + -(Ax)_{10} + X \rightarrow -(Ax)_{10}$	Add BCD source and eXtend bit to destination, BCD result
ADD ⁴	BWL	s,Dn Dn,d	*****	e	s	s	s	s	s	s	s	s	s	s	s	s	$s + Dn \rightarrow Dn$ $Dn + d \rightarrow d$	Add binary (ADDI or ADDQ is used when source is #n. Prevent ADDQ with #n.L)
ADDA ⁴	WL	s,An	-----	s	e	s	s	s	s	s	s	s	s	s	s	s	$s + An \rightarrow An$	Add address (.W sign-extended to .L)
ADDI ⁴	BWL	#n,d	*****	d	-	d	d	d	d	d	d	d	d	-	-	-	$\#n + d \rightarrow d$	Add immediate to destination
ADDQ ⁴	BWL	#n,d	*****	d	d	d	d	d	d	d	d	d	d	-	-	-	$\#n + d \rightarrow d$	Add quick immediate (#n range: l to 8)
ADDX	BWL	Dy,Dx -(Ay),-(Ax)	*****	e	-	-	-	-	-	-	-	-	-	-	-	-	$Dy + Dx + X \rightarrow Dx$ $-(Ay) + -(Ax) + X \rightarrow -(Ax)$	Add source and eXtend bit to destination
AND ⁴	BWL	s,Dn Dn,d	---*00	e	-	s	s	s	s	s	s	s	s	s	s	s	$s \text{ AND } Dn \rightarrow Dn$ $Dn \text{ AND } d \rightarrow d$	Logical AND source to destination (ANDI is used when source is #n)
ANDI ⁴	BWL	#n,d	---*00	d	-	d	d	d	d	d	d	d	d	-	-	-	$\#n \text{ AND } d \rightarrow d$	Logical AND immediate to destination
ANDI ⁴	B	#n,CCR	0000 0000	-	-	-	-	-	-	-	-	-	-	-	-	-	$\#n \text{ AND } CCR \rightarrow CCR$	Logical AND immediate to CCR
ANDI ⁴	W	#n,SR	0000 0000	-	-	-	-	-	-	-	-	-	-	-	-	-	$\#n \text{ AND } SR \rightarrow SR$	Logical AND immediate to SR (Privileged)
ASL	BWL	Dx,Dy	*****	e	-	-	-	-	-	-	-	-	-	-	-	-		Arithmetic shift Dy by Dx bits left/right
ASR	W	#n,Dy	d	d	-	-	-	-	-	-	-	-	-	-	-	-		Arithmetic shift Dy #n bits L/R (#n: l to 8)
		d		-	-	d	d	d	d	d	d	d	d	-	-	-		Arithmetic shift ds l bit left/right (.W only)
Bcc	BW ²	address ²	-----	-	-	-	-	-	-	-	-	-	-	-	-	-	if cc true then address \rightarrow PC	Branch conditionally (cc table on back) (8 or 16-bit \pm offset to address)
BCHG	B L	Dn,d #n,d	---*--	e ¹	-	d	d	d	d	d	d	d	d	-	-	-	$\text{NOT}(\text{bit number of } d) \rightarrow Z$ $\text{NOT}(\text{bit n of } d) \rightarrow \text{bit n of } d$	Set Z with state of specified bit in d then invert the bit in d
BCLR	B L	Dn,d #n,d	---*--	e ¹	-	d	d	d	d	d	d	d	d	-	-	-	$\text{NOT}(\text{bit number of } d) \rightarrow Z$ $0 \rightarrow \text{bit number of } d$	Set Z with state of specified bit in d then clear the bit in d
BRA	BW ²	address ²	-----	-	-	-	-	-	-	-	-	-	-	-	-	-	address \rightarrow PC	Branch always (8 or 16-bit \pm offset to addr)
BSET	B L	Dn,d #n,d	---*--	e ¹	-	d	d	d	d	d	d	d	d	-	-	-	$\text{NOT}(\text{bit n of } d) \rightarrow Z$ $1 \rightarrow \text{bit n of } d$	Set Z with state of specified bit in d then set the bit in d
BSR	BW ²	address ²	-----	-	-	-	-	-	-	-	-	-	-	-	-	-	PC \rightarrow -(SP); address \rightarrow PC	Branch to subroutine (8 or 16-bit \pm offset)
BTST	B L	Dn,d #n,d	---*--	e ¹	-	d	d	d	d	d	d	d	d	-	-	-	$\text{NOT}(\text{bit Dn of } d) \rightarrow Z$ $\text{NOT}(\text{bit \#n of } d) \rightarrow Z$	Set Z with state of specified bit in d Leave the bit in d unchanged
CHK	W	s,Dn	---*UUU	e	-	s	s	s	s	s	s	s	s	s	s	s	if $Dn < 0$ or $Dn > s$ then TRAP	Compare Dn with 0 and upper bound (s)
CLR	BWL	d	-0100	d	-	d	d	d	d	d	d	d	d	-	-	-	$0 \rightarrow d$	Clear destination to zero
CMP ⁴	BWL	s,Dn	-----	e	s ¹	s	s	s	s	s	s	s	s	s	s	s	set CCR with $Dn - s$	Compare Dn to source
CMPI ⁴	WL	s,An	-----	s	e	s	s	s	s	s	s	s	s	s	s	s	set CCR with $An - s$	Compare An to source
CMPI ⁴	BWL	#n,d	-----	d	-	d	d	d	d	d	d	d	d	-	-	-	set CCR with $d - \#n$	Compare destination to #n
CMPI ⁴	BWL	(Ay)+,(Ax)+	-----	-	-	-	e	-	-	-	-	-	-	-	-	-	set CCR with $(Ax) - (Ay)$	Compare (Ax) to (Ay); Increment Ax and Ay
DBcc	W	Dn,address ²	-----	-	-	-	-	-	-	-	-	-	-	-	-	-	if cc false then { $Dn-1 \rightarrow Dn$ if $Dn < -1$ then addr \rightarrow PC }	Test condition, decrement and branch (16-bit \pm offset to address)
DIVS	W	s,Dn	---*00	e	-	s	s	s	s	s	s	s	s	s	s	s	$\pm 32\text{bit } Dn / \pm 16\text{bit } s \rightarrow \pm Dn$	$Dn = [16\text{-bit remainder}, 16\text{-bit quotient}]$
DIVU	W	s,Dn	---*00	e	-	s	s	s	s	s	s	s	s	s	s	s	$32\text{bit } Dn / 16\text{bit } s \rightarrow Dn$	$Dn = [16\text{-bit remainder}, 16\text{-bit quotient}]$
EDR ⁴	BWL	Dn,d	---*00	e	-	d	d	d	d	d	d	d	d	-	-	-	$Dn \text{ XOR } d \rightarrow d$	Logical exclusive OR Dn to destination
EDRI ⁴	BWL	#n,d	---*00	d	-	d	d	d	d	d	d	d	d	-	-	-	$\#n \text{ XOR } d \rightarrow d$	Logical exclusive OR #n to destination
EDRI ⁴	B	#n,CCR	0000 0000	-	-	-	-	-	-	-	-	-	-	-	-	-	$\#n \text{ XOR } CCR \rightarrow CCR$	Logical exclusive OR #n to CCR
EDRI ⁴	W	#n,SR	0000 0000	-	-	-	-	-	-	-	-	-	-	-	-	-	$\#n \text{ XOR } SR \rightarrow SR$	Logical exclusive OR #n to SR (Privileged)
EXG	L	Rx,Ry	-----	e	e	-	-	-	-	-	-	-	-	-	-	-	register \leftrightarrow register	Exchange registers (32-bit only)
EXT	WL	Dn	---*00	d	-	-	-	-	-	-	-	-	-	-	-	-	$Dn.B \rightarrow Dn.W$ $Dn.W \rightarrow Dn.L$	Sign extend (change .B to .W or .W to .L)
ILLEGAL			-----	-	-	-	-	-	-	-	-	-	-	-	-	-	PC \rightarrow -(SSP); SR \rightarrow -(SSP)	Generate Illegal Instruction exception
JMP		d	-----	-	-	d	-	-	-	d	d	d	d	d	d	d	$\text{PC} \rightarrow d$	Jump to effective address of destination
JSR		d	-----	-	-	d	-	-	-	d	d	d	d	d	d	d	PC \rightarrow -(SP); $\text{PC} \rightarrow d$	push PC, jump to subroutine at address d
LEA	L	s,An	-----	-	e	s	-	-	-	s	s	s	s	s	s	s	$\text{PC} \rightarrow$ -(SP); $\text{PC} \rightarrow d$	Load effective address of s to An
LINK		An,#n	-----	-	-	-	-	-	-	-	-	-	-	-	-	-	$An \rightarrow$ -(SP); SP \rightarrow An; SP $+ \#n \rightarrow$ SP	Create local workspace on stack (negative n to allocate space)
LSL	BWL	Dx,Dy	***0*	e	-	-	-	-	-	-	-	-	-	-	-	-		Logical shift Dy, Dx bits left/right
LSR	W	#n,Dy	d	d	-	d	d	d	d	d	d	d	d	-	-	-		Logical shift Dy, #n bits L/R (#n: l to 8)
		d		-	-	d	d	d	d	d	d	d	d	-	-	-		Logical shift d l bit left/right (.W only)
MOVE ⁴	BWL	s,d	---*00	e	s ¹	e	e	e	e	e	e	e	e	e	e	e	$s \rightarrow d$	Move data from source to destination
MOVE	W	s,CCR	0000 0000	s	-	s	s	s	s	s	s	s	s	s	s	s	$s \rightarrow CCR$	Move source to Condition Code Register
MOVE	W	s,SR	0000 0000	s	-	s	s	s	s	s	s	s	s	s	s	s	$s \rightarrow SR$	Move source to Status Register (Privileged)
MOVE	W	SR,d	-----	d	-	d	d	d	d	d	d	d	d	-	-	-	$SR \rightarrow d$	Move Status Register to destination
MOVE	L	USP,An	-----	-	d	-	-	-	-	-	-	-	-	-	-	-	USP \rightarrow An	Move User Stack Pointer to An (Privileged)
		An,USP	-----	-	s	-	-	-	-	-	-	-	-	-	-	-	An \rightarrow USP	Move An to User Stack Pointer (Privileged)
	BWL	s,d	XNZVC	Dn	An	(An)	(An)+	-(An)	(i,An)	(i,An,Rn)	abs.W	abs.L	(i,PC)	(i,PC,Rn)	#n			

Opcode	Size	Operand	CCR	Effective Address s=source, d=destination, e=either, i=displacement													Operation	Description
	BWL	s,d	XNZVC	Dn	An	(An)	(An)+	-(An)	(iAn)	(iAn,Rn)	abs.W	abs.L	(iPC)	(iPC,Rn)	#n			
MOVEA ⁴	WL	s,An	-----	s	e	s	s	s	s	s	s	s	s	s	s	s → An	Move source to An (MOVE s,An use MOVEA)	
MOVEM ⁴	WL	Rn-Rn,d	-----	-	-	d	-	-	d	d	d	d	-	-	-	Registers → d	Move specified registers to/from memory (W source is sign-extended to L for Rn)	
		s,Rn-Rn	-----	-	-	s	-	-	s	s	s	s	s	s	-	s → Registers		
MOVEP	WL	Dn,(iAn)	-----	s	-	-	-	-	d	-	-	-	-	-	-	Dn → (iAn)...(i+2An)...(i+4A	Move Dn to/from alternate memory bytes (Access only even or odd addresses)	
		(iAn),Dn	-----	d	-	-	-	-	s	-	-	-	-	-	-	(iAn) → Dn...(i+2An)...(i+4A		
MOVEQ ⁴	L	#n,Dn	---*00	d	-	-	-	-	-	-	-	-	-	-	s	#n → Dn	Move sign extended 8-bit #n to Dn	
MULS	W	s,Dn	---*00	e	-	s	s	s	s	s	s	s	s	s	s	±16bit s * ±16bit Dn → ±Dn	Multiply signed 16-bit; result: signed 32-bit	
MULU	W	s,Dn	---*00	e	-	s	s	s	s	s	s	s	s	s	s	16bit s * 16bit Dn → Dn	Multiply unsigned 16-bit; result: unsigned 32-bit	
NBCD	B	d	*U*U*	d	-	d	d	d	d	d	d	d	-	-	-	0 - d ₀ - X → d	Negate BCD with eXtend, BCD result	
NEGB	BWL	d	*****	d	-	d	d	d	d	d	d	d	-	-	-	0 - d → d	Negate destination (2's complement)	
NEGX	BWL	d	*****	d	-	d	d	d	d	d	d	d	-	-	-	0 - d - X → d	Negate destination with eXtend	
NOP			-----	-	-	-	-	-	-	-	-	-	-	-	-	None	No operation occurs	
NOT	BWL	d	---*00	d	-	d	d	d	d	d	d	d	-	-	-	NOT(d) → d	Logical NOT destination (1's complement)	
OR ⁴	BWL	s,Dn	---*00	e	-	s	s	s	s	s	s	s	s	s	s	s OR Dn → Dn	Logical OR	
		Dn,d	---*00	e	-	d	d	d	d	d	d	d	-	-	-	Dn OR d → d	(ORI is used when source is #n)	
ORI ⁴	BWL	#n,d	---*00	d	-	d	d	d	d	d	d	d	-	-	s	#n OR d → d	Logical OR #n to destination	
ORI ⁴	B	#n,CCR	000 000 000 000	-	-	-	-	-	-	-	-	-	-	-	s	#n OR CCR → CCR	Logical OR #n to CCR	
ORI ⁴	W	#n,SR	000 000 000 000	-	-	-	-	-	-	-	-	-	-	-	s	#n OR SR → SR	Logical OR #n to SR (Privileged)	
PEA	L	s	-----	-	-	s	-	-	s	s	s	s	s	s	-	Ts → -(SP)	Push effective address of s onto stack	
RESET			-----	-	-	-	-	-	-	-	-	-	-	-	-	Assert RESET Line	Issue a hardware RESET (Privileged)	
ROL	BWL	Dx,Dy	---*0*	e	-	-	-	-	-	-	-	-	-	-	-		Rotate Dy, Dx bits left/right (without X)	
ROR	BWL	#n,Dy	---*0*	d	-	-	-	-	-	-	-	-	-	-	s		Rotate Dy, #n bits left/right (#n: 1 to 8)	
	W	d	---*0*	-	-	d	d	d	d	d	d	d	-	-	-	Rotate d 1-bit left/right (W only)		
ROXL	BWL	Dx,Dy	---*0*	e	-	-	-	-	-	-	-	-	-	-	-		Rotate Dy, Dx bits L/R, X used then updated	
ROXR	BWL	#n,Dy	---*0*	d	-	-	-	-	-	-	-	-	-	-	s		Rotate Dy, #n bits left/right (#n: 1 to 8)	
	W	d	---*0*	-	-	d	d	d	d	d	d	d	-	-	-	Rotate destination 1-bit left/right (W only)		
RTE			000 000 000 000	-	-	-	-	-	-	-	-	-	-	-	-	(SP)+ → SR; (SP)+ → PC	Return from exception (Privileged)	
RTR			000 000 000 000	-	-	-	-	-	-	-	-	-	-	-	-	(SP)+ → CCR; (SP)+ → PC	Return from subroutine and restore CCR	
RTS			-----	-	-	-	-	-	-	-	-	-	-	-	-	(SP)+ → PC	Return from subroutine	
SBCD	B	Dy,Dx	*U*U*	e	-	-	-	-	-	-	-	-	-	-	-	Dx ₀ - Dy ₀ - X → Dx ₀	Subtract BCD source and eXtend bit from destination, BCD result	
		-(Ay),-(Ax)	*U*U*	-	-	-	-	e	-	-	-	-	-	-	-	-(Ax) ₀ - -(Ay) ₀ - X → -(Ax) ₀		
SCC	B	d	-----	d	-	d	d	d	d	d	d	d	-	-	-	If cc is true then 1's → d else 0's → d	If cc true then d.B = 11111111 else d.B = 00000000	
STOP		#n	000 000 000 000	-	-	-	-	-	-	-	-	-	-	-	s	#n → SR; STOP	Move #n to SR, stop processor (Privileged)	
SUB ⁴	BWL	s,Dn	*****	e	s	s	s	s	s	s	s	s	s	s	s	Dn - s → Dn	Subtract binary (SUB) or SUBQ used when source is #n. Prevent SUBQ with #n.L	
		Dn,d	*****	e	d	d	d	d	d	d	d	d	-	-	-	d - Dn → d		
SUBA ⁴	WL	s,An	-----	s	e	s	s	s	s	s	s	s	s	s	s	An - s → An	Subtract address (W sign-extended to L)	
SUBI ⁴	BWL	#n,d	*****	d	-	d	d	d	d	d	d	d	-	-	s	d - #n → d	Subtract immediate from destination	
SUBQ ⁴	BWL	#n,d	*****	d	d	d	d	d	d	d	d	d	-	-	s	d - #n → d	Subtract quick immediate (#n range: 1 to 8)	
SUBX	BWL	Dy,Dx	*****	e	-	-	-	-	-	-	-	-	-	-	-	Dx - Dy - X → Dx	Subtract source and eXtend bit from destination	
		-(Ay),-(Ax)	*****	-	-	-	-	e	-	-	-	-	-	-	-	-(Ax) - -(Ay) - X → -(Ax)		
SWAP	W	Dn	---*00	d	-	-	-	-	-	-	-	-	-	-	-	bits(31:16) ↔ bits(15:0)	Exchange the 16-bit halves of Dn	
TAS	B	d	---*00	d	-	d	d	d	d	d	d	d	-	-	-	test d → CCR; 1 → bit7 of d	N and Z set to reflect d, bit7 of d set to 1	
TRAP		#n	-----	-	-	-	-	-	-	-	-	-	-	-	s	PC → -(SSP); SR → -(SSP); (vector table entry) → PC	Push PC and SR, PC set by vector table #n (#n range: 0 to 15)	
TRAPV			-----	-	-	-	-	-	-	-	-	-	-	-	-	If V then TRAP #7	If overflow, execute an Overflow TRAP	
TST	BWL	d	---*00	d	-	d	d	d	d	d	d	d	-	-	-	test d → CCR	N and Z set to reflect destination	
UNLK		An	-----	-	d	-	-	-	-	-	-	-	-	-	-	An → SP; (SP)+ → An	Remove local workspace from stack	
	BWL	s,d	XNZVC	Dn	An	(An)	(An)+	-(An)	(iAn)	(iAn,Rn)	abs.W	abs.L	(iPC)	(iPC,Rn)	#n			

Condition Tests (* OR, I NOT, * XOR, * Unsigned, * Alternate cc)					
cc	Condition	Test	cc	Condition	Test
T	true	I	VC	overflow clear	IV
F	false	0	VS	overflow set	V
HI [*]	higher than	I(C + Z)	PL	plus	IN
LS [*]	lower or same	C + Z	MI	minus	N
HS [*] , CC [*]	higher or same	IC	GE	greater or equal	I(N ⊕ V)
LO [*] , CS [*]	lower than	C	LT	less than	(N ⊕ V)
NE	not equal	I2	GT	greater than	I((N ⊕ V) + Z)
EQ	equal	Z	LE	less or equal	(N ⊕ V) + Z

Revised by Peter Csaszar, Lawrence Tech University – 2004-2006

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An Address register (16/32-bit, n=0-7)
Dn Data register (8/16/32-bit, n=0-7)
Rn any data or address register
s Source, d Destination
#n Either source or destination
#n Immediate data, I Displacement
BCD Binary Coded Decimal
↑ Effective address
1 Long only; all others are byte only
2 Assembler calculates offset
3 Branch sizes: .B or .S -128 to +127 bytes, .W or .L -32768 to +32767 bytes
4 Assembler automatically uses A, I, Q or M form if possible. Use #n.L to prevent Quick optimization

SSP Supervisor Stack Pointer (32-bit)
USP User Stack Pointer (32-bit)
SP Active Stack Pointer (same as A7)
PC Program Counter (24-bit)

SR Status Register (16-bit)
CCR Condition Code Register (lower 8-bits of SR)
N negative, Z zero, V overflow, C carry, X extend
* set according to operation's result, = set directly
- not affected, 0 cleared, 1 set, U undefined

Nom : Prénom : Classe :

DOCUMENT RÉPONSE À RENDRE

Exercice 1

Instruction	Mémoire	Registre
Exemple	\$005000 54 AF 00 40 E7 21 48 C0	A0 = \$00005004 A1 = \$0000500C
Exemple	\$005008 C9 10 11 C8 D4 36 FF 88	Aucun changement
MOVE.W #\$500A, -(A1)		
MOVE.W \$500A, -2(A1)		
MOVE.L \$500A, -(A1)		
MOVE.B 5(A1), 3(A2, D2.L)		
MOVE.L -4(A1), -16(A2, D0.W)		

Exercice 2

Opération	Taille (bits)	Résultat (hexadécimal)	N	Z	V	C
\$5A + \$35	8					
\$5A + \$35	16					
\$7F8C + \$FFFF	16					
\$FFFFFFFF0 + \$00000010	32					

Exercice 3

Valeurs des registres après exécution du programme. Utilisez la représentation hexadécimale sur 32 bits.	
D1 = \$	D2 = \$

Exercice 4

Question	Réponse
Combien de registres de donnée possède le 68000 ?	
Combien de registres d'adresse possède le 68000 ?	
Combien de compteurs programme possède le 68000 ?	
Combien de pointeurs de pile possède le 68000 ?	
Combien de registres d'état possède le 68000 ?	
Combien de modes de fonctionnement possède le 68000 ?	

Exercice 5

Valeurs des registres après exécution du programme. Utilisez la représentation hexadécimale sur 32 bits.		
D1 = \$	D3 = \$	D5 = \$
D2 = \$	D4 = \$	D6 = \$