Key to Midterm Exam S2
Computer Architecture

Duration: 1 hr 30 min

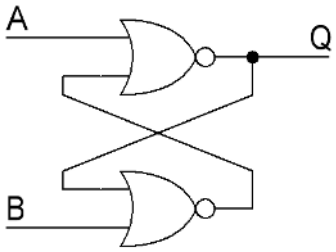
Answer on the answer sheet only.
Do not show any calculation unless you are explicitly asked.
Do not use a pencil or red ink.

Exercise 1 (9 points)

1. Convert the numbers given on the answer sheet into their **single-precision** IEEE-754 representations. Write down the final result in its **binary form** and specify the three fields.
2. Convert the **double-precision** IEEE-754 words given on the answer sheet into their associated representations. If a representation is a number, use the base-10 following form: $k \times 2^n$ where k and n are integers (either positive or negative).
3. Determine the smallest and largest absolute values of a single-precision IEEE-754 **denormalized** number. Use the following form: 2^n for the smallest number and $(1 - 2^{n1}) \times 2^{n2}$ for the largest number where n, $n1$ and $n2$ are integers (either positive or negative). Write down the base-10 numerical values of n, $n1$ and $n2$ on the answer sheet.

Exercise 2 (3 points)

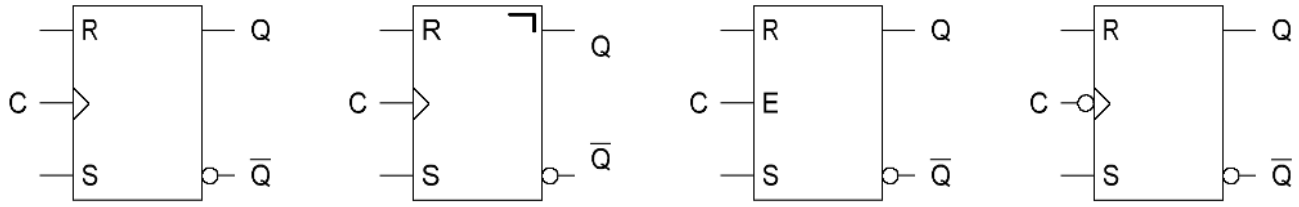
Let us consider the following circuit:



1. Complete the truth table shown on the answer sheet.
2. What is the name of this circuit?

Exercise 3 (2 points)

Give the type of each flip-flop below (answer on the answer sheet).



Flip-Flop 1 Flip-Flop 2 Flip-Flop 3 Flip-Flop 4

Exercise 4 (6 points)

1. Complete the timing diagrams shown on the answer sheet (up to the last vertical dotted line) for a gated RS latch (*Q0*), a positive-edge-triggered RS flip-flop (*Q1*), a negative-edge-triggered RS flip-flop (*Q2*) and a master-slave RS flip-flop (*Q3*).
2. Complete the timing diagrams shown on the answer sheet (up to the last vertical dotted line) for the following circuits.

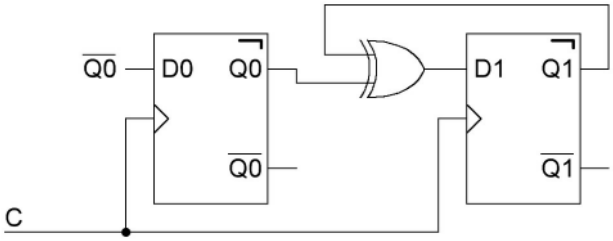


Figure 1

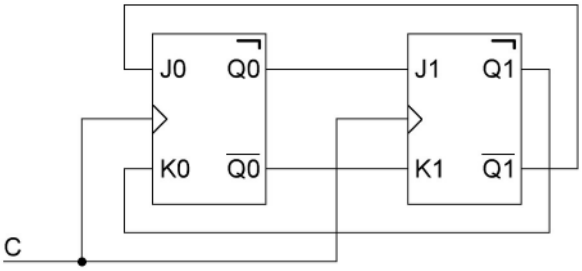


Figure 2

Last name: ..... First name: ..... Group: .....

ANSWER SHEET

Exercise 1

1.

Number	S	E	M
165	0	10000110	01001010000000000000000
59.625	0	10000100	11011101000000000000000
0.921875	0	01111110	11011000000000000000000

2.

IEEE-754 Representation	Associated Representation
485C 0000 0000 0000_{16}	7×2^{132}
7FF0 0000 0000 0000_{16}	$+\infty$
0002 3000 0000 0000_{16}	35×2^{-1030}
3FF0 0000 0000 0000_{16}	1×2^{0}

3.

n	n1	n2
-149	-23	-126

Exercise 2

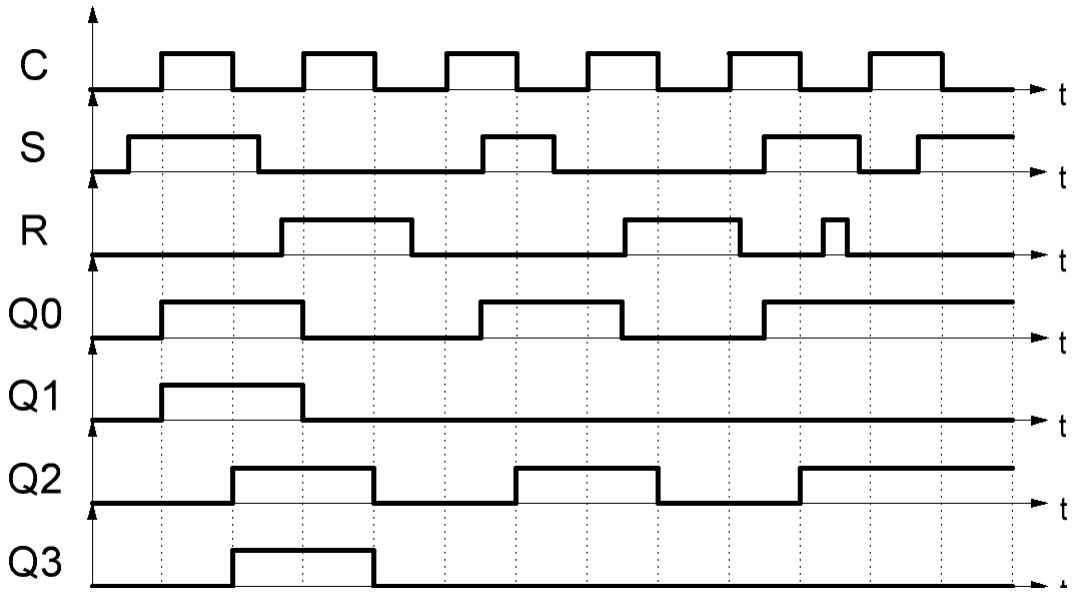
A	B	Q
0	0	q
0	1	1
1	0	0
1	1	0

Name of the circuit
RS latch

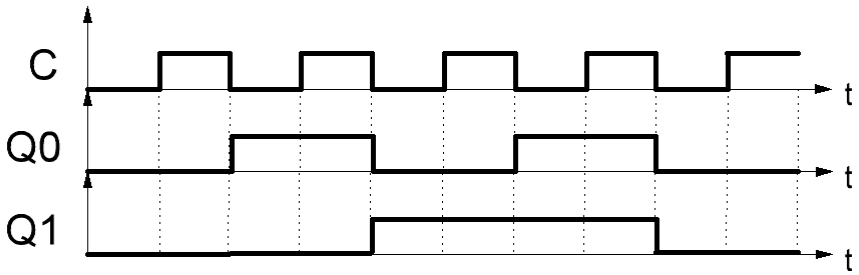
Exercise 3

Flip-Flop	Type of Flip-Flop
1	Positive-edge-triggered RS flip-flop
2	Master-slave RS flip-flop
3	Gated RS latch
4	Negative-edge-triggered RS flip-flop

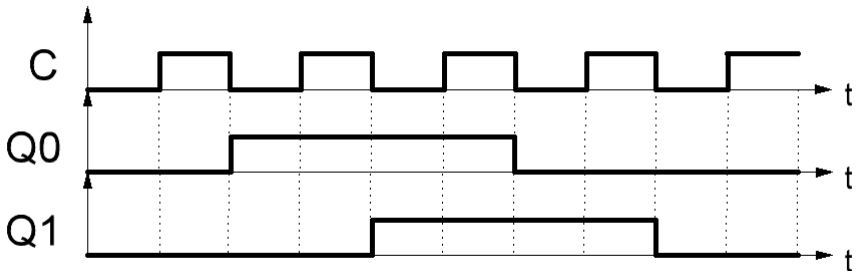
Exercise 4



RS flip-flops



Timing diagram of figure 1



Timing diagram of figure 2

Feel free to use the blank space below if you need to: