

AFE4432 Ultra-Small, Integrated AFE for Optical Bio-Sensing

1 Features

- Supports signal acquisition of up to 12 phase sets
- Supports up to 4 LEDs, 3 PDs
- Flexible allocation of LEDs, PDs in each phase
- Simultaneous signal acquisition from different sensors at different data rates
- Accurate, continuous PPG monitoring:
 - Low current for continuous heart-rate monitoring on a wearable device with a typical value: 12 μ A for the receiver
 - Peak system SNR of 115 dB in 0.5-10 Hz band enables high-accuracy SpO₂ measurement
- Transmitter:
 - 8-Bit Programmable LED current with range adjustable from 25 mA to 250 mA
 - Mode to fire two LEDs in parallel with independent per-phase current control
 - Programmable LED on-time per-phase
 - Simultaneous support of 4 LEDs for SpO₂, Multi-Wavelength HRM
- Receiver:
 - Supports 3 Time-Multiplexed PD Inputs
 - 2 parallel receivers (2 sets of TIA/filter)
 - Individual ambient offset subtraction DAC at each TIA Input with 8-bit per-phase control and range adjustable up to 255- μ A
 - Individual LED offset subtraction DAC at each TIA input with 9-bit per-phase control and 64- μ A range
 - Digital ambient subtraction at ADC output
 - Noise filtering with programmable bandwidth
 - Transimpedance gain: 3.7 k Ω to 1 M Ω
- Supports external clock or internal oscillator
- Option to acquire data synchronized with a system clock
- Automatic cancellation of DC from Ambient, LED
- FIFO with 160-sample depth
- SPI™ interface/ I2C interface
- 1.9-mm × 1.8-mm DSBGA, 0.35-mm Pitch
- Supplies: Rx:1.7 - 1.9 V, Tx: 3-5.5 V

2 Applications

- Optical Heart-Rate Monitoring (HRM) for wearables, hearables
- Heart-Rate Variability (HRV)
- Pulse Oximetry (SpO₂) measurements

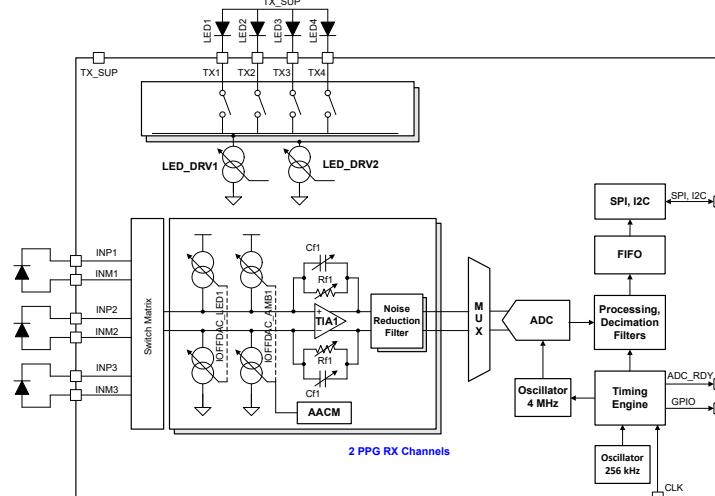
3 Description

The AFE4432 is an analog front-end for optical bio-sensing applications, such as heart-rate monitoring (HRM) and saturation of peripheral capillary oxygen (SpO₂). The device supports up to 4 switching light-emitting diodes (LEDs) and up to three photodiodes (PDs). The AFE has two LED drivers each with 8-bit current control. The device has a high dynamic range transmit-and-receive circuitry that helps with the sensing of very small signal levels. Up to 12 signal phase sets can be defined, each phase set comprising a combination of LED and Ambient phases. Low noise offset DACs at the receiver inputs can be automatically controlled to cancel DC from Ambient and LED light. The current from the PDs in each phase is converted into voltage by TIAs, filtered, and then digitized using a common ADC. The ADC code can be stored in a 160-sample FIFO block. The FIFO can be read out using a SPI or I²C interface.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
AFE4432	DSBGA (25)	1.80 mm x 1.92 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2022) to Revision A (April 2023)	Page
• Changed the PDNAFE table note for the RX_SUP current parameter in the <i>Electrical Characteristics – PPG Signal Chain</i> table.....	8
• Added table note to the frequency of internal oscillator parameter in the <i>Electrical Characteristics – Clocking</i> table.....	9
• Added parameter <i>Minimum serial clock speed</i> to the <i>Electrical Characteristics – Interface</i> table.....	10
• Changed the typical value for parameter <i>Maximum serial clock speed</i> from: 10 MHz to: 8 MHz.....	10
• Added table note to the minimum serial clock speed parameter in the <i>Electrical Characteristics – Interface</i> table.....	10
• Added parameter $t_{STECLK23}$ and table note to the <i>SPI Interface Timing</i> table.....	10
• Added parameter $t_{STECLK23}$ to <i>Figure 6-1</i>	10
• Changed <i>Figure 7-2</i>	18
• Added note on CLK_TE programming to <i>Overview - Clocking</i>	18
• Changed table note in <i>Table 7-2</i>	18
• Added table note to <i>Table 7-4</i>	18
• Changed <i>Table 7-8</i>	23
• Changed <i>Table 7-9</i>	26
• Changed <i>Figure 7-15</i>	29
• Changed the S'_0 table note in <i>Table 7-13</i>	30
• Added note for code jump stitching to <i>Maximum Ambient Rejection Mode</i>	30
• Changed <i>Figure 7-18</i>	32
• Added <i>Analog-to-Digital Converter (ADC)</i> section.....	47
• Divided <i>ADC Averaging for PPG Phase Conversions</i> section into <i>ADC Averaging for PPG Phase Conversions</i> and <i>ADC Code During Output Saturation</i>	47
• Changed <i>Dynamic Range Enhancement (DRE)</i> to <i>Dynamic Range Extension (DRE)</i> in the <i>Overview - Input DC Cancellation</i> section.....	49
• Added table note to <i>Table 7-33</i>	51
• Changed <i>Table 7-34</i>	51
• Changed <i>Figure 7-35</i>	57

• Added information to <i>Power Modes</i>	68
• Changed <i>RESET Modes</i>	68
• Added <i>Constraints When Reading Page 1 Registers Inside the Active Window</i> section.....	76
• Changed Register 3 Name information in Table 7-48	84
• Added information to the PDN_OSCL_IN_DEEP_SLEEP bit description in Table 7-59	92
• Added information to the PDNAFE bit description in Table 7-61	93
• Changed DESIGN_ID bit description in Figure 7-77 from: 0x111 to: 0x121	94
• Added Register Address 57 [Dec] <i>Register: 39h</i> [Hex] section.....	96

5 Pin Configuration and Functions

Top View

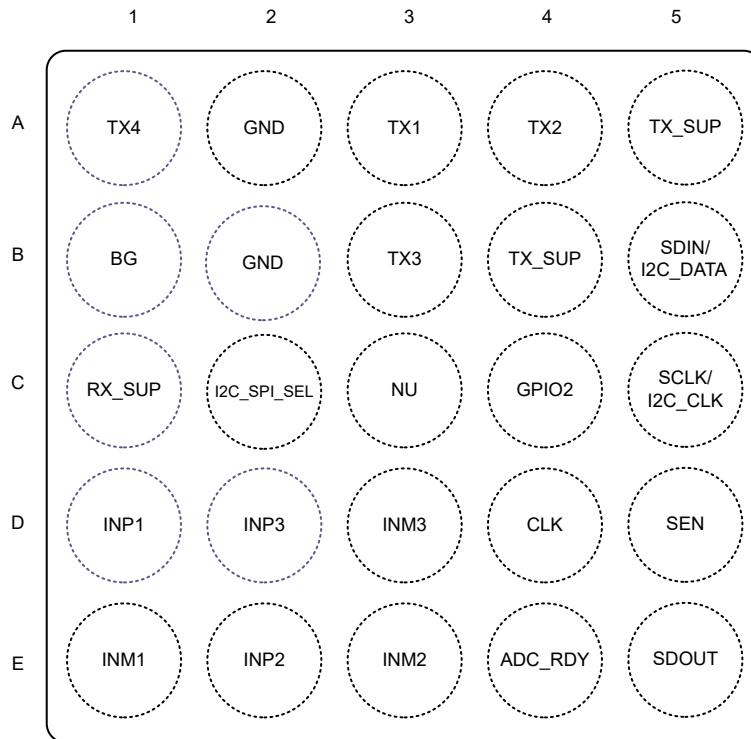


Figure 5-1. YCH Package 25-Pin DSBGA (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADC_RDY	E4	Digital	Programmable interrupt (output). Levels = 0 V to RX_SUP
BG	B1	Analog	Band-gap voltage output. Use a 1- μ F decoupling capacitor
CLK	D4	Digital	Clock input pin. Levels = 0 V to RX_SUP.
GPIO2	C4	Digital	Programmable I/O pin
GND	A2, B2	Analog	Ground. Level = 0 V.
I2C_SPI_SEL	C2	Digital	This pin enables selection between the I2C and SPI interfaces. 0 = SPI interface, 1 = I2C interface. Levels = 0 V to RX_SUP. Do not leave floating.
INM1	E1	Analog	PPG negative input 1, Connect to photodiode anode
INP1	D1	Analog	PPG positive input 1, Connect to photodiode cathode
INM2	E3	Analog	PPG negative input 2, Connect to photodiode anode
INP2	E2	Analog	PPG positive input 2, Connect to photodiode cathode
INM3	D3	Analog	PPG negative input 3, Connect to photodiode anode
INP3	D2	Analog	PPG positive input 3, Connect to photodiode cathode
NU	C3	Analog	NU (Non-usable terminal/ make no external connection)
RX_SUP	C1	Supply	Receiver supply; 1- μ F decapacitor to GND. 1.7 V to 1.9 V. Also used as the I/O supply for the Digital lines.
SCLK/I2C_CLK	C5	Digital	In I ² C mode, this pin is an I ² C clock pin. An external pullup resistor (for example, 10 k Ω) to RX_SUP is required. In SPI mode, this pin is a serial clock input. Levels = 0 V to RX_SUP.

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
SDIN/ I2C_DATA/	B5	Digital	In I ² C mode, this pin is an I ² C data pin. An external pullup resistor (for example, 10 kΩ) to RX_SUP is required. In SPI mode, this pin is a serial data input. Levels = 0 V to RX_SUP.
SDOUT	E5	Digital	In SPI mode, this pin is a serial data output. Levels = 0 V to RX_SUP.
SEN	D5	Digital	In I ² C mode, this pin inverts the LSB of the I ² C target address. In SPI mode, this pin is the chip-select pin for the SPI (active low). Levels = 0 V to RX_SUP.
TX1	A3	Analog	LED pin 1
TX2	A4	Analog	LED pin 2
TX3	B3	Analog	LED pin 3
TX4	A1	Analog	LED pin 4
TX_SUP	A5, B4	Supply	Transmitter supply; 1-µF to 10-µF decapacitor to GND. Levels = 3.0 V to 5.5 V.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT	
Supply voltage range	RX_SUP to GND	-0.3	2.1	V	
	TX_SUP to GND	-0.3	6		
Voltage applied to digital inputs		Max [-0.3, (GND – 0.3)]	Min [2.1, (RX_SUP + 0.3)]	V	
LED Duty cycle: sum of all LED phase durations as function of total period; cumulative of lifetime usage	25-mA LED current	22.4%			
	50-mA LED current	11.2%			
	100-mA LED current	5.6%			
	200-mA LED current	2.8%			
	250-mA LED current	2.2%			
Storage temperature, T _{stg}		-60	150	°C	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) If subjected to additional processing steps (for example, during PCB assembly or product manufacturing), avoid exposure of the IC to UV radiation and exposure to high temperatures (350°C and higher).

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
RX_SUP	Receiver supply	1.7	1.9	V
TX_SUP	Transmitter supply	3.0	5.5	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		WCSP (DSBGA)	UNIT
		25 BALLS	
R _{θJA}	Junction-to-ambient thermal resistance	72.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	16.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	16.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

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6.5 Electrical Characteristics – PPG Signal Chain

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, RX_SUP = 1.8 V. Default conditions (if not specified): internal clock mode, staggered mode, 100-Hz PRF, TIA $R_f = 250 \text{ k}\Omega$, $t_{LED_ON} = 117 \mu\text{s}$, 2 ADC averages, LED DC cancellation enabled, 2.5X full-scale LED current mode, 1 μF decap on BG pin, $C_{IN} = 50 \text{ pF}$ (cap across input pins to model zero bias differential capacitance of PD)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE REPETITION FREQUENCY					
f_{PRF}	Pulse repetition frequency	5	1500	SPS	
RECEIVER					
Ambient Offset DAC current range	1X range (default)	15.9375	μA		
	2X range	31.875			
	4X range	63.75			
	8X range	127.5			
	16X range	255			
Ambient Offset DAC current resolution		8	bit		
Ambient Offset DAC current step	1X range	0.0625	μA		
LED Offset DAC current range		63.875	μA		
LED Offset DAC current resolution		9	bit		
LED Offset DAC current step		0.125	μA		
TIA gain setting		3.7 k to 1M	Ω		
TIA gain accuracy		$\pm 10\%$			
CF setting		2.5 to 25	pF		
Switched RC filter bandwidth		2.5 to 77.5	kHz		
ADC averages		1,2,3,4,8			
Detector capacitance	Differential capacitance between INP, INN	10	200	200	pF
TRANSMITTER					
LED current range per driver (x2 for two drivers in parallel)	0.5X mode	0 to 25	mA		
	1X mode	0 to 50			
	2X mode	0 to 100			
	2.5X mode	0 to 125			
LED current resolution		8	Bits		
PERFORMANCE					
Full system SNR	Optical loopback test: CTR=300 nA/mA, ILED=80mA, IPD=24 μA LED DC cancellation enabled, $R_F=250\text{-k}\Omega$ PRF=1024 Hz	115 ⁽¹⁾	dB		
CURRENT CONSUMPTION FOR LOW-POWER CONTINUOUS HEART-RATE MONITORING					
RX_SUP current ⁽²⁾	Normal operation ⁽³⁾	12	μA		
	Software power-down (PDNAFE) mode ^{(4) (5)}	1	μA		
TX_SUP current	Normal operation ^{(3), (6)}	1.5	μA		
	Software power-down (PDNAFE) mode ^{(4) (6)}	1	μA		

(1) SNR measured as input referred current noise referred over the bandwidth of 0.5-10 Hz referred to IPD.

(2) All currents are average currents.

(3) Normal operation refers to operation in external clock mode with single TIA at 25 Hz PRF with 2 phases (1 AMB, 1 LED).

(4) External clock switched off.

(5) With PDN_BG_IN_DEEP_SLEEP bit set to '1' and PDN_OSCL_IN_DEEP_SLEEP bit set to '0', along with PDNAFE.

- (6) LED currents are set to 0 mA.

6.6 Electrical Characteristics – Clocking

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, RX_SUP = 1.8 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL OSCILLATOR MODE					
Frequency of internal oscillator	Internal oscillator mode		256 ⁽²⁾		kHz
Accuracy	Room temperature, without calibration		$\pm 1\%$		
Frequency drift with temperature	Full temperature range		$\pm 1\%$		
Jitter (RMS)			5		ns
CLOCK INPUT					
Input clock high level			RX_SUP		V
Input clock low level			0		V
Input capacitance of CLK pin			< 4		pF
FREE-RUNNING EXTERNAL CLOCK					
Frequency of free-running clock on CLK pin	External clock mode (CLK_MODE_EXT)		256		kHz
	Mixed clock mode (CLK_MODE_MIX)		32.768		kHz
Duty cycle on CLK pin			50		%
SINGLE-SHOT MODE					
Periodicity of pulse train on CLK pin	PPG-only acquisition mode (CLK_MODE_SS)		f_{PRF} ⁽¹⁾		Hz
High-time of pulse			30-100		μs

- (1) Periodicity of pulse train on the CLK pin should be equal to the desired PRF.
(2) Set to 128 kHz if Page 1 registers need to be read out during the Active window of the PRF cycle.

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6.7 Electrical Characteristics – Interface

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FIFO					
	FIFO Depth			160	Samples
SPI INTERFACE					
	Maximum serial clock speed			8	MHz
	Minimum serial clock speed ⁽²⁾			4	MHz
I²C INTERFACE					
	Maximum data rate			400	kHz
	I ² C target address	SEN = 0		5B	Hex
		SEN = 1		5A	Hex
t _{I²C_RISE} ⁽¹⁾	I ² C data rise time with a 10-kΩ pullup resistor with a 20-pF load from I ² C data to GND			1200	ns
t _{I²C_FALL}	Fall time (when data line is pulled down by AFE) with 20-pF from I ² C data to GND			28	ns
DIGITAL INPUTS					
V _{IH}	High-level input voltage	0.9 × RX_SUP			V
V _{IL}	Low-level input voltage	0	0.1 × RX_SUP		V
DIGITAL OUTPUTS					
V _{OH}	High-level output voltage		RX_SUP		V
V _{OL}	Low-level output voltage		0		V

(1) Maximum achievable speed of the I²C interface could be limited by this parameter if the load on the I²C lines are high.

(2) This specification is applicable only if Page 1 registers need to be read out during the Active window of the PRF cycle.

6.8 Timing Requirements - Interrupts

		MIN	TYP	MAX	UNIT
t _{DATA_RDY_RISE}	DATA_RDY rise time (10% to 90%) with a 15-pF capacitive load to ground ⁽¹⁾			12	ns
t _{DATA_RDY_FALL}	DATA_RDY fall time (90% to 10%) with a 15-pF capacitive load to ground ⁽¹⁾			12	ns

(1) The same timing applies to other interrupts as well.

6.9 SPI Interface Timing

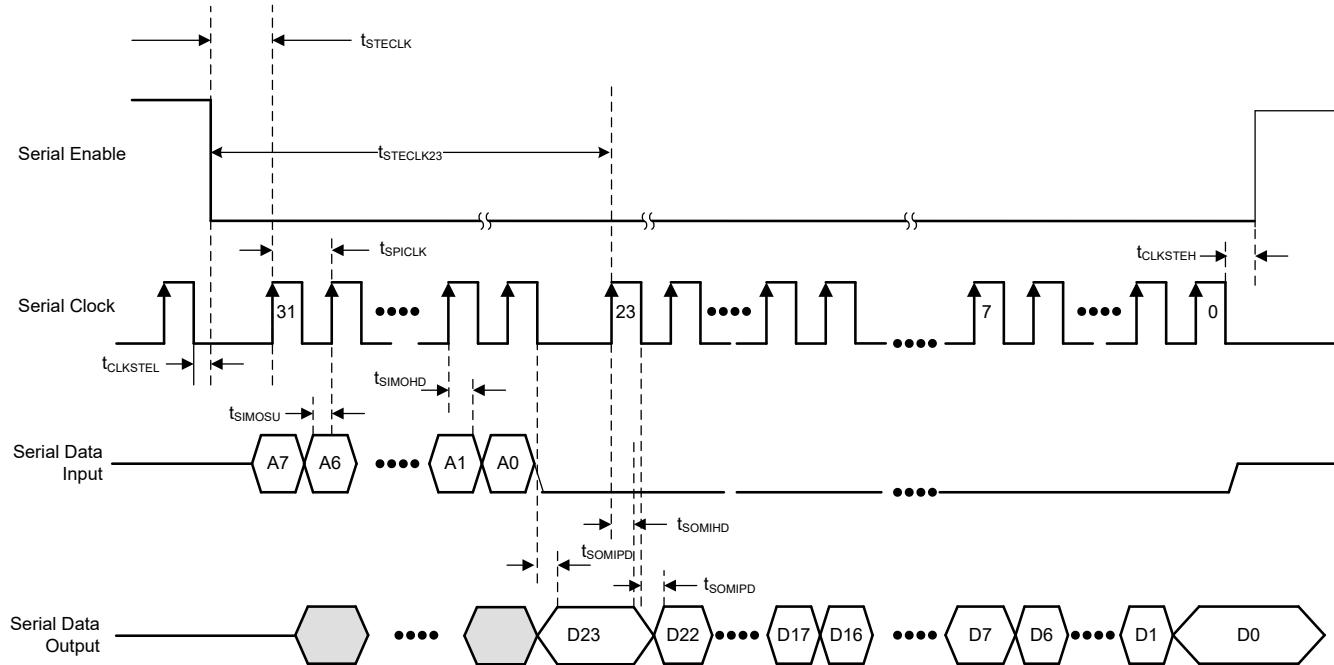
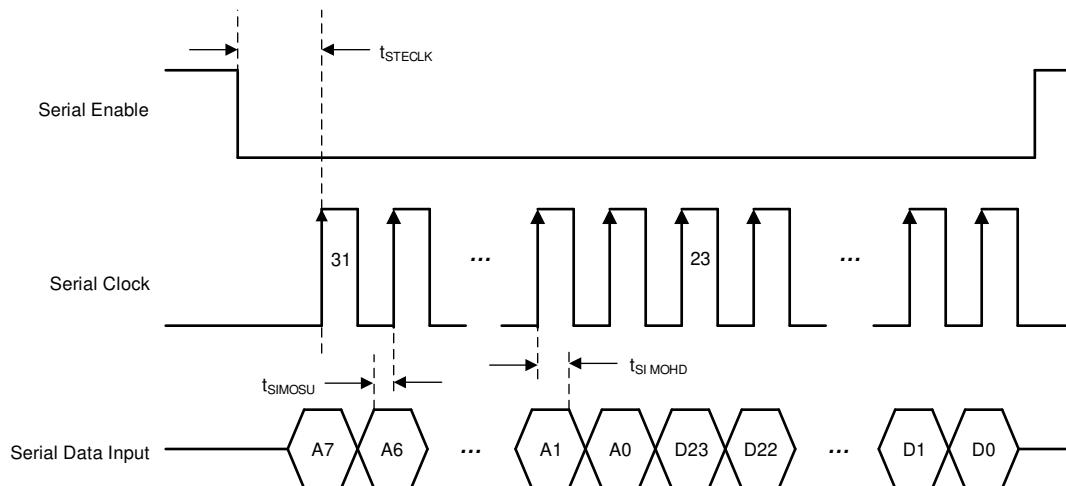
See ⁽¹⁾

		MIN	TYP	MAX	UNIT
t _{SPICLK}	Serial shift clock period	100			ns
t _{STECLK}	Serial data enable low to serial clock rising edge, setup time	15			ns
t _{CLKSTEH,L}	Serial clock transition to serial data enable high or low	15			ns
t _{PICOSU}	Serial data input to serial clock rising edge, setup time	15			ns
t _{PICOHD}	Valid serial data input after SCLK rising edge, hold time	15			ns
t _{POCIDP}	Serial clock falling edge to valid serial data output			15	ns
t _{POCIHD}	Serial clock rising edge to invalid serial data output	0.5 × t _{SPICLK}			ns
t _{STECLK23} ⁽³⁾	Time between the falling edge of Serial Enable (SEN) and the 9th rising edge of Serial clock (SCLK)			4 ⁽²⁾	μs

(1) The values in this table refer to the timings of these logic signals internal to the AFE. Additional timing margins may need to be accounted for based on the external delays and rise and fall times of these signals.

(2) See [Constraints When Reading Page 1 Registers Inside the Active Window](#)

(3) This specification is applicable only if Page 1 registers need to be read out during the Active window of the PRF cycle.

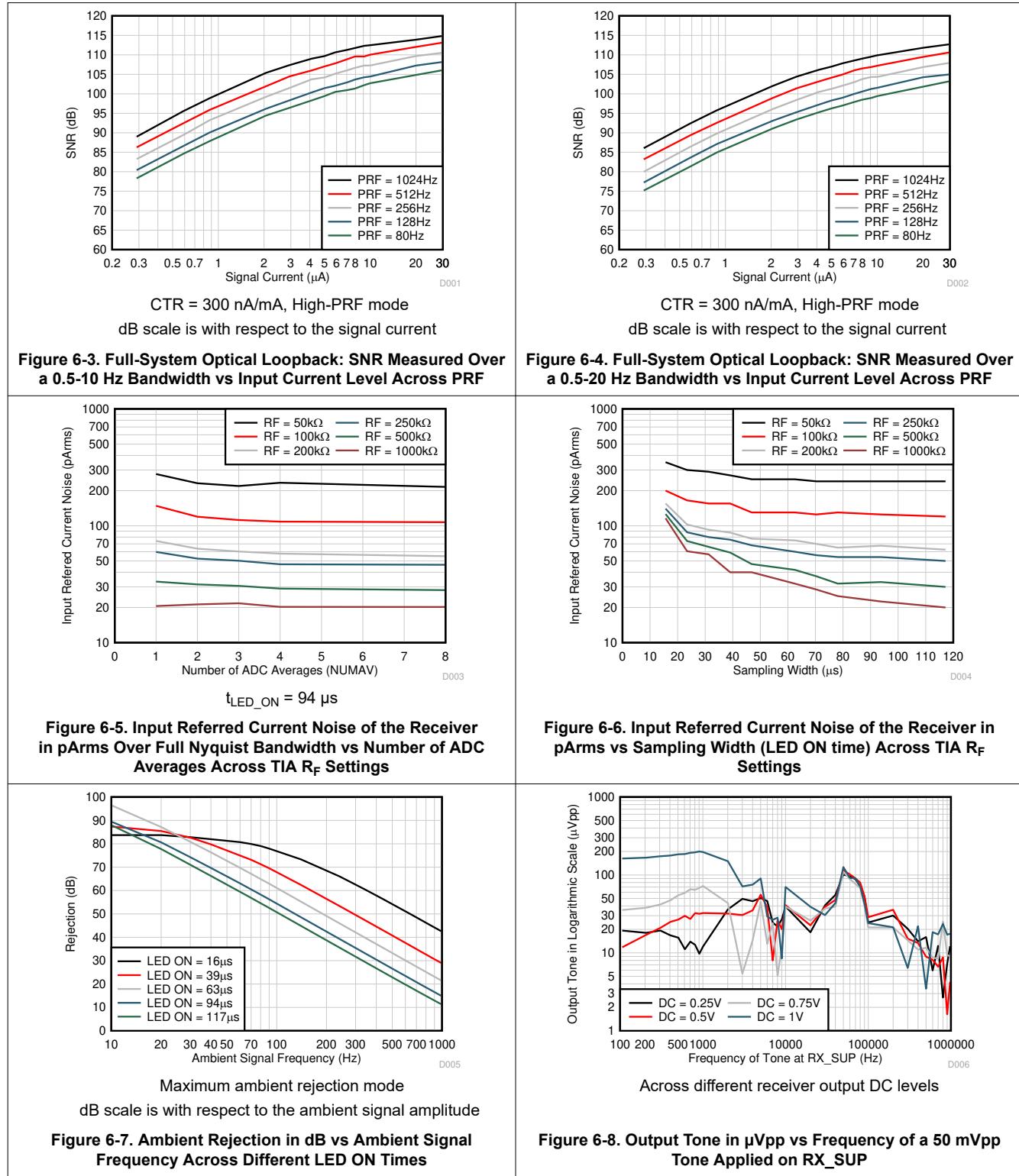
**Figure 6-1. Serial Interface Timing Diagram, Read Operation****Figure 6-2. Serial Interface Timing Diagram, Write Operation**

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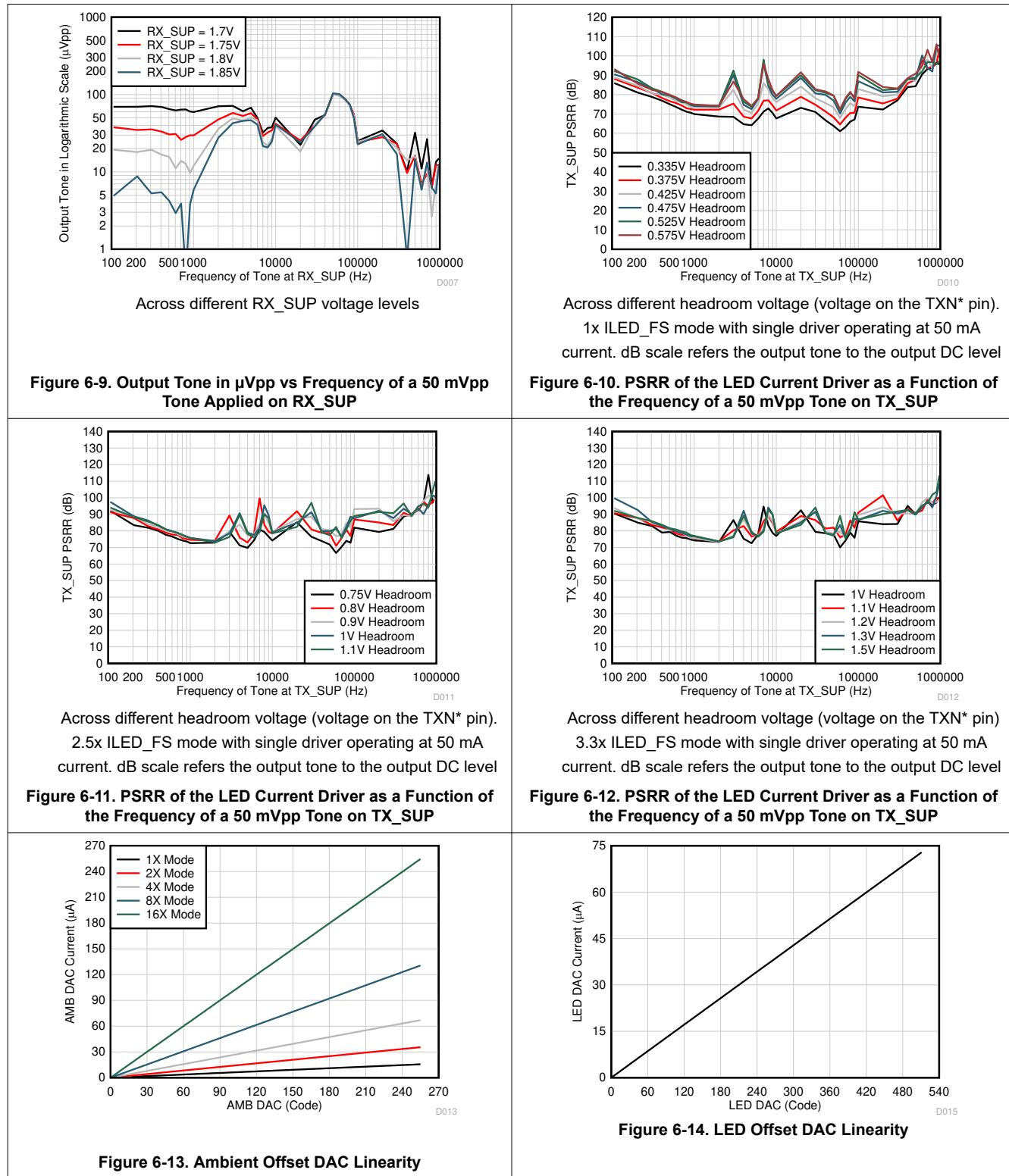
6.10 Typical Characteristics

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, RX_SUP = 1.8 V. Default conditions (if not specified): internal clock mode, staggered mode, 100-Hz PRF, TIA $R_F = 250 \text{ k}\Omega$, $t_{LED_ON} = 117 \mu\text{s}$, 2 ADC averages, LED DC cancellation enabled, 2.5X full-scale LED current mode, 1 μF decap on BG pin, $C_{IN} = 50 \text{ pF}$ (cap across input pins to model zero bias differential capacitance of PD)



6.10 Typical Characteristics (continued)

Typical specifications are at $T_A = 25^\circ\text{C}$; $\text{TX_SUP} = 5 \text{ V}$, $\text{RX_SUP} = 1.8 \text{ V}$. Default conditions (if not specified): internal clock mode, staggered mode, 100-Hz PRF, TIA $R_F = 250 \text{ k}\Omega$, $t_{\text{LED_ON}} = 117 \mu\text{s}$, 2 ADC averages, LED DC cancellation enabled, 2.5X full-scale LED current mode, 1 μF decap on BG pin, $C_{\text{IN}} = 50 \text{ pF}$ (cap across input pins to model zero bias differential capacitance of PD)



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6.10 Typical Characteristics (continued)

Typical specifications are at $T_A = 25^\circ\text{C}$; $\text{TX_SUP} = 5 \text{ V}$, $\text{RX_SUP} = 1.8 \text{ V}$. Default conditions (if not specified): internal clock mode, staggered mode, 100-Hz PRF, TIA $R_F = 250 \text{ k}\Omega$, $t_{\text{LED_ON}} = 117 \mu\text{s}$, 2 ADC averages, LED DC cancellation enabled, 2.5X full-scale LED current mode, 1 μF decap on BG pin, $C_{\text{IN}} = 50 \text{ pF}$ (cap across input pins to model zero bias differential capacitance of PD)

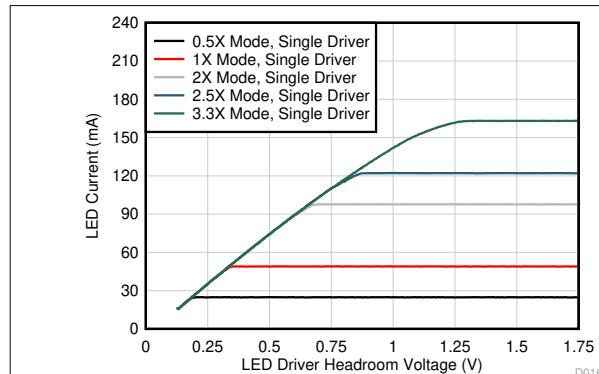


Figure 6-15. LED Current vs Voltage on TXN Pin

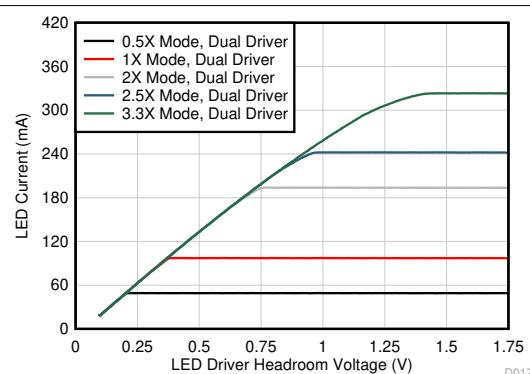


Figure 6-16. LED Current vs Voltage on TXN Pin

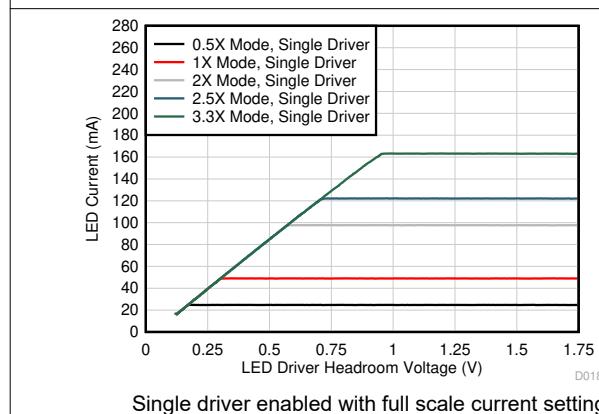


Figure 6-17. LED Current vs Voltage on TXN Pin

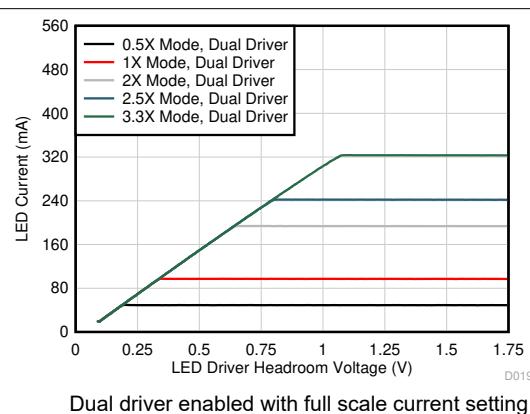


Figure 6-18. LED Current vs Voltage on TXN Pin

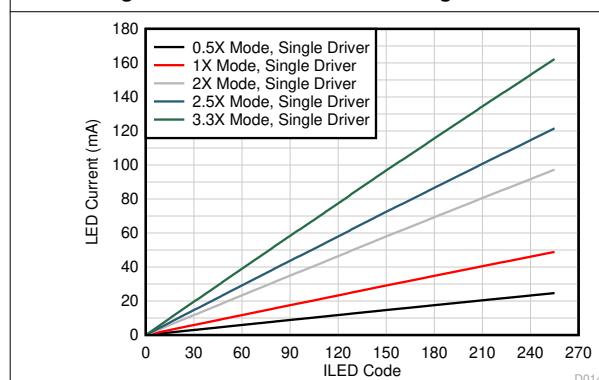


Figure 6-19. LED Current Linearity Single Driver

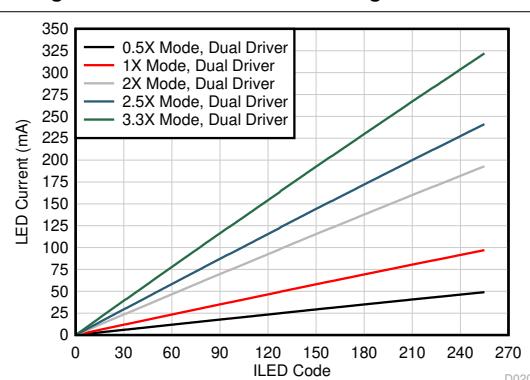


Figure 6-20. LED Current Linearity Dual Driver

6.10 Typical Characteristics (continued)

Typical specifications are at $T_A = 25^\circ\text{C}$; TX_SUP = 5 V, RX_SUP = 1.8 V. Default conditions (if not specified): internal clock mode, staggered mode, 100-Hz PRF, TIA $R_F = 250 \text{ k}\Omega$, $t_{LED_ON} = 117 \mu\text{s}$, 2 ADC averages, LED DC cancellation enabled, 2.5X full-scale LED current mode, 1 μF decap on BG pin, $C_{IN} = 50 \text{ pF}$ (cap across input pins to model zero bias differential capacitance of PD)

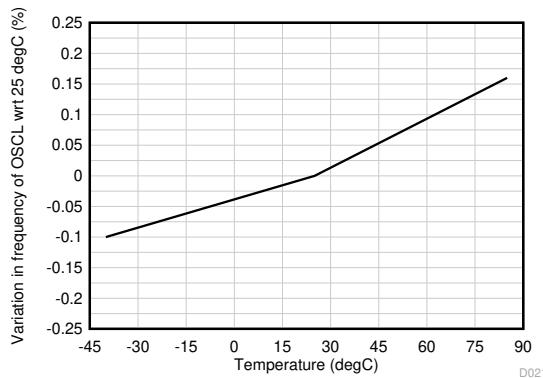


Figure 6-21. OSCL vs Temperature

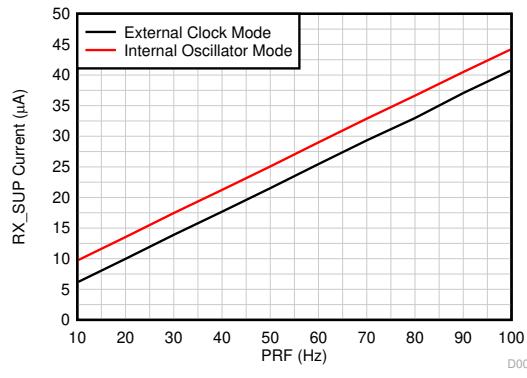


Figure 6-22. Receiver Current vs PRF External Clock/Internal Oscillator Mode
 1 Ambient phase and 1 LED phase with $t_{LED_ON} = 94 \mu\text{s}$

7 Detailed Description

7.1 Overview

The AFE4432 supports the acquisition of PPG signals. A total of three PDs and four LEDs are supported, and any combination of LED and PD can constitute a PPG signal that can be acquired by the AFE.

The clocking circuitry in the AFE is extremely flexible and supports multiple ways of clocking the device. The AFE can be clocked either by using a 32.768-kHz external clock, a train of single-shot pulses or using the 256-kHz internal oscillator.

The PPG signal chain involves a synchronized operation of a transmitter (LED driver) and a receiver (an analog front end followed by an ADC). The operation of the LEDs turning on is fully synchronized with the sampling of the signal from the photodiode by the receiver. In every cycle of a PRF (Pulse repetition frequency) cycle, up to 12 signal phase sets can be defined and the signals acquired. A signal phase set can comprise of one phase (either an LED or Ambient phase) or a set of phases (LED and the associated ambient phases). Each phase is associated with a combination of one or more LEDs (or none) turning on, and the current signal from a PD (or the sum of currents from more than one PD) getting sampled and converted. The transmitter comprises of dual LED current drivers, which can be routed in a flexible manner to any combination of four LED pins. The receiver input pins (INP^* , INM^*) are meant to be connected differentially to a photodiode. The signal current from the photodiode is converted to a differential voltage using a transimpedance amplifier (TIA). The AFE has two TIAs. One or both TIAs can be made active in each phase set, and any combination of three PDs can be connected to each active TIA in each phase set.

The *signal* in a PPG phase refers to a combination of one or more LEDs and PDs. The PPG signal chain can be configured differently in each phase. Separate current DACs at the input of the TIA can be used to cancel the DC from the Ambient and LED signals. Such input DC cancellation allows setting a much higher TIA gain than otherwise possible, resulting in the improvement of SNR. The gain of each TIA is set by the feedback resistor (R_F) and can be programmed from 3.7 k Ω to 1 M Ω (independent per-phase control for both TIAs). The transimpedance gain between the input current and output differential voltage of the TIA is equal to $2 \times R_F$. At the output of each TIA, is a programmable Noise Bandwidth reduction filter which helps to limit the bandwidth of the optical noise from the sensor. The filters get reused across multiple signal phases with a reset between phases to erase memory. The output of each filter at the end of the sampling phase is converted by an ADC. When more than one TIA is active in that phase, the ADC converts the output of the filter associated with each TIA sequentially. The ADC can also convert the output of a filter multiple times and average these multiple conversions. This ADC averaging mode reduces the contribution to noise of the ADC, but results in longer active times, and thereby higher power consumption.

The AFE has an Analog Automatic Ambient Cancellation Mode loop (Analog AACM), which can be used to suppress the input ambient in a set of phases that have a common ambient. The AFE also has eight Automatic LED DC cancellation loops, which can be used to cancel the DC at the input of the TIA from up to eight signals (LED/ PD combinations) phases. Automatic LED DC cancellation can result in glitches in the LED output whenever the loop updates the LED Offset DAC. A Dynamic range extension (DRE) mode can be configured to remove these glitches.

The acquisition rate of each PPG phase can be controlled using phase masking. Additionally, the output data rate can be controlled using the PPG decimation. The AFE also has PPG threshold detection modes, which an interrupt can be generated based on the signal level of one PPG phase or a combination of PPG phases.

A 160-sample FIFO is used to store samples from each PPG phase across multiple PRF cycles. Data from adjacent PPG phases (for example, LED minus ambient) can be combined using FIFO data controls. An output pin can be configured to serve as a FIFO_RDY interrupt, which indicates when the FIFO has been filled up to a programmed watermark level. Several other useful interrupts can also be configured to come out on the output pins. The programming of the AFE registers and the readout of the FIFO can be done using either SPI or I²C interface (selectable using the I²C_SPI_SEL pin).

In addition to the PPG signal acquisition mode, the AFE can also be made to operate in a software power-down mode controlled by a register bit. The device can be reset by setting the (self-clearing) SW_RESET bit to '1'.

7.2 Functional Block Diagram

Figure 7-1 shows a functional block diagram of the AFE.

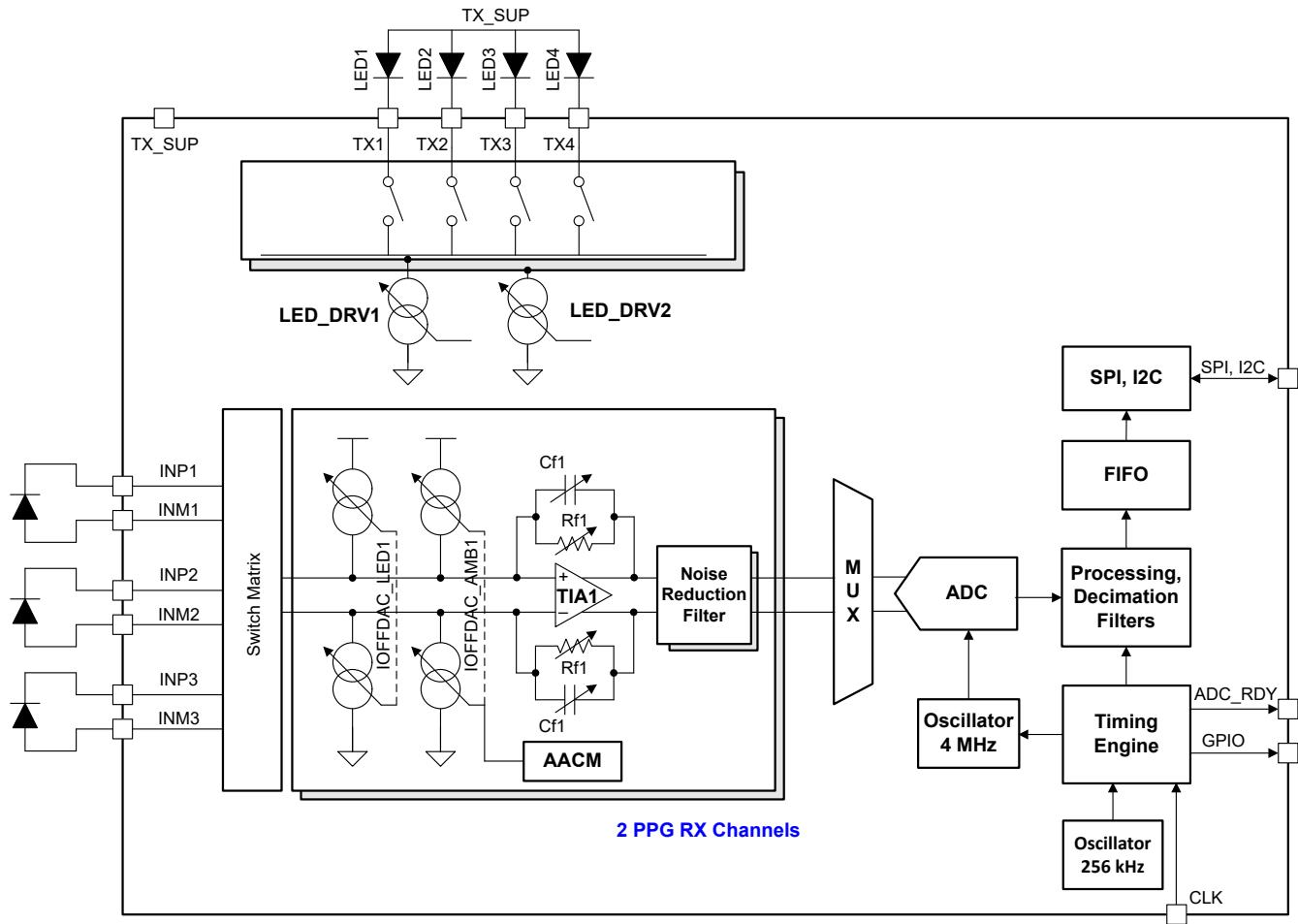


Figure 7-1. Functional Block diagram

7.3 Feature Description

7.3.1 Clocking

7.3.1.1 Overview - Clocking

There are different ways to clock the AFE as listed in Table 7-1. Each clock mode signifies a way of clocking the device either with or without an external clock.

Table 7-1. Clocking Modes

CLOCKING MODE NOTATION ⁽¹⁾	CLOCKING MODE DESCRIPTION
CLK_MODE_INT	Internal oscillator mode
CLK_MODE_EXT	External clock mode
CLK_MODE_SS	Single-shot clocking mode
CLK_MODE_MIX	Mixed clock mode

(1) These names do not represent register bits.

Figure 7-2 shows an overview of the complete clocking circuit.

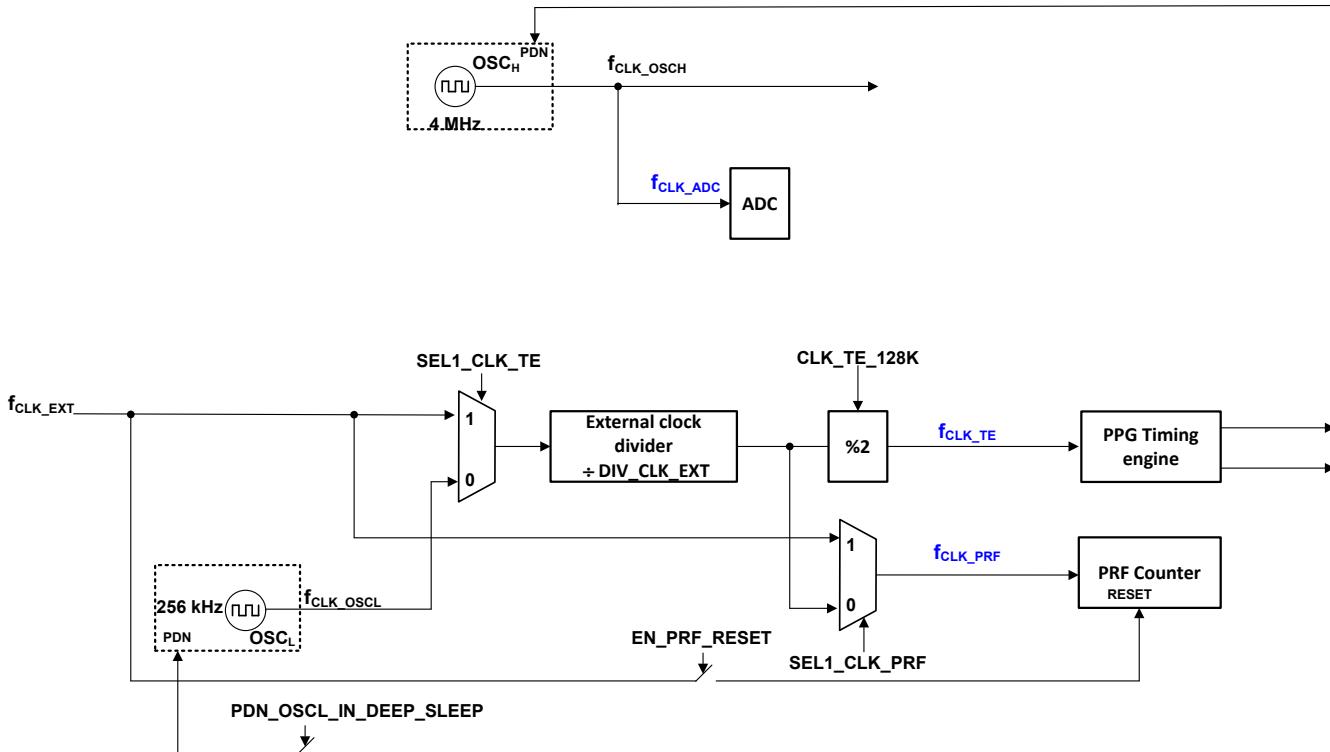


Figure 7-2. Overview of the Clocking Circuit

The clocking circuit has two oscillators:

- OSC_H: generates a 4.194 MHz clock. To configure OSC_H to generate the 4.194 MHz clock and for the blocks to use this clock appropriately, set the SET_OSCH_4M_1, SET_OSCH_4M_2 and SET_OSCH_4M_3 register bits always to '1'.
- OSC_L: generates a 256 kHz clock.

Table 7-2 shows the generation of various internal clocks across clocking modes.

Table 7-2. Generation of Internal Clocks Across Clocking Modes

CLOCKING MODE	WAVEFORM ON CLK PIN	VALUE OF f_{CLK_EXT}	BELOW CLOCKS DERIVED FROM		
			f_{CLK_TE}	f_{CLK_PRF}	f_{CLK_ADC}
CLK_MODE_INT			f_{CLK_OSCL}	f_{CLK_OSCL}	f_{CLK_OSCH}
CLK_MODE_EXT	Free running clock	256 kHz	f_{CLK_EXT}	f_{CLK_EXT}	f_{CLK_OSCH}
CLK_MODE_SS	Periodic pulse train		f_{CLK_OSCL}	Pulse train ⁽¹⁾	f_{CLK_OSCH}
CLK_MODE_MIX	Free running clock	32.768 kHz	f_{CLK_OSCL}	f_{CLK_EXT}	f_{CLK_OSCH}

(1) PRF starts by setting a high-going pulse on CLK_EXT. See [Figure 7-4](#).

OSC_H is used in all the clocking modes whereas OSC_L is not used in the external clock mode. Additionally, both OSC_L and OSC_H can be dynamically shut down to save power. The dynamic shutdown is controlled by signals generated by the PPG timing engine. OSC_L is trimmed to an accuracy of $\pm 1\%$.

The AFE timing operation involves a periodic generation of various timing control signals using a timing engine. The periodicity of the signal generation is referred to as the PRF or pulse repetition frequency. The AFE has two state machines that determine the periodicity of the timing signals as well as the generation of the signals:

1. A PRF state machine that gets reset either by a PRF counter reaching a programmed count or by a pulse on the external CLK pin. The PRF counter is enabled by setting the PRF_COUNTER_ENABLE register bit to '1'.
2. A timing engine state machine that generates the various timing control signals (for example, the LED ON and ADC Conversion signals of each phase) at the periodicity determined by the PRF state machine. The timing engine is enabled by setting the TIMER_ENABLE register bit to '1'. Setting the TM_COUNT_RST optionally keeps the timing engine in a reset state.

The time period of the timing engine clock CLK_TE ($t_{TE} = 1/f_{CLK_TE}$) determines the time resolution to which the timing signals can be programmed. CLK_PRF refers to the clock on which the PRF counter counts. f_{CLK_PRF} refers to the frequency.

Note

By default, the CLK_TE is a 256 kHz clock. Setting the bit CLK_TE_128K to '1' enables a 2% clock division and sets the CLK_TE to 128 kHz. As a result, the resolution of the timing engine signals changes from approximately 3.9 μs to 7.8 μs . TI recommends to set the CLK_TE_128K bit to '1' only if the Page 1 registers are required to be read out during the active window of the PRF cycle. See [Constraints When Reading Page 1 Registers Inside the Active Window](#) for more details.

The parameters associated with the clocking are controlled as shown in [Table 7-3](#).

Table 7-3. Parameter Values Associated with the Different Clocking Modes

CONFIG PARAMETER	DESCRIPTION	SET FOR CLOCKING MODE			
		CLK_MODE_INT	CLK_MODE_EXT	CLK_MODE_SS	CLK_MODE_MIX
SEL1_CLK_TE	Selection Control 1 for CLK_TE		1		
OSCL_DIS	Powers down 256 kHz oscillator		1		
PDN_OSCL_IN_DEEP_SLEEP	Enables dynamic power-down of OSCL			1	1
EN_PRF_RESET	Resets PRF counter with pulse on CLK pin			1	
SEL1_CLK_PRF	Selection Control 1 for CLK_PRF				1
EN_INT_IN_SINGLE_SHOT	Enables interrupt generation in CLK_MODE_SS			1	
SPLIT_CLK_FOR_TE_PRF	Splits the clocking for the Timing engine and PRF counter			1	1
EN_CLK_MODE_MIX	Additional control to enable CLK_MODE_MIX				1

Table 7-3. Parameter Values Associated with the Different Clocking Modes (continued)

CONFIG PARAMETER	DESCRIPTION	SET FOR CLOCKING MODE			
		CLK_MODE_INT	CLK_MODE_EXT	CLK_MODE_SS	CLK_MODE_MIX
SET_OSCH_4M_1	Configure OSCH to output approximately 4 MHz clock and for the blocks to use this clock	1	1	1	1
SET_OSCH_4M_2		1	1	1	1
SET_OSCH_4M_3		1	1	1	1

The parameters associated with the clock divider are controlled as listed in [Table 7-4](#).

Table 7-4. Register Controls for the Clock Dividers

DIVIDER	PARAMETER (P)	PARAMETER VALUES	RELATION
External clock divider	DIV_CLK_EXT	1,2,4,8,16,32	P=2 ^R (1)

(1) Where R represents the decimal value of the register

7.3.1.2 External Clock Mode (CLK_MODE_EXT)

The timing scheme in CLK_MODE_EXT is shown in [Figure 7-3](#). The PRF is determined by a register called PRPCT. The counter counts from 0 to (PRPCT-1) and defines a PRF cycle. The ACTIVE and DEEP SLEEP windows are automatically generated by the timing engine. Within ACTIVE, up to 12 signal phase sets can be defined and automatically generated by the phase timing engine.

A 256 kHz external clock can be used to clock the device, and the clocks for the timing engine and PRF counter are derived from this external clock. The internal oscillator is not used and can be shut down using the OSCL_DIS register bit. An external clock of higher frequency (a binary multiple of 256 kHz) can be used by setting DIV_CLK_EXT such that the divided clock frequency is approximately 256 kHz.

**Figure 7-3. Overview of Timing in the External Clock Mode and Internal Oscillator Mode**

7.3.1.3 Internal Oscillator Mode (CLK_MODE_INT)

The timing engine based clocking in the internal oscillator mode works similar to the external clock mode. The 256 kHz clock needed for CLK_PRF and CLK_TE are generated internally using the 256 kHz oscillator (OSCL).

7.3.1.4 Single Shot Clock Mode (CLK_MODE_SS)

While operating in the single-shot clocking mode, a high-going pulse (of width between 30 μ s and 100 μ s) input on the CLK pin resets the timing engine and the PRF counter and triggers the start of a new cycle of signal acquisition. In this mode, the timing engine and the PRF counter run off the internal oscillator. While enabling the single-shot acquisition mode, set the PDN_OSC_IN_DEEP_SLEEP bit to '1'. Setting this bit automatically shuts down the 256 kHz oscillator and freezes the timing engine as soon as the timing engine enters the deep sleep window (after all the active phases are completed). As a result, the timing engine stays in a frozen state until the next high-going pulse on the CLK pin, which wakes up the 256 kHz oscillator again, resets the timing engine and results in a fresh cycle of signal acquisition. Additionally, set the PRPCT count to greater than the count where the deep sleep window starts. This window start provides that the PRF counter does not get reset because of the count reaching (PRPCT-1); such an occurrence can cause a fresh set of signal acquisition.

Setting the EN_INT_IN_SINGLE_SHOT parameter enables the generation of the INT_OUT2 interrupt. The start and end counts for these interrupts are based on the 256 kHz oscillator and the interrupt needs to be positioned to start and finish before the deep sleep window starts.

While the single-shot clocking mode enables *on-demand* signal acquisition by issuing a trigger pulse on CLK pin, there can be loss of signal accuracy if the trigger pulses are spaced very far apart. Such a loss of signal accuracy can occur due to slow leakages of internal nodes of the receiver signal chain. One way to overcome such a loss of signal accuracy can be to follow the first trigger pulse with a second one after the first set of signal acquisitions are completed. The signal accuracy of the second set of signal acquisition is expected to be better than the first set.

Providing a periodic pulse train on the CLK pin with a periodicity of f_{PRF} in the single-shot clocking mode results in a uniform sampling signal acquisition at a rate equal to f_{PRF} . The single-shot clocking mode is also useful when required to synchronize the data acquisition from the AFE to a common time reference for the entire system.

The timing scheme of the single-shot clocking mode is shown in [Figure 7-4](#).

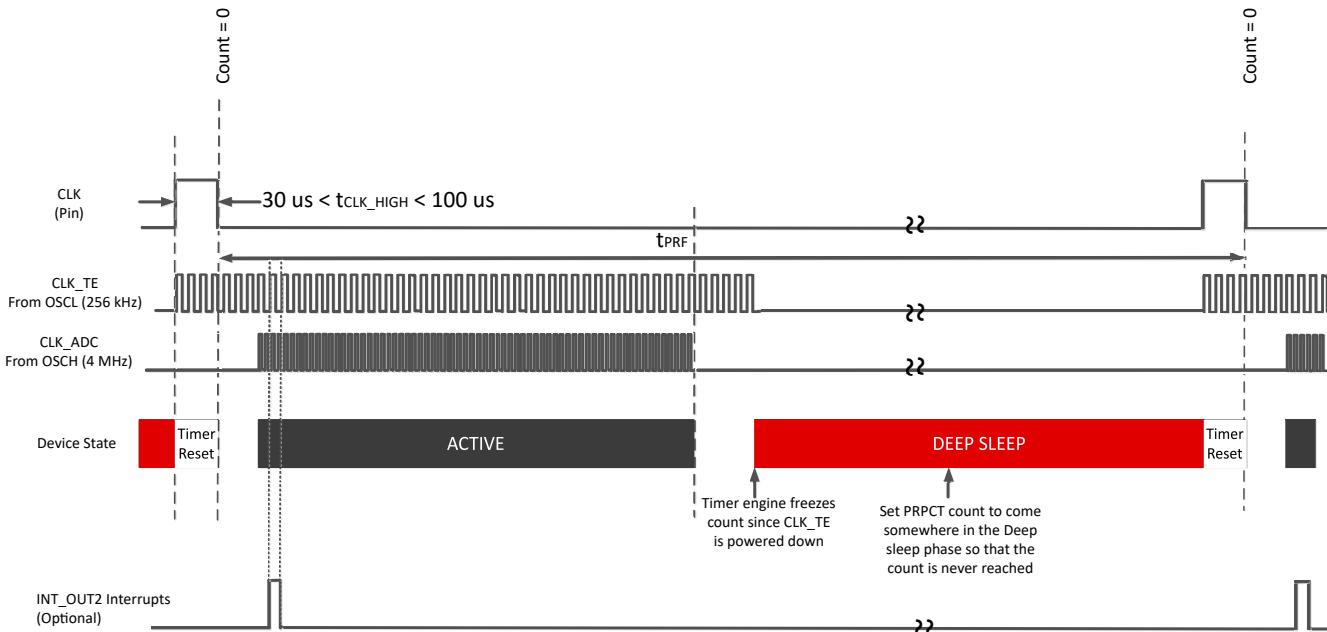


Figure 7-4. Timing Scheme in the Single-Shot Mode

7.3.1.5 Mixed Clock Mode (CLK_MODE_MIX)

In the mixed clock mode, a free-running clock on the CLK pin is used to generate the PRF count as shown in [Figure 7-5](#). The timing engine however runs off the 256-kHz internal oscillator.

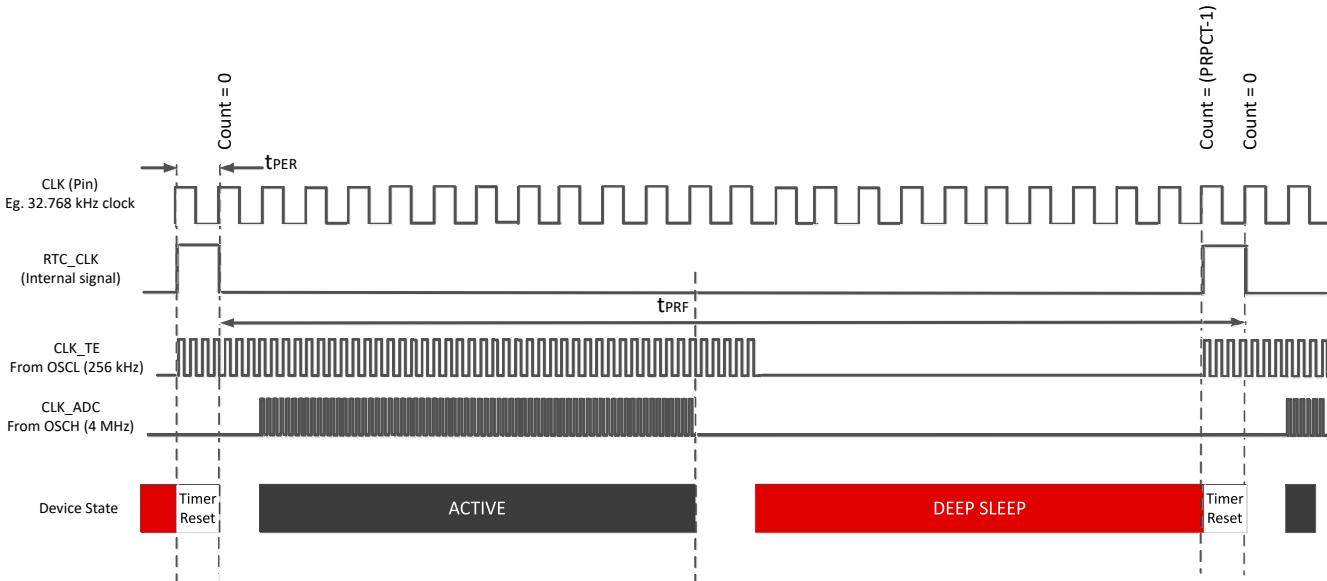


Figure 7-5. Overview of Timing in the Mixed Clock Mode

By default, the PRF counter counts from 0 to (PRPCT-1) in increments of 1 while operating in the mixed clock mode. The increment of the PRF counter can be set to a parameter STEP_COUNT programmable between 1 and 128. The parameter STEP_COUNT is derived from the register REG_STEP_COUNT as (REG_STEP_COUNT + 1).

The method of setting a 25 Hz PRF for different clocking modes is shown in [Table 7-5](#).

Table 7-5. Mechanism of Setting 25-Hz PRF Across Different Clocking Modes

CLOCKING MODE	WAVEFORM ON CLK PIN	MECHANISM OF SETTING 25-Hz PRF
CLK_MODE_EXT	256-kHz clock	PRPCT=10240 (Decimal)
CLK_MODE_INT		PRPCT=10240 (Decimal)
CLK_MODE_SS	Pulse train with periodicity of 25 Hz	Periodicity of the pulse train
CLK_MODE_MIX	32.768-kHz clock	PRPCT = 32768 (Decimal) REG_STEP_COUNT=24 (Decimal)

7.3.2 Signal Acquisition

7.3.2.1 Power-Cycling

When operating at low PRFs, the device can be put into a deep sleep state between PRF cycles. As shown in Figure 7-6, the device enters the deep sleep state after the completion of the active window. During the active window, the PPG signal acquisition happens in well-defined PPG Phase windows.

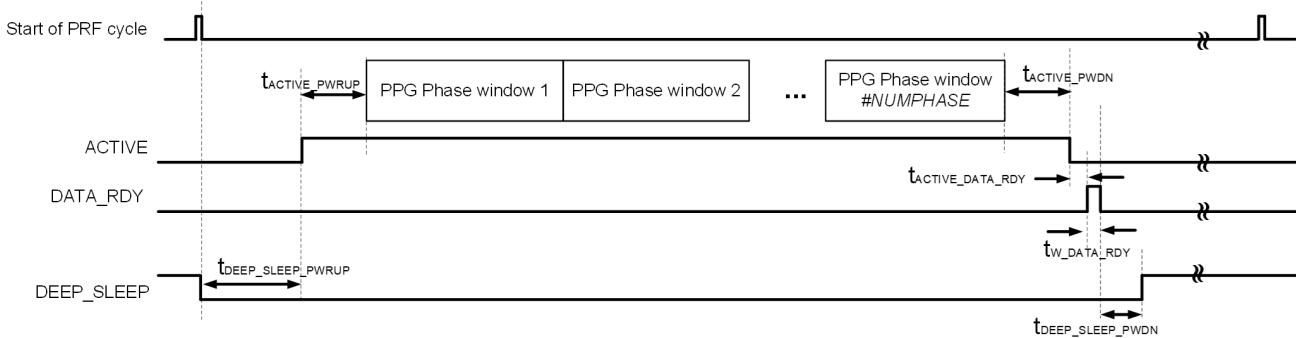


Figure 7-6. Power Cycling Within a PRF Cycle

The register control for setting the timing parameters shown in Figure 7-6 are listed in Table 7-6.

Table 7-6. Timing Parameters Associated with the Various Timing Windows (1)

PARAMETER	DESCRIPTION	SET USING REGISTER	MIN	DEFAULT(2)	UNIT
$t_{DEEP_SLEEP_PWRUP}$	Start of PRF cycle to start of Active phase	$(REG_TDEEP_SLEEP_PWRUP + 4.5) \times t_{TE}$	295	$75.5 \times t_{TE}$	μs
t_{ACTIVE_PWRUP}	Start of Active window to start of 1st PPG phase	$(REG_TACTIVE_PWRUP + 1) \times t_{TE}$	98	$25 \times t_{TE}$	μs
t_{ACTIVE_PWDN}	End of last PPG phase to end of Active window	$(REG_TACTIVE_PWDN + 2) \times t_{TE}$	Max (3 $\times t_{TE}$, 12)	$3 \times t_{TE}$	μs
$t_{ACTIVE_DATA_RDY}$	End of Active window to start of DATA_RDY pulse	$(REG_TACTIVE_DATA_RDY + 1) \times t_{TE}$	Max (4 $\times t_{TE}$, 16)	$4 \times t_{TE}$	μs
$t_{W_DATA_RDY}$	Width of DATA_RDY	$(REG_TW_DATA_RDY + 1) \times t_{TE}$	$1 \times t_{TE}$	$1 \times t_{TE}$	μs
$t_{DEEP_SLEEP_PWDN}$	DATA_RDY fall to start of Deep Sleep window	$(REG_TDEEP_SLEEP_PWDN + 1) \times t_{TE}$	$6 \times t_{TE}$	$6 \times t_{TE}$	μs
t_{SEP}	Separation between successive windows	$REG_TSEP \times t_{TE}$	0	$0 \times t_{TE}$	μs

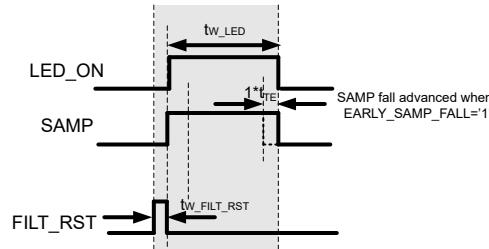
(1) Throughout this table, t_{TE} refers to one clock period of the 256 kHz clock (clock period rounded off to 4 μs).

(2) The default values (on reset) of the registers are in terms of number of timing engine clocks.

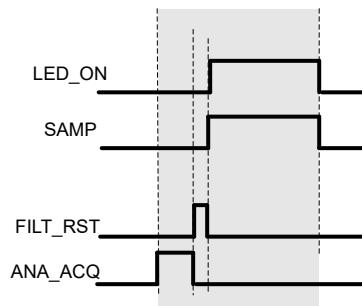
7.3.2.2 Sampling and Convert Windows

The synchronized operation of the PPG transmitter and receiver involves simultaneous firing of the LED on the transmitter side, and sampling of the TIA output by the noise reduction filter. These signals are denoted by LED_ON and SAMP respectively. The filter outputs are then converted by the ADC, with the ADC conversion signal denoted by CONV.

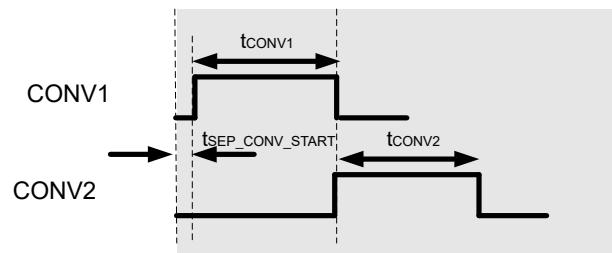
Figure 7-7 shows the timing of the sampling window. The window starts with a filter reset phase (FILT_RST) where the filter set being used during that window for sampling one or more of the TIA outputs is reset for a duration of 1 timing engine clock before use. One or more of the chosen LEDs turn on during the LED_ON signal and the filters sample the TIA outputs during the SAMP signal. The LED ON time can be programmed using a per-phase register parameter t_{W_LED} . The SAMP signal starts and ends coincident with the LED_ON signal. The falling edge of SAMP can be advanced by 1 timing engine clock with respect to the falling edge of the LED_ON signal by setting a global register control called EARLY_SAMP_FALL.

**Figure 7-7. Composition of a Sampling Window**

The timing of the sampling window is altered when the baseline of an automatic ambient cancellation loop is updated in that phase set. Automatic ambient cancellation can be enabled for a phase-set using per-phase register bit USE_ANA_AACM. If additionally, the UPDATE_BASELINE_AMB is set to 1 for the phase-set, then a short ambient acquisition window (ANA_ACQ) is automatically generated as shown in [Figure 7-8](#). The ANA_ACQ window insertion is only done for the first phase of the phase-set when the UPDATE_BASELINE_AMB bit is set to '1'. At the end of the ANA_ACQ window, the Ambient Offset DAC is updated based on the ambient value newly acquired by the Analog AACM loop. The USE_ANA_AACM and UPDATE_BASELINE_AMB controls are common for each active TIA in that phase.

**Figure 7-8. Sampling Window for a Phase Where the ANA_ACQ Window is Inserted**

Depending on the number of active TIAs that need to be converted, a convert window can contain either one or multiple CONV signals. Each CONV signal is associated with the output of one converted sample by the ADC. The timing of the convert window comprising 2 CONV signals is shown in [Figure 7-9](#). The width of the CONV signal is determined by the NUMAV parameter (number of ADC averages) used for that phase.

**Figure 7-9. Composition of a Convert Window with 2 CONV Signals**

The register controls that determine timings in the sampling signal window are listed in [Table 7-7](#).

Table 7-7. Timing Parameters Associated with the Sampling Signal Window

PARAMETER	CONTROL	DESCRIPTION	SET AS	DEFAULT	UNIT
t_{W_LED}	Per-phase	Width of LED ON signal	$(REG_TWLED + 1) \times t_{TE}$		μs
$t_{W_FILT_RST}$	N/A	Filter reset window	$1 \times t_{TE}$	$1 \times t_{TE}$	μs
t_{SAMP_SEP}	Global	Separation between sampling phases in Maximum Ambient Rejection mode	$REG_TSEP_SAMP \times t_{TE}$	$1 \times t_{TE}$	μs

The register controls that determine timings in the convert window are listed in [Table 7-8](#).

Table 7-8. Timing Parameters Associated with the Convert Window

PARAMETER	CONTROL	DESCRIPTION	SET AS	DEFAULT	UNIT
$t_{SEP_CONV_START}$	Global	Start of Convert window to start of the first CONV signal	$REG_TSEP_CONV_START \times t_{TE}$	$1 \times t_{TE}$	μs
t_{CONV}	Per-phase	Width of each CONV signal in terms of number of t_{TE} , 256 kHz clock for timing engine (t_{TE} is approximately 4 μs)	$\{(REG_NUMAV + 1) \times 10.9 + 5\} \times t_{TE}$ ⁽¹⁾		μs

(1) Rounded off to the nearest integer number of timing engine clocks indicated by the formula.

7.3.2.3 Auto-Insertion of Ambient

The general timing framework of the phases of a phase window is shown in [Figure 7-10](#).

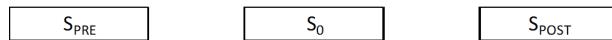


Figure 7-10. General Timing Framework of a PPG Phase Window

S_0 corresponds to the sampling window of the phase-set explicitly defined by the per-phase register. S_0 can either correspond to an LED signal or an explicitly defined ambient signal. If S_0 is an LED signal, then S_{PRE} and S_{POST} refer to sampling signal windows of optional ambient phases that can be specified to be automatically inserted in that phase-set. S_{PRE} is referred to as the pre-ambient and S_{POST} as the post-ambient. The automatic insertion of the pre-ambient (S_{PRE}) and post-ambient (S_{POST}) in a given phase window is specified by the AUTO_AMB_INSERT (per-phase) parameter as shown in [Table 7-9](#). S_0 corresponds to the defined phase which is the LED phase. Auto-inserted ambient phases inherit all settings from the per-phase settings for the S_0 signal with the only exception that their LED driver currents are set to 0. In addition to being derived as one of the auto-inserted ambient phases in a phase window, an ambient phase can also be defined explicitly as a phase, by setting AUTO_AMB_INSERT to '0' for the phase and setting the LED currents to 0.

Table 7-9. Insertion of Pre-Ambient, Post-Ambient Based on AUTO_AMB_INSERT Control

AUTO-AMBIENT THAT IS INSERTED	AUTO_AMB_INSERT ⁽¹⁾	PHASES CREATED IN THE PPG PHASE WINDOW			USABLE IN PHASE TIMING SCHEMES		
		S_{PRE}	S_0	S_{POST}	STAGGERED	HIGH PRF	HIGH AMBIENT REJECTION
None	0		Supported		Supported	Supported	
Only Pre-ambient	1	Supported	Supported		Supported	Supported	Supported ⁽²⁾
Pre- & Post-ambient	2	Supported	Supported	Supported	Supported		Supported ⁽³⁾
Only Post-ambient	3		Supported	Supported	Supported		

(1) Applicable in the Staggered mode and High PRF mode.

(2) Scheme to insert only pre-ambient is set using DIS_POST_AMB_MAX_AMB_REJ=1. The AUTO_AMB_INSERT parameter is ignored.

(3) Scheme to insert both pre-ambient and post-ambient is set using MAX_AMB_REJ=1. The AUTO_AMB_INSERT parameter is ignored.

7.3.2.4 Phase Timing Schemes

The acquisition of PPG signals happens in a well-defined **PPG phase window** which comprises a set of SAMP and CONV signals. A PPG phase window contains a set of PPG phases, referred to as a **PPG phase set**. A PPG phase set can comprise of either a single phase, or can comprise of a main defined phase (expected to be the LED phase) and one or more automatically inserted ambient phases. Each phase in a phase set can produce up to 2 signals, corresponding to the output from up to 2 parallel TIAs. The number of active phase sets is set by a parameter called NUMPHASE. The register control REG_NUMPHASE (programmable from 0 to 11) determines NUMPHASE as (REG_NUMPHASE+1). The signal chain parameters in each PPG phase set is defined by a set of 5 **per-phase PPG registers**. There are a total of 12 such sets of per-phase PPG registers.

Each PPG phase window contains the LED_ON, SAMP and CONV signals required for all the PPG phases of that PPG phase set. Both TIA outputs are sampled simultaneously (using the common SAMP signal). However, since the output signals of the 2 TIAs are converted sequentially by a common ADC, there can be up to 2 convert signals within the CONV window associated with each sampling. The number of convert signals depends on the per-phase parameter NUM_TIA set as (REG_NUM_TIA+1). Additionally, set the global parameter NUM_TIA_MAX equal to the maximum number of TIAs active across all phases (NUM_TIA_MAX=REG_NUM_TIA_MAX+1). For example, if NUM_TIA_MAX is set to 1, then TIA2 is kept in a permanently power-down state.

There are three phase timing schemes which differ in the positioning of these signals both within a PPG phase set as well as across adjacent phase sets. The three phase timing schemes are Staggered mode, High PRF mode, and Maximum Ambient Rejection mode. [Figure 7-3](#) gives an overview of the phase windows for the three phase timing schemes. Each CONV window shown in the figures can contain up to 2 ADC conversions.

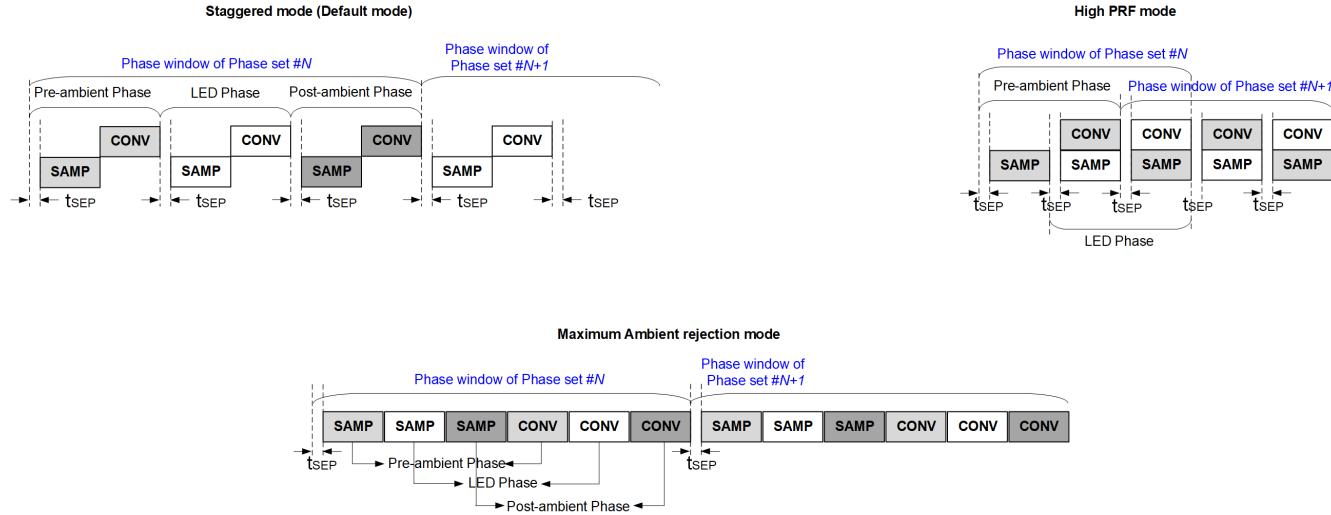


Figure 7-11. Phase Windows for the Three Phase Timing Schemes

7.3.2.4.1 Staggered Mode

Figure 7-12 shows the phase window timing in the staggered timing mode for a generic case involving a pre-ambient, LED, and post-ambient phase. There is no overlap between the SAMP and CONV signals of one phase and the next phase. The 2 convert signals (C1..C2) correspond to the ADC conversions of the 2 TIAs.

S _{PRE}			S ₀				S _{POST}		
	C1 _{PRE}	C2 _{PRE}		C1 ₀	C2 ₀		C1 _{POST}	C2 _{POST}	

Figure 7-12. Timing Within a Phase Window in the Staggered Mode

Automatic LED DC cancellation can be enabled for a phase by setting the per-phase bits (separate bit associated with each of the 2 TIAs) LED_DC_EN_TIA1..LED_DC_EN_TIA2. There are up to 8 LED DC cancellation loops available, and the loops get sequentially assigned to the corresponding signals in order of the phase number and TIAs for which the LED DC cancellation loop is enabled in that phase.

Additionally, a Dynamic Range Extension (DRE) mode can be set for a phase using the ENABLE_DRE bit. If this bit is set to 1, then the DRE mode gets applied on all the LED DC cancellation loops that are enabled in that phase. An on-demand LED phase (S'0) is generated as shown in Figure 7-13

S _{PRE}			S ₀			S'0			S _{POST}		
	C1 _{PRE}	C2 _{PRE}		C1 ₀	C2 ₀		C1' ₀	C2' ₀		C1 _{POST}	C2 _{POST}

Figure 7-13. Insertion of the On-Demand LED Phase (S'0) When ENABLE_DRE = 1

A per-phase FIFO_DATA_CTRL parameter determines the manner in which one or more FIFO data associated with the phase is generated. The FIFO_DATA_CTRL settings are listed in Table 7-10. In this table, S₋₁ corresponds to the signal sampled just prior to S₀, and can correspond to either an auto-inserted ambient phase or an explicitly defined previous phase. Similarly, S₁ corresponds to the signal sampled just after S₀ (in the case where ENABLE_DRE = 0) or just after S'0 (in the case where ENABLE_DRE=1) and could correspond to either an auto-inserted ambient phase or an explicitly defined next phase.

Table 7-10. FIFO_DATA_CTRL Settings

FIFO_DATA_CTRL	CONDITION	ENABLE_DRE = 0	ENABLE_DRE = 1
0		No data	No data
1		S ₀	DRE_S ₀ ⁽¹⁾
2	Phase set has a pre-ambient phase	S ₀ -S ₋₁	DRE_S ₀ -S ₋₁
	Phase set does not have a pre-ambient phase		Do not use
3	Phase set has a post-ambient phase	S ₀ -(S ₋₁ +S ₁)/2	Do not use
	Ambient insertion not used for current and two previous phase sets	S ₋₁ -(S ₋₂ +S ₀)/2 ⁽²⁾	
4		S ₀ and data from any auto-inserted Ambient	Any auto-inserted ambient, S ₀ , and S' ₀ ⁽³⁾

(1) DRE_S₀ refers to the data corresponding to the S₀ phase after processing by the DRE logic to stitch the code jumps.

(2) This is meant to address a case where the 3 consecutive phases correspond to AMB1(S₋₂), LED (S₋₁), AMB2 (S₀), all three of which are explicitly defined, without automatic ambient insertion. For this case, the formula realizes the difference of LED-Average(AMB1, AMB2).

(3) S'₀ refers to data from on-demand LED phase,. If S'₀ is absent in a PRF cycle, then this sample is a duplicate of LED sample, S₀.

7.3.2.4.2 High-PRF Mode

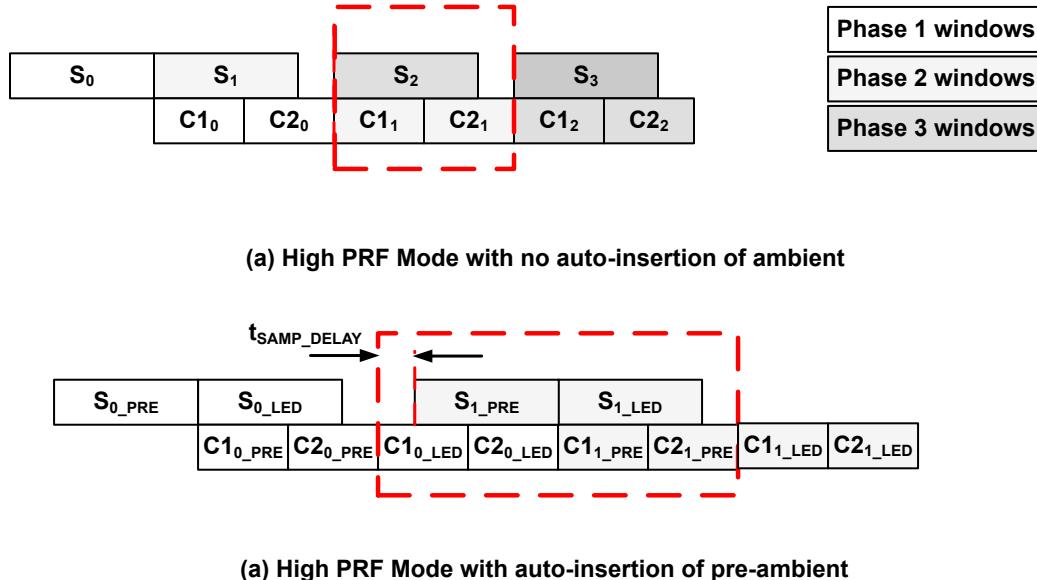
A High-PRF mode, set using the HIGH_PRF_MODE register bit, causes SAMP and CONV windows of adjacent phases to overlap. The High PRF mode is meant to achieve the maximum possible PRF setting for the desired number of signal phases. Therefore, to operate in the High PRF mode at the highest possible PRF, the device can be made to operate in the active mode throughout the PRF cycle, with the deep sleep state disabled. This is achieved as follows:

- Set the DIS_DEEP_SLEEP bit to '1' to disable the entry into deep sleep .
- Set the EN_ALWAYS_ACTIVE bit to '1' to keep the device in active state throughout the PRF cycle.
- Set REG_TDEEP_SLEEP_PWRUP and REG_TACTIVE_PWRUP registers to 0 to minimize these timing overheads and use the PRF cycle more efficiently for accommodating the PPG phases.

By default, the sampling window of Phase N is left-aligned with the first convert window of Phase N-1. The sampling window of Phase N can be delayed with respect to the first convert phase start by a delay called t_{SAMP_DELAY} as shown in [Figure 7-14 \(a\)](#). The t_{SAMP_DELAY} parameter can be set using the REG_SAMPLE_DELAY* register control. There are 4 such sets REG_SAMPLE_DELAY_SET1..REG_SAMPLE_DELAY_SET4. A 2-bit per-phase control SEL_SAMPLE_DELAY_SET can be set for each phase to select the one of the 4 delays to be applied to the SAMP window for that phase.

The High-PRF mode can be operated with two schemes for auto-insertion of ambient:

1. AUTO_AMB_INSERT bit set to '0' for all phases – in this case, no ambient is inserted for any of the phases.
2. AUTO_AMB_INSERT bit set to '1' for all phases – in this case, a pre-ambient is inserted for all phases. The t_{SAMP_DELAY} delay gets applied only to the auto-inserted pre-ambient phase. With insertion of appropriate delay as shown in [Figure 7-14 \(b\)](#), the ambient and LED SAMP windows can be made to come close to each other, resulting in good ambient rejection.

**Figure 7-14. High PRF Mode Timing**

In the High PRF mode, the samples streaming into the FIFO are as shown in [Table 7-11](#).

Table 7-11. FIFO Sample in the High PRF Mode

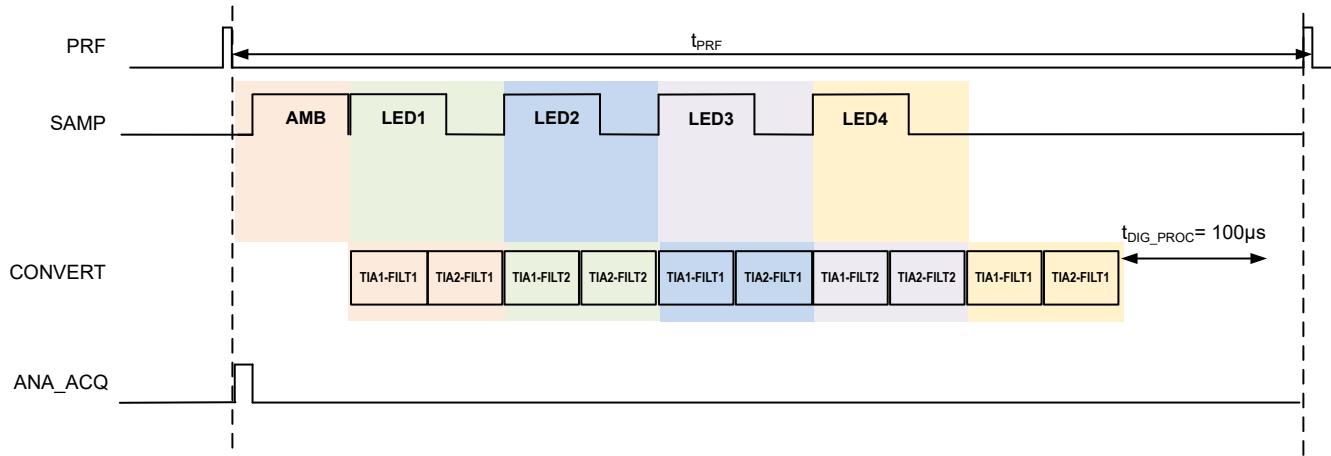
FIFO_DATA_CTRL	FIFO DATA
0	No data
1	S ₀
2	S ₀ -S ₋₁
3	Do not use
4	S ₀ and data from any auto-inserted pre-ambient

Note

When operating in the High PRF mode, an update in the Ambient DAC during any of the CONV phases can cause some noise degradation in the ADC conversion. Setting the DEGLITCH_AMB_DAC_MODE bit to '1' removes such a noise degradation with a slight power penalty.

7.3.2.4.2.1 Timing Example: High PRF Mode

[Figure 7-15](#) shows a timing diagram for a case where four LED signals are acquired in a PRF cycle. For each firing of the LED, each TIA connects to a PD such that the signal is acquired from both the PDs independently. A common ambient phase (AMB) precedes the LED signal acquisition. The Analog AACM loop can be optionally enabled at the start of the AMB phase window to update the Ambient Offset DAC for both the TIAs. The updated value of the Ambient Offset DAC for each TIA is applied throughout the PRF cycle.

**Figure 7-15. Timing Diagram for the High PRF Mode**

The LED DC cancellation loop can be enabled for any of the signals. To maximize the PRF, the phases are configured to operate in a non-staggered mode (global bit HIGH_PRF_MODE =1). As a consequence, the DRE mode cannot be used when operating in the High PRF mode.

The span of the sampling and convert signals of each phase window is color-coded. Two sets of 2 filters (one filter for each of the TIAs) alternate between sampling (concurrent operation for the 2 filters) and conversion (each filter output sequentially converted by the ADC). When FILT1 set is in sampling mode, FILT2 set is in convert mode.

Table 7-12 shows the per-phase settings illustrating a High PRF mode operation.

Table 7-12. Per-Phase Register Settings for the High PRF Mode⁽¹⁾

	AMB1	LED1	LED2	LED3	LED4	COMMENTS
Per-phase register set used to define the signal	1	2	3	4	5	Each phase explicitly defined
NUM_TIA	2	2	2	2	2	Both TIAs active in each phase
AUTO_AMB_INSERT	0	0	0	0	0	No automatic ambient insertion
USE_ANA_AACM	1	1	1	1	1	Use Analog AACM loop to control Ambient Offset DAC
UPDATE_BASELINE_AMB	1	0	0	0	0	Baseline update at start for both TIAs
LED_DC_EN_TIA n ($n=1,2$)	0	X	X	X	X	X = Set to 1 for the LED/PD combinations where Automatic LED DC cancellation is needed
FIFO_DATA_CTRL	1	1	1	1	1	Phase data written as is into FIFO

(1) Additionally set the global control HIGH_PRF_MODE to '1'.

7.3.2.4.3 Maximum Ambient Rejection Mode

A maximum ambient rejection mode can be enabled by setting the MAX_AMB_REJ bit to 1. In this mode, the pre-ambient, LED, and post-ambient sampling windows are positioned next to each other so as to maximize the ambient rejection. When the maximum ambient rejection mode is enabled, a pre-ambient and a post-ambient is inserted in every phase window around the defined LED phase. The AUTO_AMB_INSERT parameter for the phase is ignored. The USE_ANA_AACM and UPDATE_BASELINE_AMB can be enabled for the phase so that the Ambient DC can be acquired at the beginning of the phase and the Ambient Offset DAC can be updated. The sampling and convert windows are positioned as shown in Figure 7-16 (a) for the case where ENABLE_DRE is set to 0 and in Figure 7-16 (b) for the case where ENABLE_DRE is set to 1.

While operating in the maximum ambient rejection mode, both the pre-ambient and post-ambient are generated. By setting the DIS_POST_AMB_MAX_AMB_REJ bit instead of the MAX_AMB_REJ bit, only the pre-ambient can be inserted as shown in [Figure 7-16 \(c\)](#) and [Figure 7-16 \(d\)](#).

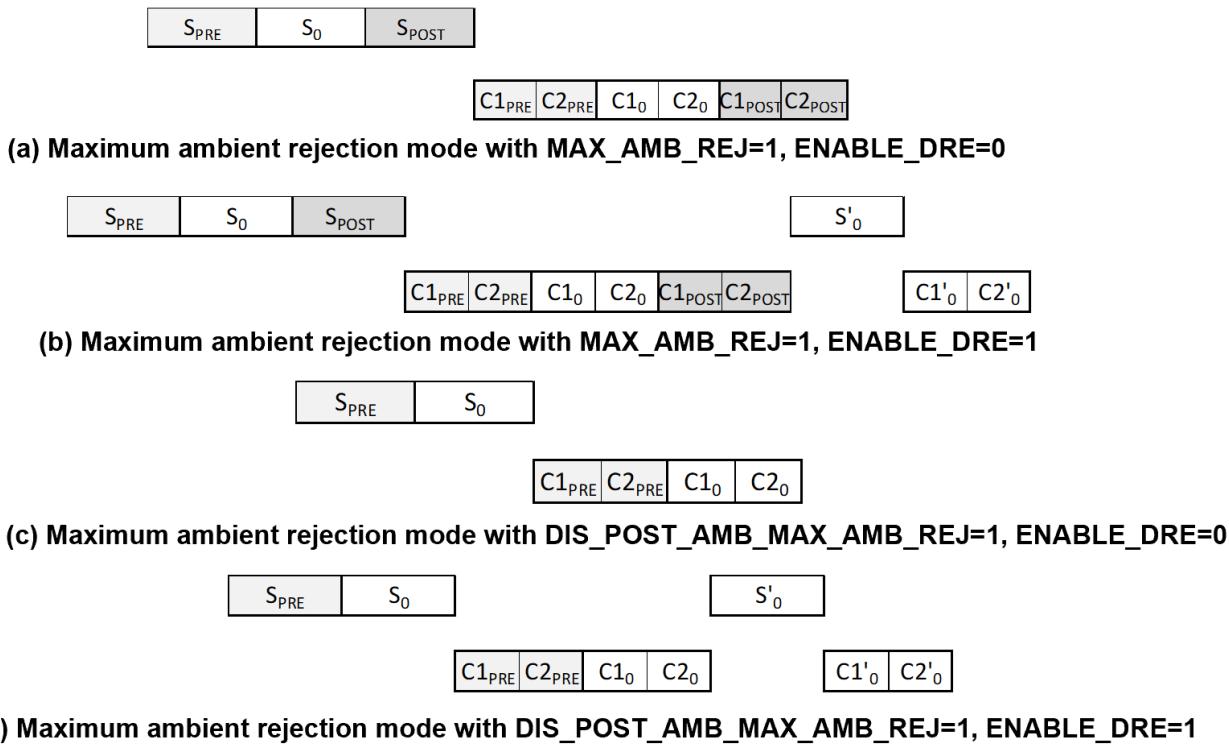


Figure 7-16. Timing Inside the Phase Window in the Maximum Ambient Rejection Mode

In the maximum ambient rejection mode, the samples streaming into the FIFO are as shown in [Table 7-13](#).

Table 7-13. FIFO Sample in the Maximum Ambient Rejection Mode

FIFO_DATA_CTRL	MAX_AMB_REJ = 1		DIS_POST_AMB_MAX_AMB_REJ = 1	
	ENABLE_DRE=0	ENABLE_DRE=1 ⁽¹⁾	ENABLE_DRE=0	ENABLE_DRE=1 ⁽¹⁾
0	No data	No data	No data	No data
1	Do not use	Do not use	Do not use	Do not use
2	Do not use	Do not use	S ₀ -S _{PRE}	Do not use
3	S ₀ -(S _{PRE} +S _{POST})/2	Do not use	Do not use	Do not use
4	S _{PRE} , S ₀ , S _{POST}	S _{PRE} , S ₀ , S _{POST} , S' ₀ ⁽²⁾	S _{PRE} , S ₀	S _{PRE} , S ₀ , S' ₀ ⁽²⁾

- (1) The maximum ambient rejection mode is not optimum for DRE mode because of the high separation between S₀ and S'₀ and the complication in the DRE post-processing in the presence of fast-changing ambient.
- (2) S'₀ refers to data from on-demand LED phase. If S'₀ is absent in a PRF cycle, then this sample is a duplicate of LED sample, S₀. With DRE enabled in the Maximum ambient rejection mode, the stitching of the code jumps is not done within the AFE. The stitching can be done in the MCU by streaming the individual data into the FIFO.

When operating the maximum ambient rejection mode, the FILT_RST phase is made common to all the three samplings, as shown in [Figure 7-17](#). By default, the t_{SAMP_SEP} parameter is 1 clock (approximately 4 µs).

Note

With DRE enabled in the Maximum ambient rejection mode, the stitching of the code jumps is not done within the AFE. The stitching can be done in the MCU by streaming the individual data into the FIFO.

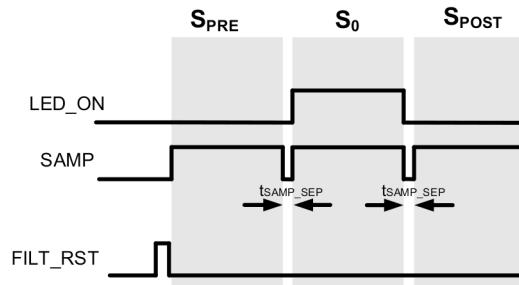


Figure 7-17. Composition of the Sampling Signal Windows in the Maximum Ambient Rejection Mode

7.3.2.4.3.1 Timing Example: Maximum Ambient Rejection Mode

Figure 7-18 shows a timing diagram for the maximum ambient rejection mode. Each phase window corresponds to an LED and the associated pre-ambient and post-ambient. Also while operating at a low enough PRF, the device can be made to enter a deep sleep mode after the completion of the active phases to save power. An associated wake-up window at the beginning of the PRF cycle allows the device to fully wake up from deep sleep before the start of the active phases.

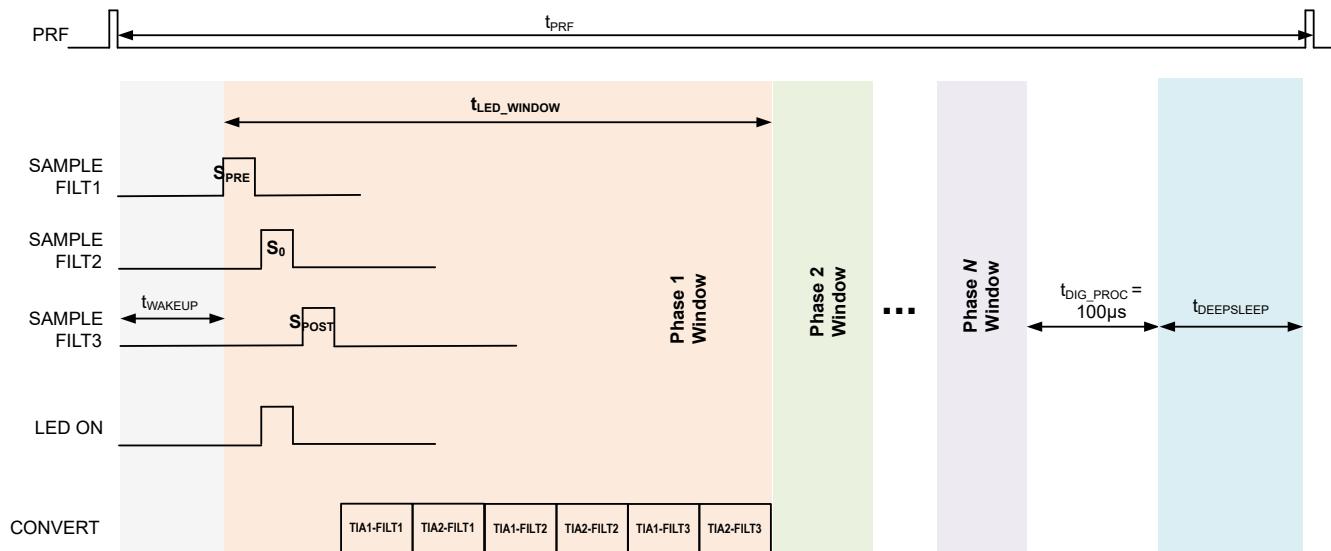


Figure 7-18. Timing Diagram for the Maximum Ambient Rejection Mode

Three sets of filters (up to 2 filters in each set and one filter for each TIA) sample the Pre-Ambient, LED and Post-Ambient in quick succession. Depending on the number of TIAs enabled, the ADC sequentially converts all the filters that have been enabled.

Table 7-14 shows the per-phase settings illustrating a maximum ambient rejection mode operation.

Table 7-14. Per-Phase Register Settings for the Maximum Ambient Rejection Mode⁽¹⁾

	LED1	LED2	...	LEDN	COMMENTS
Per-phase register set used to define the signal	1	2	...	N	Only LED phases defined
NUM_TIA	2	2	...	2	Both TIAs active in each phase
AUTO_AMB_INSERT	x	x	...	x	AUTO_AMB_INSERT ignored
USE_ANA_AACM	1	1	...	1	Use Analog AACM loop to control Ambient Offset DAC
UPDATE_BASELINE_AMB	1	1	...	1	Baseline update at start of each phase for both TIAs
LED_DC_EN_TIA n ($n=1,2$)	0	X	...	X	X = Set to 1 for the LED/PD combinations where Automatic LED DC cancellation is needed
FIFO_DATA_CTRL	3	3	...	3	LED – Average(AMB)

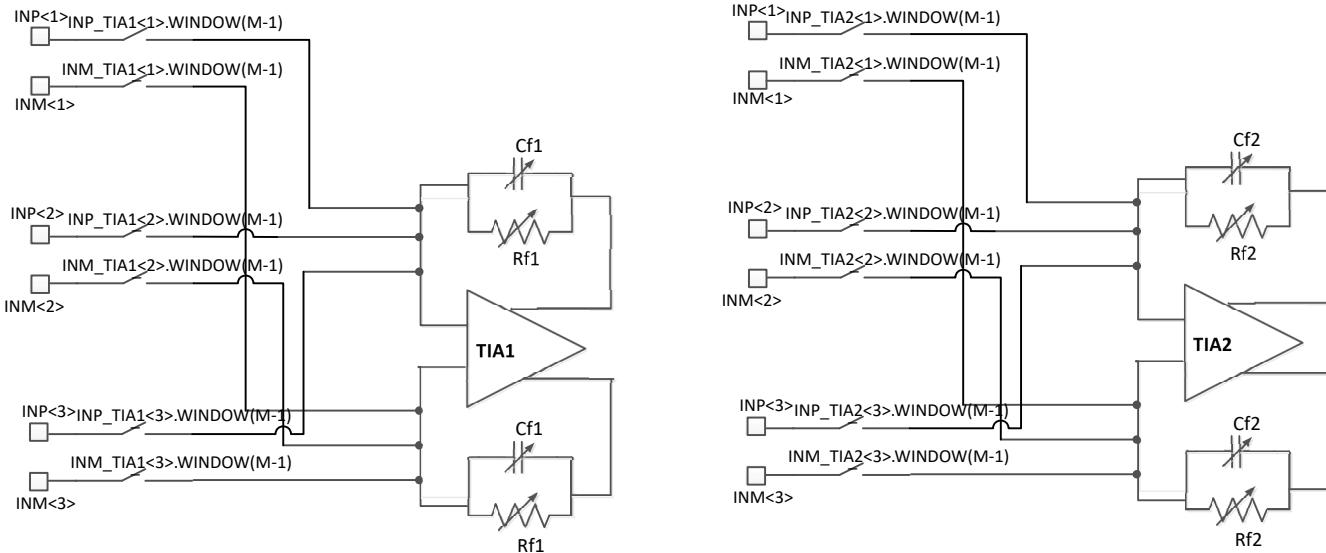
(1) Additionally set the global control MAX_AMB_REJ to '1'.

7.3.3 Signal Definition for a Phase

The signal to be acquired in a phase is defined using per-phase register controls to associate one or more PDs and one or more LEDs to be active during that phase.

7.3.3.1 PD Association for a Phase

A switch matrix that connects the input pins to any of TIA1 and TIA2. The connection to TIA1 and TIA2 is shown in [Figure 7-19](#). Signals marked INP_TIA1<3:1> and INM_TIA1<3:1> are derived from the per-phase (of Phase M) register bits IN_TIA1<3:1> and correspond to the connection of the input pins to TIA1 for Phase M. Each of the signal phases has two sets of 3 bits (IN_TIA1<3:1> for TIA1, IN_TIA2<3:1> for TIA2), which denote the TIA to which the corresponding input pins are to be connected during that particular phase. A change in any of the IN_TIA* bits takes effect at the beginning of the Phase window.

**Figure 7-19. Switch Matrix Showing Connectivity of the Input Pins to TIA1 and TIA2 in Phase M**

The PDs are connected differentially to the TIAs. So INP_TIAx<y> and INM_TIAx<y> are the same as IN_TIAx<y>, the per-phase register control bits (x:TIA# = 1,2; y:IN#=1,2, 3). If TIAx is not used in a phase, then set all the corresponding IN_TIAx* bits to '0'.

In addition to the per-phase controls for connecting or disconnecting the PDs to the TIA, global controls PD_DISCONNECT_TIA1 and PD_DISCONNECT_TIA2 causes all the PDs (both P and M side switches) to be disconnected from TIA1, TIA2 respectively even if any of the PD_ON bits have been set to '1'. When in the

PD_DISCONNECT* mode, the input current to the TIA during a phase is equal to the Offset Cancellation DAC set for that phase. The PD_DISCONNECT mode is useful to calibrate the Offset DAC.

When a particular PD is connected to the TIA, the TIA maintains the proper bias on the PD through the negative feedback mechanism. When a PD is disconnected from the TIA, a mechanism to automatically short the input pins to an internal node VCM is used to maintain the PD bias.

Note

If a TIA is not used in a particular phase, then take care to ensure that no PD is connected to that TIA. The bias of unconnected PDs is maintained by shorting the associated input pins to a common mode voltage.

7.3.3.2 LED Association for a Phase

The LED association for each phase is set by the ‘per-phase’ register controls `LED_DRV1_TXN<4:1>` and `LED_DRV2_TXN<4:1>` as shown in [Figure 7-20](#). These static signals defined for each phase combine with the dynamically switching `LED_ON` signal during that phase window to generate the appropriate switch controls to route the driver currents to the desired TX pins.

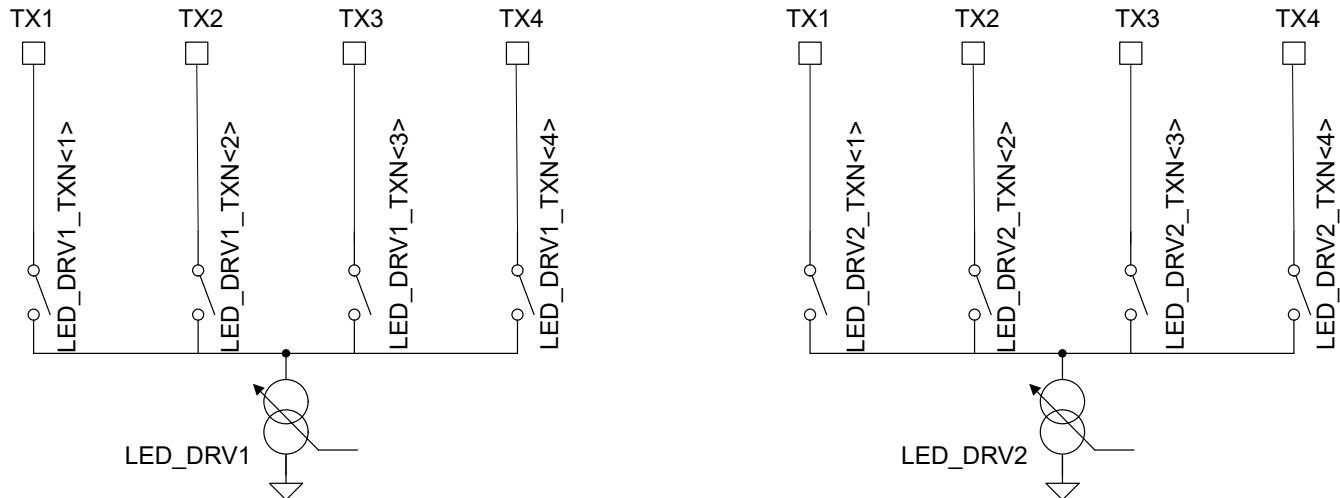


Figure 7-20. Scheme for LED Association in a Phase

Setting the `LED_DRVx_TXN<y>` bit for a phase turns on the switch between LED Driver x (where $x=1,2$) and the TX_{Ny} pin (where $y=1,2,3,4$). Any combination of the control bits can be set for each phase, resulting in a complete flexibility in which LEDs are turned on in a phase. [Figure 7-21](#) shows an example where all four of the TX pins are used to realize control over 4 LEDs.

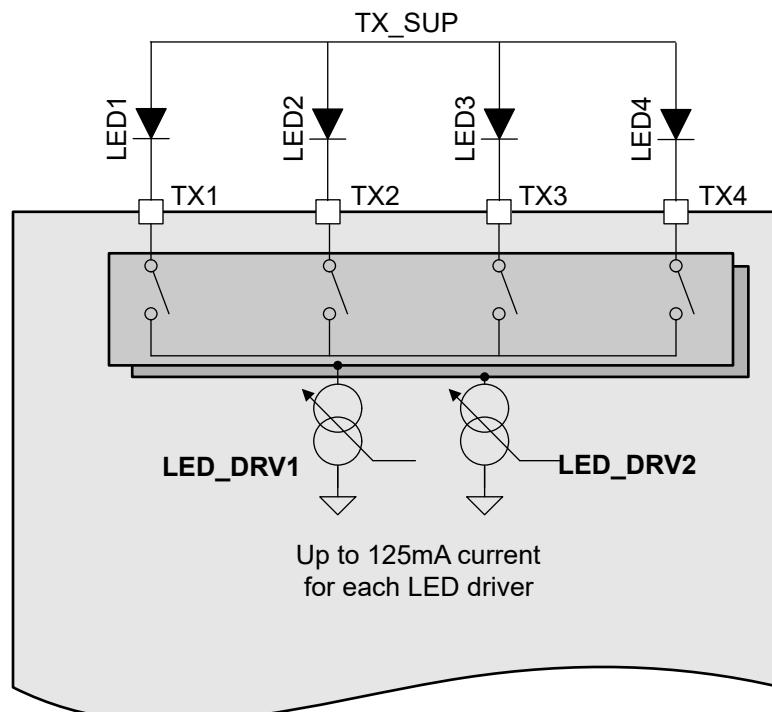


Figure 7-21. Scheme for Connecting 4 LEDs

7.3.4 PPG Signal Chain Parameters

The register controls for setting the signal chain parameters for a given PPG phase are summarized in [Table 7-15](#).

Table 7-15. Register Controls for Setting the Signal Chain Parameters of a Phase

PARAMETER	REGISTER CONTROL	NO. OF BITS	RANGE OF CONTROL	CLASSIFICATION	COMMENTS	
AMB Offset DAC range	IFS_AMB_OFFDAC_TIA1	3	1X to 16X	Global control	Ambient Offset DAC full scale range	
	IFS_AMB_OFFDAC_TIA2	3				
Enable LED Offset DAC	EN_LED_OFFDAC_TIA1	1	0 or 1	Global control	Enables LED Offset DAC	
	EN_LED_OFFDAC_TIA2	1				
Ambient Cancellation DAC setting (MCU control)	IOFFDAC_PD1	8	255 steps between 0 and full scale value	Global setting	Combined (added) based on which PDs are connected to the particular TIA in that phase	
	IOFFDAC_PD2	8				
	IOFFDAC_PD3	8				
LED Offset DAC (MCU control)	IOFFDAC_LED_TIA1	9	511 steps between 0 and full scale value	Per-phase setting for each TIA		
	IOFFDAC_LED_TIA2	9				
Offset DAC polarity	POL_IOFFDAC_AMB	1	Add or Subtract	Global control for Ambient, LED DACs of both TIAs	0 = Add, 1 = Subtract	
	POL_IOFFDAC_LED	1				
TIA gain	RF_TIA1	4	3.7 kΩ - 1 MΩ	Per-phase for TIA1		
	RF_TIA2	4		Per-phase for TIA2		
TIA feedback cap	CF_TIA1	3	2.5 pF – 25 pF	Per-phase for TIA1		
	CF_TIA2	3		Per-phase for TIA2		
Filter Controls	FILTER_SET_SEL	1	0 or 1	Per-phase control	Choose between Set 1, Set 2	
	REG_TW_FILTER_PRE	8	0 to 127	Global control common for all receivers	Pre-charge time window	
	OVERRIDE_BW_PRE	1	0 or 1		Override bit to enable control of Pre-charge filter bandwidth (Set 1 & Set 2)	
	FILTER_BW_PRE_SET1	5	2.5 kHz to 77.5 kHz		Filter BW Set 1	
	FILTER_BW_FINE_SET1					
	FILTER_BW_PRE_SET2				Filter BW Set 2	
	FILTER_BW_FINE_SET2					
# of ADC averages	REG_NUMAV	4	1,2,3,4,8 ADC averages	Per-phase – common for all TIAs	# of ADC averages = REG_NUMAV+1	
LED full scale current	ILED_FS	3	50 mA (1X) 0.5X to 3.3X	Global control		
LED current setting	ILED_DRV1	8	0 to full scale setting – 255 steps	Per-phase control	LED Driver 1	
	ILED_DRV2				LED Driver 2	

7.3.5 LED Driver

By default, the full scale current range of each of the two parallel drivers is 25 mA. The register control ILED_FS can be used to change the full-scale range as shown in [Table 7-16](#).

Table 7-16. Register Controls for Setting the LED Full-Scale Current

ILED_FS	MODE	LED FULL SCALE CURRENT – ONE DRIVER	LED FULL SCALE CURRENT – TWO DRIVERS
000	0.5X mode	25 mA	50 mA
001	1X mode	50 mA	100 mA
010	2X mode	100 mA	200 mA
011	2.5X mode	125 mA	250 mA
100	3.3X mode	167 mA	334 mA ⁽¹⁾
Other settings		Do not use	

(1) Use only up to 250 mA. Also in this mode, the minimum TX_SUP supported is 5 V.

The current setting of each of the two drivers with respect to the full-scale current is set using per-phase 8-bit controls ILED_DRV1 for driver 1 and ILED_DRV2 for driver 2 as shown in [Table 7-17](#).

Table 7-17. Register Controls for Setting the LED Current

DECIMAL EQUIVALENT OF 8-BIT ILED_DRV1 AND ILED_DRV2 CURRENT CONTROL	LED CURRENT (mA) FOR DIFFERENT MODES – TYPICAL VALUE				
	0.5X MODE ILED_FS='000'	1X MODE ILED_FS='001'	2X MODE ILED_FS = '010'	2.5X MODE ILED_FS='011'	3.3X MODE ILED_FS='100'
0	0	0	0	0	0
1	0.098	0.196	0.392	0.49	0.655
2	0.196	0.392	0.784	0.98	1.301
...					
255	25 ⁽¹⁾	50 ⁽¹⁾	100 ⁽¹⁾	125 ⁽¹⁾	167 ⁽¹⁾

(1) Due to saturation effects in the driver, the full scale current can be lower than these values.

The voltage headroom required by the LED driver depends on 2 factors:

1. The full-scale current mode as set by ILED_FS
2. The current setting through the LED, denoted by ILED

The voltage headroom (VHR) required for the LED driver (and the switches) is given by:

$$VHR = VHR_{BASELINE} + I_{LED} \times R_{TXN} \quad (1)$$

where $VHR_{BASELINE}$ is as listed in [Table 7-18](#), R_{TXN} is the routing resistance associated with the TXN* switches. The value of R_{TXN} is 1 Ω.

Table 7-18. Full-Scale LED Current Modes and Associated Values of VHR_{BASELINE}

LED FULL-SCALE MODE	FULL-SCALE CURRENT PER DRIVER (mA)	VHR _{BASELINE} AT TX_SUP = 3 V	VHR _{BASELINE} AT TX_SUP = 5 V
0.5X	25 mA	0.31 V	0.30 V
1X	50 mA	0.45 V	0.41 V
2X	100 mA	0.89 V	0.75 V
2.5X	125 mA	1.1 V	0.9 V
3.3X	167 mA		1.2 V

As an example, when operating in the 2.5X mode with $I_{LED} = 100 \text{ mA}$ at 5 V supply: $VHR = 0.9 \text{ V} + (100 \text{ mA} \times 1 \Omega) = 1.0 \text{ V}$.

For the same LED current setting, the mode with the higher VHR_{BASELINE} results in a better (lower) noise operation of the LED driver.

If none of the switches to a driver are set to be on, then the driver is switched off in that phase. For example, both drivers are off in the ambient phase by setting all the switches of both drivers to be OFF.

Note

When the LED current is set to 0 in the LED phase, the shuts off the amplifier in the LED driver. This can disturb the reference voltage and impact ambient rejection. To avoid such an occurrence, the LED driver amplifier can be kept active in the LED phase by setting TX_AMP_ACTIVE_ALWAYS bit to '1'.

7.3.6 Offset Cancellation DAC

There are two Offset DACs at the input of each TIA – these are denoted as Ambient Offset DAC and LED Offset DAC and their respective currents are denoted as IOFFDAC_AMB_TIA1 and IOFFDAC_AMB_TIA2 and IOFFDAC_LED_TIA1, IOFFDAC_LED_TIA2 respectively. The Ambient Offset DAC is enabled by default whereas the LED Offset DAC is disabled by default. The Ambient Offset DAC can be automatically controlled by the Analog AACM loop. The LED offset DAC can be automatically controlled by the LED DC cancellation loop. Additionally, both Offset DACs can be controlled by the MCU through registers. The Offset DAC circuit scheme is shown in [Figure 7-22](#).

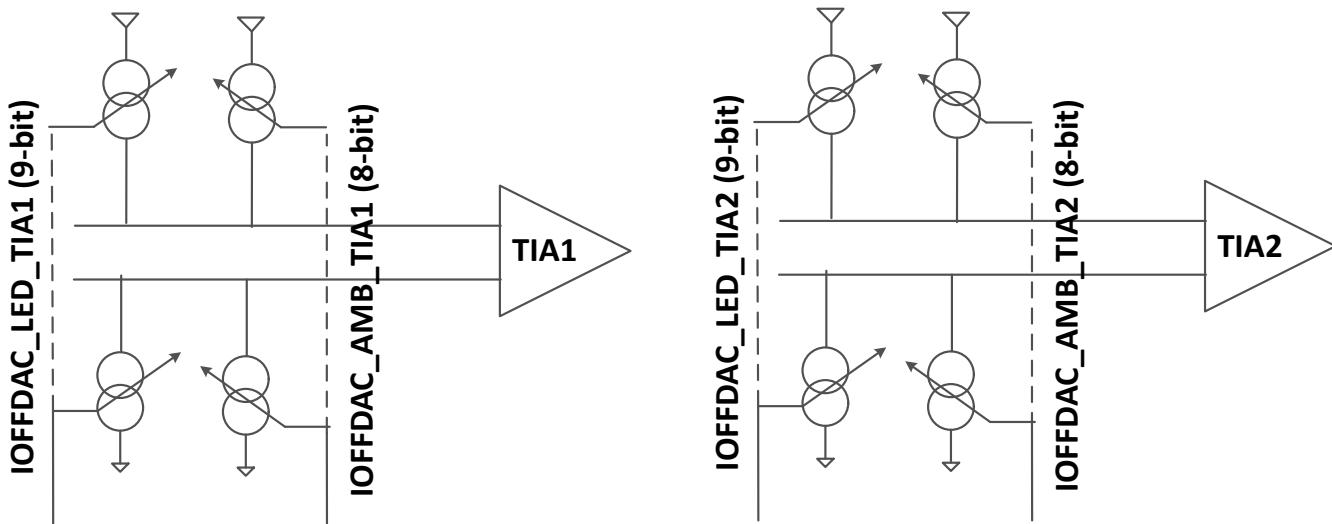


Figure 7-22. Offset DAC Scheme Showing the Ambient and LED Offset DACs

The full scale current control of the Ambient Offset DAC is set through global registers IFS_AMB_OFFDAC_TIA1, IFS_AMB_OFFDAC_TIA2 (for TIA1 and TIA2 respectively) as shown in [Table 7-19](#). The full-scale current setting is common to the IOFFDAC_AMB_TIA* across all the phases.

**Table 7-19. Full-Scale Current Control of Ambient Offset DAC Using IFS_AMB_OFFDAC Controls
(Applicable to IOFFDAC_AMB_TIA* in All the Phases)**

MODE NOTATION	REGISTER CONTROL (BINARY VALUE) TO SET THE MODE	FULL SCALE CURRENT
1X mode	000	$\pm 15.9375 \mu\text{A}$
2X mode	001	$\pm 31.875 \mu\text{A}$
4X mode	011	$\pm 63.75 \mu\text{A}$
8X mode	101	$\pm 127.5 \mu\text{A}$
16X mode	111	$\pm 255 \mu\text{A}$
	Other settings	Do not use

For the same offset DAC current setting, the mode with the lower full scale current operates with the lowest noise. Therefore, TI recommends that at low levels of ambient current, the 1X mode be used.

When controlled by the MCU, the ambient Offset DAC can be programmed using the registers IOFFDAC_PD1, IOFFDAC_PD2, IOFFDAC_PD3. These 8-bit registers represent the value of the ambient current to be subtracted from each of the 3 PDs and are applied to the ambient Offset DAC of a TIA depending on which PD is connected to the TIA (the codes are summed up if multiple PDs are connected to the same TIA).

Note

Set EN_AMB_DAC_LSB to '1' to enable the LSB control of the ambient Offset DAC.

Note

The LED Offset DAC can be optionally chopped to reduce noise contribution. Chopping can be enabled by setting the EN_IOFFDAC_LED_CHOP bit to 1. When chopping is enabled in the LED offset DAC, the PPG output can have a tone at a frequency of PRF/2. This tone can be removed by enabling decimation (with any decimation factor from 2 to 32). The noise advantage from enabling chopping is expected to be marginal at low PRFs.

Table 7-20. Mapping of the Ambient Offset DAC Setting to the Register Value⁽¹⁾⁽²⁾

DECIMAL EQUIVALENT IOFFDAC_AMB ^{(3) (4)}	AMBIENT OFFSET DAC CURRENT (μ A) FOR DIFFERENT MODES				
	1X MODE	2X MODE	4X MODE	8X MODE	16X MODE
0	0	0	0	0	0
1	0.0625	0.125	0.25	0.5	1
2	0.125	0.25	0.5	1	2
...
255	15.9375	31.875	63.75	127.5	255

(1) The ambient offset cancellation DAC is not trimmed at production and, therefore, the value of the full-scale current can vary across units by $\pm 20\%$.

(2) Above table corresponds to POL_IOFFDAC_AMB=0. With POL_IOFFDAC_AMB=1, the above currents become negative

(3) Derived from the IOFFDAC_PD1, IOFFDAC_PD2, IOFFDAC_PD3 registers

(4) The LSB control of the Ambient DAC is disabled by default. To enable the LSB control, set EN_AMB_DAC_LSB to '1'

The full scale current of the LED Offset DAC has a typical value of 63.875 μ A but can vary by +/-25% across units. Therefore, TI suggests to limit the DC signal current to 45 μ A or lower. The LED Offset DAC can also be programmed using 9-bit registers IOFFDAC_LED_TIA1, IOFFDAC_LED_TIA2 as shown in [Table 7-21](#).

Table 7-21. Mapping of the LED Offset DAC Setting to the IOFFDAC_LED_TIA* Register⁽¹⁾⁽²⁾

DECIMAL EQUIVALENT IOFFDAC_LED_TIA*<8:0>	LED OFFSET DAC CURRENT (μ A)
0	0
1	0.125
2	0.25
...	..
511	63.875

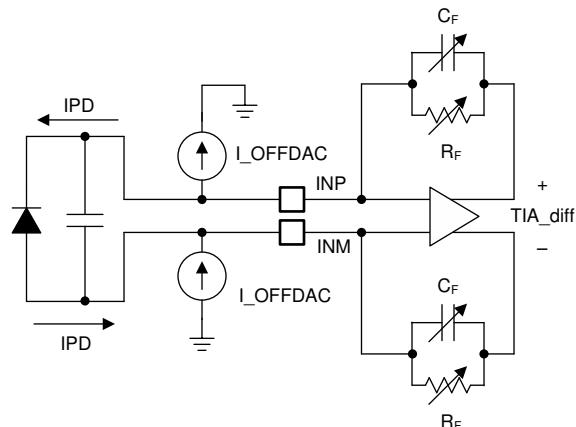
(1) The LED offset cancellation DAC is not trimmed at production and, therefore, the value of the full-scale current can vary across units by $\pm 25\%$.

(2) Above table corresponds to POL_IOFFDAC_LED=0. With POL_IOFFDAC_LED=1, the above currents become negative.

The Ambient Offset DAC is enabled by default whereas the LED Offset DAC is disabled by default. To enable the LED Offset DAC, set the global bits EN_LED_OFFSETDAC_TIA1 to enable the LED Offset DAC for TIA1.

The polarity of the Ambient offset DAC is controlled by a global register bit POL_IOFFDAC_AMB, and the polarity of the LED Offset DAC is controlled by a global register bit POL_IOFFDAC_LED.

The polarity of the Ambient offset DAC is controlled by a global register bit POL_IOFFDAC_AMB, and the polarity of the LED Offset DAC is controlled by a global register bit POL_IOFFDAC_LED. With zero input current and zero current in the offset cancellation DAC, the output of the AFE is close to zero. Based on the channel offset, the output voltage for zero input current can be a small positive or negative value, usually in the range of several millivolts. With the photodiode connected as shown in [Figure 7-23](#) and a signal current coming from the photodiode, the output code of the device is expected to be positive with the offset cancellation DAC set to zero (IOFFSET* = 0). With IOFFSET* set as a negative (POL_OFFSET* = 1), a dc offset can be subtracted from the signal. This is the case for both the Ambient DAC and the LED DAC. If the polarity of the PD connection to the input pins is reversed with respect to what is shown in [Figure 7-23](#), then setting POL_OFFSET* to 0 results in a subtraction of the Offset DAC current from the input current of the PD.



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Figure 7-23. Offset Cancellation Current Polarity Diagram shown for POL_OFFSETDAC=0 (Applicable to Both Ambient and LED Offset DAC). For POL_OFFSETAC=1, the Polarity of the Offset DAC Current Sources are Reversed

7.3.6.1 LED Offset DAC Update

The LED offset DAC is applied only during the S_0 (and S'_0) windows. The setting is based on the LED_DC_EN_TIA1.. LED_DC_EN_TIA2 per-phase bits. For example, if LED_DC_EN_TIA1=0, then the LED offset DAC value is set based on the 9-bit IOFFDAC_LED_TIA1 per-phase register. If LED_DC_EN_TIA1=1, then the LED offset DAC is automatically updated by the LED DC cancellation loop assigned to the signal processed by TIA1 in that phase. The user should ensure that the total number of LED DC cancellation loops associated with LED signals, across phases and TIAs, is limited to 8 or less.

Figure 7-24 shows the LED offset DAC update timing for the case where ENABLE_DRE is set to 0 and the case where ENABLE_DRE is set to 1.

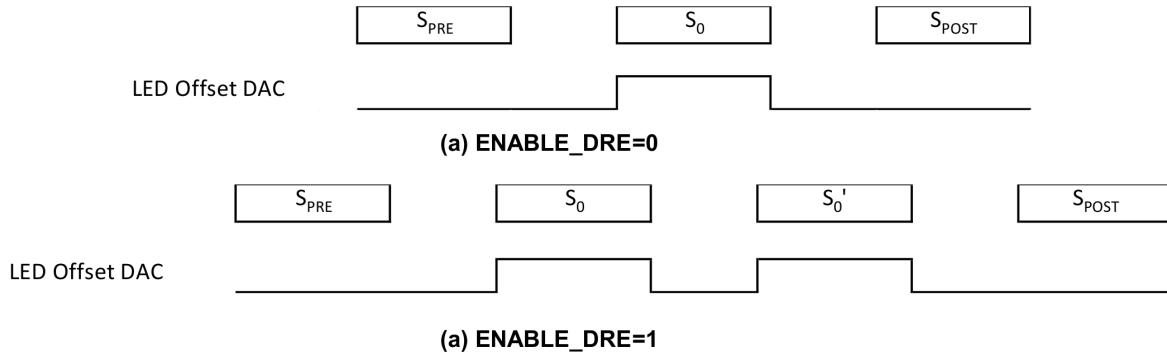


Figure 7-24. LED Offset DAC Update Timing

7.3.6.2 Ambient Offset DAC Update

The Ambient offset DAC is applied over the entire phase set window. The manner of update is based on the USE_ANA_AACM and UPDATE_BASELINE_AMB per-phase bits. If both the USE_ANA_AACM and UPDATE_BASELINE_AMB bits are 1 for a phase, then the Analog AACM loop acquires the Ambient at the input of each active TIA during the ANA_ACQ window at the start of the phase window and uses the updated value of the Ambient Offset DAC for that TIA for the rest of the phase window. If the USE_ANA_AACM bit is 1 and the UPDATE_BASELINE_AMB is 0, then the Ambient DAC value (for each TIA) from the previous phase window is used for the current phase window.

If the USE_ANA_AACM bit is 0, then the Ambient DAC value to be used for that phase window is computed from the IOFFDAC_PD1..IOFFDAC_PD3 registers. These registers need to be written with the values of the Ambient Offset DAC associated with Ambient cancellation of each of the PDs (PD1 to PD3). Based on which combination of PDs are connected to a TIA in a phase, the value of Ambient Offset DAC to be used for that TIA in that phase is automatically computed. For example, if PD1 and PD2 are connected to TIA1 in a phase, then the value of Ambient Offset DAC set for TIA1 is computed as (IOFFDAC_PD1+IOFFDAC_PD2).

7.3.7 Trans-Impedance Amplifier (TIA)

The gain of each TIA can be programmed using the per-phase controls RF_TIA1, RF_TIA2 respectively. The feedback capacitance (C_F) of each TIA can be programmed using the per-phase controls CF_TIA1, CF_TIA2, respectively. The mapping of the TIA R_F and C_F to their register controls is shown in [Table 7-22](#).

Table 7-22. Mapping of the TIA R_F and C_F to the Register Controls

RF_TIA* REGISTER VALUE	TIA GAIN (R _F)	CF_TIA* REGISTER VALUE	TIA FEEDBACK CAP (C _F)
0	3.7 KΩ	0	2.5 pF
1	5 KΩ	1	5 pF
2	10 KΩ	2	7.5 pF
3	25 KΩ	3	10 pF
4	33.3 KΩ	4	17.5 pF
5	50 KΩ	5	20 pF
6	71.5 KΩ	6	22.5 pF
7	100 KΩ	7	25 pF
8	142 KΩ		
9	166 KΩ		
10	200 KΩ		
11	250 KΩ		
12	500 KΩ		
13	1 MΩ		

The product of R_F and C_F determines the time constant of the TIA and determines the TIA transient settling during the LED_ON phase.

Note

The TIA is shared between phases and the feedback capacitor (C_F) cap is not reset between phases, which can result in a crosstalk between adjacent phases, especially when one of the phases has an over-saturated signal (input current exceeding full scale). For example, a saturated LED phase can disturb the signal in the succeeding Ambient phase. The level of crosstalk can be reduced by reducing the time constant of the TIA. Another way to reduce the crosstalk between phases is to enable a short reset phase in the TIA between phases by setting the EN_TIA_RST bit to '1'.

7.3.8 PPG Noise Reduction Filter

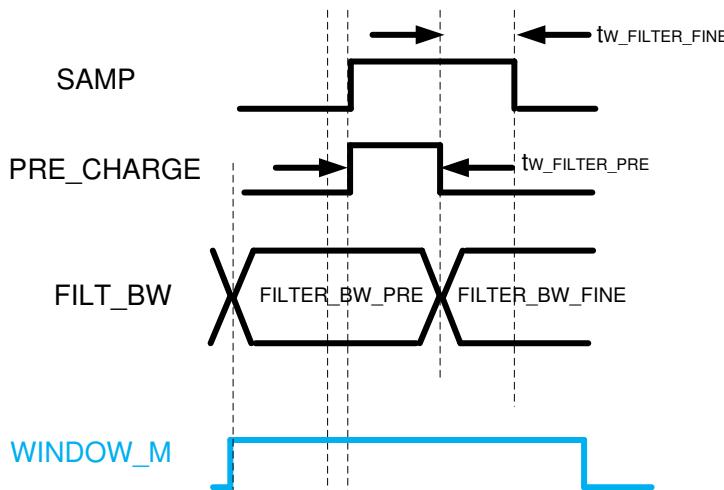
The signal from the PD contains optical noise must be band-limited before the ADC converts the signal. The Noise reduction filter at the output of the TIA helps limit the bandwidth of the optical noise and improve the system SNR. The output of the TIA is sampled by the Noise reduction filter during the SAMP phase. The bandwidth of the filter can be programmed. There are two such filters. When used as a Single Receiver, the two filters get connected to the same TIA during the SAMP of alternate phase windows. When used as a Dual receiver, each filter connects to the output of one of the two TIAs during the same SAMP. The voltage sampled across a filter in SAMP is converted by the ADC in the associated CONV. Before a filter enters SAMP, the filter is reset to erase any signal memory from use in a prior phase. The Sampling (SAMP) window is partitioned into two portions: a *Pre-charge window*, followed by a *Fine Settling window*.

The width of the pre-charge window, programmed in terms of CLK_TE, is controlled using a global control REG_TW_FILTER_PRE. The default setting of the pre-charge window width is four clocks, and the MSB of this word serves as an override bit to change the default setting as shown in [Table 7-23](#). The rest of SAMP after completion of the pre-charge window automatically gets assigned for the Fine settling window.

Table 7-23. Programming the Filter Pre-Charge Phase Width

REG_TW_FILTER_PRE								FILTER PRE-CHARGE WINDOW WIDTH ($t_{W_FILTER_PRE}$)
D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	4*CLK_TE (Default)
1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1*CLK_TE
1	0	0	0	0	0	1	0	2*CLK_TE
1								...
1	1	1	1	1	1	1	1	127*CLK_TE

Figure 7-25 shows the transition of the filter bandwidth from precharge phase to fine settling phase.

**Figure 7-25. Filter Bandwidth Transition Scheme**

Two sets of filter bandwidth controls can be programmed: Set 1 and Set 2. For each of the signal phases within a PRF cycle, either set can be selected using the per-phase register bit FILTER_SET_SEL. Each set comprises the register controls for the filter bandwidth in the pre-charge window as well as the filter bandwidth in the Fine settling window. By default, FILTER_BW_PRE of both Set 1 and Set 2 is set to 50 KHz. By setting the OVERRIDE_BW_PRE register bit to '1', FILTER_BW_PRE can be set using the global register control FILTER_BW_PRE_SET1 (when using Set 1 for the phase) and using FILTER_BW_PRE_SET2 (when using Set 2). Table 7-24 shows the bandwidth controls.

Table 7-24. Filter Bandwidth Selection

FILTER BW SETTING	SET 1 - USED FOR PHASE WHERE FILTER_SET_SEL=0		SET 2 - USED FOR PHASE WHERE FILTER_SET_SEL=1	
	OVERRIDE_BW_PRE=0	OVERRIDE_BW_PRE=1	OVERRIDE_BW_PRE=0	OVERRIDE_BW_PRE=1
In Pre-charge phase	50 kHz	FILTER_BW_PRE_SET1	50 kHz	FILTER_BW_PRE_SET2
In Fine settling phase	FILTER_BW_FINE_SET1			FILTER_BW_FINE_SET2

Each filter bandwidth register control listed in Table 7-24 is a 5-bit register word of the form FILTER_BW<4:0>. Filter bandwidth setting in kHz = FILTER_BW<0>*2.5 + FILTER_BW<1>*5+FILTER_BWZ<2>*10 + FILTER_BW<3>*20 + FILTER_BW<4>*40 where FILTER_BWZ<2> corresponds to the invert of the FILTER_BW<2> register bit.

With the 5-bit control, filter bandwidth settings from 2.5 Hz to 77.5 kHz can be achieved in steps of 2.5 kHz. A few example settings of the filter bandwidth are shown in Table 7-25. Using a low filter bandwidth provides more noise filtering to the noise from the sensor and the TIA.

Table 7-25. Filter Bandwidth Set by FILTER_BW Control

FILTER_BW<4>	FILTER_BW<3>	FILTER_BW<2>	FILTER_BW<1>	FILTER_BW<0>	TYPICAL f _{RC} (kHz)
0	0	0	0	0	10
0	0	0	0	1	12.5
0	0	0	1	0	15
0	0	0	1	1	17.5
0	0	1	0	0	Do not use
0	0	1	0	1	2.5 (Lowest)
0	0	1	1	0	5
0	0	1	1	1	7.5
0	1	0	0	0	30
0	1	0	0	1	32.5
...					
1	0	0	0	0	50
1	0	0	0	1	52.5
...					
1	1	0	1	1	77.5 (Highest)
...					
1	1	1	1	1	67.5

To support shorter SAMP widths (and thereby shorter LED ON times), the transient settling of the TIA and the filter must be fast in the Pre-charge window. The suggested settings for the TIA time constant (maximum value), filter pre-charge window width and filter bandwidth settings in the pre-charge and fine settling phases are listed in [Table 7-26](#) across SAMP widths (t_{TE} in this table corresponds to the time period of a 256 kHz clock).

Table 7-26. Filter and TIA Settings Across SAMP Widths⁽¹⁾

SAMP WIDTH (t_{W_SAMP})	MAX TIA TIME CONSTANT ($t_{TIA} = R_F \times C_F$)	PRE-CHARGE WIDTH ($t_{W_FILTER_PRE}$)	PRE-CHARGE BW (FILTER_BW_PRE)	FINE SETTLING BW (FILTER_BW_FINE)
$4 \times t_{TE} \approx 16 \mu s$	3 μs	0 ⁽²⁾	50 kHz	50 kHz
$5 \times t_{TE} \approx 20 \mu s$	4 μs	0 ⁽²⁾	40 kHz	40 kHz
$6 \times t_{TE} \approx 23 \mu s$	4.6 μs	0 ⁽²⁾	35 kHz	35 kHz
$7 \times t_{TE} \approx 27 \mu s$	5.5 μs	0 ⁽²⁾	30 kHz	30 kHz
$8 \times t_{TE} \approx 31 \mu s$	6 μs	0 ⁽²⁾	25 kHz	25 kHz
$9 \times t_{TE} \approx 35 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	17.5 kHz
$10 \times t_{TE} \approx 39 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	15 kHz
$11 \times t_{TE} \approx 43 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	10 kHz
$12 \times t_{TE} \approx 47 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	10 kHz
$13 \times t_{TE} \approx 51 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	10 kHz
$14 \times t_{TE} \approx 55 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	7.5 kHz
$15 \times t_{TE} \approx 59 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	7.5 kHz
$16 \times t_{TE} \approx 63 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	7.5 kHz
$17 \times t_{TE} \approx 66 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	7.5 kHz
$18 \times t_{TE} \approx 70 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	5 kHz
$19 \times t_{TE} \approx 74 \mu s$	3 μs	$4 \times t_{TE} \approx 16 \mu s$	50 kHz	5 kHz
$20 \times t_{TE} \approx 78 \mu s$	5 μs	$6 \times t_{TE} \approx 23 \mu s$	32.5 kHz	5 kHz
$21 \times t_{TE} \approx 82 \mu s$	5 μs	$6 \times t_{TE} \approx 23 \mu s$	32.5 kHz	5 kHz
$22 \times t_{TE} \approx 86 \mu s$	5 μs	$6 \times t_{TE} \approx 23 \mu s$	32.5 kHz	5 kHz
$23 \times t_{TE} \approx 90 \mu s$	5 μs	$6 \times t_{TE} \approx 23 \mu s$	32.5 kHz	5 kHz

Table 7-26. Filter and TIA Settings Across SAMP Widths⁽¹⁾ (continued)

SAMP WIDTH (t_{W_SAMP})	MAX TIA TIME CONSTANT ($t_{TIA} = R_F \times C_F$)	PRE-CHARGE WIDTH ($t_{W_FILTER_PRE}$)	PRE-CHARGE BW (FILTER_BW_PRE)	FINE SETTLING BW (FILTER_BW_FINE)
$24 \times t_{TE} \cong 94 \mu s$	5 μs	$6 \times t_{TE} \cong 23 \mu s$	32.5 kHz	5 kHz
$25 \times t_{TE} \cong 98 \mu s$	5 μs	$6 \times t_{TE} \cong 23 \mu s$	32.5 kHz	5 kHz
$26 \times t_{TE} \cong 102 \mu s$	5 μs	$6 \times t_{TE} \cong 23 \mu s$	32.5 kHz	5 kHz
$27 \times t_{TE} \cong 105 \mu s$	6 μs	$8 \times t_{TE} \cong 31 \mu s$	25 kHz	2.5 kHz
$28 \times t_{TE} \cong 109 \mu s$	6 μs	$8 \times t_{TE} \cong 31 \mu s$	25 kHz	2.5 kHz
$29 \times t_{TE} \cong 113 \mu s$	6 μs	$8 \times t_{TE} \cong 31 \mu s$	25 kHz	2.5 kHz
$30 \times t_{TE} \cong 117 \mu s$	6 μs	$8 \times t_{TE} \cong 31 \mu s$	25 kHz	2.5 kHz

- (1) t_{TE} in this table corresponds to a 256 kHz internal clock. If using a different t_{TE} , then follow the same guidelines as in the table based on the SAMP width in μs .
- (2) With FILTER_BW_PRE and FILTER_BW_FINE set to the same value, the setting of the pre-charge width becomes irrelevant. The pre-charge width can be set to any value (even a value higher than the SAMP width). Since the pre-charge width is a common setting between Filter set 1 and Filter set 2, this fact can be exploited to set the pre-charge width to the value as required by the lower bandwidth setting.

7.3.9 Analog-to-Digital Converter (ADC)

The AFE has an ADC that provides a 22-bit representation of the current from the photodiode. The ADC codes corresponding to the various sampling phases can be read out from 24-bit registers in two's complement format. The ADC full-scale input range ($\pm FS$) is nominally ± 1.2 V and spans bits 21 to 0. [Table 7-27](#) shows the mapping of the ADC input voltage to the ADC code.

Table 7-27. Mapping the ADC Input Voltage to the ADC Code

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT	24-BIT ADC OUTPUT CODE
-FS	11100000000000000000000000000000
(-FS / 2 ²¹)	11111111111111111111111111111111
0	00000000000000000000000000000000
(FS / 2 ²¹)	00000000000000000000000000000001
FS	00011111111111111111111111111111

Note that the TIA has an operating range of ± 1 V even though the ADC input full-scale range is ± 1.2 V, as shown in [Figure 7-26](#). When setting the TIA gain, ensure that the signal at the TIA output does not exceed ± 1 V.

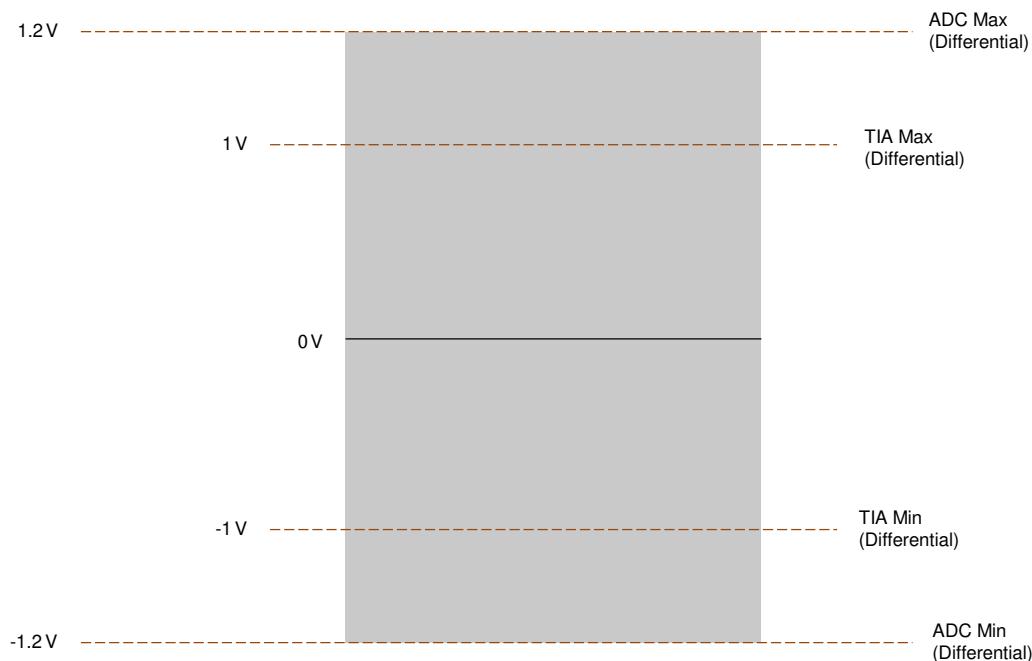


Figure 7-26. TIA and ADC Dynamic Ranges

7.3.9.1 ADC Averaging for PPG Phase Conversions

To reduce the noise, the input to the ADC (sampled on the capacitor of the filter) can be converted by the ADC multiple times and averaged. The per-phase register REG_NUMAV determines number of ADC averages for the phase (NUMAV). The number of averages is set as NUMAV = (REG_NUMAV + 1).

As an example, when NUMAV is programmed to 4 (REG_NUMAV = 3), the ADC converts the input four times in each phase, averages the four conversions, and stores the averaged value in the FIFO. The width of the CONV signal for a phase is automatically changed based on the NUMAV setting for that phase.

Averaging only helps in reducing ADC noise and not the front-end noise because the input to the ADC is the same sampled voltage across all ADC conversions used to generate the average (this voltage corresponds to the voltage sampled on the sampling capacitor of the filter). The number of samples that can be averaged can be set to 1,2,3,4,8 (REG_NUMAV can take values 0,1,2,3,7). A higher number of averages result in larger conversion times leading to higher active time and larger power consumption. A high value of NUMAV also increases the separation between the sampling instants of LED and Ambient signals, which is undesirable from perspective of Ambient rejection. In cases of high gain settings (250 KΩ and beyond), set NUMAV to 1. For gains in the range of 100 KΩ, a NUMAV of 2 provides adequate SNR improvement. Settings of NUMAV higher than 2 only help at very low TIA gain settings.

Averaging is implemented in the following manner:

Use [Equation 2](#) to calculate the ADC output for a NUMAV setting.

$$\text{ADCOUT} = \left[\sum_{i=1}^{\text{NUMAV}} (\text{ADCI}_i) \right] * 128 / X \quad (2)$$

where

- ADCI_i = the i^{th} sample converted by the ADC and X is an integer

This implementation gives an averaging function that is exact when the number of averages is a power of 2 but deviates from integer values for other settings, as shown in [Table 7-28](#).

Table 7-28. ADC Averaging Mode Settings

NUMAV	1	2	3	4	8
X	128	64	43	32	16
D	1	2	2.97	4	8

7.3.9.2 ADC Code During Output Saturation

When the input exceeds the full-scale levels, the output code saturates. The exact saturation value depends on the NUMAV setting. For different NUMAV settings, the saturation value on the positive side is between 1FFF19h and 1FFFFFFh and the saturation value on the negative side is between E080E7h and E00000h. This kind of saturation behavior is applicable to the data corresponding to an individual conversion phase (for example, the LED or the Ambient data). The behavior of the (LED—Ambient) data are different from the one outlined above. For the (LED—Ambient) data, the two MSBs of the 24-bit word serve as sign-extension bits to the 22-bit ADC code, and are equal to the MSB of the 22-bit ADC code when the input to the ADC is within full-scale range, as shown in [Table 7-29](#).

Table 7-29. Using Sign-Extension Bits to Determine the Input Operating Voltage

Bits 23-21 ⁽¹⁾	INPUT STATUS
000	Positive and within full-scale range
111	Negative and within full-scale range
001	Positive and outside full-scale
110	Negative and outside full-scale

(1) Note that D23 gets replaced by the Frame sync indicator bit when EN_FRAME_SYNC mode is set.

If a LED phase reaches saturation, then the (LED-Ambient) code need not be saturated. Therefore, if the (LED-Ambient) data is output to the FIFO, then the Bits 23-21 cannot be relied upon to give a true indication of saturation in the LED phase. To ascertain saturation (or near-saturation) in the LED phase reliably, the EN_LED_SAT_DET bit can be set to 1. When this mode is enabled, the bits 23-21 of the (LED-Ambient) data will be set as indicated in [Table 7-29](#) when the LED data is less than 90% of ADC full scale. When the LED data is higher than 90% of the ADC full scale, Bits 23-21 get set as shown in [Table 7-30](#). Note that such a change in mapping is effected only if the FIFO data associated with the phase is a computed code involving a combination of the LED and Ambient phase outputs.

Table 7-30. Sign Extension Bits in the (LED-Ambient) Data When EN_LED_SAT_DET is Set to '1', and the LED Data Exceeds 90% of ADC Full Scale

Bits 23-21 ⁽¹⁾	INPUT STATUS
100	Positive and within full-scale range
011	Negative and within full-scale range
101	Positive and outside full-scale
010	Negative and outside full-scale

(1) Note that D23 gets replaced by the Frame sync indicator bit when EN_FRAME_SYNC mode is set.

7.3.10 Input DC Cancellation

7.3.10.1 Overview - Input DC Cancellation

The Ambient signal incident on the sensor can be modeled as the sum of a DC (or slow varying) component and an AC (fast-varying) component. The AC component can show up as tones in the LED phase data, and can interfere with the detection of the heart rate from the PPG signal. The tones from the AC component of the ambient can be largely suppressed by defining LED and Ambient phases, and by subtracting the Ambient phase data from the LED phase data.

From a theoretical calculation, the ambient rejection from digital subtraction of the ambient phase data from the LED phase data is given by:

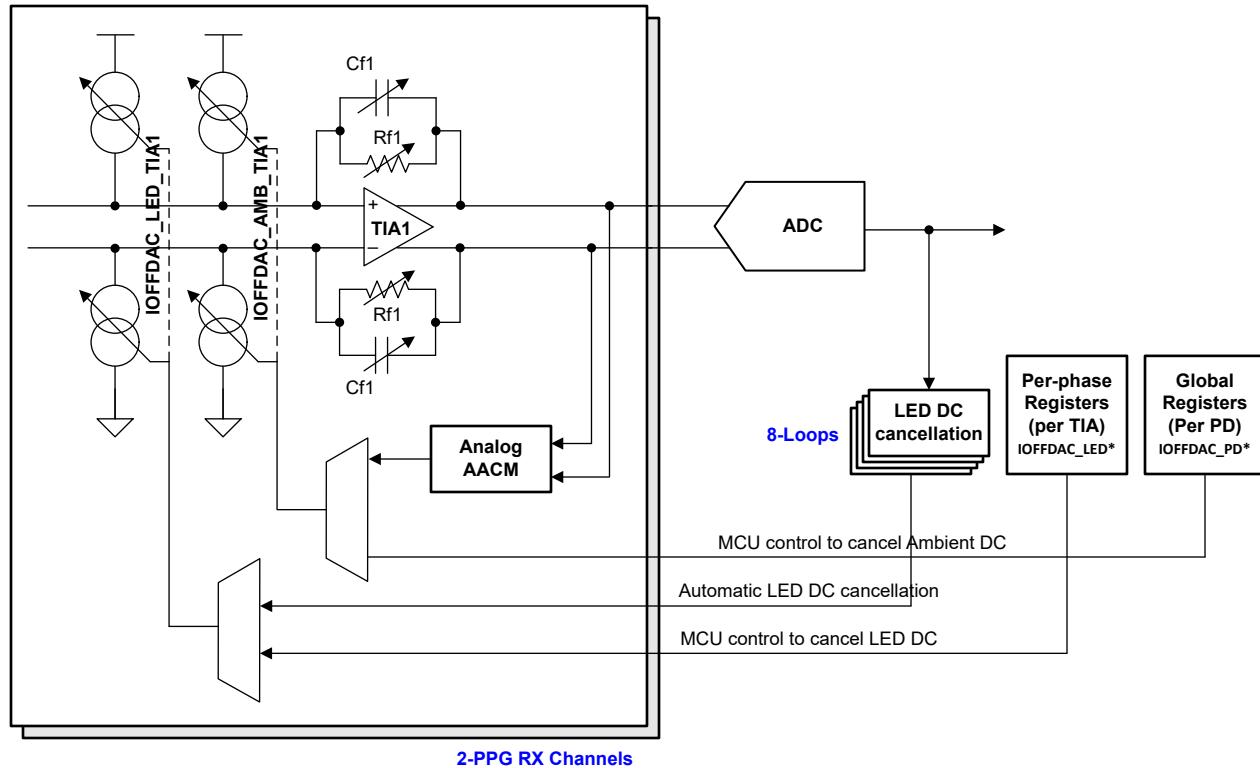
$$\text{Ambient rejection through } (LED - \text{Ambient}) = \sqrt{2 \times (1 - \cos(2\pi f_{AMB} \cdot t_{SEP}))} \quad (3)$$

where f_{AMB} is the frequency of the ambient light and t_{SEP} is the time separation between the SAMP end of the LED and Ambient phases.

An even higher level of ambient rejection can be achieved by combining the Ambient signal from more than one phase and subtracting the combined Ambient signal from the LED phase. The Digital subtraction of Ambient (or a combination of multiple Ambient phases) can help suppress tones.

The other undesirable effect of the ambient signal is that the DC component of the ambient signal can fill a portion of the dynamic range of the receiver in both the LED and ambient phases. A high ambient signal level can limit the maximum TIA gain setting and limit the achievable SNR. The Ambient Offset DACs at the input of the TIA can be configured (either automatically or by the MCU) to cancel out all or a portion of the DC signal from the Ambient. Similarly, the DC component of the signal in the LED phase also can be cancelled out using either the Ambient or the LED Offset DACs.

The AFE offers multiple schemes for controlling the LED and Ambient Offset DAC to cancel out the DC of the signal in the LED and Ambient phases. The Ambient DC cancellation can be controlled either by the MCU, or by enabling the Analog AACM control loop to estimate and cancel the Ambient DC. The LED Offset DAC can be controlled by the MCU. Alternatively, when using the Analog AACM loop to cancel the Ambient DC, the LED DC cancellation control loop can be used to estimate and cancel the additional DC in the LED phase. An overview of control schemes are depicted in [Figure 7-27](#). The LED DC Cancellation loop is realized through digital logic – the ADC output code in the LED phase serves as the input to this logic. The Analog AACM loop, on the other hand uses the Analog output of the TIA to determine the Offset DAC setting required to cancel the Ambient.

**Figure 7-27. Control Schemes for Ambient and LED DC Cancellation**

An overview of control schemes are listed in [Table 7-31](#).

Table 7-31. Control Schemes for Ambient and LED DC Cancellation⁽¹⁾

SCHEME NAME	SCHEME DESCRIPTION	AMBIENT OFFSET DAC CONTROL IOFFDAC_AMB_TIA*[7:0]	LED OFFSET DAC CONTROL IOFFDAC_LED_TIA*[8:0]
Full MCU control (SWAP_DAC = 0)	MCU controls cancellation of Ambient DC using IOFFDAC_AMB and LED DC using IOFFDAC_LED	Determined by IOFFDAC_PD*[8:1] (Global setting – code associated with PDs connected are added to determine the IOFFDAC_AMB setting for that TIA)	Determined by IOFFDAC_LED_TIA*[8:0] register (per-phase, per-TIA setting)
Full MCU control (SWAP_DAC=1)	MCU controls cancellation of Ambient DC using IOFFDAC_LED and LED DC using IOFFDAC_AMB	Determined by IOFFDAC_LED_TIA*[8:1] (per-phase, per-TIA setting)	Determined by IOFFDAC_PD*[8:0] (Global setting – code associated with PDs connected are added to determine the IOFFDAC_AMB setting for that TIA)
Automatic Ambient cancellation using Analog AACM (USE_ANA_AACM=1)	Ambient DC cancelled using Analog AACM / MCU controls LED DC cancellation	Controlled by Analog AACM loop	Determined by IOFFDAC_LED* register (per-phase, per-TIA setting)
Automatic LED DC cancellation (EN_LED_DC=1)	Ambient DC cancelled using Analog AACM / LED DC cancelled using LED DC cancellation	Controlled by Analog AACM loop	Controlled by LED DC cancellation loop

(1) Ensure that the IFS_OFFDAC is chosen so that the Ambient Offset DAC has enough range to cancel the Ambient signal range.

The schemes are summarized below:

Full MCU control: By default, the Ambient Offset DAC is used to cancel the Ambient DC and the LED Offset DAC is used to cancel the LED DC. A per-phase, per-TIA 9-bit code controls the LED Offset DAC. The Ambient Offset DAC control is derived using the IOFFDAC_PD1, IOFFDAC_PD2, IOFFDAC_PD3 registers. The Ambient DAC code for a given TIA in a given phase is determined based on which PDs are connected to that TIA in that phase – the associated IOFFDAC_PD* are added, and the 8 MSBs of the 9-bit code are used for the 8-bit Ambient Offset DAC control.

By setting the SWAP_DAC bit to 1, the functions for the two DACs can be swapped such that the Ambient Offset DAC is used to cancel the LED DC and the LED Offset DAC is used to cancel the Ambient DC. The register controls for the DACs are also swapped.

Analog AACM: The Analog AACM loop can be used to cancel the DC in the Ambient phases. In the Analog AACM scheme, a set of consecutive phases having the same Ambient signal (phases corresponding to the same PD or to the same combination of PDs) are grouped together. The first of this set of phases is defined as an Ambient phase and a convergence of the Analog AACM loop is defined at the start of this phase to acquire the baseline ambient and to update the Ambient Offset DAC. The Analog AACM loop acquires the information of the Ambient level through a convergence of the loop at the start of this phase, updates the Ambient Offset DAC and applies the same value for the cancellation of ambient in all phases in the set. Any number of such sets of phases can be defined and the Analog AACM loop can be set to acquire the ambient freshly at the start of each set. The additional DC in the LED phase can be cancelled out through MCU control by programming the LED Offset DAC. Alternatively, the LED Offset DAC can be set to be automatically cancelled by associating one of the LED DC cancellation loops with the LED phase.

Automatic LED DC cancellation: While using the Analog AACM scheme to cancel the Ambient signal, there is also a possibility to use the LED DC cancellation loops to automatically cancel the additional DC in the LED phases. Since there are 8 LED DC cancellation loops, this scheme can be used to cancel the DC in up to 8 signals (a signal constitutes an LED/PD combination). The Automatic LED DC cancellation involves an automatic update by a LED DC cancellation loop to the LED Offset DAC when the output code from the ADC in the LED phase goes out of bounds of a set programmable threshold. This update results in a glitch in the data. Fast changing DC (for example during motion) can cause frequent glitching which can interfere with the heart rate extraction. In such a scenario, the Automatic LED DC cancellation feature can be enabled for a one-time setting of the LED Offset DAC at start of signal acquisition and then frozen to avoid further updates. Alternatively, a Dummy LED phase can be defined and set to come once at the start of a time window, and the LED DC cancellation loop updates the LED Offset DAC only during the PRF cycle where the Dummy LED phase is active (not masked).

A *Dynamic Range Extension (DRE)* mode when set, automatically *stitches* the code jumps caused by the updates to the LED Offset DAC and extends the dynamic range well beyond the ADC full scale range.

7.3.10.2 Automatic Ambient Cancellation Using Analog AACM

An Analog Automatic Cancellation Mode (Analog AACM) scheme can be used to control the Ambient Offset DAC for a set of phases having the same ambient (referred to as a *Common Ambient Set*). The Analog AACM scheme uses a short ambient acquisition window during the first phase (defined to be the baseline Ambient phase) of the Common Ambient set. The TIA output during the Ambient Acquisition window is used to estimate the Baseline Ambient level and update the Ambient Offset DAC across all phases belonging to the Common Ambient set. Set the USE_ANA_AACM to associate all the phases of a Common Ambient set with the Analog AACM control. The first phase in the Common Ambient set is marked to be the Ambient Baseline phase by setting the UPDATE_BASELINE_AMB bit to '1', and a short Ambient acquisition window (ANA_ACQ*) is automatically generated (commonly for each active TIA in that phase) prior to the start of the LED_ON signal for the phase. The setting of the Ambient Offset DAC needed to cancel the ambient is automatically determined during the ANA_ACQ* window and is used for all the phases associated with the set. In a similar manner, a new Common ambient set can be defined by setting the UPDATE_BASELINE_AMB to '1' in the first of those set of phases and setting USE_ANA_AACM bit to '1' for all of them. In any of the phases, the LED Offset DACs for each of the 4 TIAs can be additionally set using the IOFFDAC_LED_TIA* register controls for that phase. The registers relevant to Analog AACM operation are listed in [Table 7-32](#).

Table 7-32. Analog AACM Register Controls

PARAMETER	REGISTER CONTROL	NO. OF BITS	CLASSIFICATION	COMMENTS
Per-phase Analog AACM loop activation bit	USE_ANA_AACM	1	Per-phase control (common for all TIAs)	Set to '1' if the phase is associated with the Analog AACM loop
Ambient Baseline Acquisition specification bit	UPDATE_BASELINE_AMB	1	Per-phase control (common for all TIAs)	Set to '1' to acquire ambient baseline in that phase (for use across the Common Ambient set)

Figure 7-28 shows a generic case of how the Analog AACM loop can be used to acquire the ambient and update the Ambient Offset DAC for a set of phases with common ambient. Figure 7-28 shows the phases in one PRF cycle. The cell marked in grey corresponds to the Ambient baseline phase for the Analog AACM loop. At the start of the baseline phase, a short Analog ambient acquisition window (shaded in black) is automatically generated during which the Analog AACM loop converges and acquires the ambient.

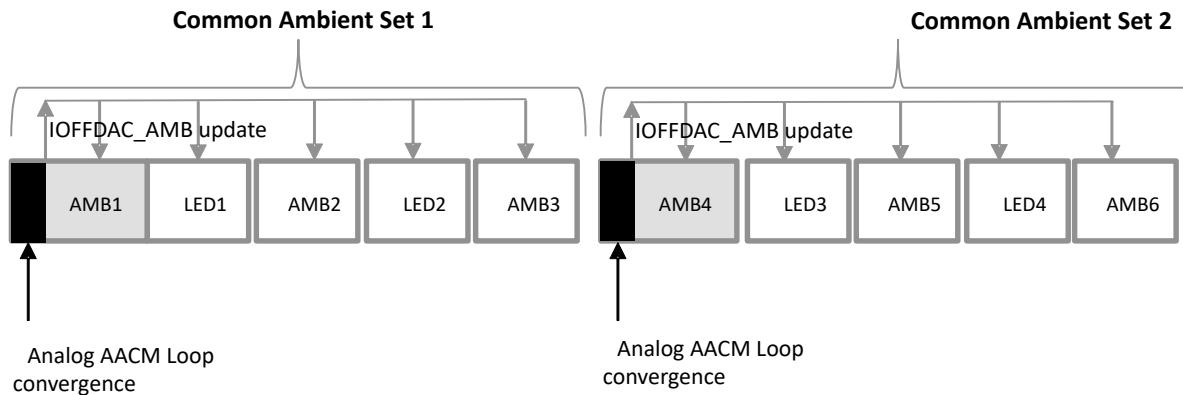


Figure 7-28. Placement of LED and AMB Phases Within One PRF Cycle Illustrating the Positioning of the Ambient Baseline Phases for the Analog AACM Loop

The transition of the Ambient Offset DAC and LED Offset DAC is shown in Figure 7-29 for two cases, one corresponding to UPDATE_BASELINE_AMB=1 and the other to UPDATE_BASELINE_AMB=0.

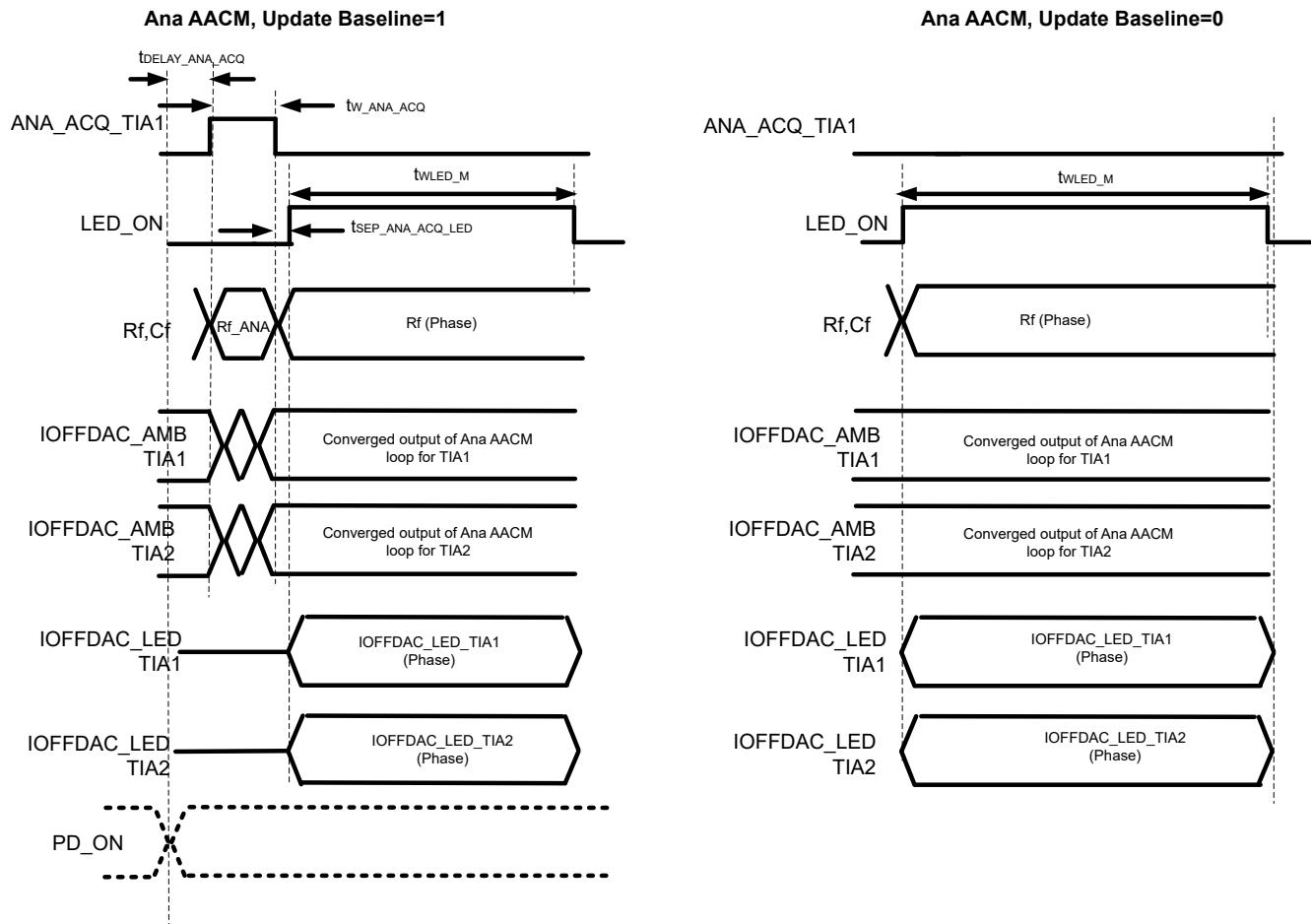


Figure 7-29. Transition of the Ambient and LED Offset DAC for Phases Where Analog AACM is Enabled

The default width of the ANA_ACQ phase is approximately 30 μ s (set as 8 counts for 256 kHz).

The parameters $t_{\text{DELAY_ANA_ACQ}}$, $t_{\text{W_ANA_ACQ}}$ and $t_{\text{SEP_ANA_ACQ_LED}}$ are calculated automatically but can be an over-ride option is available using register controls as shown in Table 7-33.

Table 7-33. Timing Parameters for the Analog AACM Loop and Their Register Controls

PARAMETER	DESCRIPTION	DEFAULT ⁽¹⁾	TO OVERRIDE	UNIT
$t_{\text{DELAY_ANA_ACQ}}$ ⁽¹⁾	Separation between start of phase window and ANA_ACQ_TIA signal	0	$\text{REG_DELAY_ANA_ACQ} \times t_{\text{TE}}$	μ s
$t_{\text{W_ANA_ACQ}}$	Width of ANA_ACQ_TIA signal	31.25	Set $\text{TW_ANA_ACQ_OVERRIDE} = 1$ and program desired value as $(\text{REG_TW_ANA_ACQ} + 1) \times t_{\text{TE}}$	μ s
$t_{\text{SEP_ANA_ACQ_LED}}$	Separation between ANA_ACQ_TIA signal and LED ON signal for that phase	$1 \times t_{\text{TE}}$	Set $\text{TSEP_ANA_ACQ_LED_OVERRIDE} = 1$ and program desired value as $(\text{REG_TSEP_ANA_ACQ_LED}) \times t_{\text{TE}}$	μ s

(1) If the phase with the ANA_ACQ window is the first phase in a sequence of phases with a certain PD, TI recommends to set $t_{\text{DELAY_ANA_ACQ}}$ to a non-zero value - this delay allows the PD time for the bias to recover before the start of the ANA_ACQ window. Giving extra time for the recovery of the PD bias becomes more relevant if there is a possibility of high intensity of light being incident on the PD in the previous phase that could cause the bias to be disturbed.

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The R_F and C_F controls during the ANA_ACQ phase are derived from global registers RF_ANA_AACM_START_TIA1 to RF_ANA_AACM_START_TIA2 (separate controls for TIA1 to TIA2) and RF_ANA_AACM_END (common control for TIA1 to TIA2). Depending on the IFS_AMB_OFFDAC mode, set these registers to the values shown in [Table 7-34](#). Note that the code mapping the register values to the R_F settings are different from the per-phase R_F code shown in [Table 7-34](#).

Table 7-34. R_F and C_F Controls During ANA_ACQ Phase of the Analog AACM

IFS_AMB_OFFDAC MODE	RF_ANA_AACM_START_TIA1/ RF_ANA_AACM_START_TIA2WORD (IN DECIMAL)	RF_ANA_AACM_END WORD (IN DECIMAL)
1X	5	10
2X	3	10
4X	2	5
8X	1	5
16X	0	5

The IOFFDAC_AMB code determined by the AACM loop in an Analog AACM phase marked with UPDATE_BASELINE='1' can be embedded into the 9 LSB of the FIFO word corresponding to that phase using the register bit EMBED_ANA_AACM_IN_FIFO. This mode can be used as a diagnostic mode to occasionally check the level of the ambient signal being canceled and to determine whether to switch to a different IFS_OFFDAC mode.

7.3.10.3 Automatic LED DC Cancellation

While using the Analog AACM to control the Ambient Offset DAC and cancel the Ambient level in Common Ambient set of phases (that can typically include Ambient and LED phases), the LED DC cancellation loops (8 in number) can be used to control the LED Offset DAC to cancel the additional DC in up to 8 signals (a signal is defined as a LED/PD combination). Unlike canceling Ambient using an update to the Ambient Offset DAC in both the Ambient and LED phases, cancelling additionally the DC in only the LED phase using an automatic update to the LED Offset DAC leads to glitches in the data. Therefore, this feature can be useful only in scenarios where the drift in the signal is small or slow. The LED DC cancellation when used in conjunction with the DRE mode, helps to remove the glitches caused by the LED Offset DAC update.

The loops get assigned in the sequence of the Phase and TIA for which the LED DC cancellation loop has been enabled. Since there are only a total of 8 loops, any LED DC cancellation loop assignments beyond 8 signals get ignored. [Table 7-35](#) lists the register controls for Automatic LED DC cancellation using the LED DC cancellation loop.

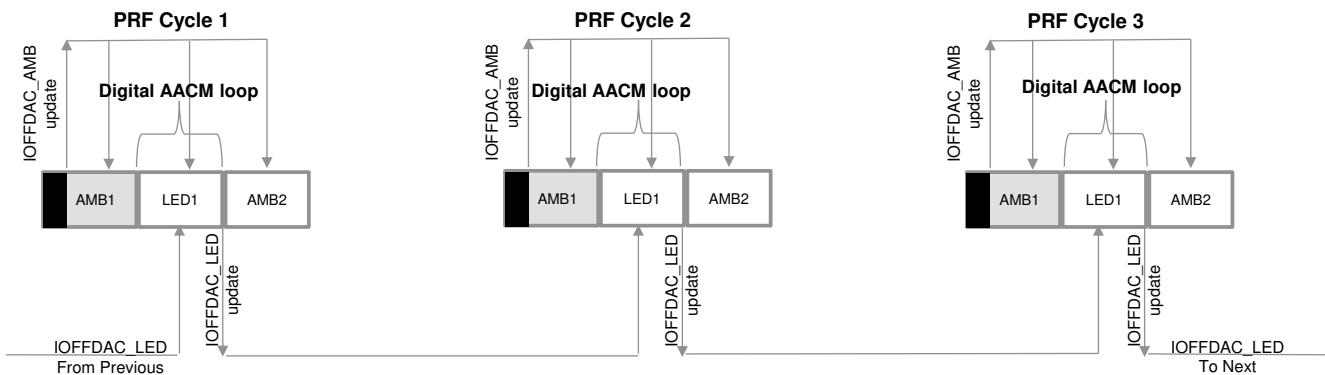
Table 7-35. Automatic LED DC Cancellation - Register Controls

PARAMETER	REGISTER CONTROL	NO. OF BITS	CLASSIFICATION	COMMENTS
Calibration words	CHANNEL_OFFSET_TIA1	12	Channel offset Calibration words (TIA specific) for Automatic LED DC cancellation	Channel offsets of each TIA Transfer function between LED Offset DAC code and ADC output code – the 4 words correspond to TIA gain settings of 142 k Ω , 166 k Ω , 200 k Ω and 250 k Ω
	CHANNEL_OFFSET_TIA2	12		
	GAIN_CALIB_LED_DC_142K	11		
	GAIN_CALIB_LED_DC_166K	11		
	GAIN_CALIB_LED_DC_200K	11		
	GAIN_CALIB_LED_DC_250K	11		
Per-phase enable for LED DC cancellation	LED_DC_EN_TIA1	1	Per-phase control (TIA specific)	Set to 1 for the TIA to which an LED DC cancellation loop must be assigned
	LED_DC_EN_TIA2	1		

Table 7-35. Automatic LED DC Cancellation - Register Controls (continued)

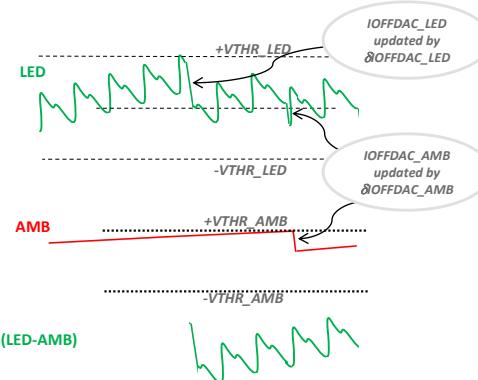
PARAMETER	REGISTER CONTROL	NO. OF BITS	CLASSIFICATION	COMMENTS
Re-convergence threshold	REG_RECONV_THR_LED_DC	8	Common setting for all loops	ADC code threshold (+/-) at which loop updates LED Offset DAC is set as $2^{13}x$ REG_RECONV_THR_LED_DC
LED DC cancellation loop output readout controls	IOFFDAC_LED_DC_READ	9	Target loop code	LED_DC_LOOP_NUM_READ specifies the target loop number (0..7). The current converged value of the LED Offset DAC for that Target loop can be read out on IOFFDAC_LED_DC_READ. The polarity can be read out on POL_LED_DC_READ.
	POL_LED_DC_READ	1	Target loop polarity	
	LED_DC_LOOP_NUM_READ	3	Specify target loop#	
Freeze LED DC cancellation loop	FREEZE_LED_DC_LOOP0.. FREEZE_LED_DC_LOOP7	8	Freeze loop	Freeze the LED DC cancellation loop number (0..7)

Figure 7-30 shows an illustration of how the Automatic LED DC cancellation functions across PRF cycles. The IOFFDAC_LED can get updated at the end of the LED phase if the residual input current (input current minus the current value of IOFFDAC_LED) exceeds the re-convergence threshold.

**Figure 7-30. Functioning of the Automatic LED DC Cancellation Across PRF Cycles**

7.3.10.3.1 Automatic LED DC Cancellation Using a Dummy LED Phase

Note that the Ambient DC level is common between the LED and Ambient phases, and therefore a change in the Ambient Offset DAC is transparent when the Ambient phase output is digitally subtracted from the LED phase output. However, a change in the LED Offset DAC happens only in the LED phase. Therefore, an update to the LED Offset DAC can cause a step change in the (LED-Ambient) data as shown in Figure 7-31.

**Figure 7-31. Glitch in (LED-AMB) Data When LED Offset DAC is Updated**

By introducing a ‘Dummy LED’ phase preceding the actual LED phase, and by setting the masking factor of the Dummy LED phase to a high enough value, a time window can be defined wherein the LED DC cancellation loop controlling the LED DC ceases to update the LED Offset DAC, thereby avoiding sudden jumps in the LED’s DC within this window. By setting an appropriate masking for the Dummy LED phases using the REG_PH_MASK_FACTOR, the update of the LED Offset DAC can be constrained to happen at the start of a time window corresponding to a set of PH_MASK_FACTOR PRF cycles. The heart rate estimation algorithm can do appropriate adjustment to the signal processing to deal with the potential steps in the LED data caused due to update in the LED Offset DAC at the start of this time window. Setting a high PH_MASK_FACTOR in the Dummy LED phase reduces the occurrence of the steps in the data, and also reduces the power overhead from having to fire the LED in the Dummy LED phase. However, the channel gain might need to be set to a low enough value that the drift in the LED phase DC over the time window does not cause the channel to saturate. It is also to be noted that the LED current setting must be same between the Dummy LED phase and the actual LED phase. [Figure 7-32](#) shows an illustration of how the Automatic LED DC cancellation using the Dummy LED phase functions across PRF cycles. The Dummy LED phase is shown to have a masking factor of 2 so that it is masked every alternate PRF cycle. A fresh update of the LED Offset DAC can happen during an active Dummy LED phase and the update gets applied to the succeeding LED phase until the next occurrence of the Dummy LED phase.

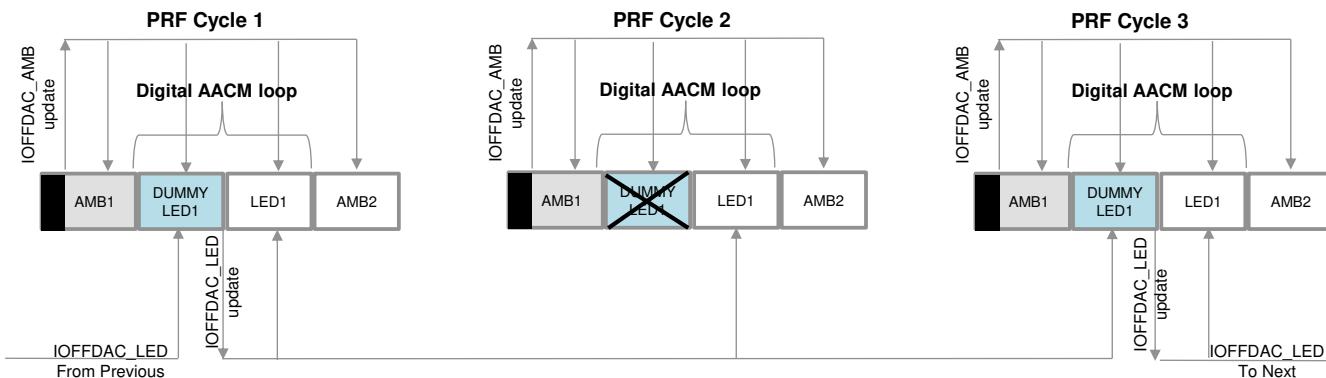


Figure 7-32. Functioning of the Automatic LED DC Cancellation Using the Dummy LED Phase Across PRF Cycles (in this Example the Dummy LED Phase is Set to Have a Masking Factor of 2)

Note that while operating in this manner with the Dummy phase also defined, the phases should be operated in a staggered manner so that the CONV signal of the Dummy LED phase completes before the start of the LED ON signal of the following LED phase.

7.3.10.3.2 Re-Convergence Threshold Setting for LED DC Cancellation

With the Automatic LED DC cancellation enabled, the effective input current to the TIA is the residual value of the PD current after subtraction of the converged value of the LED Offset DAC. The LED DC cancellation updates the LED Offset DAC based on the ADC output code exceeding a programmed re-convergence threshold value set by register REG_RECONV_THR_LED_DC, common for all the loops. The re-convergence threshold (RECONV_THR) in terms of ADC codes is set as $2^{13} \times \text{REG_RECONV_THR_LED_DC}$. So every time the ADC output code exceeds value corresponding to +/-RECONV_THR, the LED Offset DAC is updated so as to get the ADC output code close to 0. An illustration of LED DC Cancellation is shown in [Figure 7-33](#) and [Figure 7-34](#) for two cases – (i) Dummy LED phase is not used (ii) Dummy LED phase is used in conjunction with a masking factor. In (i), the LED Offset DAC gets updated every time the re-convergence threshold is crossed, whereas in Case (ii), the LED Offset DAC updates happen only if the re-convergence threshold is crossed during the PRF cycle during which the Dummy LED phase is unmasked.

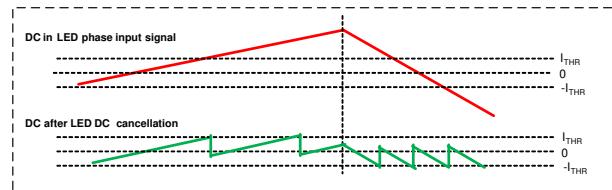


Figure 7-33. Illustration of LED DC Cancellation When Dummy LED Phase is Not Used

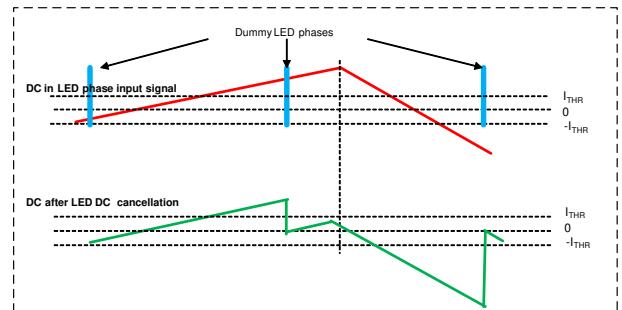


Figure 7-34. Illustration of LED DC Cancellation When Dummy LED Phase is Used

7.3.10.3.3 Calibration for Automatic LED DC Cancellation

The detection of the ambient current reaching the re-convergence threshold and the subsequent cancellation is achieved by the LED DC cancellation loop through monitoring the ADC output code in the LED phase and incrementing or decrementing the LED Offset DAC code. Since the transfer function between the LED Offset DAC code and the ADC output code is affected by part-to-part variations in gain (R_F) and Offset DAC, as well as channel offset, it is required that the MCU run a calibration routine after device power up, and writes calibration words into designated registers. These calibration words serve as reference for the LED DC cancellation loop(s) to accurately translate the ADC output code to an appropriate increment/ decrement to the LED Offset DAC in order to cancel the DC from the LED. The calibration word can be written one-time as part of the device initialization and left unchanged subsequently. Note that the registers get erased every time the device is power cycled or when it comes out of the hardware power-down mode, and therefore need to be re-written. There are 2 sets of calibration words:

1. Gain calibration words: The 4 words (GAIN_CALIB_LED_DC_142K, GAIN_CALIB_LED_DC_166K, GAIN_CALIB_LED_DC_200K, GAIN_CALIB_LED_DC_250K) are a representation of the ADC code change caused by 1 LSB change (approximately 125 nA) to LED Offset DAC when R_F is set to 142 kΩ, 166 kΩ, 200 kΩ, 250 kΩ respectively. The AFE automatically scales the value of the appropriate GAIN_CALIB_LED_DC* word based on R_F set for a particular loop.
2. Offset calibration word for each TIA that is used (CHANNEL_OFFSET_TIA1...CHANNEL_OFFSET_TIA2).

A coarse functioning of the LED DC cancellation loop can be achieved by setting the Offset calibration words to '0' and by setting GAIN_CALIB_LED_DC_250K to a decimal value of 109226 (scale the other 3 words in the R_F ratio).

For a more accurate functioning of the LED DC cancellation, TI strongly recommends to run a calibration routine on start-up to accurately determine the calibration words. The calibration routine is described below:

1. Set the PD_DISCONNECT mode to disconnect all the PDs from the TIA.
2. Regardless of polarity of the PD connection to the AFE input pins, set POL_OFFSETDAC_LED to '0' while performing calibration. Also ensure that LED Offset DAC of TIA1 is enabled (EN_LED_OFFSETDAC_TIA1 =1).
3. To generate the GAIN_CALIB_LED_DC_250K calibration word, program the AFE to operate with two phases (REG_NUMPHASE = 1) both with NUM_TIA = 2 and the R_F for all TIAs set to 250 kΩ. Using the Manual MCU control mode, set the LED Offset DAC to 0 LSB and 1 LSB in the two phases respectively for all TIAs. The Ambient Offset DAC should be set to 0 μA during this calibration. Program the LED Offset DAC currents as shown in Table 7-36.

Table 7-36. Configuration of Phase Settings in the Calibration Routine for Automatic LED DC Cancellation

PHASE NO.	1	2
IOFFDAC_LED_TIA* (set) ⁽¹⁾	00000000	00000001
Measured Output code (22-bit) ⁽²⁾	CODE1	CODE2

(1) Set POL_OFFSETDAC_LED to 0

(2) 2 sets of codes, one corresponding to each TIA

4. Derive GAIN_CALIB_LED_DC_250K and channel-specific CHANNEL_OFFSET_TIA* words as shown in Figure 7-35

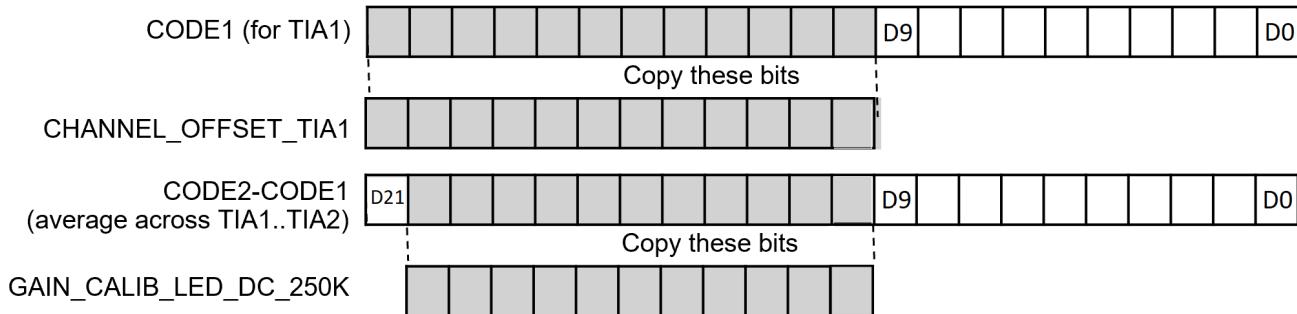


Figure 7-35. Derivation of GAIN_CALIB_LED_DC_250K and CHANNEL_OFFSET* Words

5. To derive the other Gain calibration words, repeat steps 1..4 with the R_f setting appropriately changed. For example to derive the GAIN_CALIB_LED_DC_200K word, set the R_F to 200 kΩ. The CHANNEL_OFFSET_TIA* words do not need to be recalculated.

7.3.10.4 Dynamic Range Extension Mode

The Automatic LED DC cancellation mode introduces a step in the LED phase data every time the LED Offset DAC is updated. By enabling the Dynamic Range Extension (DRE) mode, the steps can be removed and the dynamic range of the AFE can be significantly increased for a smooth, step-free operation over a dynamic range which is several times higher than the dynamic range of the ADC. What this achieves in effect is an ability to operate at a high TIA gain setting (which results in low noise operation) while extending the dynamic range to a value corresponding to a low TIA gain setting. The dynamic range can be extended up to a factor of 64, which means that a dynamic range of up to 32 μA can be achieved for a TIA gain setting of 1 MΩ which can otherwise support an input dynamic range of only 0.5 μA.

Figure 7-36 shows the DRE scheme.

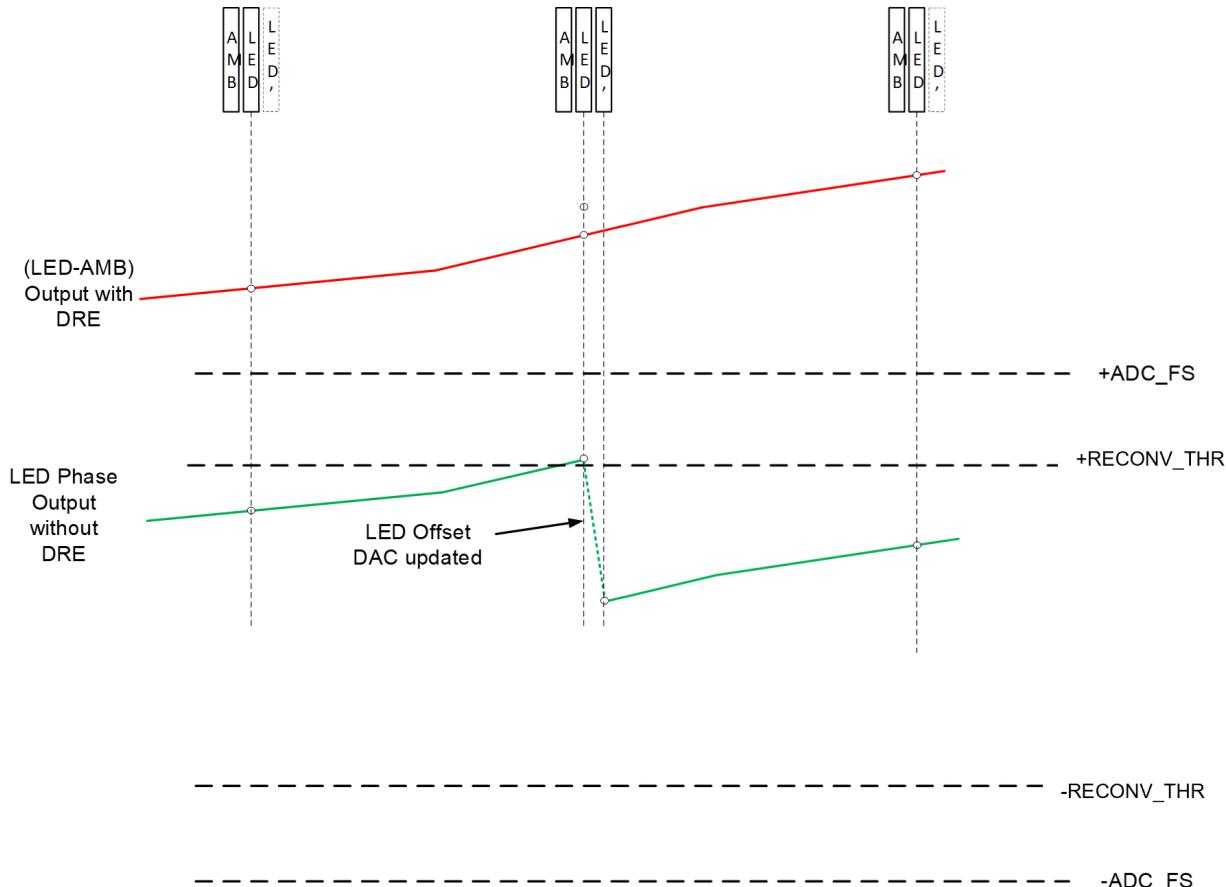


Figure 7-36. Illustration of the Dynamic Range Extension (DRE) Mode

The DRE mode is enabled through the following means:

1. For the phase for which the DRE logic must be enabled, set the per-phase ENABLE_DRE bit to 1. The DRE logic gets applied to the TIAs for which the LED DC cancellation has been enabled (`LED_DC_EN_TIA*=1`) in that phase.
2. The DRE logic automatically reserves a time window for a second LED firing (LED') which is the On-demand LED phase. While the main LED phase is fired in every PRF cycle, the On-demand LED phase is fired only on-demand whenever there is an update of the LED Offset DAC by the LED DC cancellation loop as determined based on the ADC output of the first LED phase. A firing of LED' can result from an update of the LED Offset DAC from at least one of the LED DC cancellation loops (associated with one of the TIAs).
3. The time window for the LED' phase comprises the sampling window as well as convert windows for all the active TIAs (`=NUM_TIA`) for that phase, including those that do not have associated LED DC cancellation. However, out of all the reserved convert phases, the ADC conversion happens only for the TIA phases which are either associated with a LED DC cancellation loop or have an LED Offset DAC updated in that PRF cycle.
4. Set REG_SCALE_DRE register word (common for all the loops) to represent the factor by which the Dynamic range is to be extended. The dynamic range gets extended by a factor `SCALE_DRE` equal to $2^{\text{REG_SCALE_DRE}}$. `REG_SCALE_DRE` takes values from 0 to 6, resulting in `SCALE_DRE` taking values from 1 to 64. The ADC range is extended to represent the extension of the AFE dynamic range by right-shifting the bits by a number of bits equal to `SCALE_DRE`. The 22-bit output of the AFE is now a representation of the extended dynamic range. [Figure 7-37](#) shows the right-shifting of the bits to accommodate the dynamic range extension for a case where `SCALE_DRE` is programmed to 8. Setting the USE_MSB_FOR_DRE bit to 1 remaps the DRE code to the D23 through D0 bits.

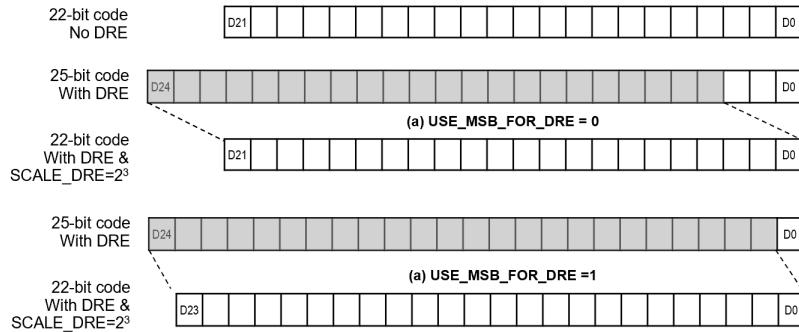
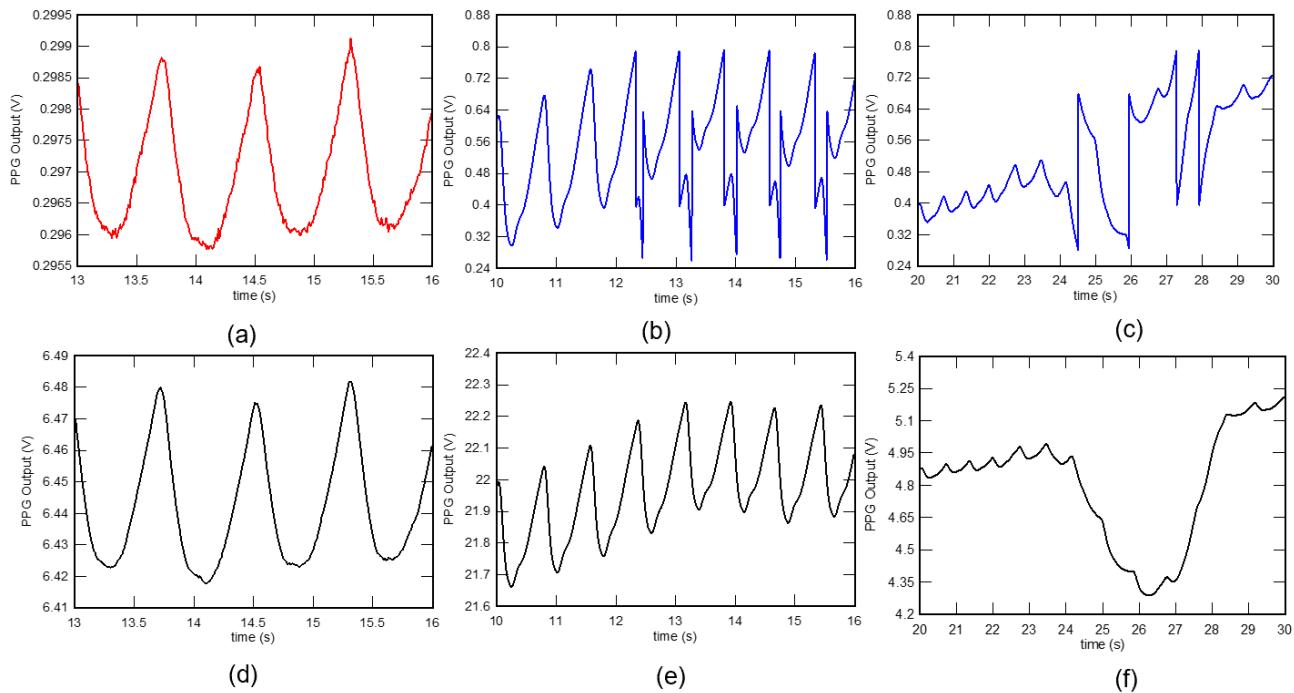
**Figure 7-37. Right-Shifting of Bits with DRE Enabled and SCALE_DRE set to 2³**

Figure 7-38 shows the PPG raw data for a few cases.

(a) $R_F=25\text{ k}\Omega$, No DRE: The PPG signal is seen to be within the full scale range but the AC signal is small and noisy.

(b) and (c) $R_F = 500\text{ k}\Omega$, With Automatic LED DC cancellation enabled but DRE disabled. The AC signal has gotten amplified but the steps because of the LED offset DAC updates cause the PPG signal to become distorted.

(d), (e) & (f) $R_F = 500\text{ k}\Omega$, With Automatic LED DC cancellation, DRE enabled: The amplified AC signal is fully restored and the steps are completely removed by enabling the DRE.

**Figure 7-38. PPG Raw Data Without and With DRE Enabled****Note**

When the DRE mode is enabled, any transient that causes saturation of the signal chain can result in the DC information to get lost. In such a case, the output code (after processing by the DRE logic) is not a true indicator of the DC level of the signal.

7.3.11 PPG Data Rate Controls

By default, each PPG phase results in an ADC conversion that generates a sample that can be configured to stream into the FIFO. The AFE has controls for controlling the ADC conversion rate (signal acquisition rate) as well as the output data rate. The output data rate for can be controlled using the PPG decimation filters. There are 8 such filters, each of which can be used to decimate data associated with any PPG phase (such data can, for example correspond to LED minus Ambient). Additionally, the acquisition rate of any of the phases can be controlled using per-phase masking controls. Masking a given PPG phase with a programmable masking factor results in a combination of PRF cycles of normal operation of that phase interspersed with PRF cycles where the operations of LED ON, SAMP and CONV associated with that phase are masked.

7.3.11.1 PPG Decimation

The signal bandwidth of interest for a PPG signal is usually 20 Hz or lower. Operating at a higher data rate helps lower the noise in the bandwidth of interest and results in improved SNR. However, operating at a higher data rate also fills up the FIFO faster and results in higher FIFO readout rates which increases the system level power consumption. To reduce the output data rate while still achieving the in-band SNR benefits from operating at a higher acquisition rate, the AFE has a decimation feature. The decimation filter is a moving average filter which averages the successive samples from the signal and generates a data stream at a lower rate.

The device has a total of 8 PPG decimation filters. For a given phase, use the REG_DEC_FACTOR as a control to enable and disable decimation and set the desired decimation factor commonly for all the active TIA signals for that phase. The decimation factor refers to the number of PRF cycles over which the averaging operation is done. The data used for decimation is same as the FIFO data specified through the FIFO_DATA_CTRL for that phase. The decimation filter performs a moving average of the output code from that PPG phase across PRF cycles. When decimation is enabled, the periodicity of the data from that PPG phase entering the FIFO automatically scales down by a factor equal to the decimation factor. For example, when the decimation factor is set to 4, the periodicity of the data from that phase becomes PRF / 4. The data enters the FIFO only every 4th PRF cycle in a manner similar to the masking mode.

The REG_DEC_FACTOR controls are shown in [Table 7-37](#).

Table 7-37. REG_DEC_FACTOR Controls

REG_DEC_FACTOR	NO. OF SAMPLES AVERAGED (DECIMATION FACTOR)
0	1 (No Decimation)
1	2
2	4
3	8
4	16
5	32
Other settings	Do not use

The decimation filters get assigned in the sequence of the phases (each active phase with a non-zero REG_DEC_FACTOR gets one decimation filter assigned to each active TIA in that phase). There are only a total of 8 decimation filters available, and ensure that the number of signals with decimation enabled should be 8 or lower.

Note

PPG decimation cannot be used on a phase for which phase masking is programmed.

Note

While using the LED offset DAC, the PPG output can have a tone at a frequency of PRF/2. This tone can be removed by enabling decimation (with any decimation factor from 2 to 32).

7.3.11.2 PPG Phase Masking

By default, each defined PPG phase in a PRF cycle results in a signal acquisition and generation of a data word. The data rate of each PPG signal is equal to the PRF rate. A Per-phase PPG masking mode can be programmed individually for each PPG phase-set to control the signal acquisition (and output data) rate for that phase-set relative to the PRF. When a PPG phase-set is masked, signals for that phase-set continue to occupy the designated timeslots but do not perform any associated operations (for example LEDs turning on or the ADC converting). This applies to S₀, S_{PRE} and S_{POST}. Also, a masked phase does not result in a FIFO sample.

By default, the last PRF cycle of the repeating sequence contains the unmasked PPG phase. By setting the global bit MASK_REVERSE bit to '1', the first PRF cycle of the repeating sequence can be set as the unmasked (active) phase and the later phases become masked phases.

Table 7-38 lists the Per-phase PPG masking modes that can be programmed through per-phase register control REG_PH_MASK_FACTOR. This table corresponds to the case where MASK_REVERSE is set to '1'.

Table 7-38. Masking Controls for a PPG Phase (MASK_REVERSE Set to 1)

REG_PH_MASK_FACTOR	MASKING MODE	MASKING FACTOR PH_MASK_FACTOR	COMMENTS
0	Never mask	1	Never mask the phase
1	2X	2	Mask phase in the last cycle of every 2 PRF cycles
...			
M	2 ^M X	2 ^M	Mask phase in the last (2 ^M -1) cycles of every 2 ^M PRF cycles
...			
10	1024X	1024	Mask phase in the last 1023 cycles of every 1024 PRF cycles
11-15	Always mask		Always mask the phase

Figure 7-39 shows an example where Phase 1 and Phase 5 are never masked), Phase 2 is set to 2X masking, Phase 3 is set to 4X masking and Phase 4 is always masked. In this example, MASK_REVERSE is set to 1.

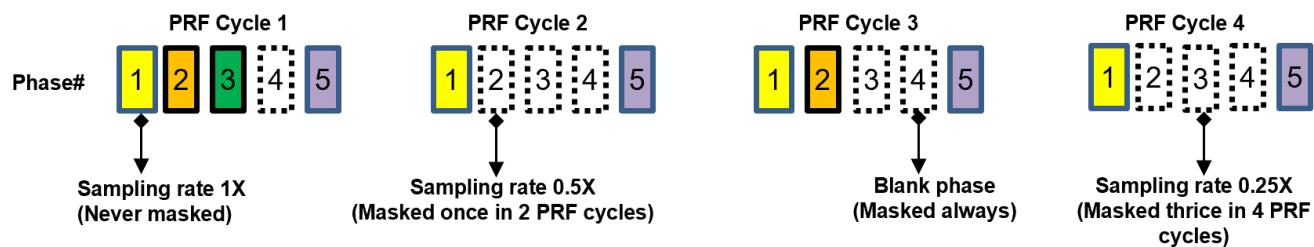


Figure 7-39. Illustration of Masking Modes (MASK_REVERSE set to '1')

The masking mode can be applied in certain use cases that include:

1. Setting acquisition rate of different PPG sensors to different values
2. Setting rate of Dummy ambient phase higher than the other signal phases so that the AACM loop updates faster.
3. Setting rate of Dummy LED phase lower than actual LED phase to limit update rate of LED DC cancellation loop

When using masking, the number of FIFO samples is likely to change across PRF cycles. To simplify the software handling of the FIFO data, TI recommends that the watermark level be chosen such that the data from an integer number of PRF cycles fills the FIFO up to the watermark level, and the arrangement of signals up to the watermark level constitutes a repetitive pattern that serves a template for how a block of FIFO data must get split into the constituent data streams. While choosing large masking factors, meeting this constraint cannot be possible. In such cases, the MCU can handle the additional complexity of mapping the FIFO data to constituent data streams.

7.3.12 PPG Threshold Detection

The AFE has threshold detection modes using which of the levels of the signal in a phase can be compared with pre-programmed threshold levels and an interrupt can be generated to alert the MCU. For example, the signal levels in a phase can be low when the sensor is left open, not worn, but increase when worn by the user. The threshold detection can be used to generate an interrupt to wake up the MCU. The AFE has two threshold detect modes. In single-phase threshold detect, output of any one phase is used for threshold detection. In combinational threshold detect, a logical combination of threshold detection across multiple phases can be used for interrupt generation.

7.3.12.1 Single-Phase Threshold Detect Mode

The device has a single-phase threshold detect mode that can be enabled by setting the THR_DET_EN register bit. In this mode, the device compares the output code of the selected phase-set with respect to a programmed set of lower and upper limits. Based on the comparison, a THR_DET_RDY interrupt goes high during the corresponding window of the DATA_RDY pulse of that PRF cycle. The number of the phase-set, the data from which is to be used for the threshold detect comparison is as (REG_THR_DET_PHASE+1) where the register takes values from 0 to 15. The output of the TIA# is to be used for the threshold detection is specified using the per-phase parameter THR_SEL_TIA_NUM (value from 0 to 1). The appropriate data associated with the phase selected for threshold detection is set by the per-phase control THR_SEL_DATA_CTRL, as shown in [Table 7-39](#).

Table 7-39. Manner in Which the Data from Phase Selected for Threshold Detection is Used for Comparison

THR_SEL_D ATA_CTRL	WHICH DATA IS USED FOR COMPARISON IN THE PHASE ⁽¹⁾				
	STAGGERED MODE		HIGH PRF MODE	MAXIMUM AMBIENT REJECTION MODE	
	WITH POST-AMBIENT	WITHOUT POST-AMBIENT		WITH POST-AMBIENT	WITHOUT POST-AMBIENT
0	Not used		Not used	Not used	Not used
1	S ₀ ⁽²⁾	S ₀ ⁽²⁾	S ₀	Do not use	Do not use
2	S ₀ -S ₋₁ ⁽²⁾	S ₀ -S ₋₁ ⁽²⁾	S ₀ -S ₋₁	Do not use	S ₀ -SPRE
3	S ₀ -(S ₋₁ +S ₋₂)/2 ⁽²⁾	Do not use	Do not use	S ₀ -(SPRE+SPOST)/2	Do not use

(1) The definition of S₀, S₁, and S₋₁ are same as in the table specifying FIFO_DATA_CTRL.

(2) Not supported if DRE is enabled.

The data as selected from [Table 7-39](#) for the chosen phase can be compared against a set of signed 12-bit codes called HIGH_THRESHOLD_CODE1 and LOW_THRESHOLD_CODE1. The THR_DET_RDY is generated if the output word (signed) constructed using the 12 MSBs of the 22-bit output code of the threshold detection phase falls within the programmed high and low thresholds. By programming the THR_SEL_LOGIC bit to '01', the THR_DET_RDY can be made to get generated if the output word falls outside the high and low thresholds.

7.3.12.2 Combinational Threshold Detect Mode

The device has a combinational threshold detect mode that can be enabled by setting the THR_DET_EN and COMB THR_DET_EN register bits. In this mode, the device compares the output code of a selected combination of phases with respect to a programmed set of lower and upper limits. Based on the combination of comparisons, a THR_DET_RDY interrupt is generated. The per-phase THR_SEL_DATA_CTRL and THR_SEL_TIA_NUM determine the manner in which the data from a phase can be used for the comparison. This data can be compared against either of two sets of 12-bit codes (selection of which set to use is based on the per-phase register bit THR_SEL).

Table 7-40. Selection of High and Low Thresholds for a Phase

THR_SEL	12-BIT HIGH CODE USED FOR COMPARISON	12-BIT LOW CODE USED FOR COMPARISON
0	HIGH_THRESHOLD_CODE1	LOW_THRESHOLD_CODE1
1	HIGH_THRESHOLD_CODE2	LOW_THRESHOLD_CODE2

The result from the comparison of Phase N is stored in a register flag THR_PPG_FLAG[N-1] (N from 1..12) which can be read out through the I2C and SPI. For example, the result of comparison of Phase 1 is stored in the register flag THR_PPG_FLAG[0]. By default, the THR_DET_RDY interrupt is generated if all of the selected phases are within the range as set by the respective low and high threshold codes. The manner of combining the different checks to generate the THR_DET_RDY can be altered by using the register control THR_SEL_LOGIC as shown in [Table 7-41](#).

Table 7-41. Register Control for Setting the Combination Logic for the Combinational Threshold Detect

THR_SEL_LOGIC REGISTER SETTING (IN BINARY)	CONDITION USED FOR THR_DET_RDY GENERATION
00	ALL of the chosen checks IN range
01	ANY of the chosen checks OUT of range
10	ANY of the chosen checks IN range
11	ALL of the chosen checks OUT of range

7.3.13 First-In, First-Out (FIFO) Block

7.3.13.1 FIFO Pointers and Watermark Level

The AFE has a 160-sample FIFO that can be used to store data from the various signal acquisitions. Data from each signal chain streams into the FIFO in the sequence and is generated. Each sample corresponds to a 3-byte ADC word. The FIFO read and write pointers are reset to 0 whenever a hardware or software reset is applied. When the FIFO is enabled by setting the FIFO_EN bit to 1, the write pointer starts to progress whenever a data word streams into the FIFO. The read pointers progress when a data word is read out from the FIFO.

The FIFO_RDY interrupt is an indicator to the MCU to read out the data from the FIFO and can be made to be output on one of the output pins (see [Interrupts](#)). Note that the AFE can also output interrupts other than FIFO_RDY depending on the state of the interrupt selection mux. For example, by default, the ADC_RDY pin outputs a DATA_RDY interrupt once in every PRF cycle. The MCU can take care to not treat such interrupts as FIFO_RDY interrupts, and avoid reading data from the FIFO. This inadvertent readout of data from the FIFO based on an interrupt that is not the FIFO_RDY interrupt can result in a mismatch in the FIFO phase ordering. This situation can be avoided by configuring the interrupt mux to output the FIFO_RDY interrupt on the desired pin before the FIFO is enabled.

The FIFO_RDY gets generated when the difference between the write and read pointers exceeds a programmed Watermark (WM) level referred to as WM_FIFO. The REG_WM_FIFO register control sets the Watermark level (WM_FIFO) to be equal to (REG_WM_FIFO+1). With WM_FIFO thus set, the FIFO_RDY interrupt is now an indication to the MCU that a number of samples equal to WM_FIFO are ready to be read out. The position of the FIFO_RDY within the PRF cycle is fixed to come after the last defined phase and before the start of the deep sleep window. If the MCU fails to start reading before the completion of the active window of the next PRF cycle, then the FIFO_RDY interrupt repeats and keeps repeating in every subsequent PRF cycle until sufficient samples have been read out and the pointer difference has dropped below the watermark level. WM_FIFO can be chosen such that the FIFO fills to the Watermark level on completion of an integer number of PRF cycles.

The instantaneous difference between the write and read pointers can be read out through an 8-bit register REG_POINTER_DIFF. The difference between the write and read pointers (POINTER_DIFF) is equal to (REG_POINTER_DIFF+1). On receiving a FIFO_RDY, the MCU can read out this register (prior to reading out the FIFO) to confirm that POINTER_DIFF is indeed equal to WM_FIFO. [Figure 7-40](#) illustrates the case of how the FIFO_RDY interrupt gets generated in the Watermark FIFO mode for a case where WM_FIFO is set to 32. In this example, the MCU is shown as reading only 8 samples after receipt of the first FIFO_RDY. Note that in this example, only 1 data sample is stored in the FIFO in every PRF cycle and so the write pointer advances by 1 in every PRF cycle.

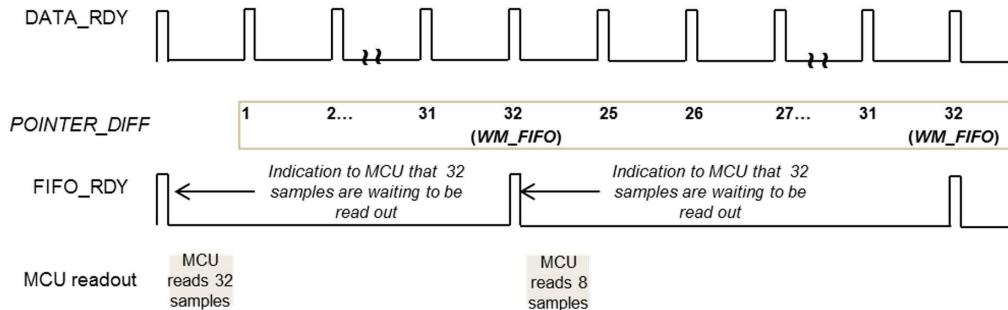


Figure 7-40. FIFO Mode Based on Programmable Watermark Level

7.3.13.2 FIFO Overflow Indicator

A register bit FIFO_OVERFLOW can be read out to check for a FIFO overflow condition. The FIFO_OVERFLOW bit goes high as soon as the pointer difference exceeds 160 and stays high for the entire duration of overflow. To come out of the overflow condition, the MCU can disable and re-enable the FIFO (using the FIFO_EN bit) and causes the FIFO pointer difference and FIFO overflow bit to get reset to 0.

7.3.13.3 FIFO Interrupt Masking

The generation of FIFO_RDY interrupt can be masked using the MASK_FIFO_RDY register control. Such masking can be useful in cases where the MCU is not interested in reading data from the AFE for a period of time but can retrieve prior data stored in the FIFO when reading starts again. To achieve this, the read pointer can be forced relative to the write pointer by setting the FORCE_FIFO_OFFSET to '1', and then programming FIFO_OFFSET_TO_FORCE to force the location of the read pointer relative to current location of write pointer.

The recommended method of achieving the masking is shown in Figure 7-41. In this figure, the AFE has been configured to output a THR_DET_RDY interrupt which can be an indication to the MCU that the signal level in a particular phase has crossed a certain threshold and the MCU must wake up and read the FIFO data. Since the THR_DET_RDY interrupt is also positioned at the start of the deep sleep window, and is an indication to the MCU that the FIFO has been most recently updated with a full PRF cycle of data. The MCU must complete all the indicated register write and FIFO read before the end of the deep sleep window before unmasking the FIFO_RDY interrupt.

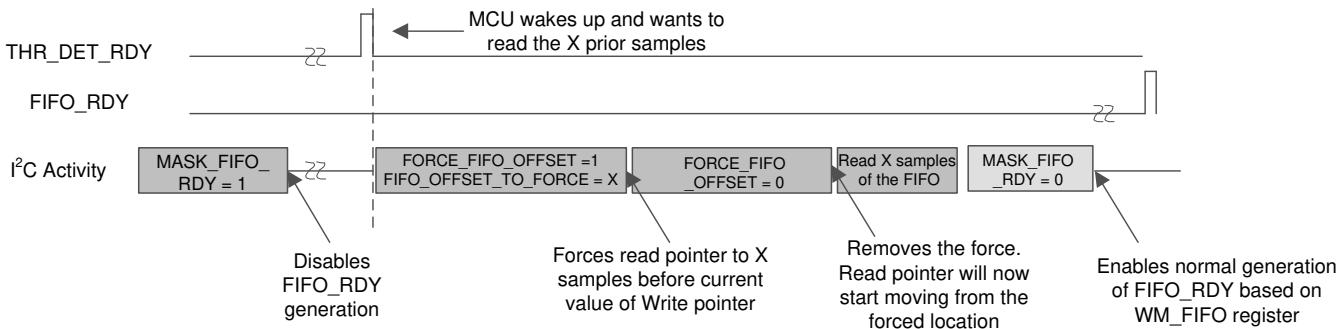


Figure 7-41. Method of Resuming FIFO Read Following a FIFO_RDY Masking Phase

When the MCU continues accesses the FIFO but cannot start reading out data before the start of the next PRF cycle, the repetitive interrupts can be undesirable. To prevent the occurrence of repetitive interrupts, an AUTO_MASK_FIFO_RDY bit can be set, to '1'; when set, only the first FIFO_RDY interrupt is given out. Subsequent interrupts are masked. To unmask the FIFO_RDY interrupt generation, the MCU must set this bit to '0' for a duration of at least one PRF cycle and then to '1' after the interrupt is serviced by reading the FIFO data.

7.3.13.4 FIFO Data Tagging

A frame sync indicator tag to indicate the first FIFO sample from a PRF cycle can be enabled by setting the EN_FRAME_SYNC bit to '1'. By default, the MSB bit (D23) is replaced by the frame sync indicator tag, which is

set to '1' for the first FIFO word in a PRF cycle, and set to '0' for other words in that cycle as shown in Figure 7-42.

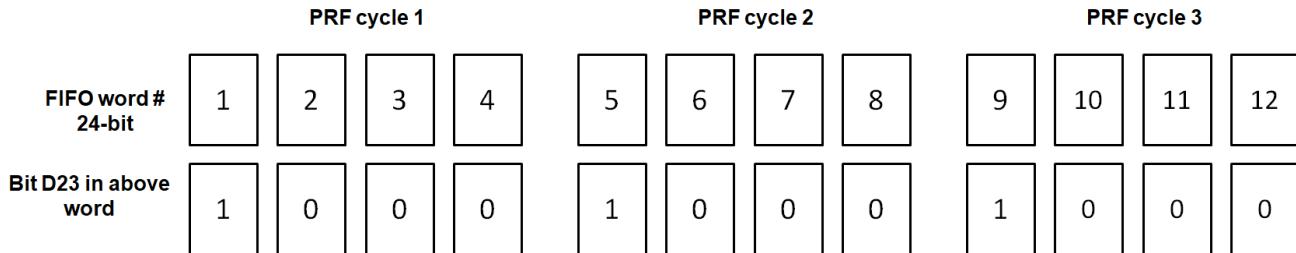


Figure 7-42. Scheme for Frame Synchronization

By additionally setting the FRAME_SYNC_ON_LSB bit to 1, the frame sync indicator can be made to replace the LSB (Bit D0) instead of the MSB (D23).

A ‘LED Offset DAC update’ tag to indicate whether the sample corresponds to an update of the LED offset DAC can be enabled by setting the EN_LED_OFFSETDAC_MARKER bit to ‘1’. By default, D23 is replaced by the LED Offset DAC update tag, which is set to ‘1’ for the data sample where the LED DC cancellation loop has updated the LED Offset DAC. By additionally setting the LED_OFFSETDAC_MARKER_ON_LSB bit to 1, the LED Offset update tag can be made to replace D0 instead of D23.

7.3.14 Interrupts

Several useful interrupts can be made to output on the ADC_RDY and GPIO2 pins. There are two types of interrupts:

- Dedicated interrupts
 - Single-pin (shared) interrupts

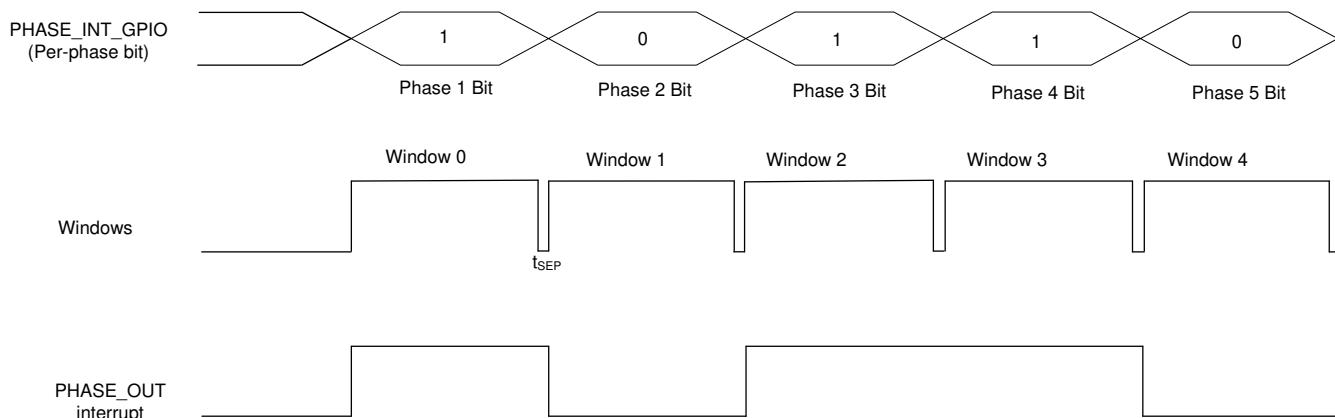
7.3.14.1 Dedicated Interrupts

Dedicated interrupts refer to interrupts that output on the ADC_RDY or GPIO2 pin based on the same logical condition every time. Dedicated interrupts are listed in [Table 7-42](#).

Table 7-42. Types of Dedicated Interrupts

INTERRUPT	DESCRIPTION	POSITION
DATA_RDY	Interrupt that comes out at the same rate as the output data rate. Rate is equal to the PRF.	DATA_RDY pulse
FIFO_RDY	Interrupt issued when the Watermark level is reached	Same as DATA_RDY pulse (delayed by 1 count)
THR_DET_RDY	Threshold detect interrupt applicable when the device is in threshold detect mode; goes high during the corresponding DATA_RDY window in the periods where the threshold comparisons result in a TRUE	Same as DATA_RDY pulse (delayed by 1 count)
INT_OUT2	Interrupt that is generated as a pulse every period.	Set through timing counts of PRF counter as PROG_INT2_STC to PROG_INT2_ENDC + 1
PRF_RST	An interrupt that is generated to mark the start of the PRF cycle, which can be used to synchronize the PRF cycles between two devices in parallel operation	Start of every new PRF cycle
PHASE_OUT	Phase-based interrupt that is generated on a per-phase control bit PHASE_INT_GPIO	Goes high in all the phase windows where the PHASE_INT_GPIO bit is high

The PHASE_OUT interrupt can be made to go high during any PPG signal phase by setting the per-phase PPG control bits PHASE_INT GPIO. An illustration of the PHASE_OUT interrupt is shown in Figure 7-43.

**Figure 7-43. Generation of PHASE_OUT Interrupt Based on the Per-Phase PPG Control**

The register controls for the selection of interrupts on the various output pins is shown in [Table 7-43](#) and [Table 7-44](#).

Table 7-43. Selection of Interrupts Output on the ADC_RDY Pin

INT_MUX_ADC_RDY	INTERRUPT OUTPUT ON ADC_RDYPIN ⁽¹⁾	ADDITIONAL CONTROL SREQUIRED
000	DATA_RDY	—
001	THR_DET_RDY	Set THR_DET_EN = 1
010	FIFO_RDY	Set FIFO_EN = 1
011	INT_OUT2	
100	PRF_RST ⁽²⁾	INPUT_PRF_RST_ON_GPIO2 = '0'
Other settings	Do not use	

(1) When the EN_GPIO2_INT_ON_ADC_RDY bit is set to '1', the interrupts on ADC_RDY is determined by [Table 7-44](#).

(2) PRF_RST corresponds to a pulse that is synchronized to the start of the PRF cycle. AFE is PRF_RST source in a parallel AFE configuration.

Table 7-44. Selection of Input/ Output on GPIO2 Pin

EN_GPIO2_I	EN_GPIO2_OUT	INT_MUX_GPIO2	EN_PHASE_INT_GPIO	EN_OSCL_CLKOUT	GPIO2 – INPUT OR OUTPUT	OUTPUT ON GPIO2	INPUT ON GPIO2	ADDITIONAL CONTROL REQUIRED ^{(1) (2)}
0	1	x	1	0	OUTPUT	PHASE_OUT		
0	1	x	0	1	OUTPUT	CLK_256KHz		
0	1	000	0	0	OUTPUT	INT_OUT2		
0	1	001	0	0	OUTPUT	DATA_RDY		
0	1	010	0	0	OUTPUT	THR_DET_RDY		THR_DET_EN = 1
0	1	011	0	0	OUTPUT	FIFO_RDY		FIFO_EN = 1
1	0	x	0	0	INPUT		PRF_RST ⁽³⁾	INPUT_PRF_RST_ON_GPIO2 = '1'

(1) While operating in the Single-shot clocking mode, additionally set EN_INT_IN_SINGLE_SHOT register bit to '1' and position the interrupt before the start of the deep sleep window. The start and end counts are based on the internal (256 kHz) clock.

(2) Interrupts programmed to come out on the GPIO2 pin can be made to come out on ADC_RDY pin by setting the EN_GPIO2_INT_ON_ADC_RDY bit to '1'

(3) PRF_RST corresponds to a pulse that is synchronized to the start of the PRF cycle. AFE is PRF_RST secondary in a parallel AFE configuration.

7.4 Device Functional Modes

7.4.1 Power Modes

The AFE has the following power modes:

1. Normal mode.
2. Software power-down mode: Can be enabled by setting the PDNAFE bit to '1'. Additionally set the PDN_BG_IN_DEEP_SLEEP to '1' and the PDN_OSCL_IN_DEEP_SLEEP bit to '0' to get to the lowest power.

7.4.2 RESET Modes

The AFE has internal registers that must be reset before valid operation. The registers can be reset using a self-clearing SW_RESET register bit.

7.4.3 Clocking Modes

The AFE has the following clocking modes:

1. *Internal oscillator mode*: This is the default mode. The internal 256 kHz oscillator is made active and the timing engine runs on this oscillator. All the timing counts are referenced to the oscillator. The PRF setting by PRPCT is also based on the oscillator.
2. *External clock mode*: A free running clock on the CLK pin is used for the timing engine and the PRF counter. Timing counts and PRF setting are based on the external clock.
3. *Single-shot mode*: A high pulse on CLK pin triggers a fresh set of signal acquisition. The 256 kHz oscillator is kept active until start of the deep sleep window. Timing counts are based on the 256 kHz oscillator. However, periodicity of signal acquisition is determined by the separation of the pulses on CLK pin.
4. *Mixed clock mode*: A free running clock on the CLK pin is used by the PRF counter to set the PRF. The timing engine runs on the internal 256 kHz oscillator.

7.4.4 Parallel AFE Operation Modes

AFE4432 provides a synchronized way to operate two AFEs in either sequential or concurrent mode:

1. Parallel AFEs with sequential operation.
2. Parallel AFEs with concurrent operation.

7.4.4.1 Parallel AFEs with Sequential Operation

[Figure 7-44](#) shows two AFEs connected to operate with sequential active phases. AFE1 is operated in the mixed clock mode with 32.768 kHz RTC clock on CLK pin. The 256 kHz clock of AFE1 is output on GPIO2. The GPIO2 pin of AFE1 is connected to the CLK pin of AFE2. AFE2 is operated in external clock mode. Programmable interrupt INT_OUT2 from AFE1 is positioned to come after the active phases of AFE1, and is routed from the ADC_RDY pin of AFE1 to the GPIO2 pin of AFE2. Configure GPIO2 as an input pin. Configure AFE2 so that the interrupt on GPIO2 serves as a PRF reset pulse for AFE2. [Figure 7-45](#) shows the timing scheme.

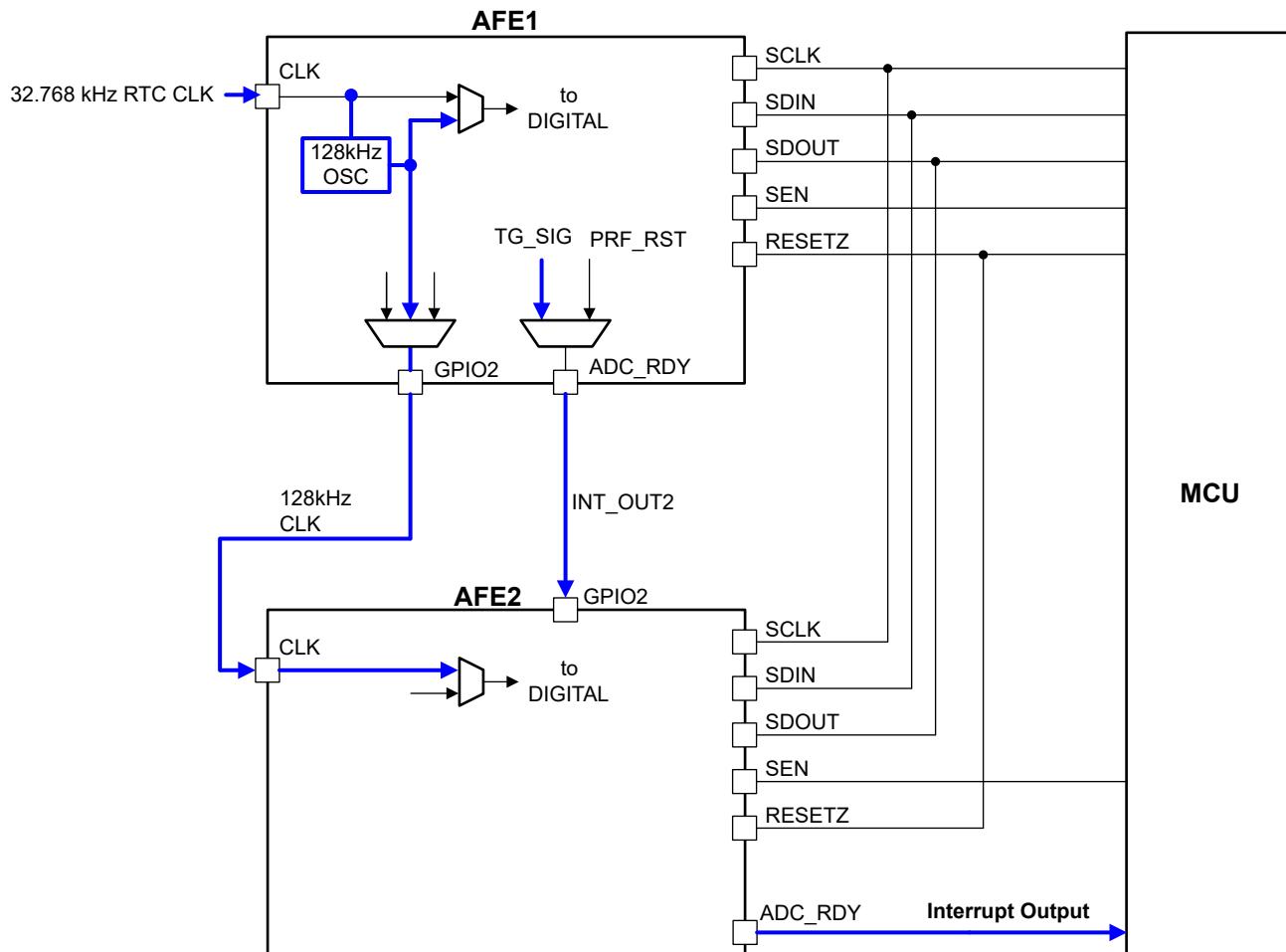


Figure 7-44. Two AFEs Connected to Operate with Sequential Active Phases

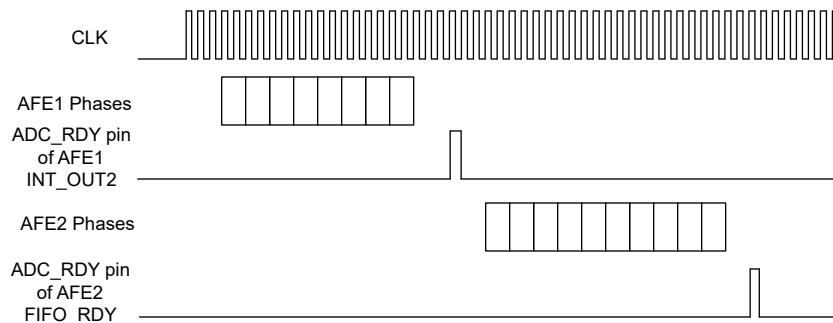


Figure 7-45. Timing for Two AFEs Connected to Operate with Sequential Active Phases

7.4.4.2 Parallel AFEs with Concurrent Operation

Figure 7-46 shows two AFEs connected to operate with concurrent active phases. AFE1 is operated in the mixed clock mode with 32.768 kHz RTC clock on CLK pin. The 256 kHz clock of AFE1 is output on GPIO2. The GPIO2 pin of AFE1 is connected to the CLK pin of AFE2. AFE2 is operated in external clock mode. An interrupt PRF_RST (timed at the reset point of the PRF counter of AFE1) is output on the ADC_RDY pin of AFE1. This PRF_RST is connected to the GPIO2 pin of AFE2. Configure GPIO2 of AFE2 as an input pin. Also configure AFE2 so that the interrupt on GPIO2 serves as a PRF reset pulse for AFE2. Figure 7-47 shows the timing scheme.

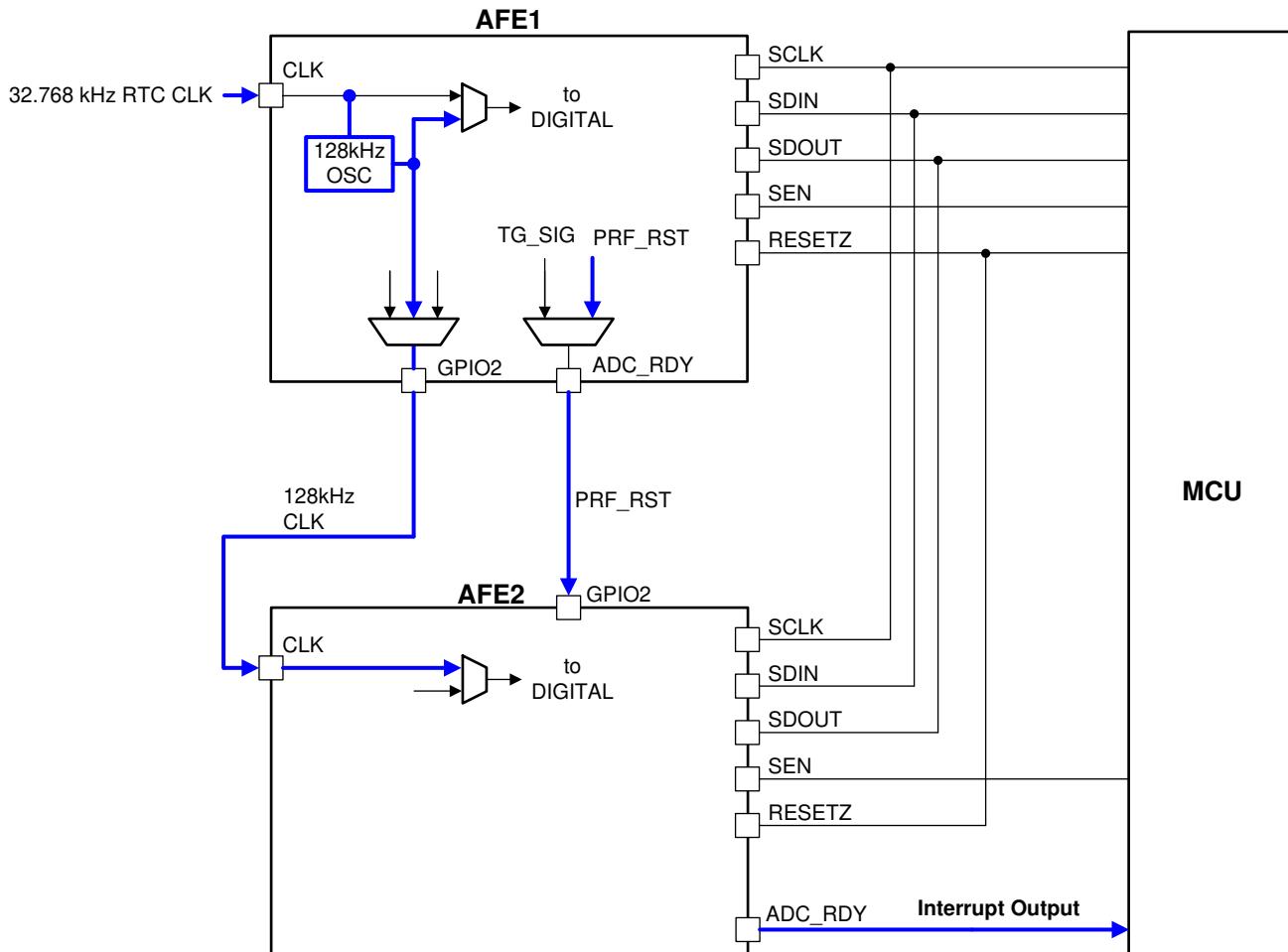


Figure 7-46. Two AFEs Connected for Concurrent Operation with Simultaneous Active Phases

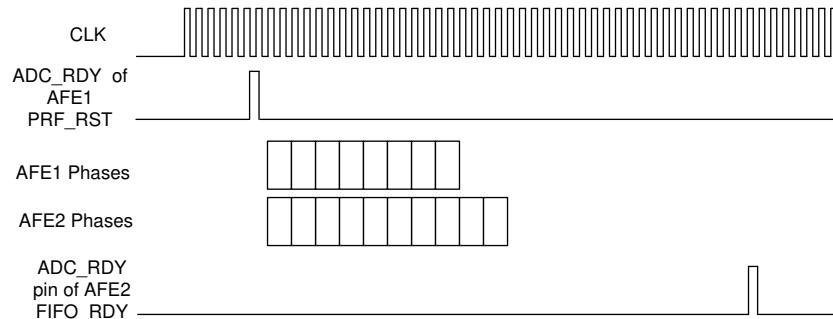


Figure 7-47. Timing for Two AFEs Connected for Concurrent Operation with Simultaneous Active Phases

7.5 Programming

The AFE has both a SPI and an I2C, which can be selected using the I2C_SPI_SEL pin.

7.5.1 SPI Interface

7.5.1.1 Serial Programming Interface

The SPI consists of four signals: SCLK (serial clock), SDOUT (serial interface data output), SDIN (serial interface data input), and SEN (serial interface enable). The pins controlling the SPI are listed in [Table 7-45](#).

Table 7-45. Pin Functions in SPI

PIN	SPI INTERFACE PIN DESCRIPTION
SCLK	SCLK: serial clock input
SDIN	SDIN: serial clock data
SEN	SEN: chip select (active low)
SDOUT	SDOUT: serial data output

The serial clock (SCLK) is the serial peripheral interface (SPI) serial clock. SCLK shifts in commands and shifts out data from the device. SCLK features a schmitt-triggered input and clocks data out on SDOUT. Data are clocked in on SDIN. Even though the input has hysteresis, SCLK is recommended to be kept as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low. The serial interface enable (SEN) enables the serial interface to clock data from SDIN into the device.

7.5.1.2 Writing Data

The SPI_REG_READ register bit must be set to 0 before writing to a register. When SEN is low:

- Serially shifting bits into the device is enabled.
- Serial data (on SDIN) are latched at every SCLK rising edge.
- The serial data are loaded into the register at every 32nd SCLK rising edge.

The first eight bits form the register address and the remaining 24 bits form the register data. [Figure 7-48](#) shows an SPI timing diagram for a single write operation.

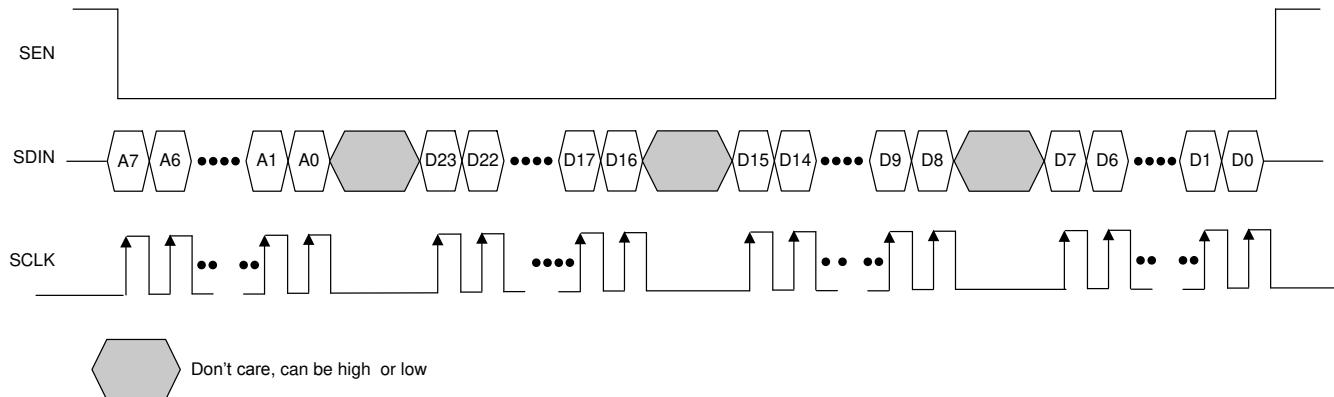


Figure 7-48. AFE SPI Write Timing Diagram

7.5.1.3 Reading Data

The AFE includes a mode where the contents of the internal registers can be read back on SDOUT. This mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the AFE. To enable this mode, first set the SPI_REG_READ register bit to '1' using the SPI write command. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SDOUT pin. [Figure 7-49](#) shows an SPI timing diagram for a single read operation. The SDOUT is in tri-state whenever SEN is high (inactive) and is active when SEN is low. The SDOUT buffer can be permanently tri-stated by using the SDOUT_TRISTATE register bit.

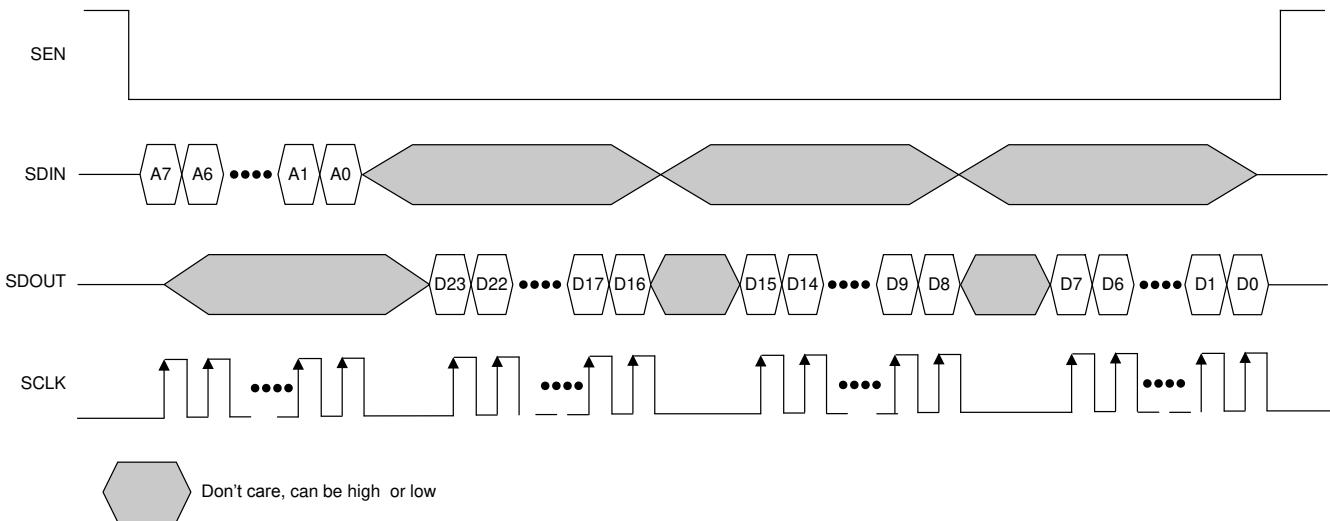


Figure 7-49. AFE SPI Read Timing Diagram

7.5.1.4 Continuous Read or Write Mode in the SPI

The SPI can be operated in a continuous read or write mode by writing 1 to the RW_CONT bit. In this mode, the address is specified at the start of the read or write cycle. Subsequently, the address of the register being read or written auto-increments until SEN is pulled high. The continuous write and read modes are illustrated in [Figure 7-50](#) and [Figure 7-51](#), respectively.

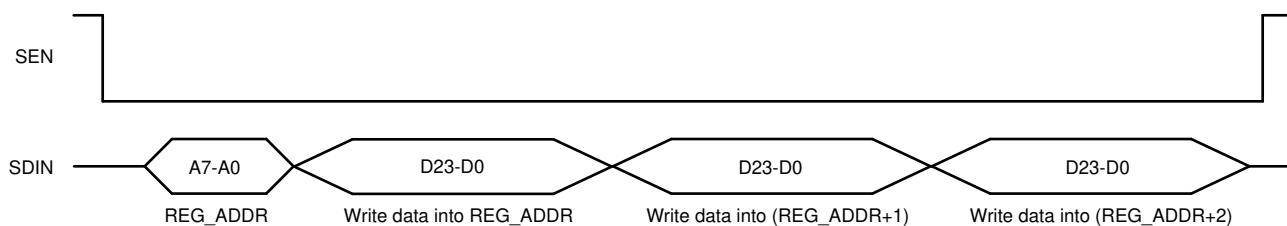


Figure 7-50. Continuous SPI Write (RW_CONT = 1)

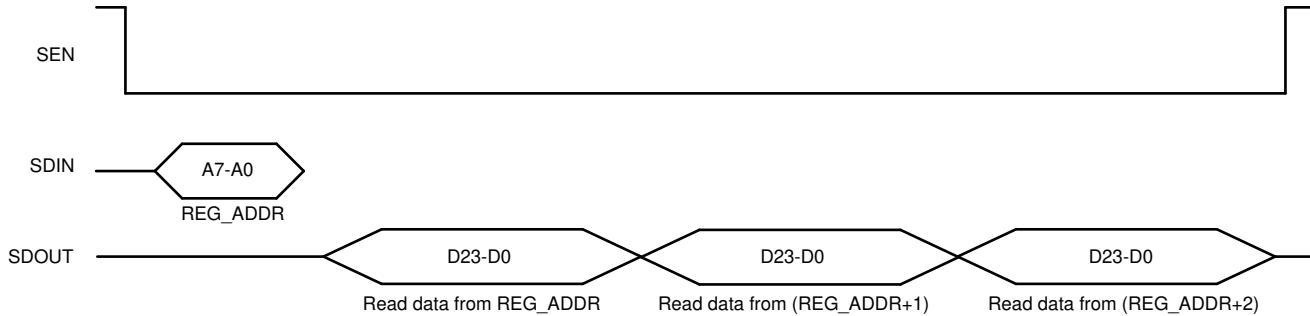


Figure 7-51. Continuous SPI Read (RW_CONT = 1, SPI_REG_READ = 1**)**

7.5.1.5 FIFO Readout Through SPI Over a Single Continuous Read Operation

The contents of the FIFO can be read out in a continuous manner using the SPI. The **RW_CONT** bit is not required to be set to 1 to continuously read out the FIFO. The **SPI_REG_READ** bit is also not required to be set to 1 when reading out the FIFO. The **REG_ADDR** used for reading out the FIFO must be set to FFh. The readout method is shown in [Figure 7-52](#).

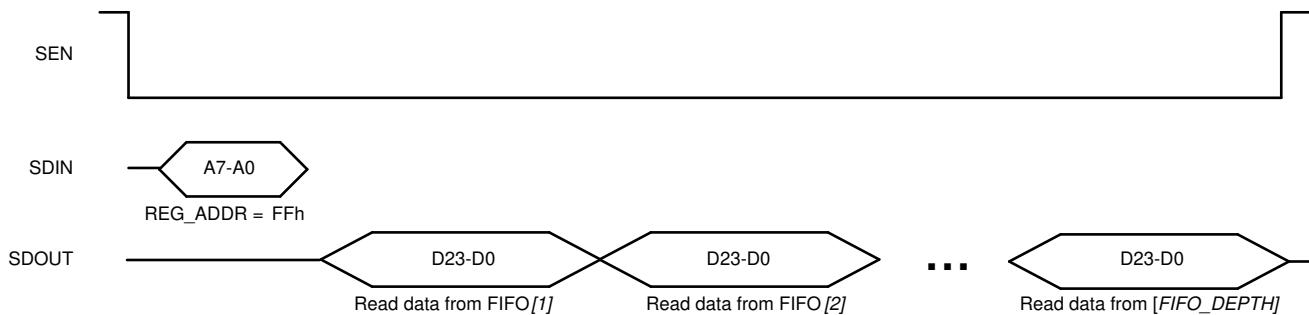


Figure 7-52. Continuous FIFO Readout Through the SPI

7.5.1.6 FIFO Readout Through the SPI Over Multiple Read Operations

The FIFO can also be read out over multiple read operations. [Figure 7-53](#) shows the FIFO being read out over two read operations.

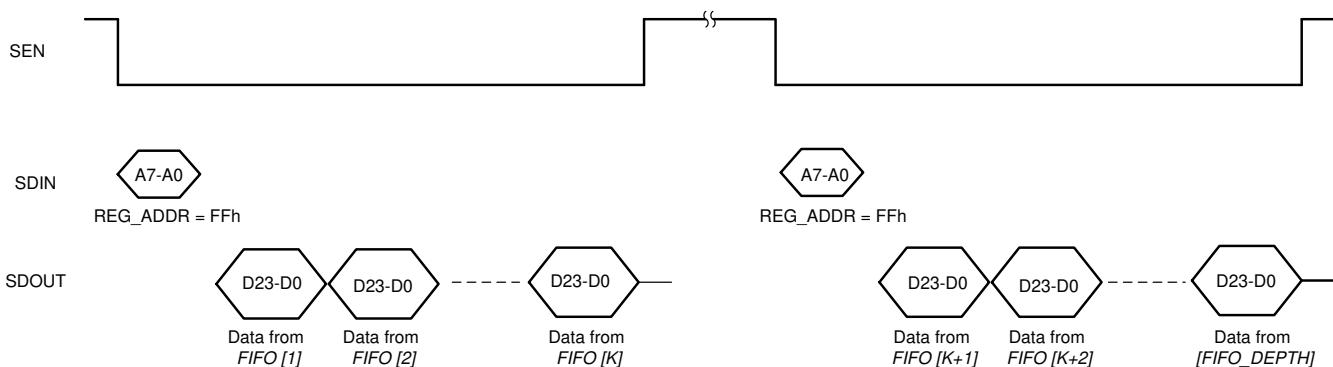


Figure 7-53. FIFO Readout Over Two Read Operations

7.5.2 I²C Interface

7.5.2.1 I²C Protocol

The AFE has an I²C interface for communication. The I²C_CLK and I²C_DAT lines require external pullup resistors to RX_SUP. See the I²C protocol standards documents for details of the I²C interface. This section only

describes certain key features of the interface. The data on I²C_DAT must be stable during the high level of I²C_CLK and can transition during the low level of I²C_CLK, as shown in Figure 7-54.

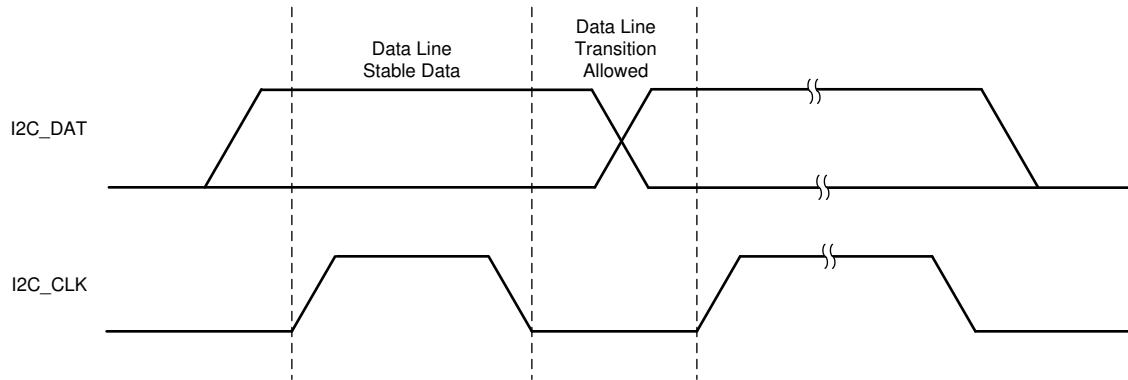


Figure 7-54. Allowed Transition of I²C_DAT During Data Bit Transmission

The start condition is indicated by a high-to-low transition of the I²C_DAT line when the I²C_CLK is high. A stop condition is indicated by a low-to-high transition of the I²C_DAT line when the I²C_CLK is high. Figure 7-55 shows the start and stop conditions.

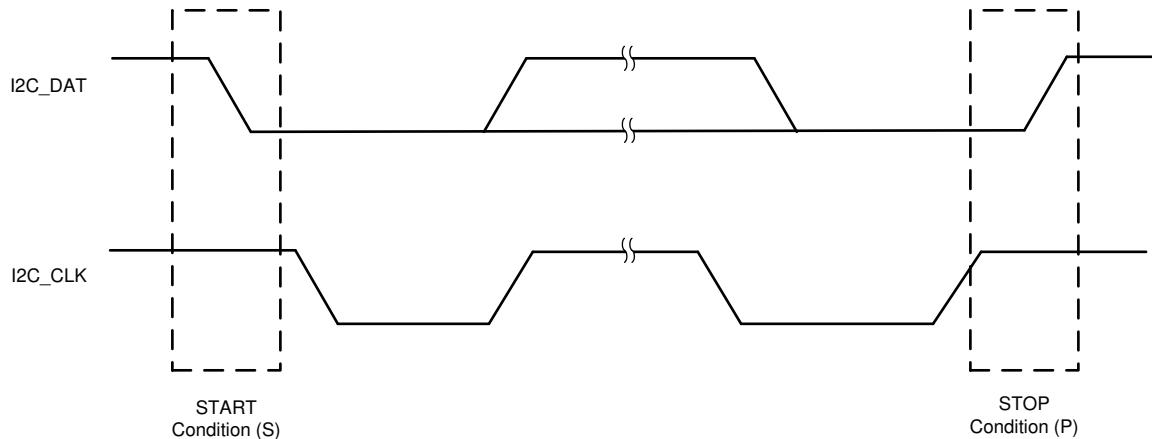


Figure 7-55. Transition of I²C_DAT During Start and Stop Conditions

7.5.2.2 I²C Write and Read Operations

With the previously mentioned protocols for data, start, and stop conditions, the write and read operations are as shown in Figure 7-56 and Figure 7-57, respectively. The target address for the AFE (indicated as SA6 to SA0) is a 7-bit representation of the address. The R/W bit is the read/write bit and is set to 1 for reads and 0 for writes. In the figures, the activity performed by the host is shown in black whereas the activity from the AFE is shown in red. Thus, after the host sends the target address during a write operation, the AFE pulls the I²C_DAT line low (shown as ACK) if the target address matches 5Bh. Similarly, the host pulls the I²C_DAT line high (shown as NACK) as an acknowledgment of a successfully completed read operation involving three bytes of data.

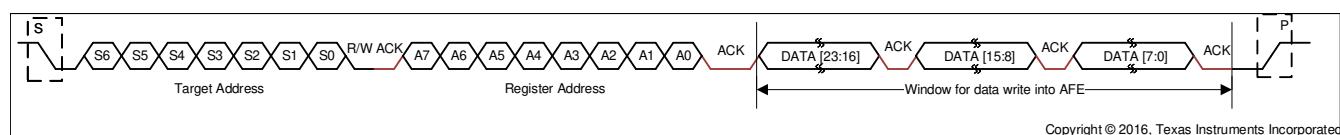
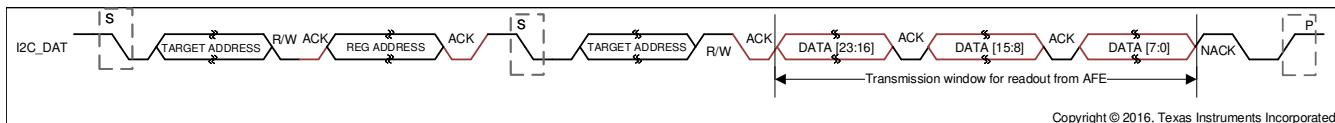
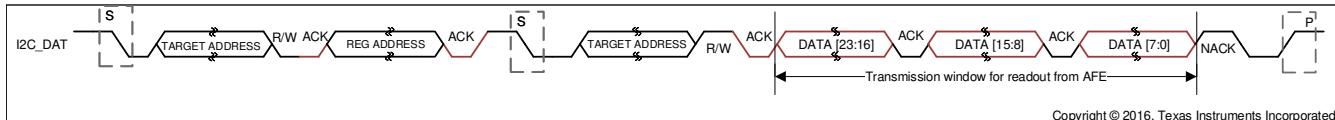
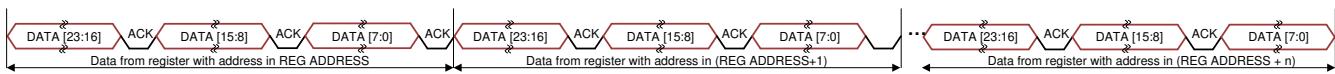


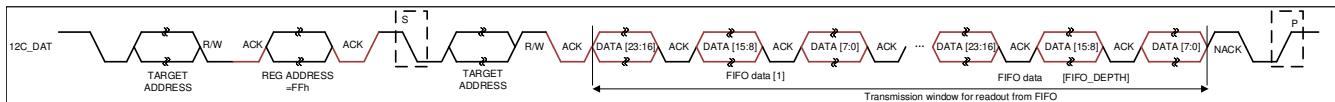
Figure 7-56. I²C Write Option Timing Diagram

**Figure 7-57. I²C Read Option Timing Diagram****7.5.2.3 Continuous I²C Read or Write Mode**

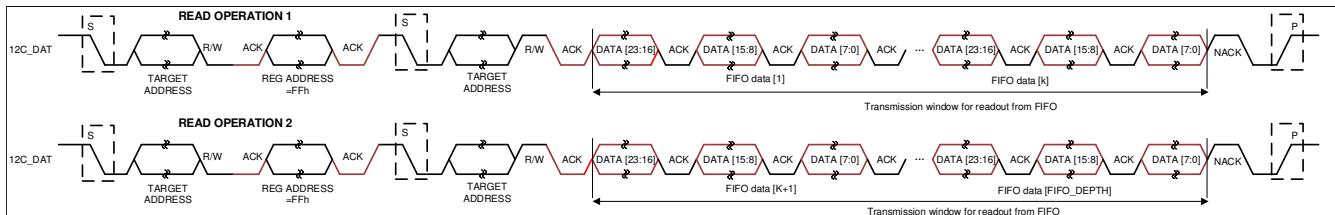
Continuous read/write mode is supported by enabling the RW_CONT bit. The FIFO, however, can be read out continuously without setting this bit. The protocol for the continuous write and read modes are shown in [Figure 7-58](#) and [Figure 7-59](#), respectively.

**Figure 7-58. Window for Data Writes Into the AFE in Continuous I²C Write Mode (RW_CONT = 1)****Figure 7-59. Transmission Window for Readout From the AFE in Continuous I²C Read Mode (RW_CONT = 1)****7.5.2.4 Data Readout From the FIFO Using a Single Continuous Read Operation**

When the MCU receives the FIFO_RDY interrupt, the FIFO can be read out through the I²C interface in continuous readout mode, as shown in [Figure 7-60](#). The REG ADDRESS for reading out the FIFO is FFh. The MCU must read out the full depth of the FIFO before the next FIFO_RDY.

**Figure 7-60. I²C Readout From the FIFO****7.5.2.5 Data Readout From the FIFO Over Multiple Read Operations**

The data from the FIFO can also be read out over multiple read operations with a break in between the operations. A readout over two such read operations is shown in [Figure 7-61](#).

**Figure 7-61. I²C Readout From the FIFO Over Two Read Operations**

7.6 Register Map

7.6.1 Page Selection

The register map has two pages as shown in [Table 7-46](#). The per-phase registers are located in Page 1 (PAGE_SEL='1') starting from address 20h to 5Fh. Set the PAGE_SEL register bit to the appropriate value to read and write from the desired page.

Registers with address from 00h to 1Fh and 60h to FFh can be written to and read from any page irrespective of the setting of the PAGE_SEL. The SPI_REG_READ bit in register 0h serves as the register read enable bit for registers in both Page 0 as well as in Page 1.

Table 7-46. Register Map Organization (Register Addresses in Decimal)

Page 0	Page 1
	Reg Address = 0
	Reg Address = 1
	Reg Address = 31
Reg Address = 32	Reg Address = 32
.	.
Reg Address = 95	Reg Address = 95
	Reg Address = 96
	.
	Reg Address = 255

7.6.2 Constraints When Reading Page 1 Registers Inside the Active Window

Per-phase registers for PPG are in Page 1 of the Register map (selected by setting PAGE_SEL=1). In case the Page 1 registers are required to be read out, it is recommended to read out the Page 1 registers only during the Deep sleep phase of the PRF cycle. If the Page 1 registers are read out in the Active window of the PRF cycle, then there are some constraints to be followed to ensure a reliable readout.

[Figure 7-62](#) shows the readout windows where these constraints do not apply, and where these constraints apply.



Figure 7-62. Readout Window for Page 1 Registers (Per-Phase PPG Registers)

Figure 7-63 shows the timing for an SPI read operation. The SPI clock rate is defined as $1/t_{\text{SPICLK}}$. Parameter t_{STECLK23} refers to the time between the falling edge of Serial Enable (SEN) and the 9th rising edge of Serial clock (SCLK).

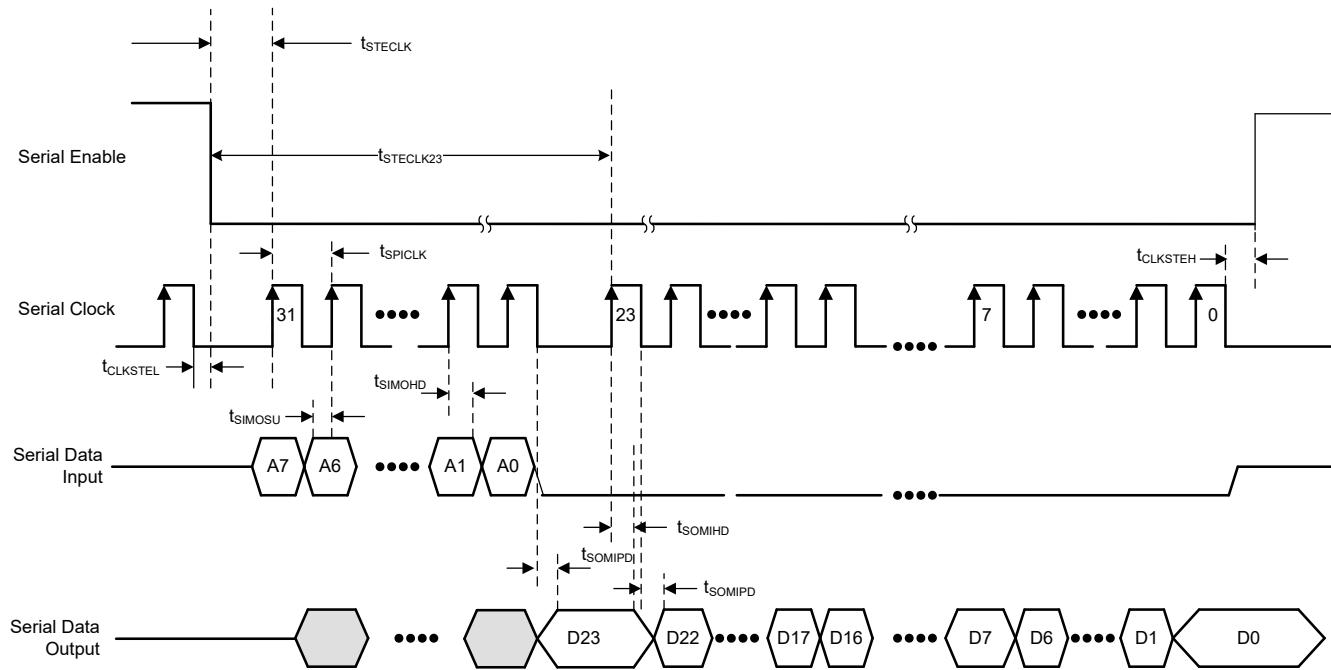


Figure 7-63. Timing for a SPI Read Operation

Table 7-47 lists the constraints to be followed if the Page 1 registers are required to be readout during the Active window of the PRF cycle.

Table 7-47. Constraints to Follow in AFE4432 if Page 1 Registers (Per-Phase PPG Registers) are Read out During the ACTIVE Window

	IF PAGE 1 READOUT DOES NOT NEED TO BE SUPPORTED IN 'CONSTRAINTS' ZONE	IF PAGE 1 READOUT MUST BE SUPPORTED IN 'CONSTRAINTS' ZONE
Timing engine clock $f_{\text{CLK_TE}}$	256 kHz	128 kHz ⁽¹⁾
Max value of t_{STECLK23}	N/A	4 μ s

(1) Change from default value of 256 kHz by programming the register bit CLK_TE_128K to '1'.

7.6.3 Register Map - Page 0

ADDRESS		REGISTER Default	REGISTER DATA																									
Dec	Hex	(Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
1	1	000200	0	0	0	0	0	0	0	0	0	0	0	DIS_POST_AMB_MAX_AMB_REJ	MAX_AMB_REJ	HIGH_PRF_MODE	MASK_REVERSE	EN_LED_SAT_DET	FIFO_EN	0	0	RW_CONT	SW_RESET	0	0	SP1_REG_READ		
5	5	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
6	6	000000	0	REG_NUM_TIA_MAX		0	0	0	IOFFDAC_PD2												IOFFDAC_PD1							
7	7	000000	0	0	PD_DISCONNECT_TIA2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IOFFDAC_PD3						
10	A	000000	0	0	PD_DISCONNECT_TIA1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
														INT_MUX_GPIO2				0	0	0	0	0	0	0	0	0	0	0

ADDRESS		REGISTER Default	REGISTER DATA																							
Dec	Hex	(Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
11	B	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	E	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	F	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
28	1C	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
29	1D	000000	TIMER_ENABLE	0	REG_NUMPHASE						PRPCT															
35	23	000000	0	0	0	0	0	0	0	ILED_FS	EN_AMB_DAC_LSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
36	24	000000	0	0	0	0	0	0	0	0	EN_LED_OFFSETDAC_TIA2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
40	28		x	x	x	x				DESIGN_ID	SET_OSCH_4M_2	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x
											SET_OSCH_4M_3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			x	x	x	x					PDN_OSCL_IN_DEEP_SLEEP															
											OSCL_DIS															
										SEL1_CLK_TE																

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ADDRESS		REGISTER Default	REGISTER DATA																											
Dec	Hex	(Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0				
41	29	000000	EN_GPIO2_INT_ON_ADC_RDY	0	0	0		EN_GPIO2_OUT	0	0	0	0	0	0	0	SDOUT_TRISTATE	0	0	0	0	0	0	0	0	0	0				
49	31	000000	0	0	0	0	0		0	0	0	0	0	0	0	EN_GPIO2_IN	0	0	0	0	0	0	0	0	0	0				
57	39	000000	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
66	42	000000	AUTO_MASK_FIFO_RDY						FIFO_OFFSET_TO_FORCE												REG_WM_FIFO									
67	43	000000	0	0	0	0	0		0	0	0	0	0	0	0	FIFO_OVERFLOW	0	0	0	0	0	0	0	0	0	0				
68	44		0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	REG_POINTER_DIFF											

ADDRESS		REGISTER Default	REGISTER DATA																							
Dec	Hex	(Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
75	4B	000000	0	EN_OSCL_CLKOUT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
80	50	000000	0	0	0	0	0	0	0	SPLIT_CLK_FOR_TE_PRF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
115	73	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IFS_AMB_OFFDAC_TIA2	IFS_AMB_OFFDAC_TIA1	0	0				
116	74	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TX_AMP_ACTIVE_ALWAYS	0	0	0	0	PDN_BG_IN_DEEP_SLEEP	0	0	
120	78	000000	OVERRIDE_BW_PRE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FILTER_BW_FINE_SET1	0	0	0	0	FILTER_BW_FINE_SET1			
121	79	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FILTER_BW_FINE_SET2	0	0	0	0	FILTER_BW_FINE_SET2			
128	80	000000	HIGH_THRESHOLD_CODE1										LOW_THRESHOLD_CODE1													
129	81	000000	HIGH_THRESHOLD_CODE2										LOW_THRESHOLD_CODE2													
131	83	000000	REG_SAMPLE_DELAY_SET2										REG_SAMPLE_DELAY_SET1													
132	84	000000	REG_SAMPLE_DELAY_SET4										REG_SAMPLE_DELAY_SET3													

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ADDRESS		REGISTER Default	REGISTER DATA																														
Dec	Hex	(Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0							
136	88	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN_PHASE_INT_GPIO	0	0	0	0	0	0	0	0							
137	89	000110	0	0	REG_TSEP			EARLY_SAMP_FALL	0	0	0	0	0	0	0	0	0	1	0	REG_TSEP_SAMP		0	REG_TSEP_CONV_STA RT										
138	8A	018047	0	0	REG_TACTIVE_PWRUP								0	0	REG_TDEEP_SLEEP_PWRUP																		
141	8D	000003	0	0	0	0	REG_TW_DATA_RDY		0	0	0	0	0	0	0	0	0	0	0	0	REG_TACTIVE_DATA_RDY												
142	8E	005001	0	0	0	REG_TDEEP_SLEEP_PWDN											0	0	0	REG_TACTIVE_PWDN													
146	92	000000	0	0	0	0	0	REG_STEP_COUNT						0	0	0	0	0	0	0	0	0	0	0	0	0	0						
148	94	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	REG_TW_FILTER_PRE														
149	95	000050	EMBED_ANA_AACM_IN_FIFO	0	TSEP_ANA_ACQ_LED_OVERRIDE	TW_ANA_ACQ_OVERRIDE	REG_TSEP_ANA_ACQ_LED				REG_TW_ANA_ACQ				REG_DELAY_ANA_ACQ				RF_ANA_AACM_END			0	0	0	0								
150	96	002222	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	RF_ANA_AACM_START_TIA2			RF_ANA_AACM_START_TIA1										
151	97	000000	CHANNEL_OFFSET_TIA2												CHANNEL_OFFSET_TIA1																		
154	9A	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	REG_RECONV_THR_LED_DC													
155	9B		0	0	0	0	0	0	0	0	0	0	0	0	0	LED_DC_LOOP_NUM_READ				POLLED_DC_READ	IOFFDAC_LED_DC_READ												

ADDRESS		REGISTER Default	REGISTER DATA																							
Dec	Hex	(Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
156	9C	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FREEZE_LED_DC_LOOP7	FREEZE_LED_DC_LOOP6	FREEZE_LED_DC_LOOP5	FREEZE_LED_DC_LOOP4	FREEZE_LED_DC_LOOP3	FREEZE_LED_DC_LOOP2	FREEZE_LED_DC_LOOP1	FREEZE_LED_DC_LOOP0
158	9E	000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	REG_SCALE_DRE			
159	9F	00003D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GAIN_CALIB_LED_DC_142K							
160	A0	000047	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GAIN_CALIB_LED_DC_166K							
161	A1	000055	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GAIN_CALIB_LED_DC_200K							
162	A2	00006B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GAIN_CALIB_LED_DC_250K							
180	B4	000000	COMB_THR_DET_EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	REG_THR_DET_PHASE						THR_SEL_LOGIC	THR_DET_EN
181	B5		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	THR_PPG_FLAG								
202	CA		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

7.6.4 Register Map Page 1

The following sets of registers are in Page 1:

Per-phase PPG register controls: REGy_PHx where x corresponds to the phase number (1 to 12) and y takes values from 1 to 5 (number of registers per phase)

The addresses of the 8 registers associated with each phase is listed in [Table 7-48](#). It is important to note that the per-phase registers in Page 1 do not have any default values on reset. *Therefore, all 5 address of all the defined phases (#1 to #NUMPHASE) need to be written even if some of these registers contain features not intended for use.*

Table 7-48. List of Addresses (in Hex) Associated With Each Phase

Phase	Register 1		Register 2		Register 3		Register 4		Register 5	
	Name	ADDR1	Name	ADDR2	Name	ADDR3	Name	ADDR4	Name	ADDR5
1	LED_SW_PH1	20	LED_ON_PH1	21	CONTROL_TIA1_PH1	22	CONTROL_TIA2_PH1	23	MISC_PH1	24
2	LED_SW_PH2	25	LED_ON_PH2	26	CONTROL_TIA1_PH2	27	CONTROL_TIA2_PH2	28	MISC_PH2	29
3	LED_SW_PH3	2A	LED_ON_PH3	2B	CONTROL_TIA1_PH3	2C	CONTROL_TIA2_PH3	2D	MISC_PH3	2E
4	LED_SW_PH4	2F	LED_ON_PH4	30	CONTROL_TIA1_PH4	31	CONTROL_TIA2_PH4	32	MISC_PH4	33
5	LED_SW_PH5	34	LED_ON_PH5	35	CONTROL_TIA1_PH5	36	CONTROL_TIA2_PH5	37	MISC_PH5	38
6	LED_SW_PH6	39	LED_ON_PH6	3A	CONTROL_TIA1_PH6	3B	CONTROL_TIA2_PH6	3C	MISC_PH6	3D
7	LED_SW_PH7	3E	LED_ON_PH7	3F	CONTROL_TIA1_PH7	40	CONTROL_TIA2_PH7	41	MISC_PH7	42
8	LED_SW_PH8	43	LED_ON_PH8	44	CONTROL_TIA1_PH8	45	CONTROL_TIA2_PH8	46	MISC_PH8	47
9	LED_SW_PH9	48	LED_ON_PH9	49	CONTROL_TIA1_PH9	4A	CONTROL_TIA2_PH9	4B	MISC_PH9	4C
10	LED_SW_PH10	4D	LED_ON_PH10	4E	CONTROL_TIA1_PH10	4F	CONTROL_TIA2_PH10	50	MISC_PH10	51
11	LED_SW_PH11	52	LED_ON_PH11	53	CONTROL_TIA1_PH11	54	CONTROL_TIA2_PH11	55	MISC_PH11	56
12	LED_SW_PH12	57	LED_ON_PH12	58	CONTROL_TIA1_PH12	59	CONTROL_TIA2_PH12	5A	MISC_PH12	5B

Table 7-49 shows the per-phase register controls associated with each phase.

Table 7-49. Per-Phase Register Controls Associated with Each Phase

REGISTER Name	ADDRESS		REGISTER DATA																						
	Dec	Hex	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
LED_SW	32	20			PHASE_INT_GPIO		THR_SEL_DATA_CTRL		THR_SEL_SEL								LED_DRV2_TXN<4:1>		0	0	0	0		LED_DRV1_TXN<4:1>	
LED_ON	33	21			REG_TWLED					ILED_DRV2								ILED_DRV1							
CONTROL_TIA1	34	22	0	0	0	0	IN_TIA1<3:1>										IOFFDAC_LED_TIA1		CF_TIA1		RF_TIA1				
CONTROL_TIA2	35	23	0	0	0	0	IN_TIA2<3:1>		LED_DC_EN_TIA2	LED_DC_EN_TIA1							IOFFDAC_LED_TIA2		CF_TIA2		RF_TIA2				
MISC	36	24	SEI_SAMPLE_DELAY_SET		REG_DEC_FACTOR		FIFO_DATA_CTRL										REG_NUMAV		ENABLE_DRE	0	REG_NUM_TIA		FILTER_SET_SEL		
																	REG_PH_MASK_FACTOR		AUTO_AMB_INSERT		USE_ANA_AACM		UPDATE_BASELINE_AMB		

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7.6.5 Page 0: Register Description

Register: 00h

Figure 7-64. Register : 00h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	RW_CONT	SW_RESET	0	0	SPI_REG_READ
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 7-50. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
23-5	0	W	0h	Must write 0
4	RW_CONT	W	0h	0 = Read or write only one register at a time 1 = Read or write continuously
3	SW_RESET	W	0h	Self-clearing reset bit. For a software reset, write 1.
2:1	0	W	0h	Must write 0
0	SPI_REG_READ	W	0h	Register readout enable for write 0 = Register write mode 1 = Enables the readout of write registers Not required for readout of read-only registers with address FFh.

Register: 01h**Figure 7-65. Register: 01h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	DIS_POST_AMB_MAX_AMB_REJ	0	MAX_AMB_REL_J	HIGH_PRF_MODE	MASK_REVERSE	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h
7	6	5	4	3	2	1	0
EN_LED_SAT_DET	FIFO_EN	0	0	0	0	TM_COUNT_RST	PAGE_SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-51. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
23-14	0	R/W	0h	Must write 0
13	DIS_POST_AMB_MAX_AMB_REJ	R/W	0h	Set the AFE in 'Maximum Ambient rejection mode' with only pre-ambient insertion.
12	0	R/W	0h	Must write 0
11	MAX_AMB_REL_J	R/W	0h	Set the AFE in 'Maximum Ambient rejection mode' with both pre-ambient and post-ambient insertion.
10	HIGH_PRF_MODE	R/W	0h	Set to '1' to enable the 'High PRF mode'.
9	MASK_REVERSE	R/W	1h	Change the order of masked/ unmasked phase across a sequence of PRF cycles.
8	0	R/W	0h	Must write 0
7	EN_LED_SAT_DET	R/W	0h	When this mode is enabled, it will detect when the LED phase value gets close to saturation (>90% of ADC Full Scale) and set a FIFO output flag in the digital processed data (LED-AMB or LED-avg(AMB1,AMB2)).
6	FIFO_EN	R/W	0h	0 = FIFO disabled 1 = FIFO enabled
5-2	0	R/W	0h	Must write 0
1	TM_COUNT_RST	R/W	0h	This bit is used to suspend the count and keep the timing counter in a reset state.
0	PAGE_SEL	R/W	0h	Page select bit 0 = Subsequent read/ write accesses registers in Page 0 1 = Subsequent read/ write accesses registers in Page 1.

Register: 05h**Figure 7-66. Register: 05h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	EN_TIA_RST
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	EN_IOFFDAC_LED_CHOP	SWAP_DAC	POL_IOFFDAC_AMB	POL_IOFFDAC_LED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-52. Register 05h Field Descriptions

Bit	Field	Type	Reset	Description
23-17	0	R/W	0h	Must write 0
16	EN_TIA_RST	R/W	0h	When this bit is set to '1', the TIA is reset with a low gain of 10kΩ between adjacent phases in order to reduce the crosstalk between adjacent phases.
15-4	0	R/W	0h	Must write 0
3	EN_IOFFDAC_LED_CHOP	R/W	0h	Enables chopping in the LED Offset DAC to reduce the noise
2	SWAP_DAC	R/W	0h	By setting the SWAP_DAC bit to 1, the functions for the two DACs can be swapped such that the Ambient Offset DAC is used to cancel the LED DC and the LED Offset DAC is used to cancel the Ambient DC. The register controls for the DACs are also swapped.
1	POL_IOFFDAC_AMB	R/W	0h	Polarity of Ambient Offset DAC – if anode of PD connects to INM and cathode of PD connects to INP, set polarity to '1' to subtract offset DAC current from the PD current.
0	POL_IOFFDAC_LED	R/W	0h	Polarity of LED Offset DAC - if anode of PD connects to INM and cathode of PD connects to INP, set polarity to '1' to subtract offset DAC current from the PD current.

Register: 06h**Figure 7-67. Register: 06h**

23	22	21	20	19	18	17	16
0	REG_NUM_TIA_MAX	0	0	0	0	0	IOFFDAC_PD2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
			IOFFDAC_PD2				IOFFDAC_PD1
			R/W-0h				R/W-0h
7	6	5	4	3	2	1	0
			IOFFDAC_PD1				
			R/W-0h				

Table 7-53. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22	REG_NUM_TIA_MAX	R/W	0h	Global parameter NUM_TIA_MAX equal to the maximum number of TIAs active across all phases is set as NUM_TIA_MAX = (REG_NUM_TIA_MAX+1).
21-18	0	R/W	0h	Must write 0
17-9	IOFFDAC_PD2	R/W	0h	IOFFDAC_PD2 represent the value of the ambient current to be subtracted from PD2. Used when the Ambient Offset DAC is controlled by the MCU.
8-0	IOFFDAC_PD1	R/W	0h	IOFFDAC_PD1 represent the value of the ambient current to be subtracted from PD1. Used when the Ambient Offset DAC is controlled by the MCU.

Register: 07h**Figure 7-68. Register: 07h**

23	22	21	20	19	18	17	16
0	0	PD_DISCONNECT_TIA2	PD_DISCONNECT_TIA1	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	IOFFDAC_PD3
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
			IOFFDAC_PD3				
			R/W-0h				

Table 7-54. Register 07h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
21	PD_DISCONNECT_TIA2	R/W	0h	Disconnect all PDs from the TIA2 inputs. When set to '1', input current to the TIA2 in a phase is equal to Offset DAC current setting for that phase.
20	PD_DISCONNECT_TIA1	R/W	0h	Disconnect all PDs from the TIA1 inputs. When set to '1', input current to the TIA1 in a phase is equal to Offset DAC current setting for that phase.
19-9	0	R/W	0h	Must write 0
8-0	IOFFDAC_PD3	R/W	0h	IOFFDAC_PD3 represent the value of the ambient current to be subtracted from PD3. Used when the Ambient Offset DAC is controlled by the MCU.

Register: 0Ah**Figure 7-69. Register: 0Ah**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0

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Figure 7-69. Register: 0Ah (continued)

R/W-0h	R/W-0h						
15	14	13	12	11	10	9	8
0	0	0	0	0		INT_MUX_GPIO2	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
0	0	0	0	0		INT_MUX_ADC_RDY	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

Table 7-55. Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10-8	INT_MUX_GPIO2	R/W	0h	Selection of interrupt on GPIO2 pin
7-3	0	R/W	0h	Must write 0
2-0	INT_MUX_ADC_RDY	R/W	0h	Selection of interrupt on ADC_RDY pin

Register: 0Bh**Figure 7-70. Register: 0Bh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	INPUT_PRF_R ST_ON_GPIO2	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-56. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	R/W	0h	Must write 0
14	INPUT_PRF_RST_ON_GPIO2	R/W	0h	Configure two AFEs in primary-secondary mode for PRF reset.
13-0	0	R/W	0h	Must write 0

Register: 0Eh**Figure 7-71. Register: 0Eh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PROG_INT2_STC							
R/W-0h							
7	6	5	4	3	2	1	0
PROG_INT2_STC							
R/W-0h							

Table 7-57. Register 0Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	R/W	0h	Must write 0
15-0	PROG_INT2_STC	R/W	0h	Start count for INT_OUT2 (programmable interrupt on GPIO2).

Register: 0Fh**Figure 7-72. Register: 0Fh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PROG_INT2_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
PROG_INT2_ENDC							
R/W-0h							

Table 7-58. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	R/W	0h	Must write 0
15-0	PROG_INT2_ENDC	R/W	0h	End count for INT_OUT2 (programmable interrupt on GPIO2)

Register: 1Ch**Figure 7-73. Register: 1Ch**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
SET_OSCH_4M_1	0	0	0	EN_CLK_MOD_E_MIX	EN_INT_IN_SINGLE_SHOT	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DIV_CLK_EXT			SEL1_CLK_PRF	EN_PRF_RESET	PDN_OSCL_IN_DEEP_SLEEP	OSCL_DIS	SEL1_CLK_TE
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-59. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	R/W	0h	Must write 0
15	SET_OSCH_4M_1	R/W	0h	Must write 1
14-12	0	R/W	0h	Must write 0
11	EN_CLK_MODE_MIX	R/W	0h	Additional control to enable CLK_MODE_MIX
10	EN_INT_IN_SINGLE_SHOT	R/W	0h	Enables interrupt generation in CLK_MODE_SS
9-8	0	R/W	0h	Must write 0
7-5	DIV_CLK_EXT	R/W	0h	Division ratio control for external clock. An external clock of higher frequency (a binary multiple of 256 kHz) can be used by setting DIV_CLK_EXT such that the divided clock frequency is approximately 256 kHz.
4	SEL1_CLK_PRF	R/W	0h	Selection Control 1 for CLK_PRF
3	EN_PRF_RESET	R/W	0h	Resets PRF counter with pulse on CLK pin
2	PDN_OSCL_IN_DEEP_SLEEP	R/W	0h	Enables dynamic power-down of OSCL. When setting PDNAFE to 1 (for enabling software power down), set the PDN_OSCL_IN_DEEP_SLEEP bit to 0.
1	OSCL_DIS	R/W	0h	Powers down OSCL (256 kHz oscillator)
0	SEL1_CLK_TE	R/W	0h	Selection Control 1 for CLK_TE

Register: 1Dh**Figure 7-74. Register: 1Dh**

23	22	21	20	19	18	17	16
TIMER_ENABLE	PRF_COUNTER_ENABLE	0		REG_NUMPHASE		PRPCT	
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
			PRPCT				
			R/W-0h				
7	6	5	4	3	2	1	0
			PRPCT				
			R/W-0h				

Table 7-60. Register 1Dh Field Descriptions

Bit	Field	Type	Reset	Description
23	TIMER_ENABLE	R/W	0h	The timing engine is enabled by setting the TIMER_ENABLE register bit to '1'.
22	PRF_COUNTER_ENABLE	R/W	0h	The PRF counter is enabled by setting the PRF_COUNTER_ENABLE register bit to '1'.
21	0	R/W	0h	Must write 0
20-17	REG_NUMPHASE	R/W	0h	The number of active phase sets is set by a parameter called NUMPHASE. The register control REG_NUMPHASE (programmable from 0 to 15) determines NUMPHASE as (REG_NUMPHASE+1)
16-0	PRPCT	R/W	0h	The PRF is determined by a register called PRPCT. The counter counts from 0 to (PRPCT-1) and defines a PRF cycle.

Register: 23h**Figure 7-75. Register: 23h**

23	22	21	20	19	18	17	16
0	0	0	0	0		ILED_FS	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
EN_AMB_DAC_LSB	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PDNAFE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-61. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
23-19	0	R/W	0h	Must write 0
18-16	ILED_FS	R/W	0h	Full scale current setting for the LED drivers.
15	EN_AMB_DAC_LSB	R/W	0h	Set EN_AMB_DAC_LSB to '1' to enable the LSB control of the Ambient Offset DAC.
14-1	0	R/W	0h	Must write 0
0	PDNAFE	R/W	0h	Enables software power-down mode. When setting PDN_AFE bit to 1, set PDN_OSCL_IN_DEEP_SLEEP bit to 0.

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Register: 24h**Figure 7-76. Register: 24h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	EN_LED_OFFD AC_TIA2	EN_LED_OFFD AC_TIA1	0	0	0	SET_OSCH_4 M_2	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SET_OSCH_4 M_3	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-62. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	R/W	0h	Must write 0
14	EN_LED_OFFDAC_TIA2	R/W	0h	Enables LED Offset DAC for TIA2
13	EN_LED_OFFDAC_TIA1	R/W	0h	Enables LED Offset DAC for TIA1
12-10	0	R/W	0h	Must write 0
9	SET_OSCH_4M_2	R/W	0h	Must write 1
8	0	R/W	0h	Must write 0
7	SET_OSCH_4M_3	R/W	0h	Must write 1
6-0	0	R/W	0h	Must write 0

Register: 28h**Figure 7-77. Register: 28h**

23	22	21	20	19	18	17	16
x	x	x	x			DESIGN_ID	
R	R	R	R			R-111h	
15	14	13	12	11	10	9	8
				DESIGN_ID			
				R-111h			
7	6	5	4	3	2	1	0
DESIGN_ID	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

Table 7-63. Register 28h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	x	R	x	-
19-7	DESIGN_ID	R	x	Design revision id: Release Silicon version - 0x121
6-0	x	R	x	-

Register: 29h**Figure 7-78. Register: 29h**

23	22	21	20	19	18	17	16
EN_GPIO2_INT_ON_ADC_RDY	0	0	0	EN_GPIO2_OUT	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	SDOUT_TRISTATE	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-64. Register 29h Field Descriptions

Bit	Field	Type	Reset	Description
23	EN_GPIO2_INT_ON_ADC_RDY	R/W	0h	Interrupts programmed to come out on the GPIO2 pin can be made to come out on ADC_RDY pin by setting the EN_GPIO2_INT_ON_ADC_RDY bit to '1'.
22-20	0	R/W	0h	Must write 0
19	EN_GPIO2_OUT	R/W	0h	Set to '1' to configure GPIO2 as output pin.
18-11	0	R/W	0h	Must write 0
10	SDOUT_TRISTATE	R/W	0h	The SDOUT buffer can be permanently tri-stated by using the SDOUT_TRISTATE register bit.
9-0	0	R/W	0h	Must write 0

Register: 31h**Figure 7-79. Register: 31h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	EN_GPIO2_IN	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-65. Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	R/W	0h	Must write 0
14	EN_GPIO2_IN	R/W	0h	Set to '1' to configure GPIO2 as input pin.
13-0	0	R/W	0h	Must write 0

Register: 39h**Figure 7-80. Register: 39h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	CLK_TE_128K	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-66. Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
23-3	0	R/W	0h	Must write 0
2	CLK_TE_128K	R/W	0h	Enables a 2% in the CLK_TE path and causes the timing engine clock to be set to 128 kHz. Meant to be used only if it is required to read out the Page 1 registers during the Active window of the PRF cycle.
13-0	0	R/W	0h	Must write 0

Register: 42h**Figure 7-81. Register: 42h**

23	22	21	20	19	18	17	16
AUTO_MASK_FIFO_RDY	MASK_FIFO_RDY	FORCE_FIFO_OFFSET	FIFO_OFFSET_TO_FORCE				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
15	14	13	12	11	10	9	8
FIFO_OFFSET_TO_FORCE			0	0	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
REG_WM_FIFO							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-67. Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
23	AUTO_MASK_FIFO_RDY	R/W	0h	Set to '1' to prevent the occurrence of repetitive FIFO_RDY interrupts when the pointer difference has exceeded the watermark level.
22	MASK_FIFO_RDY	R/W	0h	Masks the FIFO_RDY interrupt generation.
21	FORCE_FIFO_OFFSET	R/W	0h	Force the FIFO read pointer with respect to the write pointer. The offset to force is set by FIFO_OFFSET_TO_FORCE.
20-13	FIFO_OFFSET_TO_FORCE	R/W	0h	Offset of the read pointer relative to the write pointer. Use in conjunction with FORCE_FIFO_OFFSET set to 1.
12-8	0	R/W	0h	Must write 0
7-0	REG_WM_FIFO	R/W	0h	The FIFO_RDY gets generated when the difference between the Write and Read pointers exceeds a programmed Watermark (WM) level referred to as WM_FIFO. The REG_WM_FIFO register control sets the Watermark level (WM_FIFO) to be equal to (REG_WM_FIFO+1).

Register: 43h**Figure 7-82. Register: 43h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	EN_FRAME_SYNC	FRAME_SYNC_ON_LSB	EN_LED_OFFDAC_MARKER	LED_OFFSETDAC_MARKER_ON_LSB
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-68. Register 43h Field Descriptions

Bit	Field	Type	Reset	Description
23-4	0	R/W	0h	Must write 0
3	EN_FRAME_SYNC	R/W	0h	A 'Frame sync indicator' tag to indicate the first FIFO sample from a PRF cycle can be enabled by setting the EN_FRAME_SYNC bit to '1'.
2	FRAME_SYNC_ON_LSB	R/W	0h	By default, the MSB bit (D23) is replaced by the Frame sync indicator tag. By additionally setting the FRAME_SYNC_ON_LSB bit to 1, the Frame sync indicator can be made to replace the LSB (Bit D0) instead of the MSB (D23).
1	EN_LED_OFFDAC_MARKER	R/W	0h	A 'LED Offset DAC update' tag to indicate whether the sample corresponds to an update of the LED offset DAC can be enabled by setting the EN_LED_OFFDAC_MARKER bit to '1'.

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Table 7-68. Register 43h Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LED_OFFDAC_MARKER_ON_LSB	R/W	0h	By default, D23 is replaced by the LED Offset DAC update tag, which is set to '1' for the data sample where the LED DC cancellation loop has updated the LED Offset DAC. By additionally setting the LED_OFFDAC_MARKER_ON_LSB bit to 1, the LED Offset update tag can be made to replace D0 instead of D23.

Register: 44h**Figure 7-83. Register: 44h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
15	14	13	12	11	10	9	8
0	0	0	0	0	FIFO_OVERFLOW	0	0
R-x	R-x	R-x	R-x	R-x	R/x	R-x	R-x
7	6	5	4	3	2	1	0
REG_POINTER_DIFF							
R/x							

Table 7-69. Register 44h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R	x	Must write 0
10	FIFO_OVERFLOW	R/W	x	A register bit FIFO_OVERFLOW can be read out to check for a FIFO overflow condition. The FIFO_OVERFLOW bit goes high as soon as the pointer difference exceeds 160 and stays high for the entire duration of overflow.
9-8	0	R/W	x	Must write 0
7-0	REG_POINTER_DIFF	R/W	x	The instantaneous difference between the write and read pointers can be read out through an 8-bit register REG_POINTER_DIFF. The difference between the write and read pointers (POINTER_DIFF) is equal to (REG_POINTER_DIFF+1).

Register: 4Bh**Figure 7-84. Register: 4Bh**

23	22	21	20	19	18	17	16
0	EN_OSCL_CLKOUT	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-70. Register 4Bh Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Must write 0
22	EN_OSCL_CLKOUT	R/W	0h	Set to '1' to get the 256 kHz oscillator output on GPIO2 pin.
21-0	0	R/W	0h	Must write 0

Register: 50h**Figure 7-85. Register: 50h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	SPLIT_CLK_FOR_TE_PRF
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h							

Table 7-71. Register 50h Field Descriptions

Bit	Field	Type	Reset	Description
23-17	0	R/W	0h	Must write 0
16	SPLIT_CLK_FOR_TE_PRF	R/W	0h	Splits the clocking for the Timing engine and PRF counter.
15-0	0	R/W	0h	Must write 0

Register: 73h**Figure 7-86. Register : 73h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
IFS_AMB_OFFSETDAC_TIA2			IFS_AMB_OFFSETDAC_TIA1			0	0
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Table 7-72. Register 73h Field Descriptions

Bit	Field	Type	Reset	Description
23-8	0	R/W	0h	Must write 0
7-5	IFS_AMB_OFFSETDAC_TIA2	R/W	0h	Full scale range of Ambient Offset DAC associated with TIA2
4-2	IFS_AMB_OFFSETDAC_TIA1	R/W	0h	Full scale range of Ambient Offset DAC associated with TIA1
1-0	0	R/W	0h	Must write 0

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Register: 74h**Figure 7-87. Register: 74h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	DEGLITCH_AM B_DAC_MODE	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	TX_AMP_ACTI VE_ALWAYS	0	0	0	PDN_BG_IN_D EEP_SLEEP	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-73. Register 74h Field Descriptions

Bit	Field	Type	Reset	Description
23-10	0	R/W	0h	Must write 0
9	DEGLITCH_AMB_DAC_MODE	R/W	0h	When operating in the High PRF mode, an update in the Ambient DAC during any of the CONV phases can cause some noise degradation in the ADC conversion. Setting the DEGLITCH_AMB_DAC_MODE bit to '1' removes such a noise degradation with a slight power penalty.
8-6	0	R/W	0h	Must write 0
5	TX_AMP_ACTIVE_ALWAYS	R/W	0h	When the LED current is set to 0 in the LED phase, it shuts off the amplifier in the LED driver. This can disturb the reference voltage and impact ambient rejection. To avoid such an occurrence, the LED driver amplifier can be kept active in the LED phase by setting TX_AMP_ACTIVE_ALWAYS bit to '1'.
4-2	0	R/W	0h	Must write 0
1	PDN_BG_IN_DEEP_SLEEP	R/W	0h	Set the PDN_BG_IN_DEEP_SLEEP to '1' to get to the lowest power.
0	0	R/W	0h	Must write 0

Register: 78h**Figure 7-88. Register: 78h**

23	22	21	20	19	18	17	16
OVERRIDE_B_W_PRE	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0			FILTER_BW_PRE_SET1			
R/W-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
0	0			FILTER_BW_FINE_SET1			
R/W-0h	R/W-0h			R/W-0h			

Table 7-74. Register 78h Field Descriptions

Bit	Field	Type	Reset	Description
23	OVERRIDE_BW_PRE	R/W	0h	Override bit to enable control of Pre-charge filter bandwidth (Set 1 & Set 2).
22-14	0	R/W	0h	Must write 0
13-8	FILTER_BW_PRE_SET1	R/W	0h	Bandwidth setting control for Filter bandwidth in pre-charge phase (Set 1)
7-6	0	R/W	0h	Must write 0
5-0	FILTER_BW_FINE_SET1	R/W	0h	Bandwidth setting control for Filter bandwidth in Fine settling phase (Set 1)

Register: 79h**Figure 7-89. Register: 79h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0			FILTER_BW_PRE_SET2			
R/W-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
0	0			FILTER_BW_FINE_SET2			
R/W-0h	R/W-0h			R/W-0h			

Table 7-75. Register 79h Field Descriptions

Bit	Field	Type	Reset	Description
23-14	0	R/W	0h	Must write 0
13-8	FILTER_BW_PRE_SET2	R/W	0h	Bandwidth setting control for Filter bandwidth in pre-charge phase (Set 2)
7-6	0	R/W	0h	Must write 0
5-0	FILTER_BW_FINE_SET2	R/W	0h	Bandwidth setting control for Filter bandwidth in Fine settling phase (Set 2)

Register: 80h**Figure 7-90. Register: 80h**

23	22	21	20	19	18	17	16
HIGH_THRESHOLD_CODE1							
R/W-0h							
15	14	13	12	11	10	9	8
HIGH_THRESHOLD_CODE1				LOW_THRESHOLD_CODE1			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
LOW_THRESHOLD_CODE1							
R/W-0h							

Table 7-76. Register 80h Field Descriptions

Bit	Field	Type	Reset	Description
23-12	HIGH_THRESHOLD_CODE1	R/W	0h	High threshold code (Set 1) used for comparison in Threshold detect mode.
11-0	LOW_THRESHOLD_CODE1	R/W	0h	Low threshold code (Set 1) used for comparison in Threshold detect mode.

Register: 81h**Figure 7-91. Register: 81h**

23	22	21	20	19	18	17	16
HIGH_THRESHOLD_CODE2							
R/W-0h							
15	14	13	12	11	10	9	8
HIGH_THRESHOLD_CODE2				LOW_THRESHOLD_CODE2			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
LOW_THRESHOLD_CODE2							
R/W-0h							

Table 7-77. Register 81h Field Descriptions

Bit	Field	Type	Reset	Description
23-12	HIGH_THRESHOLD_CODE2	R/W	0h	High threshold code (Set 2) used for comparison in Threshold detect mode.
11-0	LOW_THRESHOLD_CODE2	R/W	0h	Low threshold code (Set 2) used for comparison in Threshold detect mode.

Register: 83h**Figure 7-92. Register: 83h**

23	22	21	20	19	18	17	16
REG_SAMPLE_DELAY_SET2							
R/W-0h							
15	14	13	12	11	10	9	8
REG_SAMPLE_DELAY_SET2				REG_SAMPLE_DELAY_SET1			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
REG_SAMPLE_DELAY_SET1							
R/W-0h							

Table 7-78. Register 83h Field Descriptions

Bit	Field	Type	Reset	Description
23-12	REG_SAMPLE_DELAY_SET2	R/W	0h	The sampling window of Phase N can be delayed with respect to the first convert phase start by a delay which can be set using one of 4 sets of REG_SAMPLE_DELAY* register control. REG_SAMPLE_DELAY_SET2 is the 2nd set.
11-0	REG_SAMPLE_DELAY_SET1	R/W	0h	The sampling window of Phase N can be delayed with respect to the first convert phase start by a delay which can be set using one of 4 sets of REG_SAMPLE_DELAY* register control. REG_SAMPLE_DELAY_SET1 is the 1st set.

Register: 84h**Figure 7-93. Register: 84h**

23	22	21	20	19	18	17	16
REG_SAMPLE_DELAY_SET4							
R/W-0h							
15	14	13	12	11	10	9	8
REG_SAMPLE_DELAY_SET4				REG_SAMPLE_DELAY_SET3			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
REG_SAMPLE_DELAY_SET3							
R/W-0h							

Table 7-79. Register 84h Field Descriptions

Bit	Field	Type	Reset	Description
23-12	REG_SAMPLE_DELAY_SET4	R/W	0h	The sampling window of Phase N can be delayed with respect to the first convert phase start by a delay which can be set using one of 4 sets of REG_SAMPLE_DELAY* register control. REG_SAMPLE_DELAY_SET4 is the 4th set.
11-0	REG_SAMPLE_DELAY_SET3	R/W	0h	The sampling window of Phase N can be delayed with respect to the first convert phase start by a delay which can be set using one of 4 sets of REG_SAMPLE_DELAY* register control. REG_SAMPLE_DELAY_SET3 is the 3rd set.

Register: 88h**Figure 7-94. Register: 88h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15 14 13 12 11 10 9 8							
0	0	0	0	0	0	0	EN_PHASE_IN_T_GPIO
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-80. Register 88h Field Descriptions

Bit	Field	Type	Reset	Description
23-9	0	R/W	0h	Must write 0
8	EN_PHASE_INT_GPIO	R/W	0h	Enable per-phase interrupt on GPIO2 pin.
7-0	0	R/W	0h	Must write 0

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Register: 89h**Figure 7-95. Register: 89h**

23	22	21	20	19	18	17	16
0	0		REG_TSEP		EARLY_SAMP_FALL	0	0
R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0		REG_TSEP_SAMP		0		REG_TSEP_CONV_START	
R/W-0h		R/W-1h		R/W-0h		R/W-0h	

Table 7-81. Register: 89h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	R/W	0h	Must write 0
21-19	REG_TSEP	R/W	0h	Controls the separation between successive windows.
18	EARLY_SAMP_FALL	R/W	0h	The falling edge of SAMP can be advanced by 1 timing engine clock with respect to the falling edge of the LED_ON signal by setting a global register control called EARLY_SAMP_FALL.
17-9	0	R/W	0h	Must write 0
8	1	R/W	1h	Must write 1
7	0	R/W	0h	Must write 0
6-4	REG_TSEP_SAMP	R/W	1h	Controls the separation between sampling phases in Maximum Ambient Rejection mode
3	0	R/W	0h	Must write 0
2-0	REG_TSEP_CONV_START	R/W	0h	Controls the separation between the start of the Convert window to start of the first CONV signal

Register: 8Ah**Figure 7-96. Register: 8Ah**

23	22	21	20	19	18	17	16
0	0		REG_TACTIVE_PWRUP				
R/W-0h	R/W-0h			R/W-18h			
15	14	13	12	11	10	9	8
	REG_TACTIVE_PWRUP			0	0	REG_TDEEP_SLEEP_PWRUP	
	R/W-18h			R/W-0h	R/W-0h	R/W-47h	
7	6	5	4	3	2	1	0
		REG_TDEEP_SLEEP_PWRUP					
		R/W-47h					

Table 7-82. Register 8Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Must write 0
21-12	REG_TACTIVE_PWRUP	R/W	18h	Controls separation between the start of the Active window to the start of the 1st PPG phase.
11-10	0	R/W	0h	Must write 0
9-0	REG_TDEEP_SLEEP_PWRUP	R/W	47h	Controls the separation between the start of the PRF cycle and the start of the Active phase.

Register: 8Dh**Figure 7-97. Register: 8Dh**

23	22	21	20	19	18	17	16
0	0	0	0		REG_TW_DATA_RDY		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
				REG_TACTIVE_DATA_RDY			
				R/W-3h			

Table 7-83. Register 8Dhh Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	0h	Must write 0
19-16	REG_TW_DATA_RDY	R/W	0h	Controls the width of DATA_RDY.
15-8	0	R/W	0h	Must write 0
7-0	REG_TACTIVE_DATA_RDY	R/W	3h	Controls separation between the end of Active window to the start of DATA_RDY pulse.

Register: 8Eh**Figure 7-98. Register: 8Eh**

23	22	21	20	19	18	17	16
0	0	0		REG_TDEEP_SLEEP_PWDN			
R/W-0h	R/W-0h	R/W-0h		R/W-5h			
15	14	13	12	11	10	9	8
		REG_TDEEP_SLEEP_PWDN		0	0	0	REG_TACTIVE_PWDN
		R/W-5h		R/W-0h	R/W-0h	R/W-1h	
7	6	5	4	3	2	1	0
				REG_TACTIVE_PWDN			
				R/W-1h			

Table 7-84. Register 8Ehh Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	R/W	0h	Must write 0
20-12	REG_TDEEP_SLEEP_PWDN	R/W	5h	Controls separation between DATA_RDY fall to start of Deep Sleep window.
11-9	0	R/W	0h	Must write 0
8-0	REG_TACTIVE_PWDN	R/W	1h	Controls separation from the End of the last PPG phase to end of Active window.

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Register: 92h**Figure 7-99. Register: 92h**

23	22	21	20	19	18	17	16
0	0	0	0	0		REG_STEP_COUNT	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
	REG_STEP_COUNT			0	0	0	0
		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-85. Register 92h Field Descriptions

Bit	Field	Type	Reset	Description
23-19	0	R/W	0h	Must write 0
18-12	REG_STEP_COUNT	R/W	0h	By default, the PRF counter counts from 0 to (PRPCT-1) in increments of 1 while operating in the Mixed clock mode. The increment of the PRF counter can be set to a parameter STEP_COUNT programmable between 1 and 128. The parameter STEP_COUNT is derived from the register REG_STEP_COUNT as (REG_STEP_COUNT + 1).
11-0	0	R/W	0h	Must write 0

Register: 94h**Figure 7-100. Register: 94h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
		REG_TW_FILTER_PRE					
			R/W-0h				

Table 7-86. Register 94h Field Descriptions

Bit	Field	Type	Reset	Description
23-8	0	R/W	0h	Must write 0
7-0	REG_TW_FILTER_PRE	R/W	0h	Register control to program Filter Pre-charge phase width.

Register: 95h**Figure 7-101. Register: 95h**

23	22	21	20	19	18	17	16
EMBED_ANA_AACM_IN_FIFO	0	TSEP_ANA_ACQ_LED_OVERRIDE	TW_ANA_ACQ_OVERRIDE		REG_TSEP_ANA_ACQ_LED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		
15	14	13	12	11	10	9	8
		REG_TW_ANA_ACQ			REG_DELAY_ANA_ACQ		
		R/W-0h			R/W-0h		
7	6	5	4	3	2	1	0
		RF_ANA_AACM_END		0	0	0	0
		R/W-5h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-87. Register 95h Field Descriptions

Bit	Field	Type	Reset	Description
23	EMBED_ANA_AACM_IN_FIFO	R/W	0h	Using this diagnostic mode, the IOFFDAC_AMB code determined by the AACM loop in an Analog AACM phase marked with UPDATE_BASELINE='1' can be embedded into the 9 LSB of the corresponding FIFO word.
22	0	R/W	0h	Must write 0
21	TSEP_ANA_ACQ_LED_OVERRIDE	R/W	0h	Set to '1' to override t _{SEP_ANA_ACQ_LED} using the register control REG_TSEP_ANA_ACQ_LED
20	TW_ANA_ACQ_OVERRIDE	R/W	0h	Set to '1' to override t _{W_ANA_ACQ} using the register control REG_TW_ANA_ACQ.
19-16	REG_TSEP_ANA_ACQ_LED	R/W	0h	Register control for t _{SEP_ANA_ACQ_LED} . Used to override default value when TSEP_ANA_ACQ_LED_OVERRIDE is set to '1'.
15-12	REG_TW_ANA_ACQ	R/W	0h	Register control for t _{W_ANA_ACQ} . Used to override default value when TW_ANA_ACQ_OVERRIDE is set to '1'
11-8	REG_DELAY_ANA_ACQ	R/W	0h	Register control for t _{DELAY_ANA_ACQ} .
7-4	RF_ANA_AACM_END	R/W	5h	R _F control code during end of ANA_ACQ_TIA1 and ANA_ACQ_TIA2
3-0	0	R/W	0h	Must write 0

Register: 96h**Figure 7-102. Register: 96h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	1	0	0	0	1	0
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h
7	6	5	4	3	2	1	0
		RF_ANA_AACM_START_TIA2			RF_ANA_AACM_START_TIA1		
		R/W-2h			R/W-2h		

Table 7-88. Register 96h Field Descriptions

Bit	Field	Type	Reset	Description
23-14	0	R/W	0h	Must write 0
13	1	R/W	1h	Must write 1
12-10	0	R/W	0h	Must write 0
9	1	R/W	1h	Must write 1
8	0	R/W	0h	Must write 0
7-4	RF_ANA_AACM_START_TIA2	R/W	2h	Controls the R _F of TIA2 during the ANA_ACQ phase.

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Table 7-88. Register 96h Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	RF_ANA_AACM_START_TIA1	R/W	2h	Controls the R _f of TIA1 during the ANA_ACQ phase.

Register: 97h**Figure 7-103. Register: 97h**

23	22	21	20	19	18	17	16
CHANNEL_OFFSET_TIA2							
R/W-0h							
15	14	13	12	11	10	9	8
CHANNEL_OFFSET_TIA2				CHANNEL_OFFSET_TIA1			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
CHANNEL_OFFSET_TIA1							
R/W-0h							

Table 7-89. Register 97h Field Descriptions

Bit	Field	Type	Reset	Description
23-12	CHANNEL_OFFSET_TIA2	R/W	0h	Calibration word denoting channel offset to be written as part of AACM calibration – this word corresponds to the channel offset of TIA2
11-0	CHANNEL_OFFSET_TIA1	R/W	0h	Calibration word denoting channel offset to be written as part of AACM calibration – this word corresponds to the channel offset of TIA1

Register: 9Ah**Figure 7-104. Register : 9Ah**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
REG_RECONV_THR_LED_DC							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-90. Register 9Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-8	0	R/W	0h	Must write 0
7-0	REG_RECONV_THR_LED_DC	R/W	0h	ADC code threshold (\pm) at which loop updates LED Offset DAC is set as $2^{13} \times \text{REG_RECONV_THR_LED_DC}$

Register: 9Bh**Figure 7-105. Register: 9Bh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	LED_DC_LOOP_NUM_READ			POL_LED_DC_READ	IOFFDAC_LED_DC_READ
R/W-0h	R/W-0h			R-x		R-x	
7	6	5	4	3	2	1	0
IOFFDAC_LED_DC_READ							
R-x							

Table 7-91. Register 9Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-13	0	R/W	0h	Must write 0
12-10	LED_DC_LOOP_NUM_READ	R/W	0h	LED_DC_LOOP_NUM_READ specifies the target loop number (0..19) for readout.
9	POL_LED_DC_READ	R	x	The polarity value of the LED Offset DAC for that Target loop can be read out on POL_LED_DC_READ.
8-0	IOFFDAC_LED_DC_READ	R	x	The current converged value of the LED Offset DAC for that Target loop can be read out on IOFFDAC_LED_DC_READ.

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Register: 9Ch**Figure 7-106. Register: 9Ch**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h							
7	6	5	4	3	2	1	0
FREEZE_LED_DC_LOOP7	FREEZE_LED_DC_LOOP6	FREEZE_LED_DC_LOOP5	FREEZE_LED_DC_LOOP4	FREEZE_LED_DC_LOOP3	FREEZE_LED_DC_LOOP2	FREEZE_LED_DC_LOOP1	FREEZE_LED_DC_LOOP0
R/W-0h							

Table 7-92. Register 9Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-8	0	R/W	0h	Must write 0
7	FREEZE_LED_DC_LOOP7	R/W	0h	Freezes the LED DC cancellation loop number #7
6	FREEZE_LED_DC_LOOP6	R/W	0h	Freezes the LED DC cancellation loop number #6
5	FREEZE_LED_DC_LOOP5	R/W	0h	Freezes the LED DC cancellation loop number #5
4	FREEZE_LED_DC_LOOP4	R/W	0h	Freezes the LED DC cancellation loop number #4
3	FREEZE_LED_DC_LOOP3	R/W	0h	Freezes the LED DC cancellation loop number #3
2	FREEZE_LED_DC_LOOP2	R/W	0h	Freezes the LED DC cancellation loop number #2
1	FREEZE_LED_DC_LOOP1	R/W	0h	Freezes the LED DC cancellation loop number #1
0	FREEZE_LED_DC_LOOP0	R/W	0h	Freezes the LED DC cancellation loop number #0

Register: 9Eh**Figure 7-107. Register: 9Eh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	USE_MSB_FOR_DRE	REG_SCALE_DRE		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-93. Register 9Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-4	0	R/W	0h	Must write 0
3	USE_MSB_FOR_DRE	R/W	0h	Setting the USE_MSB_FOR_DRE bit to 1 remaps the DRE code to the D23..D0 bits.
2-0	REG_SCALE_DRE	R/W	0h	Set REG_SCALE_DRE register word (common for all the loops) to represent the factor by which the Dynamic range is to be extended.

Register: 9Fh**Figure 7-108. Register: 9Fh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	GAIN_CALIB_LED_DC_142K		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-3Dh		
7	6	5	4	3	2	1	0
				GAIN_CALIB_LED_DC_142K			
				R/W-3Dh			

Table 7-94. Register 9Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10-0	GAIN_CALIB_LED_DC_142K	R/W	3Dh	Transfer function between LED Offset DAC code and ADC output code corresponding to a TIA gain setting of 142 kΩ.

Register: A0h**Figure 7-109. Register: A0h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	GAIN_CALIB_LED_DC_166K		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-47h	
7	6	5	4	3	2	1	0
				GAIN_CALIB_LED_DC_166K			
					R/W-47h		

Table 7-95. Register A0h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10-0	GAIN_CALIB_LED_DC_166K	R/W	47h	Transfer function between LED Offset DAC code and ADC output code corresponding to a TIA gain setting of 166 kΩ.

Register: A1h**Figure 7-110. Register: A1h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	GAIN_CALIB_LED_DC_200K		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-55h	
7	6	5	4	3	2	1	0
				GAIN_CALIB_LED_DC_200K			
					R/W-55h		

Table 7-96. Register A1h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10-0	GAIN_CALIB_LED_DC_200K	R/W	55h	Transfer function between LED Offset DAC code and ADC output code corresponding to a TIA gain setting of 200 kΩ.

Register: A2h**Figure 7-111. Register: A2h**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	GAIN_CALIB_LED_DC_250K		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-6Bh	
7	6	5	4	3	2	1	0
				GAIN_CALIB_LED_DC_250K			
					R/W-6Bh		

Table 7-97. Register A2h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Must write 0
10-0	GAIN_CALIB_LED_DC_250K	R/W	6Bh	Transfer function between LED Offset DAC code and ADC output code corresponding to a TIA gain setting of 250 kΩ.

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Register: B4h**Figure 7-112. Register: B4h**

23	22	21	20	19	18	17	16
COMB_THR_D ET_EN	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	REG_THR_DE T_PHASE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
REG_THR_DET_PHASE				0	THR_SEL_LOGIC	THR_DET_EN	
R/W-0h				R/W-0h	R/W-0h	R/W-0h	

Table 7-98. Register B4h Field Descriptions

Bit	Field	Type	Reset	Description
23	COMB_THR_DET_EN	R/W	0h	Set to '1' (along with the THR_DET_EN bit) to enable the Combinational Threshold detect mode.
22-7	0	R/W	0h	Must write 0
8-4	REG_THR_DET_PHASE	R/W	0h	The number of the phase-set, the data from which is to be used for the Threshold detect comparison is as (REG_THR_DET_PHASE+1).
3	0	R/W	0h	Must write 0
2-1	THR_SEL_LOGIC	R/W	0h	The manner of combining the different checks to generate the THR_DET_RDY can be altered by using the register control THR_SEL_LOGIC.
0	THR_DET_EN	R/W	0h	Enables the threshold detect mode.

Register: B5h**Figure 7-113. Register: B5h**

23	22	21	20	19	18	17	16
x	x	x	x	x	x	x	x
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
15	14	13	12	11	10	9	8
THR_PPG_FLAG							
R-x							
7	6	5	4	3	2	1	0
THR_PPG_FLAG							
R-x							

Table 7-99. Register B5h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	x	R	x	-
15-0	THR_PPG_FLAG	R	x	Flag register that indicates the result of threshold detect comparison. THR_PPG_FLAG[N] corresponds to the result of threshold detect comparison from PPG phase [N]

Register: CAh**Figure 7-114. Register: CAh**

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	EN_ALWAYS_ACTIVE	DIS_DEEP_SLEEP_EEP	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-100. Register CAh Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	R/W	0h	Must write 0
14	EN_ALWAYS_ACTIVE	R/W	0h	Set the EN_ALWAYS_ACTIVE bit to '1' to keep the device in active state throughout the PRF cycle.
13	DIS_DEEP_SLEEP	R/W	0h	Set the DIS_DEEP_SLEEP bit to '1' to disable the entry into deep sleep.
12-0	0	R/W	0h	Must write 0

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LED_SW: Register 20h

Figure 7-115. Register 20h

23	22	21	20	19	18	17	16
PHASE_INT_G PIO	0	THR_SEL_DATA_CTRL	THR_SEL	0	THR_SEL_TIA_NUM	0	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15	14	13	12	11	10	9	8
0	0	0	0		LED_DRV2_TXN<4:1>		
R/W-x	R/W-x	R/W-x	R/W-x		R/W-x		
7	6	5	4	3	2	1	0
0	0	0	0		LED_DRV1_TXN<4:1>		
R/W-x	R/W-x	R/W-x	R/W-x		R/W-x		

Table 7-101. Register 20h Field Descriptions

Bit	Field	Type	Reset	Description
23	PHASE_INT_GPIO	R/W	x	The PHASE_OUT interrupt goes high in the phase window if the PHASE_INT_GPIO bit is high.
22	0	R/W	x	Must write 0
21-20	THR_SEL_DATA_CTRL	R/W	x	The appropriate data associated with the phase selected for threshold detection is set by the per-phase control THR_SEL_DATA_CTRL.
19	THR_SEL	R/W	x	Selection of which set of high/ low threshold codes to use is set by THR_SEL
18	0	R/W	x	Must write 0
17	THR_SEL_TIA_NUM	R/W	x	The TIA# whose output is to be used for the threshold detection is specified using the per-phase parameter THR_SEL_TIA_NUM.
16-12	0	R/W	x	Must write 0
11-8	LED_DRV2_TXN<4:1>	R/W	x	Control to turn on the switches for LED driver 2.
7-4	0	R/W	x	Must write 0
3:0	LED_DRV1_TXN<4:1>	R/W	x	Control to turn on the switches for LED driver 1.

LED_ON: Register 21h

Figure 7-116. Register 21h

23	22	21	20	19	18	17	16
REG_TWLED							
R/W-x							
15	14	13	12	11	10	9	8
ILED_DRV2							
R/W-x							
7	6	5	4	3	2	1	0
ILED_DRV1							
R/W-x							

Table 7-102. Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	REG_TWLED	R/W	x	LED ON time control.
15-8	ILED_DRV2	R/W	x	Current setting for LED driver 2
7:0	ILED_DRV1	R/W	x	Current setting for LED driver 1

Control_TIA1: Register 22h**Figure 7-117. Register 22h**

23	22	21	20	19	18	17	16
0	0	0	0	IN_TIA1<3:1>		LED_DC_EN_TIA1	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		R/W-x
15	14	13	12	11	10	9	8
			IOFFDAC_LED_TIA1				
			R/W-x				
7	6	5	4	3	2	1	0
IOFFDAC_LED_TIA1		CF_TIA1			RF_TIA1		
R/W-x		R/W-x			R/W-x		

Table 7-103. Register 22h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	x	Must write 0
19-17	IN_TIA1<3:1>	R/W	x	Controls the connection of the 3 PD input pairs to TIA1.
16	LED_DC_EN_TIA1	R/W	x	Enable LED DC cancellation for TIA1.
15-7	IOFFDAC_LED_TIA1	R/W	x	MCU control of LED Offset DAC for TIA1.
6-4	CF_TIA1	R/W	x	C _F setting for TIA1
3-0	RF_TIA1	R/W	x	R _F setting for TIA1

Control_TIA2: Register 23h**Figure 7-118. Register 23h**

23	22	21	20	19	18	17	16
0	0	0	0	IN_TIA2<3:1>		LED_DC_EN_TIA2	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		R/W-x
15	14	13	12	11	10	9	8
			IOFFDAC_LED_TIA2				
			R/W-x				
7	6	5	4	3	2	1	0
IOFFDAC_LED_TIA2		CF_TIA2			RF_TIA2		
R/W-x		R/W-x			R/W-x		

Table 7-104. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	x	Must write 0
19-17	IN_TIA2<3:1>	R/W	x	Controls the connection of the 3 PD input pairs to TIA2.
16	LED_DC_EN_TIA2	R/W	x	Enable LED DC cancellation for TIA2.
15-7	IOFFDAC_LED_TIA2	R/W	x	MCU control of LED Offset DAC for TIA2.
6-4	CF_TIA2	R/W	x	C _F setting for TIA2
3-0	RF_TIA2	R/W	x	R _F setting for TIA2

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MISC: Register 24h**Figure 7-119. Register 24h**

23	22	21	20	19	18	17	16
SEL_SAMPLE_DELAY_SET		REG_DEC_FACTOR			FIFO_DATA_CTRL		
R/W-x		R/W-x			R/W-x		
15	14	13	12	11	10	9	8
REG_NUMAV			REG_PH_MASK_FACTOR				
R/W-x			R/W-x				
7	6	5	4	3	2	1	0
ENABLE_DRE	AUTO_AMB_INSERT		0	REG_NUM_TIA	FILTER_SET_SEL	USE_ANA_AACM	UPDATE_BASELINE_AMB
R/W-x	R/W-x		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

Table 7-105. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	SEL_SAMPLE_DELAY_SET	R/W	x	Determines which of the 4 sets of register control for tSAMP_DELAY is used.
21-19	REG_DEC_FACTOR	R/W	x	Controls decimation factor for the phase.
18-16	FIFO_DATA_CTRL	R/W	x	Determines how the FIFO word associated with the phase is computed.
15-12	REG_NUMAV	R/W	x	Setting of number of ADC averages.
11-8	REG_PH_MASK_FACTOR	R/W	x	Controls the masking factor for the phase.
7	ENABLE_DRE	R/W	x	A Dynamic Range Extension (DRE) mode can be set for a phase using the ENABLE_DRE bit. If this bit is set to 1, then the DRE mode gets applied on all the LED DC cancellation loops that are enabled in that phase.
6-5	AUTO_AMB_INSERT	R/W	x	Controls the automatic insertion of Ambient phases before and/or after the phase.
4	0	R/W	x	Must write 0
3	REG_NUM_TIA	R/W	x	Determines the number of TIAs used in the phase. The number of convert signals is set as (REG_NUM_TIA+1).
2	FILTER_SET_SEL	R/W	x	Select between Filter set 1 and set 2.
1	USE_ANA_AACM	R/W	x	Associate an Analog AACM loop operation with the phase.
0	UPDATE_BASELINE_AMB	R/W	x	Setting this bit to '1' is an indication that this phase is meant to serve as the baseline ambient phase, and that the ambient must be acquired in this phase. Setting this bit to '0' uses the baseline value of the ambient from the previous baseline ambient phase.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Important Guidelines

The AFE has several knobs for adapting the signal chain to the actual operating conditions. A set of guidelines for maximizing the performance from the AFE are listed below.

1. Use ambient cancellation (either through MCU control or using the Analog AACM loop) to cancel the ambient current right at the AFE input using the Ambient Offset DAC.
2. If there is a significant DC from LED, then use the LED Offset DAC to remove the DC of the LED. This cancellation is done either through MCU control or by enabling Automatic LED DC cancellation. However, such a dynamic control of the LED Offset DAC to cancel the DC in the LED phase can result in discontinuities in the output waveform, which must be handled by the heart rate extraction algorithm. By enabling the DRE mode, such discontinuities can be removed. Additionally, applications like SpO₂ require an accurate estimate of the DC component that is subtracted from the signal using the LED offset DAC. Contact the factory for details on how to recover the DC information.
3. With both Ambient and LED DC suppressed, use a high gain setting (R_F) to reduce the input referred noise of the AFE. A setting of 250 kΩ or lower can be sufficient to achieve the required SNR for most scenarios. Also use the highest value of C_F such that the TIA time constant is consistent with the guidelines in [Table 7-26](#). Choice of a higher LED ON time allows setting of a lower filter bandwidth as shown in [Table 7-26](#), leading to a lower system noise.
4. Use the lowest full-scale range of the Offset DAC (taking into account the ±20% variation) that can be sufficient to cancel the ambient current. For example, if the Ambient DC is less than 10 μA, then set IFS_OFFSETDAC to operate in the 1X mode. The extra noise added by the Offset DAC is lowest in the 1X mode and increases when the higher full scale modes are used.
5. Operating the LED driver with the highest headroom (V_{HR}) reduces the noise contribution from the LED driver. For the same current setting, operating in the 3.3X mode gives the lowest noise and operating in the 1X mode gives the highest noise.
6. Defining an ambient phase and digitally subtracting the ambient from the LED phase is highly recommended. This subtraction helps to suppress ambient tones and also helps cancel low frequency noise and drifts internal to the AFE. The closer the position of the ambient and LED phases, the better the suppression of the ambient tones. If there are multiple LED phases, then having a separate ambient phase next to each LED phase can give better suppression as compared to using an ambient phase spaced far apart from the LED phase. Defining and combining multiple ambient phases can result in improved ambient cancellation. Contact the factory for details.
7. For best ambient rejection, especially at higher ambient frequencies, use the maximum ambient rejection mode.
8. Ensure that none of the signal phases saturates the signal chain. In phases immediately following a phase where the signal chain is saturated, the performance of the receiver can be worse than expected. Ambient cancellation can also degrade with saturation of the signal chain in channels adjacent to the signal phases of interest. The EN_TIA_RST bit enables reset of the TIA between phases, and can lead to a lower level of signal disturbance due to a previous saturated phase.
9. The differential connection of the PD to the AFE causes the PD to operate close to zero bias. However, a slight forward bias can be developed across the PD especially in the presence of a signal current in the PD. Therefore, TI recommends to use a PD that has a relatively flat sensitivity between zero bias and approximately 150 mV of forward bias.

10. Dynamically control the TIA gain (R_F) and LED current (I_{LED}) through the MCU to achieve excellent signal quality.
11. The per-phase registers in Page 1 are not reset to any default values. Therefore, all per-phase registers corresponding to all the active phases can be explicitly programmed before starting the PPG signal acquisition.

8.2 Typical Application

8.2.1 Application

A typical application of the device is optical heart rate monitoring (OHRM). [Figure 8-1](#) shows an overview of a heart rate monitoring signal chain using the AFE4432.

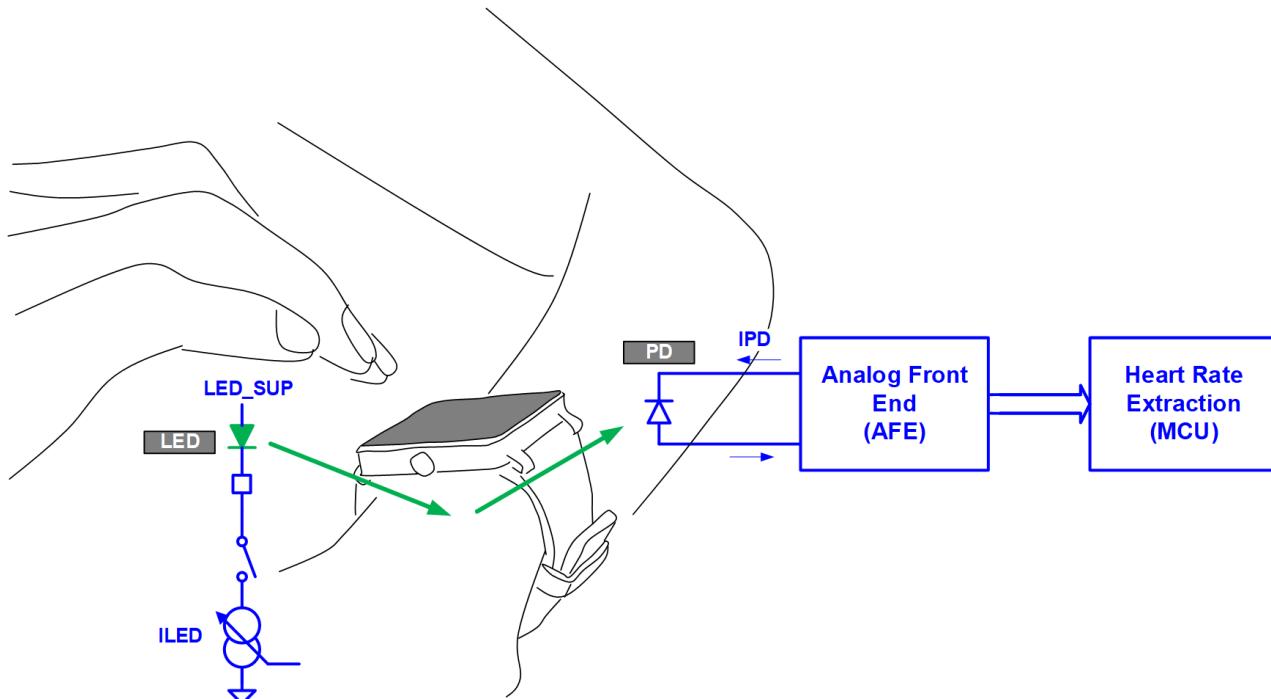


Figure 8-1. Overview of a Typical OHRM System

The OHRM system uses the LED to make a light incident on the human skin. The pulsatile signal reflection is converted to a current using a photodiode (PD) and processed by the AFE4432. The digital equivalent of the PD current is output from the AFE4432 on an SPI or I₂C interface and processed by the MCU to extract the heart rate. The signal processing block in the MCU can also calibrate and optimize the device signal chain settings to maximize the signal strength output from the AFE4432. The OHRM system can involve usage of multiple LEDs (typically green) and PDs, spatially arranged to reduce artefacts like motion. Additionally, the system can include additional LEDs (typically red and IR) for measurement of SpO₂. A large number of LEDs can be used in spectroscopy applications.

8.2.2 Design Requirements

Table 8-1 shows the typical design requirements of an OHRM system using the AFE4432.

Table 8-1. Design Requirements of OHRM System

PARAMETER	EXAMPLE VALUE	COMMENTS
RX_SUP	1.8 V	Have enough margin for DC inaccuracy and ripple in the supply driver. An external LDO may be required to achieve the required PSRR and to eliminate output tones.
TX_SUP	5 V	If directly driven from the battery, the LED driver is functional down to the lowest battery voltage where the headroom requirements are satisfied. If driven by the output of a boost converter, choose the boost converter output voltage based on the LED forward voltage and the voltage headroom requirements of the AFE4432 current driver at the maximum current setting.
PRF	50 Hz	Based on the sampling rate required by the heart rate monitoring algorithm in the MCU. Set by the PRPCT setting.
Output heart rate	0.5 Hz to 4 Hz	Typical range of the human heart rate to be measured.

8.2.3 Detailed Design Procedure

The following important factors are key to extracting the full performance benefit from the AFE4432:

1. Good optics including bright LEDs, and high sensitivity photodiodes and their excellent construction and placement.
2. Good mechanical design.
3. An automatic gain control (AGC) loop in the MCU that sets excellent device settings based on the signal conditions.

The AFE4432 has a high dynamic range. This high dynamic range can be very useful in enabling accurate heart rate monitoring even when the pulsatile signal is weak or in the presence of highly interfering ambient and motion artifacts. The control knobs include TIA gain (R_F), TIA bandwidth, LED current (I_{LED}), offset cancellation DAC (I_{OFFDAC}), and the bandwidth setting of the noise-reduction filter (f_{RC}). The PPG signal as observed at the output of the AFE is one-sided (either always positive or always negative, depending on the polarity of the PD connection to the AFE inputs) and contains a high dc signal and a small ac signal (which is the signal of interest from which the heart rate frequency can be calculated). If such a signal is directly input to the TIA, then severe underutilization of the device dynamic range results. However, by subtracting a programmable current at the input of the TIA using the offset cancellation DAC, the signal going into the TIA can be centered around zero and a high gain can be applied so that the signal of interest fills a larger fraction of the dynamic range. Operating at higher TIA gains results in a lower input referred noise and better signal quality at the AFE output. The DC signal in the ambient phase can be automatically cancelled by enabling the AACM loop. The MCU can set an additional Offset DAC increment to cancel out all or a portion of the DC signal in the LED phase or the Automatic LED DC cancellation feature can be used to do this same function.

The DC from the ambient signal can be automatically cancelled using the Analog AACM loop. In this manner, the control of the Ambient Offset DAC can be automatically handled by the AFE without MCU intervention. In cases where the DC in the LED phase drifts slowly, the LED Offset DAC can be controlled by the AFE using the Automatic LED DC cancellation feature. In that case, the MCU can need to periodically update only the TIA gain and the LED current to achieve an optimum signal level. For example, if the AC signal is weak (as determined by the heart rate extraction algorithm), the LED current can need to be increased. Also, if the signal level in the LED phase changes fast causing the output to approach saturation (or for the LED Offset DAC to constantly keep getting updated by the Automatic LED DC cancellation), the TIA gain can need to be reduced. Intelligent control involves periodic updating of these parameters to achieve optimum utilization of the full dynamic range of the AFE, while not causing disruption to the acquired signal so often that the heart rate extraction accuracy is compromised.

AFE4432 has multiple phase timing schemes to help adapt to different system challenges. When the ambient signal is high and fast-changing, the best ambient rejection can be achieved by using the *Maximum Ambient rejection mode*. When a large number of LEDs and PDs are used and a large number of signals need to be acquired at high sampling rate, this is useful to operate in the *High PRF mode*.

8.2.4 Application Performance Plots

[Figure 6-3](#) shows the Signal to Noise ratio (SNR) measured as a function of input signal current. The SNR is defined by the ratio of the input signal current and the input referred current noise. The AFE is hooked up to a LED and PD (indicative of the complete system). The light from the LED is made to reflect on to the PD, which generates the indicated level of input signal current. The Current transfer ratio (CTR) is set to 300 nA/mA. By adjusting the LED current up to 100 mA, the signal current from the PD is swept up to approximately 30 μ A. The LED Offset DAC is set to cancel out the DC level of the input signal at each setting so that the AFE output is roughly zero. The TIA gain is set to 250 k Ω . The total output noise from the AFE (in the LED minus Ambient data) integrated over the 0.5-10 Hz band is converted to an input referred current noise. This noise current is inclusive of the noise from all the components in the system - the optical noise from the LED and PD as well as the electrical noise from the AFE transmit and receive paths, including the Offset DAC. The noise is computed in the frequency band of 0.5 Hz to 10 Hz from the FFT of the data stream, and is referred to the AFE input as a current noise. The SNR is computed in dB by referring the rms value of the input-referred current noise to the input signal current from the PD set for the measurement. The various curves correspond to different PRF settings. At higher PRF settings, the total system noise spreads over a wider Nyquist bandwidth, resulting in a lower noise in the 0.5-10 Hz band (and hence, a better SNR). For this plot, an LED ON width (and SAMP width) of approximately 117 μ s is used.

[Figure 6-4](#) is similar to [Figure 6-3](#), but the noise is computed in a 0.5-10 Hz band and converted to SNR.

[Figure 6-5](#) shows the input referred current noise of the receiver versus Number of ADC Averages (NUMAV). The multiple curves correspond to different TIA gain settings. The SNR improves with higher number of ADC averages but the improvement becomes marginal for the higher TIA gains. This is because the contribution of the ADC noise to the total noise becomes less significant at higher TIA gain settings. An LED ON time of approximately 94 μ s is used.

[Figure 6-6](#) shows Input referred noise current of the Receiver over the full Nyquist bandwidth for different settings of the SAMP width (same as LED ON time) across different TIA gains. For each LED ON time setting, the TIA time constant and Filter settings are chosen as per the guidelines in [Table 7-26](#). The measurement is done with zero input current signal. The output noise from the AFE is measured and converted to input referred noise current (the transfer function between the output voltage noise and input referred current noise is determined by the TIA gain used for the measurement). At higher TIA gains, the input referred current noise from the AFE receiver reduces. Similarly, at higher LED ON times, the filter can be operated at a lower bandwidth. This too results in a lowering of the input-referred noise. This plot shows the two differentiating features of the AFE architecture - the benefits of input DC cancellation which allow operating at high TIA gain, and the noise bandwidth reduction resulting from the filter.

[Figure 6-7](#) shows the Ambient rejection in dB vs. Ambient signal frequency across different LED ON times. The dB scale refers to the magnitude of the ambient tone seen at the AFE output referred to the ambient signal amplitude. The device is operated in the Maximum ambient rejection mode. The high-frequency ambient rejection improves with lower LED ON times due to the reducing separation between the sampling instants of the LED and Ambient phases.

[Figure 6-8](#) shows the effect of a tone on the RX_SUP pin. The amplitude of the tone is set to 50 mVpp and the frequency is swept. The TIA gain is set to 500 K Ω and the input current for the four different curves is adjusted, which results in output DC levels of 0.25 V, 0.5 V, 0.75 V and 1 V respectively. The output tone as a function of the frequency of the tone on RX_SUP is plotted.

[Figure 6-9](#) shows the output tone due to the 50 mVpp tone on RX_SUP around different levels of the RX_SUP voltage.

[Figure 6-10](#) shows the effect of a tone on the TX_SUP pin when the LED driver current is set to 50 mA in the 1X ILED_FS mode (and a single driver is turned on). The amplitude of the tone on TX_SUP is set to 50 mVPP and the frequency is swept. The PSRR is defined as the equivalent tone on the LED driver current (deduced from the tone at the receiver output) referred to the current setting of 50 mA. The PSRR curve is plotted for different values of LED driver headroom, which is measured as the lowest voltage at the TX pin during the transient wave form resulting from the tone on TX_SUP.

[Figure 6-11](#) shows the TX_SUP PSRR for a LED driver current of 50 mA in the 2.5X ILED_FS mode.

[Figure 6-12](#) shows the TX_SUP PSRR for a LED driver current of 50 mA in the 3.3X ILED_FS mode.

[Figure 6-13](#) shows the Ambient Offset DAC current across the decimal equivalent of the code for the different full-scale modes.

[Figure 6-14](#) shows the LED Offset DAC current across the decimal equivalent of the code.

[Figure 6-15](#) shows the LED current as a function of the voltage at the TX pin for the single driver case when TX_SUP is set to 3 V. The voltage at the TX pin is swept by connecting a load resistor from the TX pin to LED_SUP (a supply different from TX_SUP) and changing the voltage of LED_SUP to control the voltage on the TX pin. The voltage headroom required by the driver can be determined by the TX pin voltage beyond which the current curve becomes flat.

[Figure 6-16](#) shows the LED current as a function of the voltage at the TX pin for the dual driver case when TX_SUP is set to 3 V.

[Figure 6-17](#) shows the LED current as a function of the voltage at the TX pin for the single driver case when TX_SUP is set to 5 V.

[Figure 6-18](#) shows the LED current as a function of the voltage at the TX pin for the dual driver case when TX_SUP is set to 5 V.

[Figure 6-19](#) shows the LED driver current across the decimal equivalent of the code as set by the ILED* register for the different full-scale modes. A single driver is enabled in these measurements.

[Figure 6-20](#) shows the LED driver current across code with both drivers enabled.

[Figure 6-21](#) shows the % variation of the 256 kHz oscillator frequency as a function of temperature on a typical unit.

[Figure 6-22](#) shows the RX_SUP current versus PRF with Internal and External Clock modes. As the PRF is reduced, the device spends more time in the Deep sleep phase which results in a reduction in the RX_SUP current at the lower PRF settings.

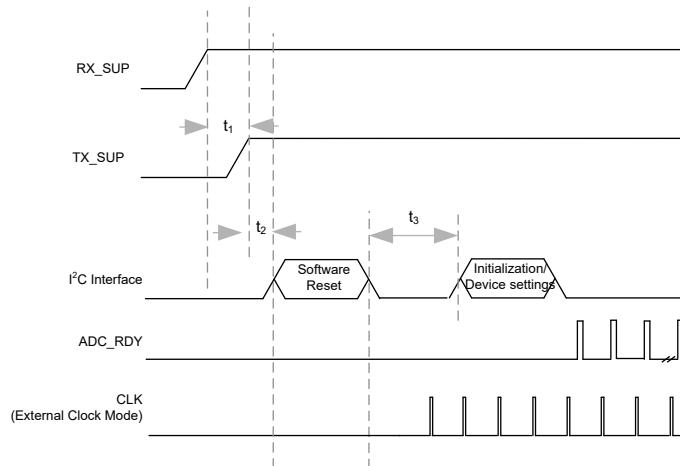
8.3 Power Supply Recommendations

The power supply recommendations are listed below:

1. Choose the voltages on the supply rails based on the ranges listed in the Recommended Operating Conditions section. Ensure that the voltages never exceed the values listed in the [Absolute Maximum Ratings](#) table.
2. Follow the supply ramp-up sequence suggested in the [Power Supply Ramp-Up](#) and [Device Initialization](#) sections while powering up the device, and while using the hardware power-down mode. A failure to follow the suggested sequence could result in an erroneous operation of the AFE.
3. Never operate the device for any extended duration of time with any one of the supplies switched ON and the other switched OFF.
4. Refer to the PSRR plots in the [Typical Characteristics](#) section to determine the maximum allowed ripple in the RX_SUP rail. Use appropriate values of decoupling capacitors on all the supply rails.
5. If using a boost converter to drive the TX_SUP rail, check if the PSRR of the LED driver is within acceptable limits based on the switching frequency of the boost converter and the estimated ripple.

8.3.1 Power Supply Ramp-Up

The suggested sequence of operations while powering up the device is illustrated in [Figure 8-2](#). The corresponding parameters are listed in [Table 8-2](#).

**Figure 8-2. Suggested Sequence of Operations While Powering up the Device****Table 8-2. Parameters Associated with Powering up the Device**

		VALUE
t_1	Time between the end of the RX_SUP Ramp-up window and the ramp-up of TX_SUP	Keep t_1 as small and no more than 100 ms
t_2	Time between both supplies stabilizing and resetting the device	> 1 ms
t_3	Time between applying a reset and writing registers for Device initialization and configuration	> 1 ms

8.3.2 Device Initialization

8.3.2.1 Initialization Sequence After Power up

After the AFE has been powered up with all supplies switched on, use the following sequence to initialize the device:

1. Wait for 1 ms
2. Apply a reset (software or hardware)
3. Write PAGE_SEL to '1'
4. Write the relevant register settings in Page 1 of the register map. All the per-phase registers associated with the intended number of phases (1...NUMPHASE) need to be written. This applies even to per-phase registers which do not contain functions intended for use, and which need to have all bits set to zero. Registers in Page 1 do not have default values and do not get reset. Therefore, not writing all the per-phase registers explicitly can result in one or more bits have unintended values.
5. Write PAGE_SEL to '0'
6. Program the registers in Page 0. The registers can be programmed in any order (with the exception that TIMER_ENABLE and PRF_COUNTER_ENABLE should be programmed in Step 8).
7. TI recommends that the Interrupt service routine in the MCU is enabled to service interrupts from the AFE only after Step 6, to prevent the MCU from responding to a spurious interrupt that could have come during device power up or during the middle of the initialization sequence.
8. Set the TIMER_ENABLE and PRF_COUNTER_ENABLE bits to '1'. The timing engine starts running and the FIFO starts off in an initialized state.

This initialization sequence must be followed after every power-up cycle of the device. The same device initialization sequence can be performed when coming out of the software power down mode. However, during software power down, the registers retain their state and need not be reprogrammed if there is no change required in their values.

8.3.2.2 Sequence to Reconfigure the FIFO

If PRF or the number of signal phases in a PRF must be changed, or if any of the FIFO configuration must be changed or if the FIFO must be reset and fresh signal must be acquired in the FIFO, the FIFO must be first disabled (set FIFO_EN to '0'). To re-enable the FIFO, follow the below sequence:

1. Set bits TIMER_ENABLE AND PRF_COUNTER_ENABLE to '0'
2. Set TM_COUNT_RST bit to '1' and FIFO_EN to '0'
3. Make changes to any of the parameters in Page 0 or Page 1
4. Program register 00h in Page 0, setting FIFO_EN to '1' and TM_COUNT_RST to '0'
5. Set the TIMER_ENABLE and PRF_COUNTER_ENABLE bits to '1'. The timing engine once again starts running and the FIFO starts off in an initialized state.

This initialization sequence can also be followed every time the device comes out of software power-down mode.

8.3.2.3 Sequence to Change any PPG Signal Chain Parameters

The MCU may dynamically update the parameters of the PPG signal chain to optimize the signal quality. If any of the parameters related to the PPG signal chain (like R_F , C_F , LED current, offset DAC and so on) are required to be changed on-the-fly during the device operation and if these changes do not involve any parameters determining the FIFO data streaming, then follow the below guidelines:

1. Wait for the FIFO_RDY interrupt.
2. On receiving the FIFO_RDY interrupt, change the signal chain parameters (only registers that need change).
3. Complete all the programming within the deep sleep window before the start of the next PRF cycle.

8.4 Layout

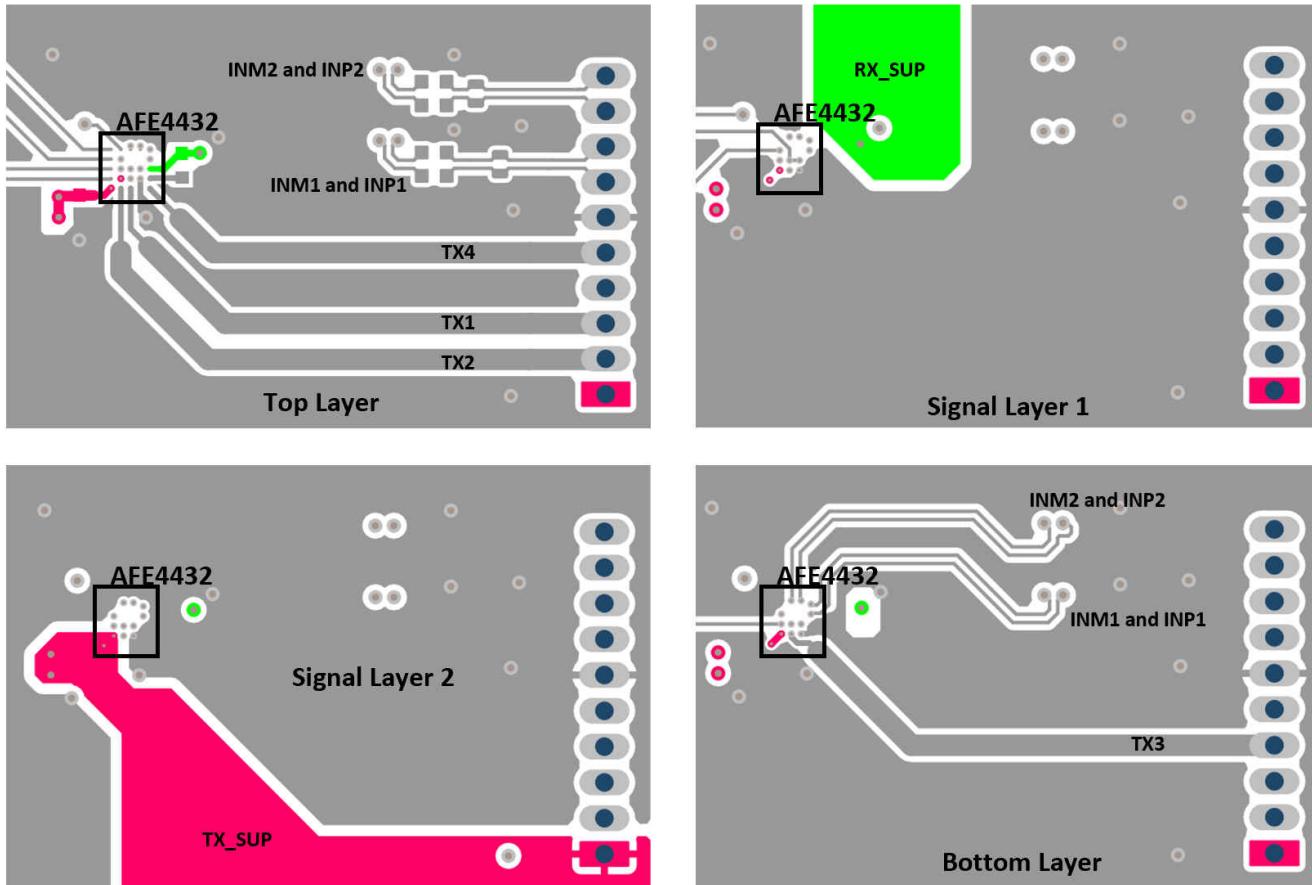
8.4.1 Layout Guidelines

Two key layout guidelines are:

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1. TX pins are fast-switching lines and must be routed away from sensitive lines (such as the INP*, INN* inputs).
2. The device can draw high-switching currents from the TX_SUP pin. A decoupling capacitor must be electrically close to the pin. The extra routing drops in the path of the LEDs should be kept low to minimize resistive losses.

8.4.2 Layout Example**Figure 8-3. Layout Example**

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Package Option Addendum

Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(4) (5)}
AFE4432YCHR	ACTIVE	DSBGA	YCH	25	3000	Green (RoHS & no Sn/Br)	SNAGCU	Level-1-260C-UNLIM	-20 to 85	AFE4432
AFE4432YCHT	ACTIVE	DSBGA	YCH	25	250	Green (RoHS & no Sn/Br)	SNAGCU	Level-1-260C-UNLIM	-20 to 85	AFE4432

- (1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

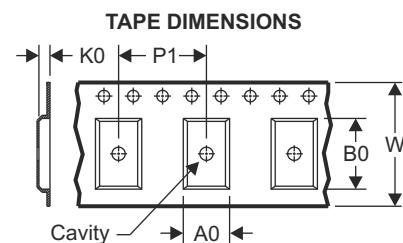
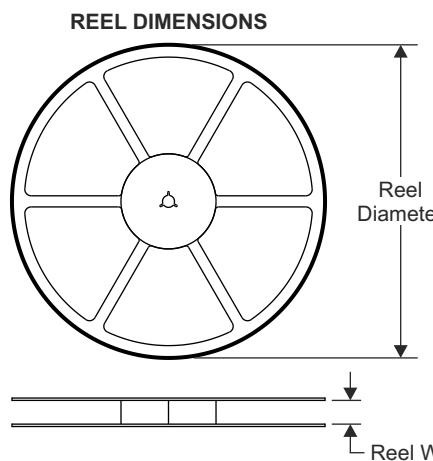
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

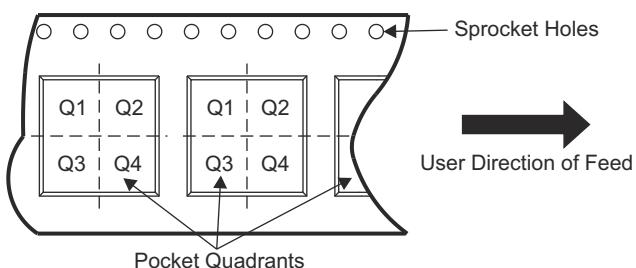
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

10.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

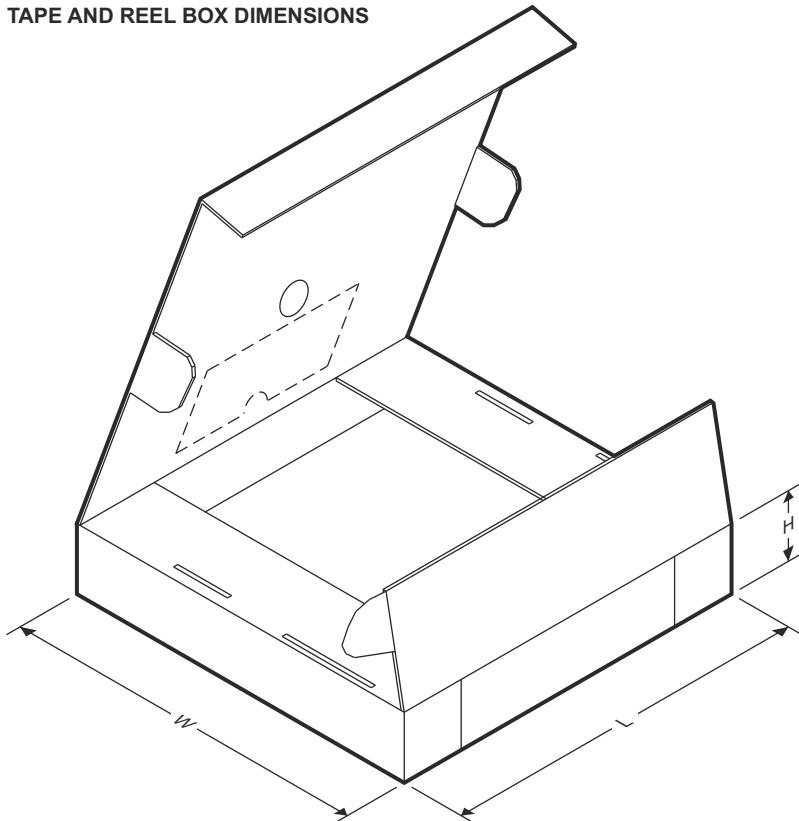


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE4432YCHR	DSBGA	YCH	25	3000	128.0	9.2	1.92	2.02	0.48	4.0	12.0	Q1
AFE4432YCHT	DSBGA	YCH	25	250	128.0	9.2	1.92	2.02	0.48	4.0	12.0	Q1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE4432YCHR	DSBGA	YCH	25	3000	345.0	365.0	55.0
AFE4432YCHT	DSBGA	YCH	25	250	345.0	365.0	55.0

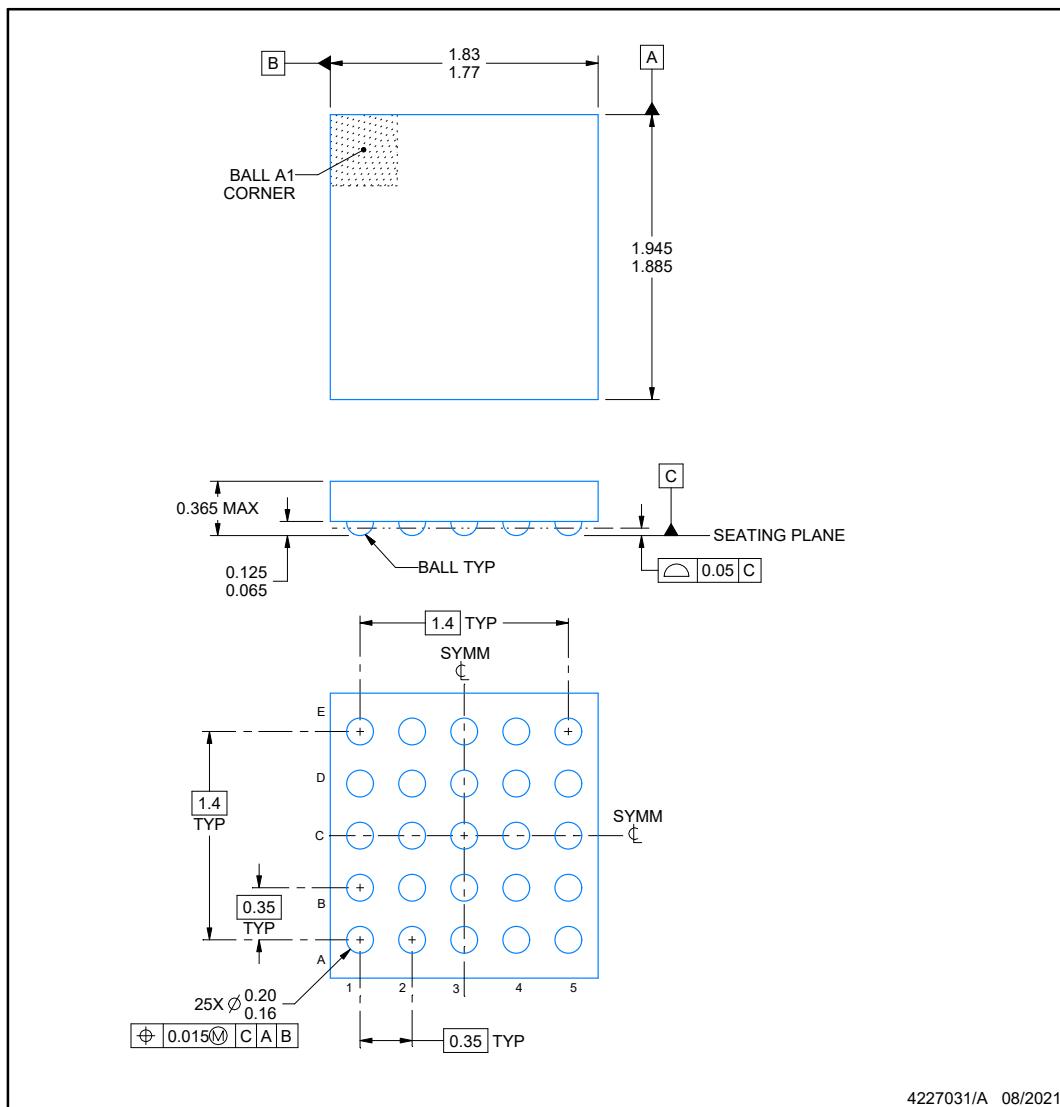
10.3 Mechanical Data

PACKAGE OUTLINE

YCH0025-C01

DSBGA - 0.365 mm max height

DIE SIZE BALL GRID ARRAY



4227031/A 08/2021

NOTES:

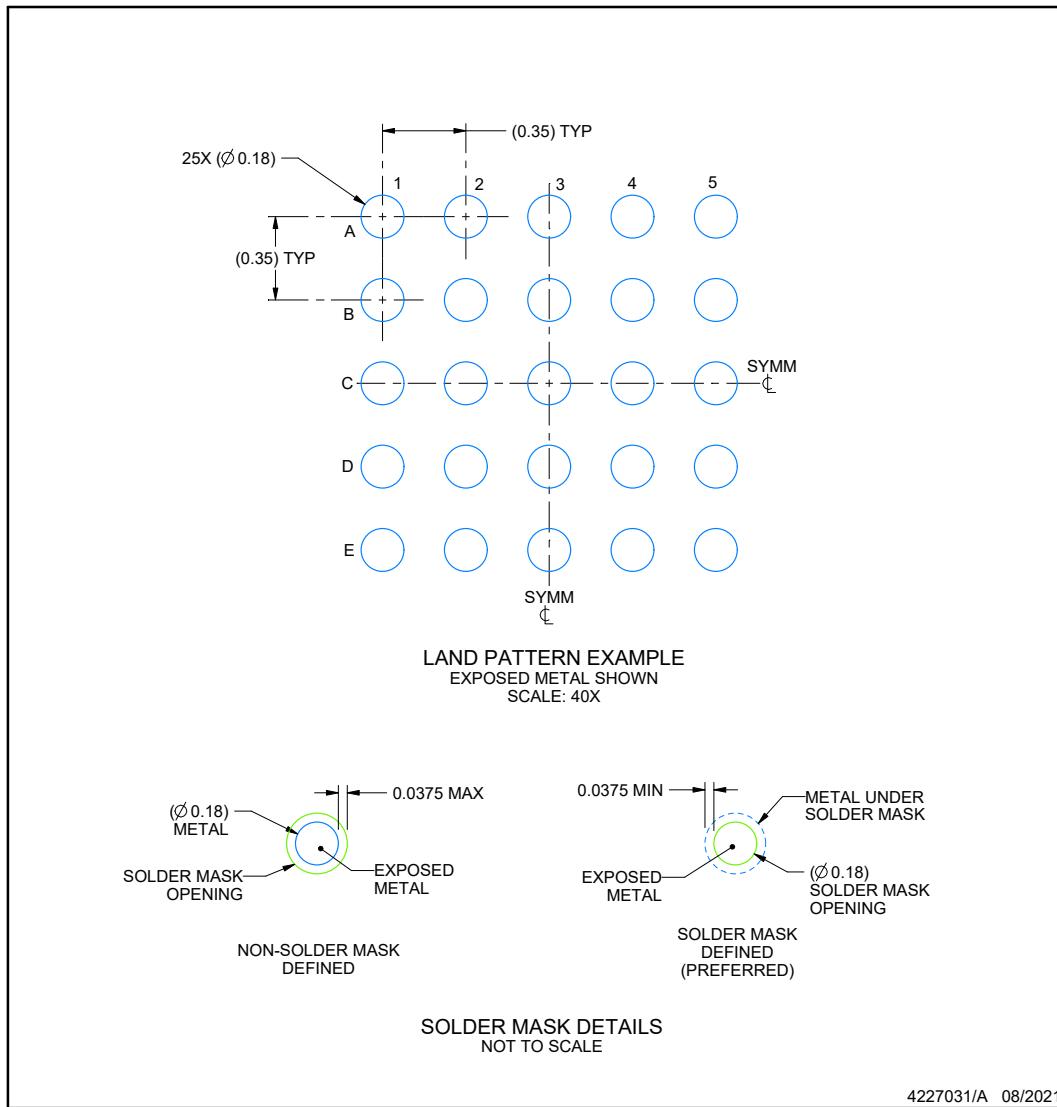
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

AFE4432

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EXAMPLE BOARD LAYOUT**YCH0025-C01****DSBGA - 0.365 mm max height**

DIE SIZE BALL GRID ARRAY

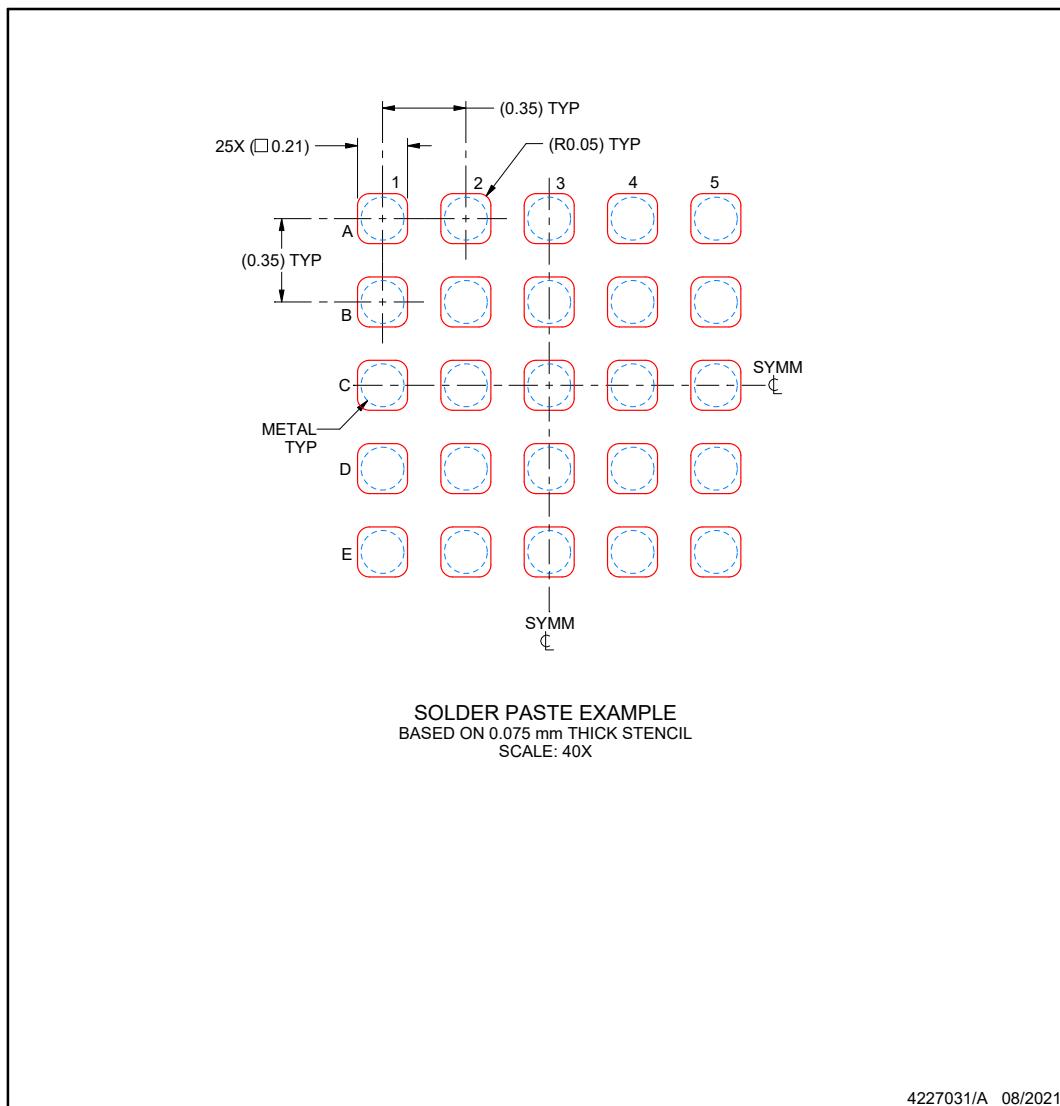


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN**YCH0025-C01****DSBGA - 0.365 mm max height**

DIE SIZE BALL GRID ARRAY



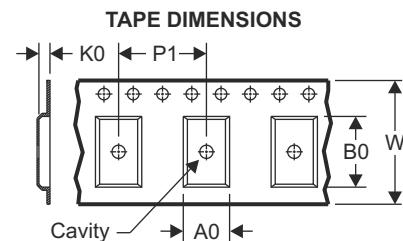
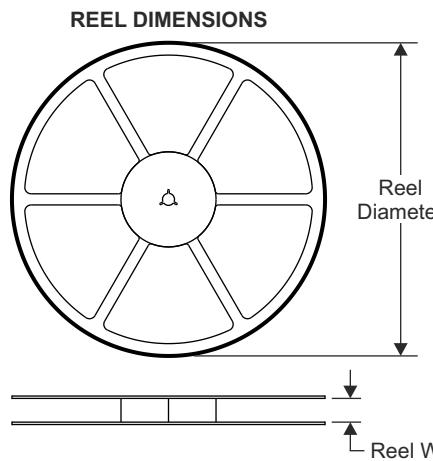
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

AFE4432

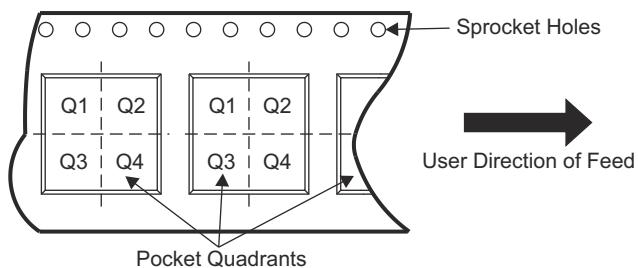
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10.2 Tape and Reel Information

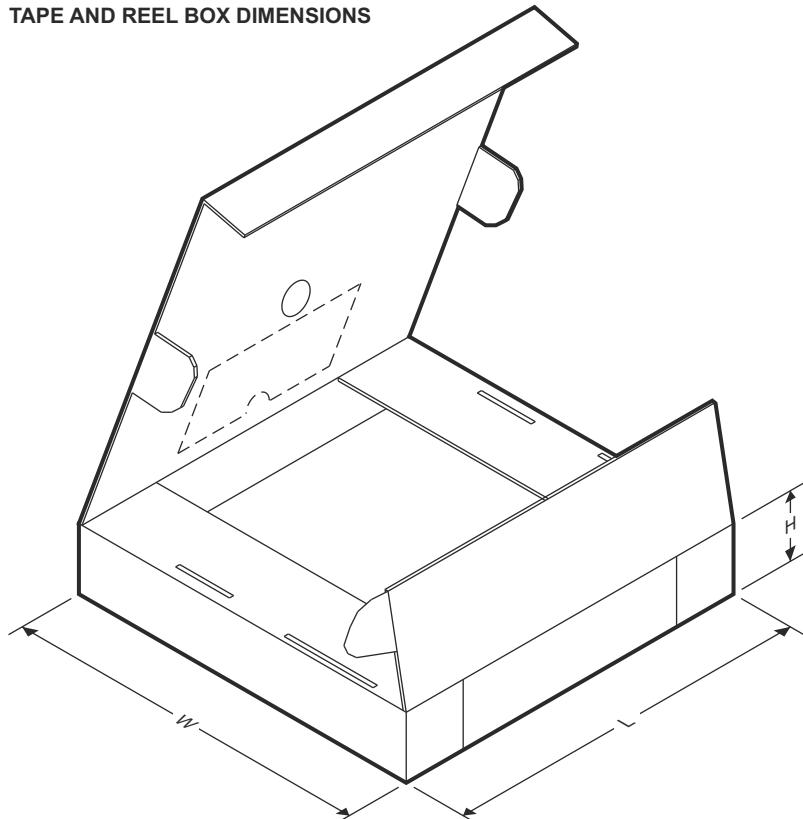


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
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QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE4432YCHR	DSBGA	YCH	25	3000	128.0	9.2	1.92	2.02	0.48	4.0	12.0	Q1
AFE4432YCHT	DSBGA	YCH	25	250	128.0	9.2	1.92	2.02	0.48	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

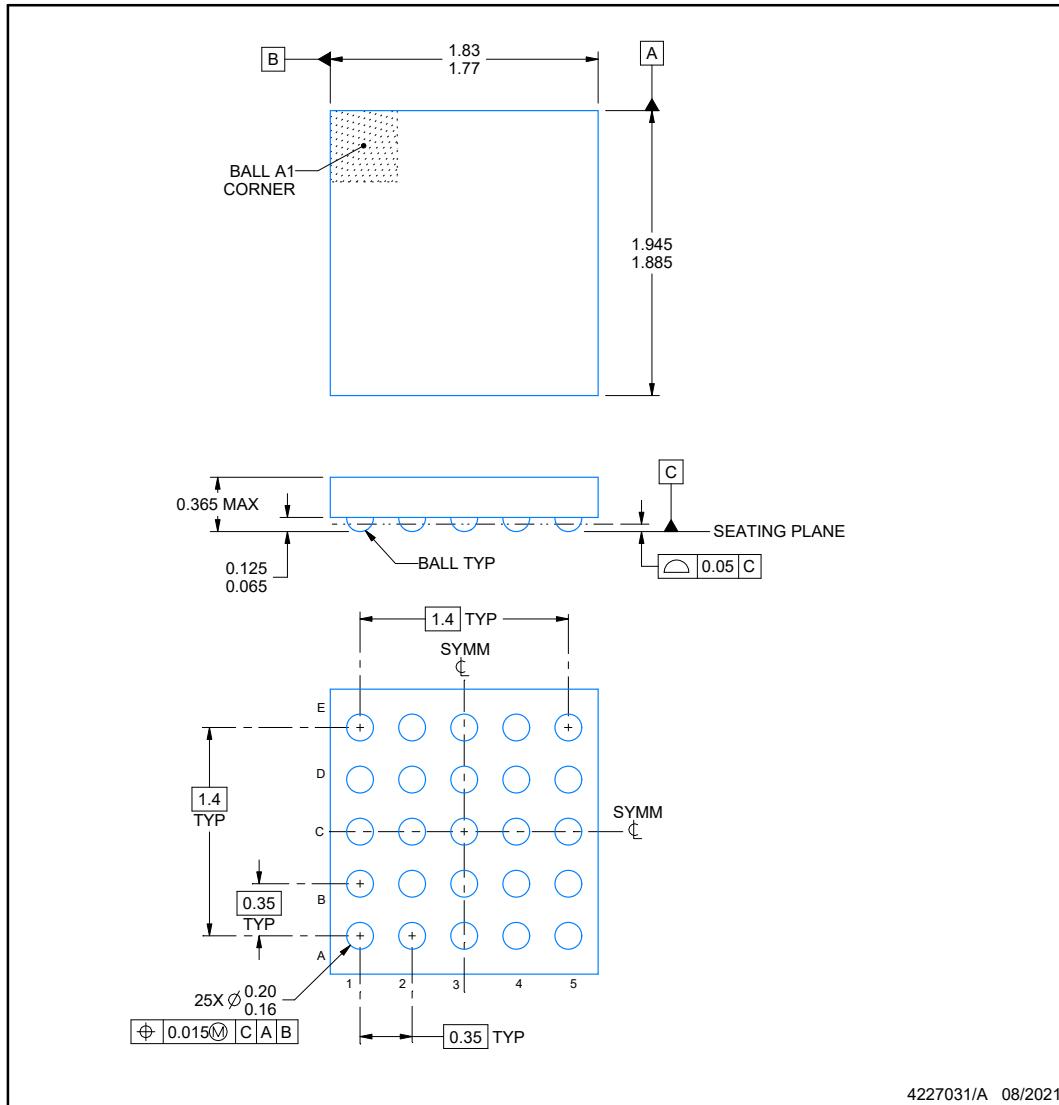
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE4432YCHR	DSBGA	YCH	25	3000	345.0	365.0	55.0
AFE4432YCHT	DSBGA	YCH	25	250	345.0	365.0	55.0

AFE4432

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10.3 Mechanical Data

PACKAGE OUTLINE
YCH0025-C01 **DSBGA - 0.365 mm max height**
DIE SIZE BALL GRID ARRAY



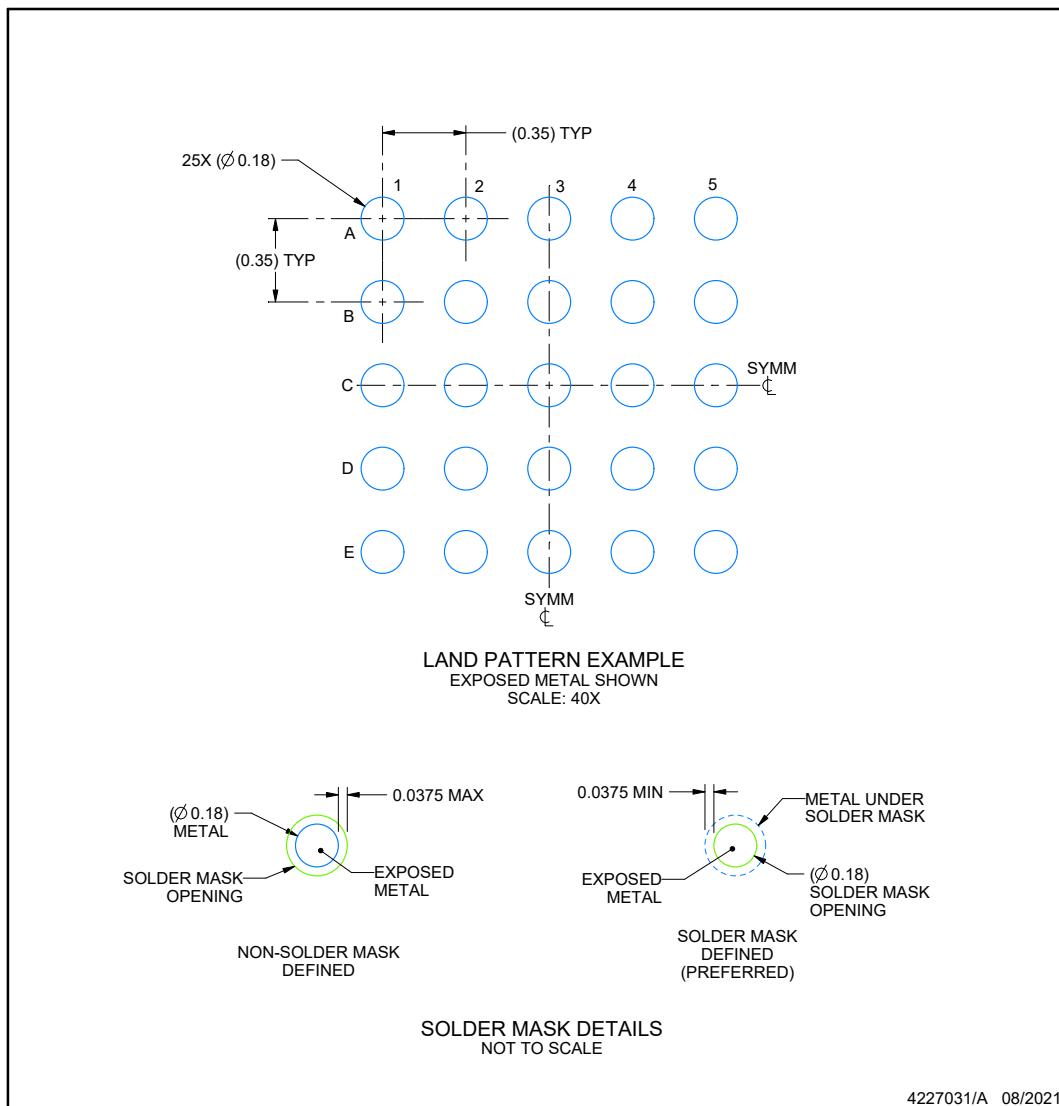
4227031/A 08/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT**YCH0025-C01****DSBGA - 0.365 mm max height**

DIE SIZE BALL GRID ARRAY

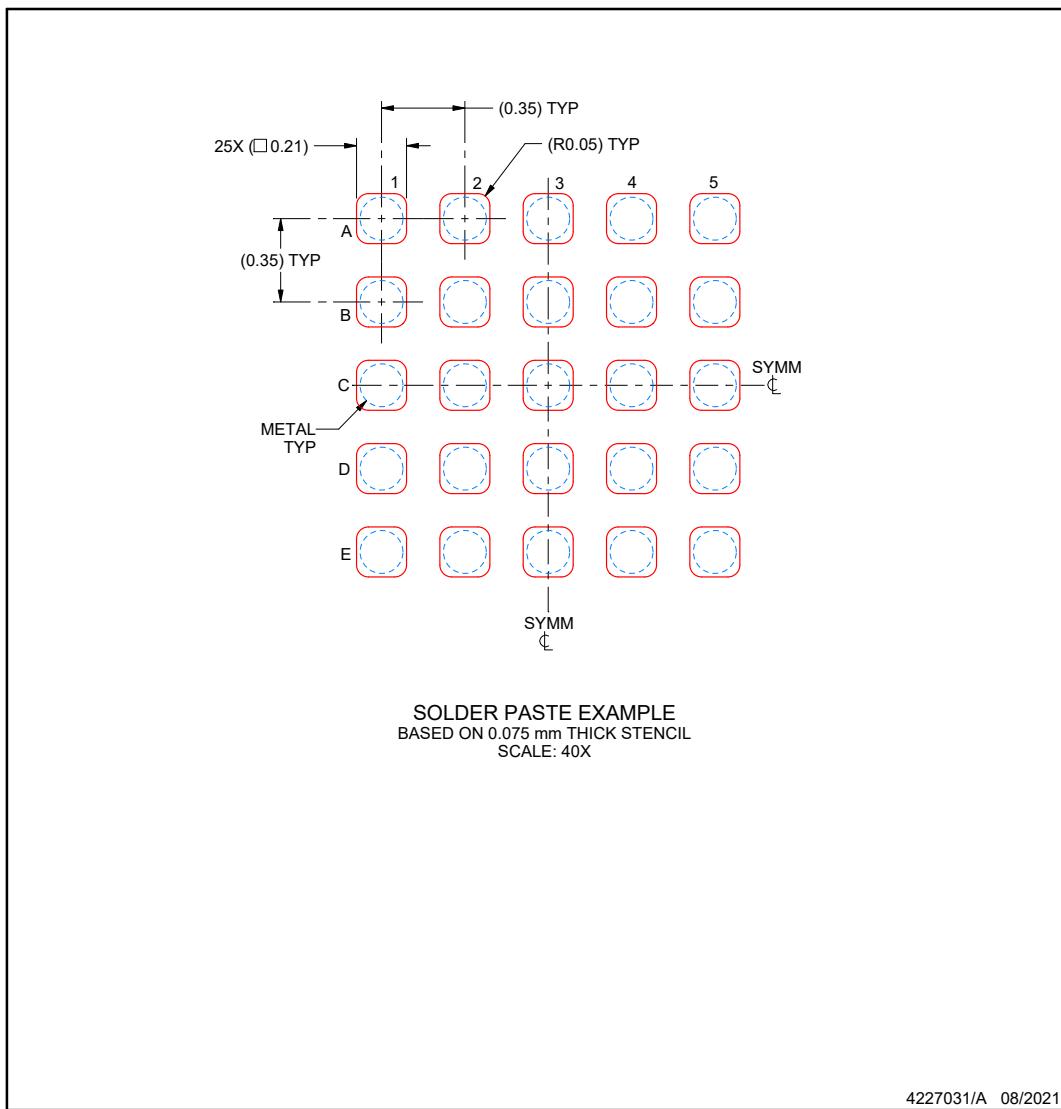


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN**YCH0025-C01****DSBGA - 0.365 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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