Computer-Aided VLSI System Design
Lab6: Innovus Lab (1/2)

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Data Preparation

1. Extract data from the folder **Lab6**.
2. The extracted directory contains
   - **design_data**
     A. CHIP.v
     B. CHIP.ioc
     C. CHIP.sdc
     D. CHIP_scan.sdc
   - **celtic**
     A. fast.cdB
     B. slow.cdB
   - **tsmc13_8lm.cl**
     A. icecaps_8lm.tch
   - **gds**
     A. tsmc13gfsg_fram.gds
     B. tpz013g3_v2.0.gds
   - **lef**
     A. tsmc13fsg_8lm_cic.lef
     B. tpz013g3_8lm_cic.lef
     C. RF2SH64x16.vclef
     D. antenna_8.lef
   - **lib**
     A. slow.lib
     B. fast.lib
     C. tpz013g3wc.lib
     D. tpz013g3lt.lib
     E. RF2SH64x16_slow_syn.lib
     F. RF2SH64x16_fast@0C_syn.lib
   - streamOut.map
   - tsmc013.capTbl
   - mmmc.view
   - addIoFiller_tpz.cmd

Introduction

In this lab, you will learn how to use Innovus to run the APR flow, and generate the required data for demonstration.

Data Preparation (Library)

1. Copy libraries to the folder **Lab6**. and **unzip Lab6.tar**

```
cd Lab6
cp -R /home/raid7_4/raid1_1/PnR/SOCE_Lab/library .
```

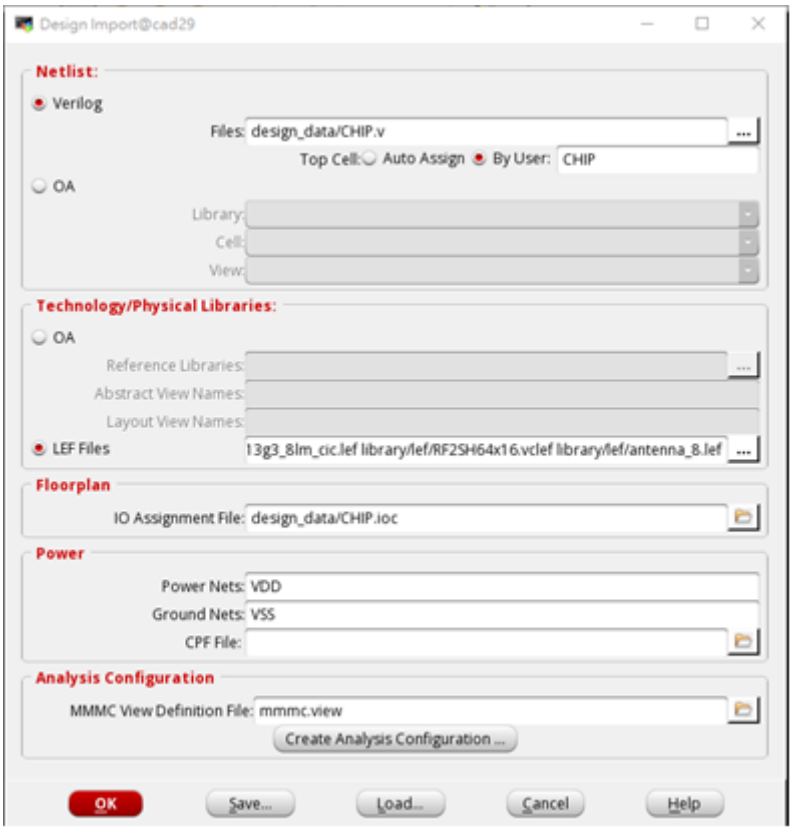
2. Start Innovus: (change the directory to **Lab6**)

```
innovus
```

3. Remember do not use background execution
4. Fail to open Innovus:

```
source /usr/cad/innovus/CIC/license.cshrc
source /usr/cad/innovus/CIC/innovus.cshrc
```

5. Design Import
   - 5.1 ***File → Import Design…***
   - 5.2 Verilog
     - Files: **design_data/CHIP.v**
     - Top Cell: ◆ By User: **CHIP**
   - 5.3 Technology/Physical Libraries
     - LEF Files: **library/lef/tsmc13fsg_8lm_cic.lef (must be in first order)**
       library/lef/tpz013g3_8lm_cic.lef
       library/lef/RF2SH64x16.vclef
       library/lef/antenna_8.lef
   - 5.4 Floorplan
     - IO Assignment Files: **design_data/CHIP.ioc**
   - 5.5 Power
     - Power Nets: **VDD**
     - Ground Nets: **VSS**
   - 5.6 Multi-Mode-Multi-Corner
     - MMMC View Definition File: **mmmc.view**
   - 5.7 Save current settings:
     - Click Save… button
     - File name: **CHIP.conf**
     - Click OK button



Global Net Connect

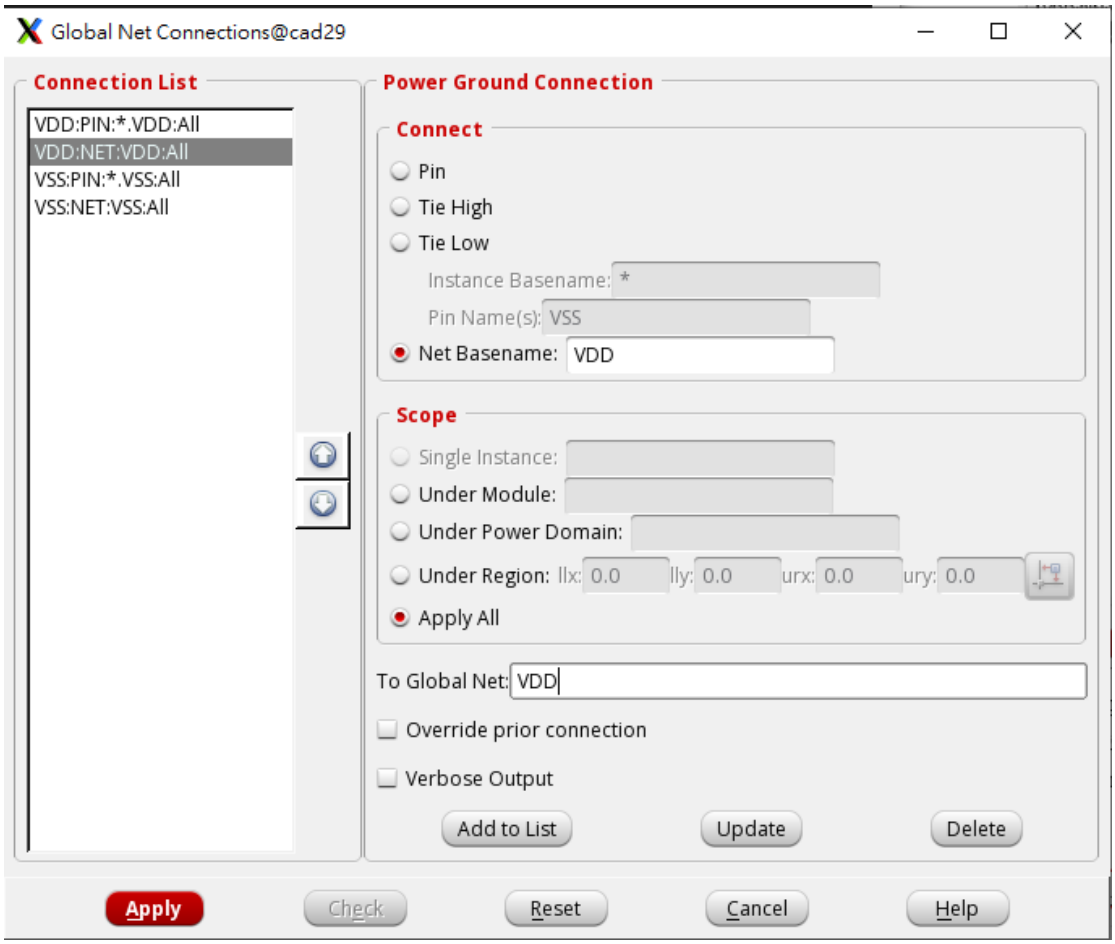
1. Open ***Power → Connect Global Nets…***
2. Add all VDD pins to Connection List:
   - Connect ◆ Pin ◆ Pin Name(s): **VDD**
   - Scope ◆ **Apply All**
   - To Global Nets: **VDD**
   - Click Add to List button
3. Add all VDD nets to Connection List:
   - Connect ◆ Net Basename: **VDD**
   - Scope ◆ **Apply All**
   - To Global Nets: **VDD**
   - Click Add to List button
4. Add all Tie High pins to Connection List:
   - Connect ◆ **Tie High**
   - Scope ◆ **Apply All**
   - To Global Nets: **VDD**
   - Click Add to List button

Skip step 4 and step 7 here. We will add tie high and tie low cells later.

5. Add all VSS pins to Connection List:
   - Connect ◆ Pin ◆ Pin Name(s): **VSS**

- Scope ◆ **Apply All**
- To Global Nets: **VSS**
- Click Add to List button

6. Add all VSS nets to Connection List:
   - Connect ◆ Net Basename: **VSS**
   - Scope ◆ **Apply All**
   - To Global Nets: **VSS**
   - Click Add to List button
7. Add all Tie Low pins to Connection List:
   - Connect ◆ **Tie Low**
   - Scope ◆ **Apply All**
   - To Global Nets: **VSS**
   - Click Add to List button



8. Apply the connection list and check:
   - Click Apply button
   - Click Check button
   - Click Cancel button

```
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_5_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_5_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_4_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_4_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_3_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_3_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_2_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_2_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_1_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_1_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_0_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S43/S5_reg_0_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/ST_MAL_i0/S17_reg is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/ST_MAL_i0/S17_reg is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/ST_MAL_i0/S16_reg is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/ST_MAL_i0/S16_reg is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/Finish_reg is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/Finish_reg is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/S20_reg_1_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/S20_reg_1_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/S20_reg_0_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/S20_reg_0_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_0_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_0_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_1_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_1_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_2_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_2_ is not connect to global special net.
Warning: term SN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_3_ is not connect to global special net.
Warning: term RN of inst DCT/tposemem/Bisted_RF2SH64x16/BistCtrl_i0/S44/State_reg_3_ is not connect to global special net.
```

9. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: **DBS/init**
   - Click OK button

```
Generated self-contained design init.dat
#% End save design ... (date=11/20 22:08:02, to
*** Message Summary: 0 warning(s), 0 error(s)
```

10. Restore file
    - Open ***File → Restore Design…***
    - Choose ◆ Innovus
    - Restore Design File: **DBS/init**
11. Set process node
    - innovus #> **setDesignMode -process 130**

Specifying Scan Chain

1. innovus # > **specifyScanChain scan1 -start ipad_SCAN_IN/C -stop opad_SCAN_OUT/I**
2. innovus # > **scanTrace**

```
*** Scan Trace Summary (runtime: cpu: 0:00:00.0 , real: 0:00:00.0):
Successfully traced 1 scan chain  (total 1574 scan bits).
*** Scan Sanity Check Summary:
*** 1 scan chain  passed sanity check.
```

Floorplan

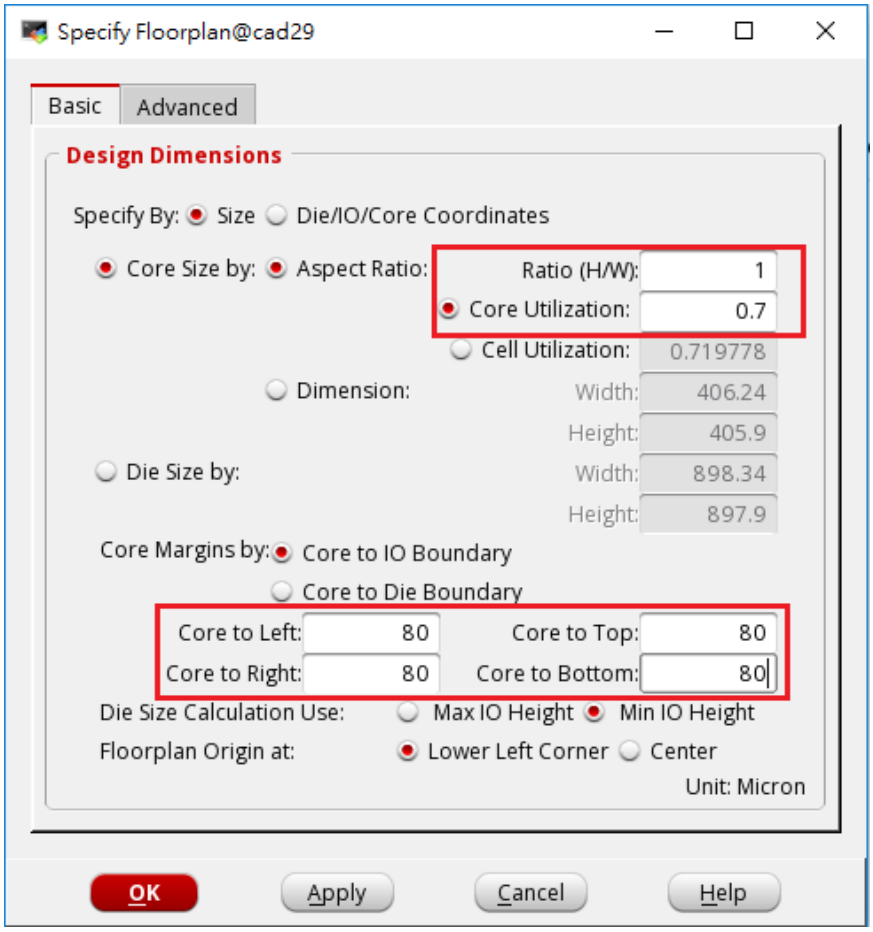
1. Open ***Floorplan → Specify Floorplan…***
2. Specify core size:
   - Ratio (H/W): 1
   - Core Utilization: 0.7
3. Specify core margin:
   - Core to IO Boundary

     Core to Left: **80**

     Core to Right: **80**

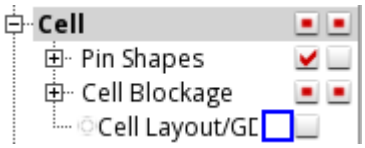
     Core to Top: **80**

     Core to Bottom: **80**
4. Click OK button



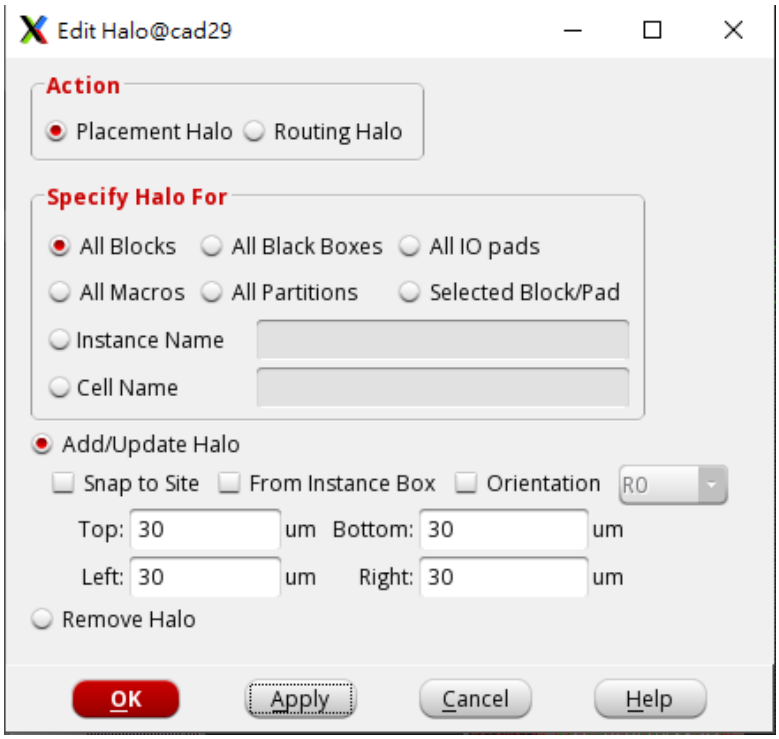
Plan Design

1. Change to **floorplan view** 
2. Open ***Floorplan → Automatic Floorplan → Plan Design…***
3. Click OK button
4. Set **Visible** to Cell/Pin Shapes in color control



Edit Halo

1. Open ***Floorplan → Edit Floorplan → Edit Halo…***
2. Choose ◆ **All Blocks**
3. Add/Update Halo
   - Top: **30 um**
   - Bottom: **30 um**
   - Left: **30 um**
   - Right: **30 um**
4. Click OK button
5. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: **DBS/floorplan**



Checkpoints

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Show your final results as follows. (Please make sure your screenshots can show your student ID with the server or you will not be graded)

a. To insert a scan chain and the placement process

```
No user-set net weight.
Net fanout histogram:
2               : 3855 (65.3%) nets
3               : 980 (16.6%) nets
4     - 14      : 976 (16.5%) nets
15    - 39      : 91 (1.5%) nets
40    - 79      : 3 (0.1%) nets
80    - 159     : 0 (0.0%) nets
160   - 319     : 0 (0.0%) nets
320   - 639     : 0 (0.0%) nets
640   - 1279    : 0 (0.0%) nets
1280  - 2559    : 2 (0.0%) nets
2560  - 5119    : 0 (0.0%) nets
5120+           : 0 (0.0%) nets
Options: timingDriven clkGateAware pinGuide congEffort=auto gpeffort=medium
#std cell=4408 (0 fixed + 4408 movable) #buf cell=193 #inv cell=485 #block=1 (1 floating + 0 preplaced)
#ioInst=44 #net=5907 #term=20654 #term/net=3.50, #fixedIo=44, #floatIo=0, #fixedPin=32, #floatPin=0
stdCell: 4408 single + 0 double + 0 multi
Total standard cell length = 27.2357 (mm), area = 0.1005 (mm^2)
Average module density = 0.759.
Density for the design = 0.759.
       = (stdcell_area 59208 sites (100500 um^2) + block_area 14576 sites (24742 um^2)) / alloc_area 97220 sites (165022 um^2).
Pin Density = 0.2124.
            = total # of pins 20654 / total area 97240.
Fence Initialization: numPrefixFence = 0,  numAutoFence = 0, numPrefixGuide = 0  numAutoGuide = 0 numNoCon = 0
=== lastAutoLevel = 8
Iteration  1: Total net bbox = 2.548e+04 (1.23e+04 1.32e+04)
              Est.  stn bbox = 3.059e+04 (1.42e+04 1.64e+04)
              cpu = 0:00:00.1 real = 0:00:00.0 mem = 1382.4M
User specified -module_cluster_mode =  0

Iteration  2: Total net bbox = 2.552e+04 (1.23e+04 1.32e+04)
              Est.  stn bbox = 3.074e+04 (1.42e+04 1.66e+04)
              cpu = 0:00:00.0 real = 0:00:00.0 mem = 1380.4M
Iteration  3: Total net bbox = 3.219e+04 (1.48e+04 1.74e+04)
              Est.  stn bbox = 3.773e+04 (1.68e+04 2.10e+04)
              cpu = 0:00:00.0 real = 0:00:00.0 mem = 1386.9M


Iteration  4: Total net bbox = 1.233e+05 (7.00e+04 5.33e+04)
              Est.  stn bbox = 1.370e+05 (7.70e+04 6.00e+04)
              cpu = 0:00:01.6 real = 0:00:01.0 mem = 1387.9M
```

b. To edit the halo blocks

```
Checking core/die box is on Grid.....
**WARN: (IMPFP-7236):   DIE's corner: (1058.8200000000 , 1058.6200000000) is NOT on PlacementGrid,  Please use command getFPlanMode to check
 current Grid settings, use command setFPlanMode to change which grid to snap to. And use command get_snap_grid_info to get grids' offset an
d pitch. Command floorplan can be used to fix this issue.
Checking snap rule ......
Checking Row is on grid......
Checking AreaIO row.....
Checking row out of die ...
Checking routing blockage.....
Checking components.....
**WARN: (IMPFP-10013):  Halo should be created around block DCT/tposemem/Bisted_RF2SH64x16/RF2SH64x16_u0/SRAM_i0 and snapping rules are not
checked since it's width is not multiple of default tech site's width.
**WARN: (IMPFP-10013):  Halo should be created around block DCT/tposemem/Bisted_RF2SH64x16/RF2SH64x16_u0/SRAM_i0 and snapping rules are not
checked since it's height is not multiple of default tech site's height.
Checking IO Pads out of die...
Checking constraints (guide/region/fence).....
Checking groups.....

Checking Preroutes.....
No. of regular pre-routes not on tracks : 0

Reporting Utilizations.....

Core utilization  = 70.027118
Effective Utilizations
Average module density = 0.759.
Density for the design = 0.759.
       = (stdcell_area 59208 sites (100500 um^2) + block_area 14576 sites (24742 um^2)) / alloc_area 97240 sites (165055 um^2).
Pin Density = 0.2124.
            = total # of pins 20654 / total area 97240.

*** Summary of all messages that are not suppressed in this session:
Severity  ID               Count  Summary
WARNING   IMPFP-7236           1  DIE's corner: %s is NOT on %s,  Please u...
WARNING   IMPFP-10013          2  Halo should be created around block %s a...
*** Message Summary: 3 warning(s), 0 error(s)
```

Submission

1. **Due Tuesday, Dec. 14, 19:00**

2. Put the snapshots mentioned in the previous section in a .tar and name the .tar with the format: **studentID_lab6_v*k***
   Note1: Use **lower case** for the letter in your student ID. (Ex. d06943027_lab6_v1)
   Note2: TA will only check the last version of your result.

3. Submit to FTP
   - IP: 140.112.175.68
   - Port: 21
   - Account: 1101cvsd_student
   - Password: ilovecvsd

Appendix 1: Multi-Mode-Multi-Corner

1. Open ***File → Import Design…***
2. Press Create Analysis Configuration …
3. Click Library Sets and include the max and min delay library:
   - Max delay
     Name: **lib_max**
     (containing the worst-cast conditions for setup-time analysis)
     Timing Library:
     slow.lib, tpz013g3wc.lib, RF2SH64x16_slow_syn.lib
     SI Library: **slow.cdB**
   - Min delay
     Name: **lib_min**
     (containing the best-cast conditions for hold-time analysis)
     Timing Library:
     fast.lib, tpz013g3lt.lib, RF2SH64x16_fast@0C_syn.lib
     SI Library: **fast.cdB**
4. Click RC Corners to include the RC corner library:
   - Name: **RC_corner**
   - Cap Table: **tsmc013.capTbl**
   - QRC Technology File: **icecaps_8lm.tch**
5. Click Delay Corners and create max and min delay constraints:
   - Max delay
     Name: **Delay_Corner_max**
     RC Corner: **RC_Corner**
     Library Set: **lib_max**
   - Min delay
     Name: **Delay_Corner_min**
     RC Corner: **RC_Corner**
     Library Set: **lib_min**
6. Click Constraints Mode and create a function mode/scan mode:
   - Function mode
     Name: **func_mode**
     SDC Constraint Files: **CHIP.sdc**
   - Scan mode
     Name: **scan_mode**
     SDC Constraint Files: **CHIP_scan_ideal.sdc**
7. Click Analysis Views to create max and min delay analysis
   - Max delay (function mode)

Name: **av_func_mode_max**

Constraint Mode: **func_mode**

Delay Corner: **Delay_Corner_max**

- Min delay (function mode)

  Name: **av_func_mode_min**

  Constraint Mode: **func_mode**

  Delay Corner: **Delay_Corner_min**

- Max delay (scan mode)

  Name: **av_scan_mode_max**

  Constraint Mode: **scan_mode**

  Delay Corner: **Delay_Corner_max**

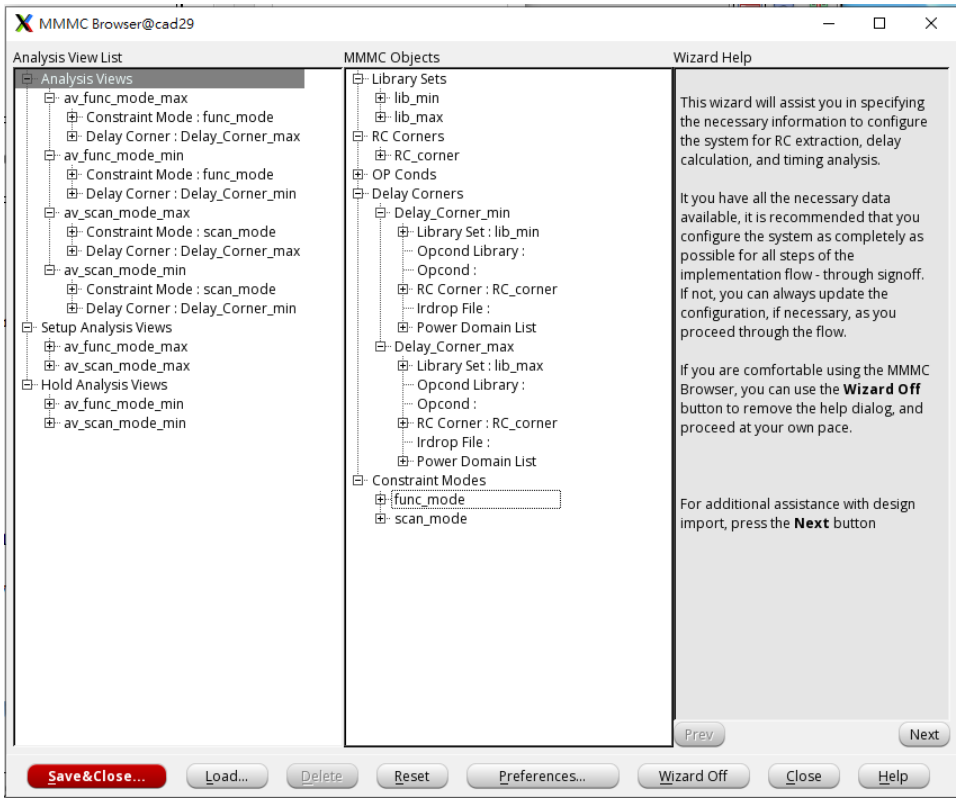
- Min delay (scan mode)

  Name: **av_scan_mode_min**

  Constraint Mode: **scan_mode**

  Delay Corner: **Delay_Corner_min**

8. Click Setup Analysis View and specify the max analysis mode
   - Choose: **av_func_mode_max**, **av_scan_mode_max**
9. Click Hold Analysis View and specify the min analysis mode
   - Choose: **av_func_mode_min**, **av_scan_mode_min**
10. Save as "**mmmc.view**"



Appendix 2: Generate CHIP.ioc

Do after Import Design

1. Open ***File → Save → I/O File…***
   - Save IO ◆ sequence
   - To File: **CHIP.ioc**
   - ◆ Generate template IO File
   - Click OK button
2. Open ***File → Load → I/O File…***
   - Choose **CHIP.ioc**
   - Click Open button