Computer-Aided VLSI System Design
Lab7: Innovus Lab (2/2)

TA：謝伊妍 D06943001@ntu.edu.tw

Data Preparation

1. Extract data from the folder **Lab6**.
2. The extracted directory contains
   - **design_data**
     A. CHIP.v
     B. CHIP.ioc
     C. CHIP.sdc
     D. CHIP_scan.sdc
   - **celtic**
     A. fast.cdB
     B. slow.cdB
   - **tsmc13_8lm.cl**
     A. icecaps_8lm.tch
   - **gds**
     A. tsmc13gfsg_fram.gds
     B. tpz013g3_v2.0.gds
   - **lef**
     A. tsmc13fsg_8lm_cic.lef
     B. tpz013g3_8lm_cic.lef
     C. RF2SH64x16.vclef
     D. antenna_8.lef
   - **lib**
     A. slow.lib
     B. fast.lib
     C. tpz013g3wc.lib
     D. tpz013g3lt.lib
     E. RF2SH64x16_slow_syn.lib
     F. RF2SH64x16_fast@0C_syn.lib
   - streamOut.map
   - tsmc013.capTbl
   - mmmc.view
   - addIoFiller_tpz.cmd

Introduction

In this lab, you will learn how to use Innovus to run the APR flow, and generate the required data for demonstration.

Power Planning

1. Start Innovus (remember do not use background execution)

```
innovus
```

If fail to open Innovus:

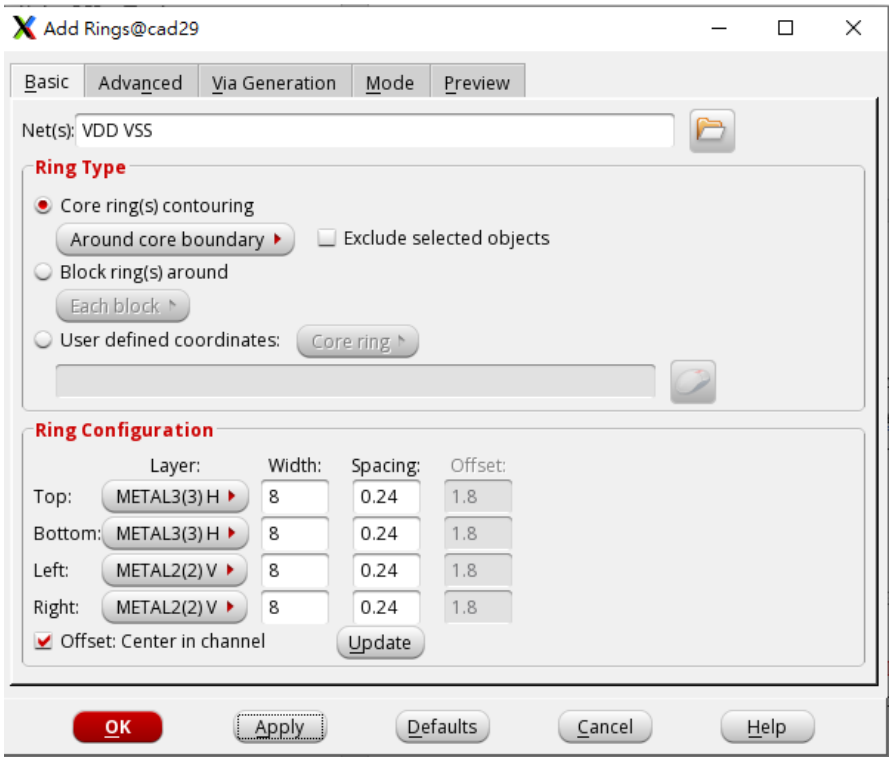
```
source /usr/cad/innovus/CIC/license.cshrc
source /usr/cad/innovus/CIC/innovus.cshrc
```

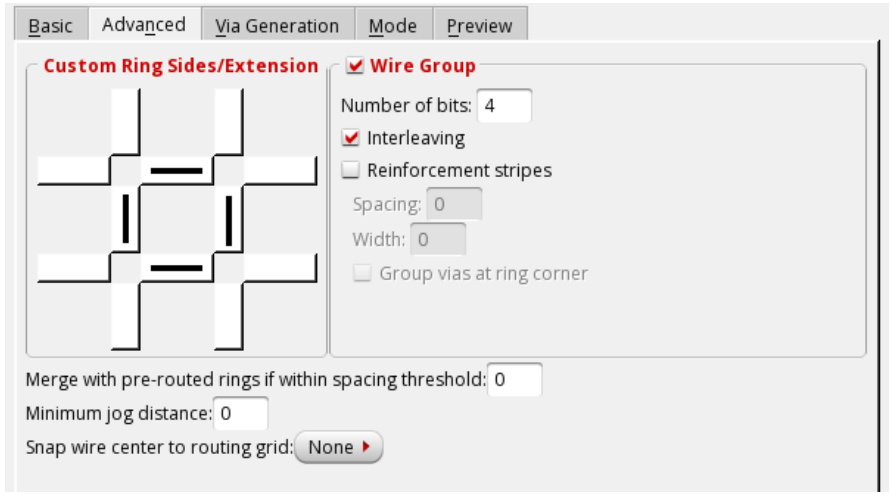
Restore file

- Open ***File → Restore Design…***
- Choose ◆ Innovus

2. Restore Design File: **DBS/floorplan**
3. Add Power Rings
   1.1 Open ***Power → Power Planning → Add Ring…***
   1.2 In the Basic tab:
      1.2.1 Fill in Net(s) names: **VDD VSS**
      1.2.2 Specify metal layers and width
         - Top Layer: **METAL3 H** Width: **8**
         - Bottom Layer: **METAL3 H** Width: **8**
         - Left Layer: **METAL2 V** Width: **8**
         - Right Layer: **METAL2 V** Width: **8**
      1.2.3 Click Update button
      1.2.4 Choose ◆ **Offset: Center in channel**
   1.3 In the Advanced tab:
      1.3.1 Configure wire group
         - ◆ Use wire group
         - Number of bits: **4**
         - ◆ Interleaving
   1.4 Apply the specification:
      1.4.1 Click Apply button
      1.4.2 Click Cancel button

Check if the ring is correctly created. If not, click **undo** button (in Innovus toolbar) and repeat step 1.2~1.4 again.





4. Connect Core Power Pin

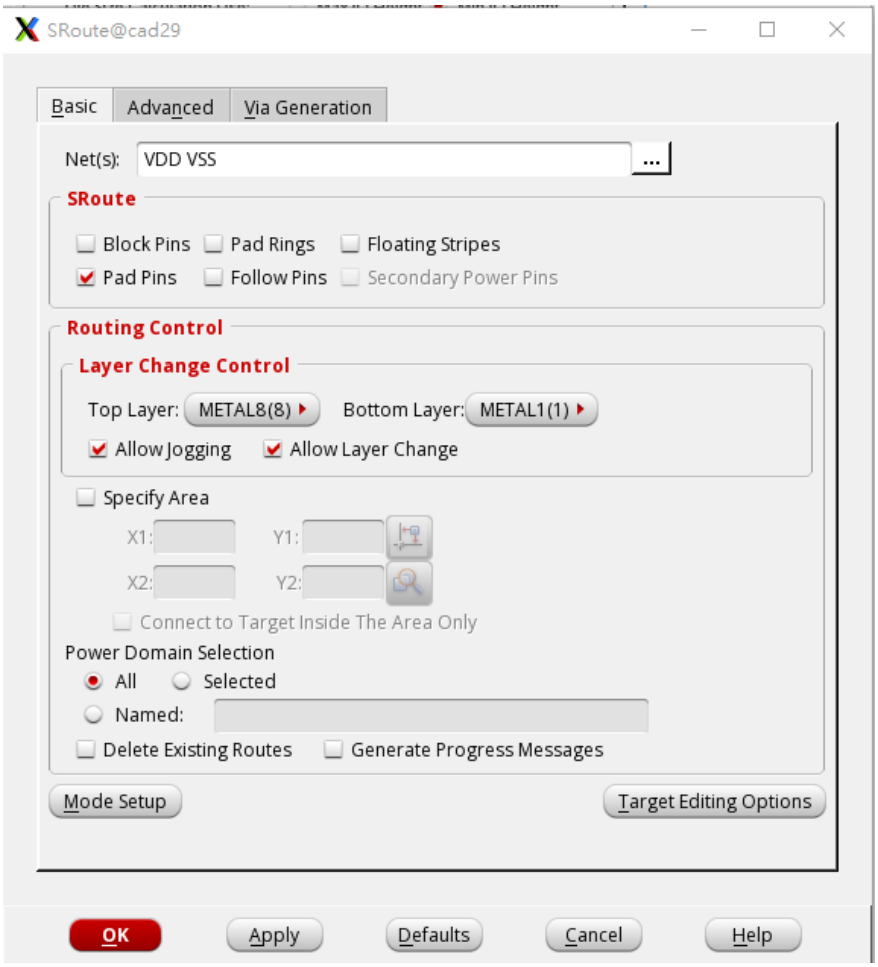
   2.1 Open ***Route → Special Route…***

   2.2 Fill in Net(s): **VDD VSS**

   2.3 Set the following configuration

   - ◦ Block pins
   - ◆ Pad pins
   - ◦ Pad rings
   - ◦ Follow pins

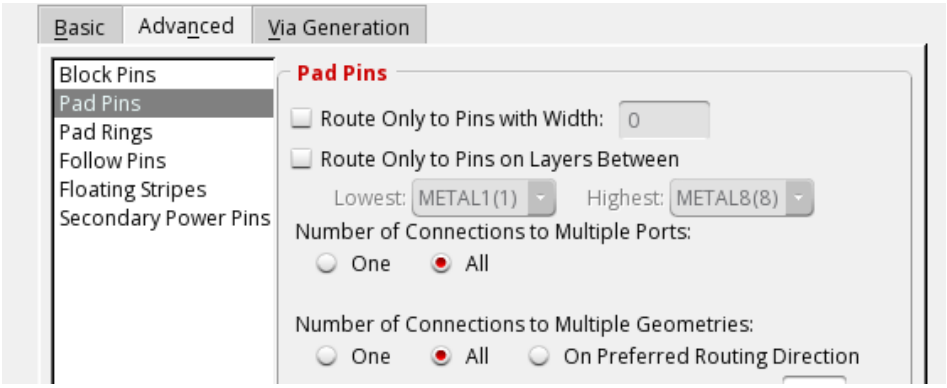
Ignore errors of core power pad here.



2.4 In the Advanced page:

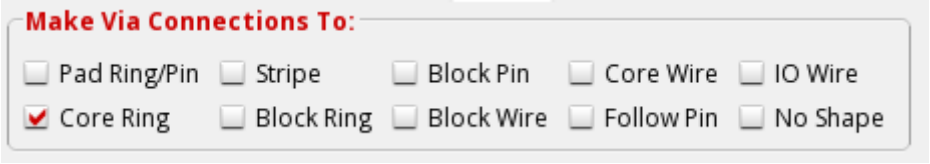
2.4.1 Select **Pad Pins**

2.4.2 Number of Connections to Multiple Geometries: ◆ All



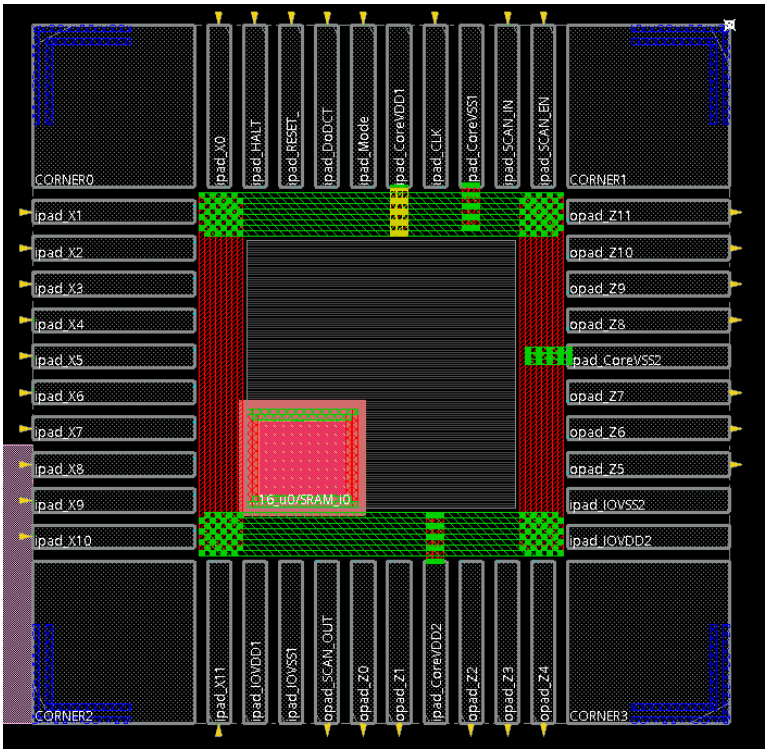
2.5 In the Via Generation page:

➢ Make Via Connections To: ◆ Core Ring



2.6 Click OK button

5. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: **DBS/powerring**



6. Add Stripes

   4.1 Open ***Power → Power Planning → Add Stripes…***

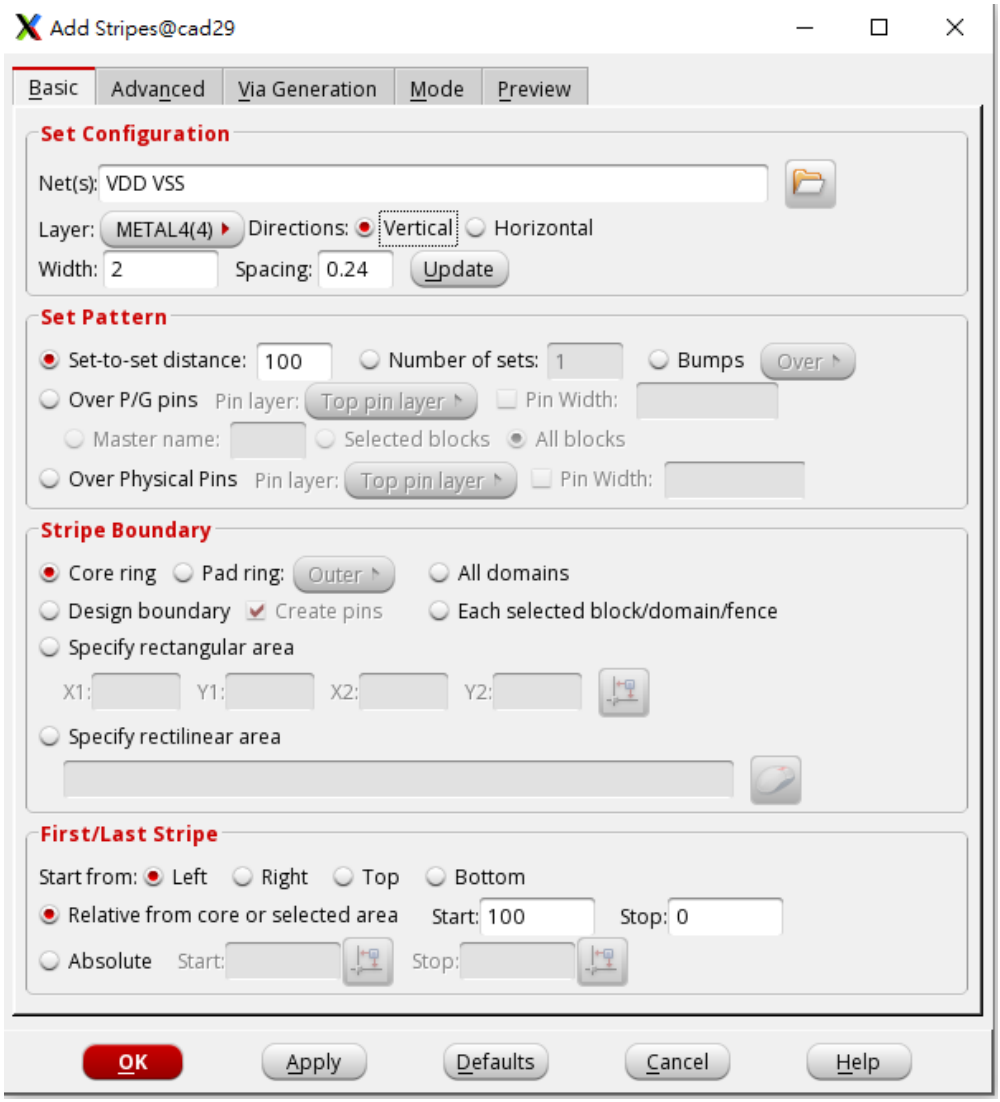
   4.2 Create vertical power stripes:

   4.2.1 Specify metal layer, width, direction and spacing
   - Net(s): **VDD VSS**
   - Layer: **METAL4**
   - Directions: **Vertical**
   - Width: **2**
   - Click Update Button

   4.2.2 Specify set-to-set distance
   - Set-to-set distance: **100**

   4.2.3 Specify locations by Relative from core or selected area
   - Start from: ◆ **Left**
   - Relative from core or selected area Start: **100** Stop: **0**

   4.2.4 Click Apply button



4.3 Create horizontal power stripes:

4.3.1 Specify metal layer, width, direction and spacing

- Net(s): **VDD VSS**
- Layer: **METAL5**
- Directions: **Horizontal**
- Width: **4**
- Click Update Button

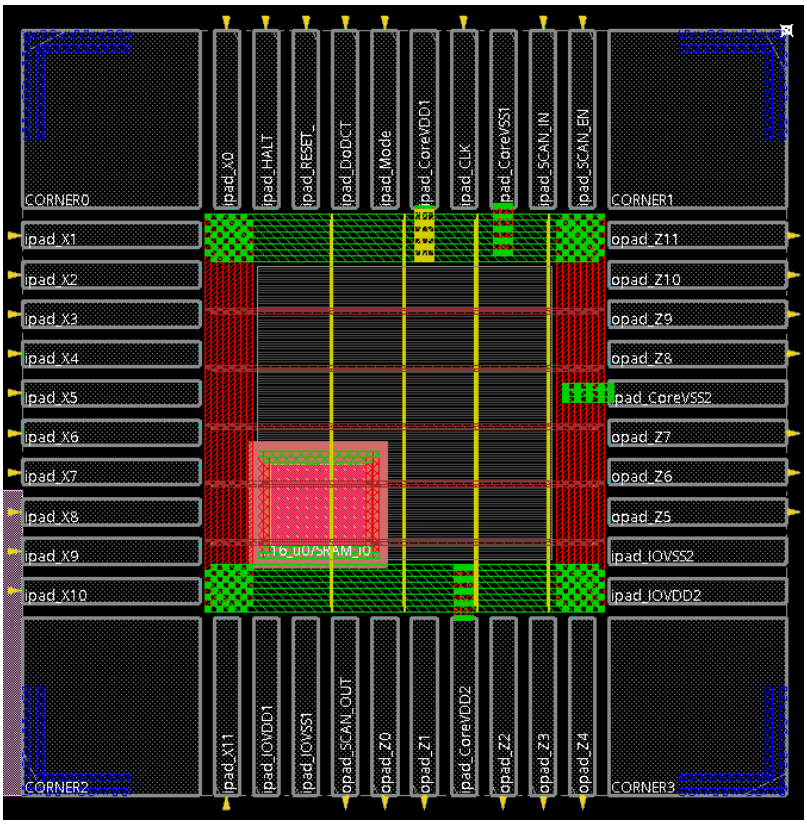
4.3.2 Specify set-to-set distance

- Set-to-set distance: **80**

4.3.3 Specify locations by Relative from core or selected area

- Start from: ◆ **Bottom**
- Relative from core or selected area Start: **20** Stop: **0**

4.3.4 Click Apply button



7. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: **DBS/powerstripe**
8. Connect Standard Cell Power Line

   6.1 Open ***Route → Special Route…***

   6.2 Fill in Net(s): **VDD VSS**

   6.3 Set the following configuration
   - ◦ Block pins
   - ◦ Pad pins
   - ◦ Pad rings
   - ◆ Follow pins

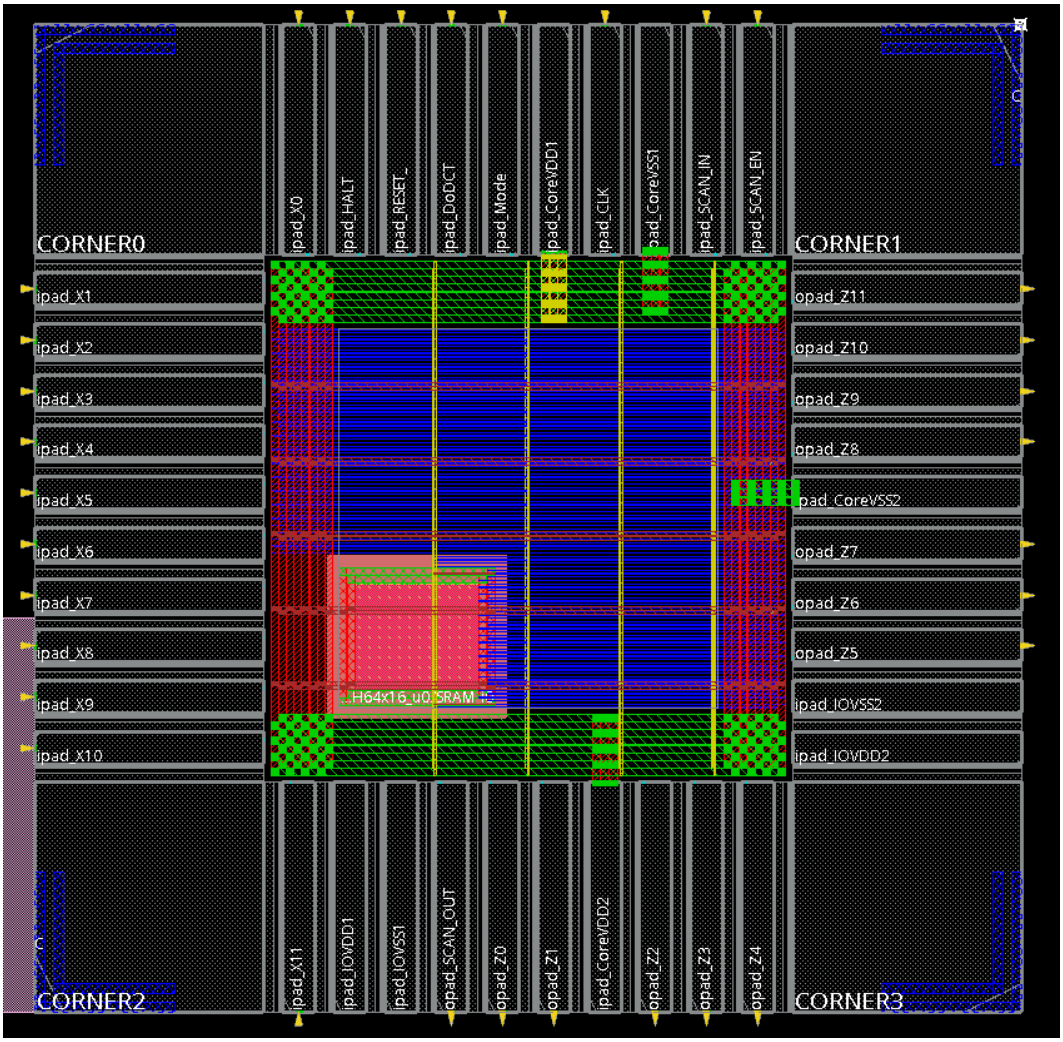
6.4 In the Via Generation page:

- Make Via Connections To: ◆ Core Ring ◆ Stripe ◆ Block Ring

6.5 Click OK button

Add IO Filler

1. innovus # > **source library/addIoFiller_tpz.cmd**



Verify Geometry & Connectivity

1. Verify geometry
   1.1 innovus # > **verify_drc**

```
Verification Complete : 0 Viols.
```

2. Verify connectivity
   2.1 Open ***Verify → Verify Connectivity …***
   2.2 Net Type ◆ **Special Only**
   2.3 Nets ◆ Named: **VDD VSS**
   2.4 Click OK button

```
Begin Summary
  Found no problems or warnings.
End Summary
```

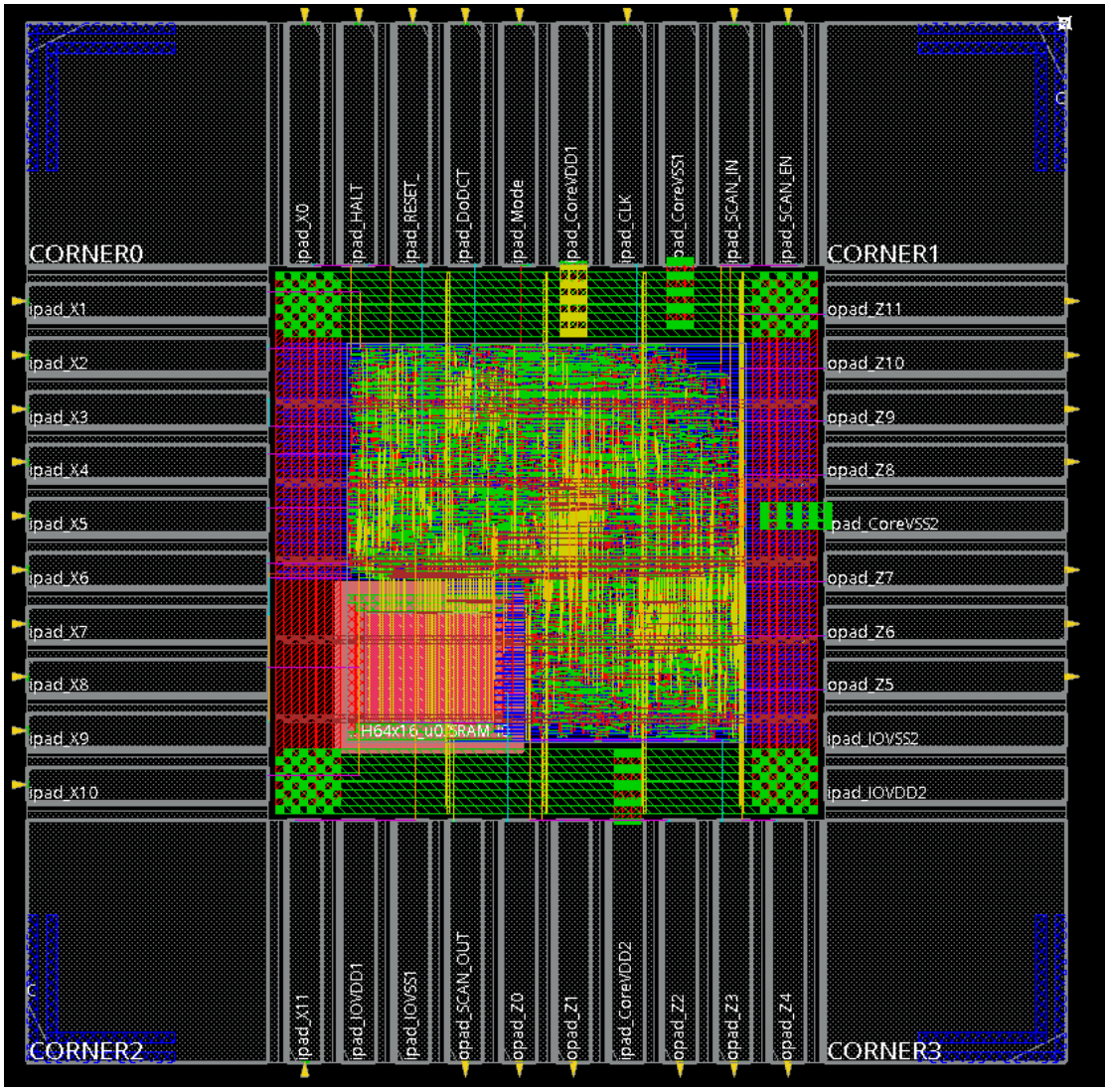
3. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/powerplan

If there are dangling wires, use hot key T (shift + t) to fix it.

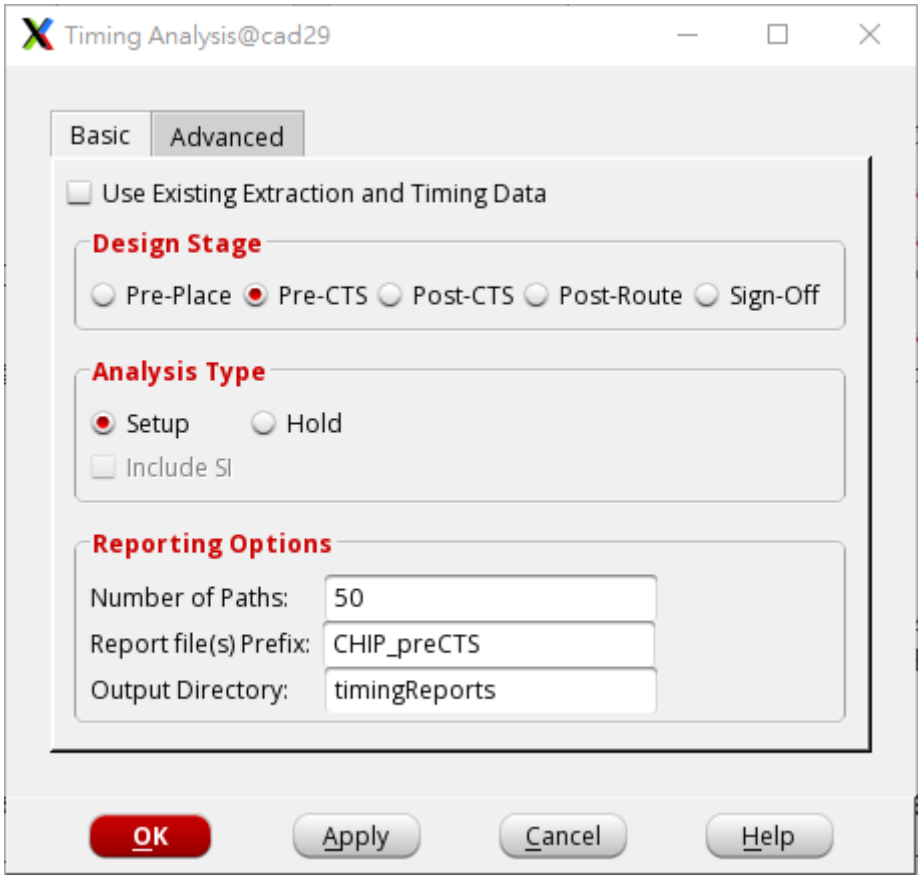
Placement

1. innovus # > **createBasicPathGroups -expanded**
2. innovus # > **get_path_groups**
3. innovus # > **place_opt_design**

Change to **Physical view**  to check if the cells are placed correctly.



4. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/place
5. In-Place Optimization – Before Clock Tree Synthesis
   5.1 Open ***Timing → Report Timing…***
   5.2 Perform First Encounter trial route to model the interconnection RC effects
   - Design Stage ◆ pre-CTS
   - Analysis Type ◆ Setup
   - Click OK button




```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.010  |  0.010  |  3.446  |  0.218  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |    109 (109)     |    -55     |    110 (110)     |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+
```

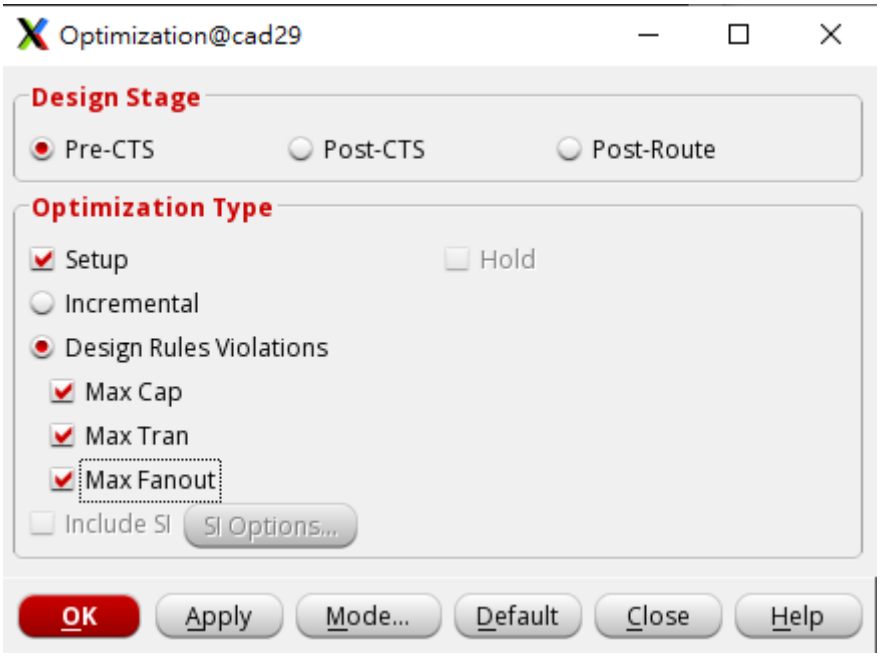
5.3 If the timing slack is negative, or there are DRVs, open ***ECO → Optimize Design…***

5.4 Perform pre-CTS IPO

- Design Stage ◆ pre-CTS
- Optimization Type

- Setup
- Design Rule Violations
- Max Cap
- Max Tran
- Max Fanout

➢ Click OK button




```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.005  |  0.005  |  3.491  |  0.235  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-----------------------------------+------------------+
|                |              Real                 |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  |  Worst Vio     |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |   0.000        |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000        |      0 (0)       |
|   max_fanout   |      0 (0)       |     0          |      1 (1)       |
|   max_length   |      0 (0)       |     0          |      0 (0)       |
+----------------+------------------+----------------+------------------+
```

6. Save file
   - ➢ Open ***File → Save Design…***
   - ➢ Choose ◆ Innovus
   - ➢ File Name: DBS/place

Clock Tree Synthesis (CTS)

1. Create new sdc files for CTS (not execute in innovus)

   1.1 Copy **CHIP.sdc** and **CHIP_scan_ideal.sdc** (in the **design_data** directory)

   - % **cp CHIP.sdc CHIP_cts.sdc**
   - % **cp CHIP_scan_ideal.sdc CHIP_scan_cts.sdc**

   1.2 Remove **set_clock_latency** & **set_clock_uncertainty** that estimated clock network delay

   1.3 Remove **set_ideal_network**

```
set sdc_version 1.2
current_design CHIP
create_clock [get_ports {CLK}] -name CLK1 -period 10 -waveform {0 5}
set_case_analysis 0 [get_ports {SCAN_EN}]
set_max_fanout 15 [current_design]
set_max_transition 2.7 [current_design]

#set_clock_latency 2 [get_clocks {CLK1}]

set_input_delay     1 -clock CLK1 \
                    [remove_from_collection [all_inputs] [get_ports CLK]]
set_output_delay    1 -clock CLK1 [all_outputs]

set_drive 0.1 [all_inputs]
set_load -pin_load 1 [all_outputs]

set_false_path  -from [get_ports {DoDCT}]
set_false_path  -from [get_ports {RESET_}]
set_false_path  -from [get_ports {Mode}]
```

2. Update sdc file

   4.1 innovus #> **update_constraint_mode -name func_mode -sdc_files design_data/CHIP_cts.sdc**

   4.2 innovus #> **update_constraint_mode -name scan_mode -sdc_files design_data/CHIP_scan_cts.sdc**

```
innovus 5> update_constraint_mode -name func_mode -sdc_files design_data/CHIP_cts.sdc
Reading timing constraints file 'design_data/CHIP_cts.sdc' ...
Current (total cpu=0:04:37, real=0:11:11, peak res=1219.4M, current mem=1094.8M)
CHIP
INFO (CTE): Constraints read successfully.
Ending "Constraint file reading stats" (total cpu=0:00:00.1, real=0:00:00.0, peak res=1108.1M, current mem=1108.1M)
Current (total cpu=0:04:37, real=0:11:11, peak res=1219.4M, current mem=1108.1M)
Reading timing constraints file '/tmp/innovus_temp_67022_cad29_d06001_EYR89c/.mmmcTJXlR7/modes/scan_mode/scan_mode.sdc' ...
Current (total cpu=0:04:37, real=0:11:11, peak res=1219.4M, current mem=1108.1M)
CHIP
INFO (CTE): Constraints read successfully.
Ending "Constraint file reading stats" (total cpu=0:00:00.0, real=0:00:00.0, peak res=1108.4M, current mem=1108.4M)
Current (total cpu=0:04:37, real=0:11:11, peak res=1219.4M, current mem=1108.4M)
Reading latency file '/tmp/innovus_temp_67022_cad29_d06001_EYR89c/.mmmcTJXlR7/views/av_scan_mode_max/latency.sdc' ...
Reading latency file '/tmp/innovus_temp_67022_cad29_d06001_EYR89c/.mmmcTJXlR7/views/av_scan_mode_min/latency.sdc' ...
Current (total cpu=0:04:37, real=0:11:11, peak res=1219.4M, current mem=1108.4M)
Ending "Constraint file reading stats" (total cpu=0:00:00.1, real=0:00:00.0, peak res=1112.6M, current mem=1112.6M)
Current (total cpu=0:04:37, real=0:11:11, peak res=1219.4M, current mem=1112.6M)
innovus 6> update_constraint_mode -name scan_mode -sdc_files design_data/CHIP_scan_cts.sdc
Reading timing constraints file '/tmp/innovus_temp_67022_cad29_d06001_EYR89c/.mmmcTIyqDH/modes/func_mode/func_mode.sdc' ...
Current (total cpu=0:04:38, real=0:11:21, peak res=1219.4M, current mem=1096.5M)
CHIP
INFO (CTE): Constraints read successfully.
Ending "Constraint file reading stats" (total cpu=0:00:00.1, real=0:00:00.0, peak res=1109.2M, current mem=1109.2M)
Current (total cpu=0:04:38, real=0:11:21, peak res=1219.4M, current mem=1109.2M)
Reading timing constraints file 'design_data/CHIP_scan_cts.sdc' ...
Current (total cpu=0:04:38, real=0:11:21, peak res=1219.4M, current mem=1109.2M)
CHIP
INFO (CTE): Constraints read successfully.
Ending "Constraint file reading stats" (total cpu=0:00:00.0, real=0:00:00.0, peak res=1109.6M, current mem=1109.6M)
Current (total cpu=0:04:38, real=0:11:21, peak res=1219.4M, current mem=1109.6M)
Reading latency file '/tmp/innovus_temp_67022_cad29_d06001_EYR89c/.mmmcTIyqDH/views/av_func_mode_max/latency.sdc' ...
Reading latency file '/tmp/innovus_temp_67022_cad29_d06001_EYR89c/.mmmcTJXlR7/views/av_scan_mode_max/latency.sdc' ...
Reading latency file '/tmp/innovus_temp_67022_cad29_d06001_EYR89c/.mmmcTIyqDH/views/av_func_mode_min/latency.sdc' ...
Reading latency file '/tmp/innovus_temp_67022_cad29_d06001_EYR89c/.mmmcTJXlR7/views/av_scan_mode_min/latency.sdc' ...
Current (total cpu=0:04:39, real=0:11:21, peak res=1219.4M, current mem=1109.6M)
Ending "Constraint file reading stats" (total cpu=0:00:00.1, real=0:00:00.0, peak res=1113.8M, current mem=1113.8M)
Current (total cpu=0:04:39, real=0:11:21, peak res=1219.4M, current mem=1113.8M)
innovus 7>
```

3. Create spec file for CTS

   5.1 innovus #> **create_ccopt_clock_tree_spec -file ./ccopt.spec**

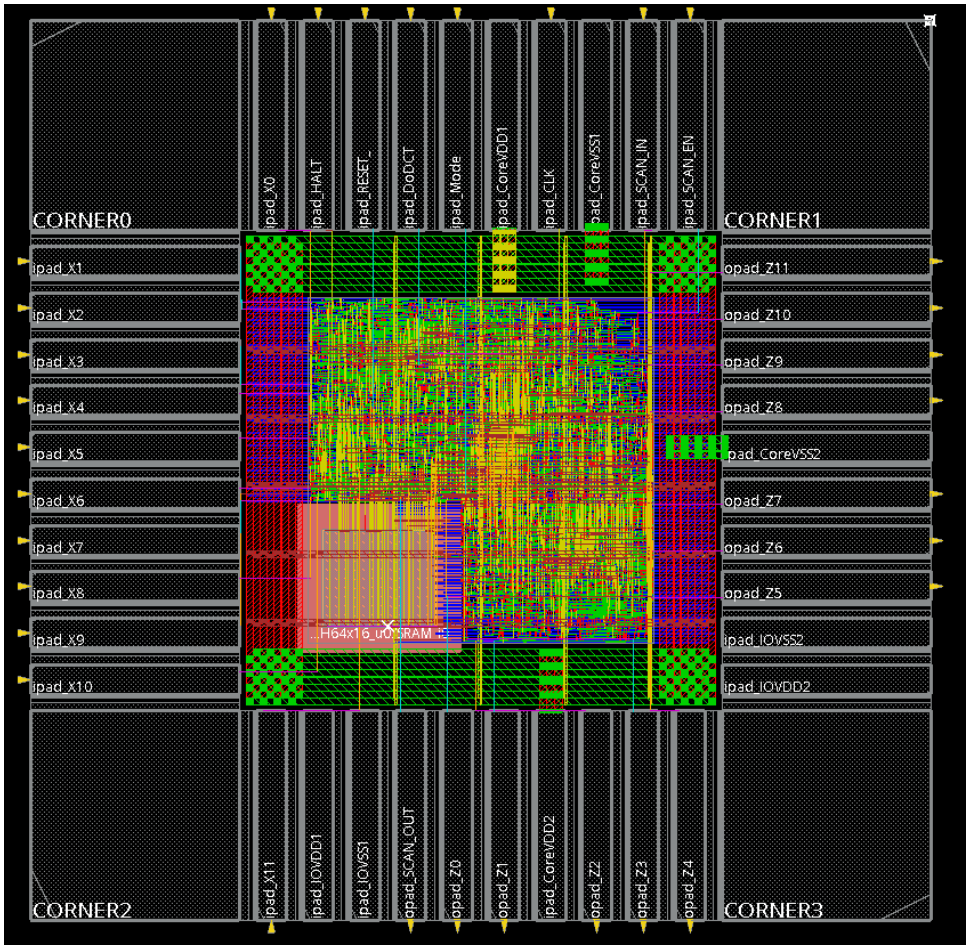
   5.2 Add **set_ccopt_property update_io_latency false** in ccopt.spec if io pads are added

   5.3 innovus #> **source ./ccopt.spec**

   5.4 innovus #> **ccopt_design -cts**

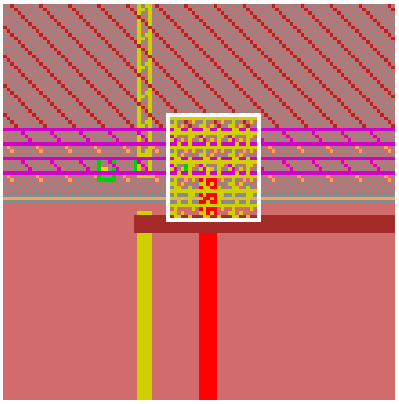
```
# Skew group to balance non generated clock:i_clk in timing_config:func_mod
create_ccopt_skew_group -name i_clk/func_mode -sources i_clk -auto_sinks
set_ccopt_property include_source_latency -skew_group i_clk/func_mode true
set_ccopt_property extracted_from_clock_name -skew_group i_clk/func_mode i_
set_ccopt_property extracted_from_constraint_mode_name -skew_group i_clk/fu
set_ccopt_property extracted_from_delay_corners -skew_group i_clk/func_mode

set_ccopt_property update_io_latency false
check_ccopt_clock_tree_convergence
# Restore the ILM status if possible
```

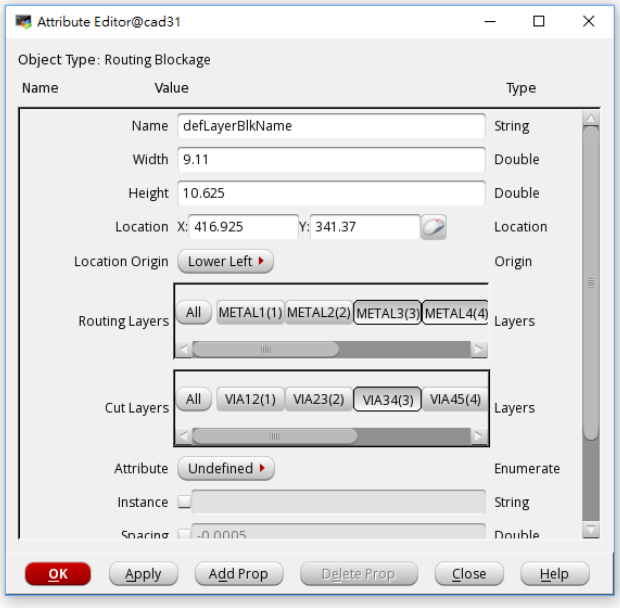
4. Find DRC error



4.1 Create Routing Blockage

- Block the place appear DRC violation
- Select the blockage and press q to set **Routing Layers** and **Cut Layers**

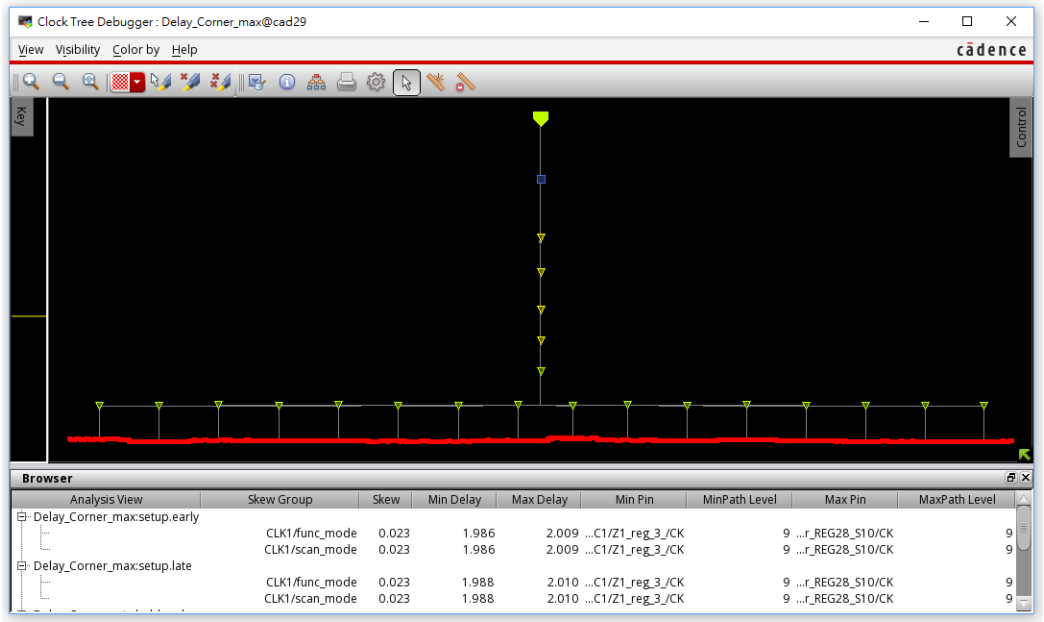




4.2 Create Routing Blockage with innovus #>

```
createRouteBlk -box 416.34550 338.51000 425.76600 351.46300
uiSetTool select
selectRouteBlk -box 416.345 338.51 425.765 351.465 defLayerBlkName -layer METAL3
setSelectedRouteBlk 416.345 338.51 425.765 351.465 defLayerBlkName {{3 } {4 } {V4 }}
{Undefined ALLNET} {} {}
ccopt_design -cts
```

5. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/cts
6. CCOpt clock tree debugger
   - Open ***Clock → CCopt Clock Tree Debugger…***
   - Click OK button



8. In-Place Optimization – After Clock Tree Synthesis

8.1 Open ***Timing → Report Timing…***

8.2 Perform First Encounter trial route to model the interconnection RC effects

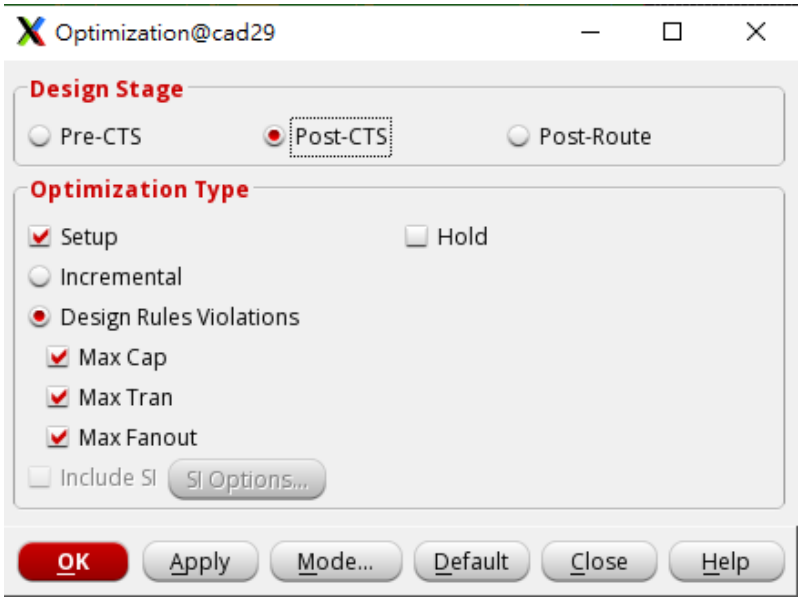
- Design Stage ◆ post-CTS
- Analysis Type ◆ Setup
- Click OK button

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):| -0.390  | -0.390  |  3.593  | -0.203  |   N/A   |  0.000  |
|           TNS (ns):| -2.297  | -2.093  |  0.000  | -0.203  |   N/A   |  0.000  |
|    Violating Paths:|   13    |   12    |    0    |    1    |   N/A   |    0    |
|         All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |     17 (17)      |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+
```

8.3 After CTS, further timing optimization is performed to meet timing constraints if there is negative timing slack or DRVs. Open ***ECO → Optimize Design…***

8.4 Perform post-CTS IPO

- Design Stage ◆ post-CTS
- Optimization Type
  - Setup
  - Design Rule Violations
  - Max Cap
  - Max Tran
  - Max Fanout
- Click OK button



```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.032  |  0.032  |  3.884  |  0.081  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |     17 (17)      |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+
```

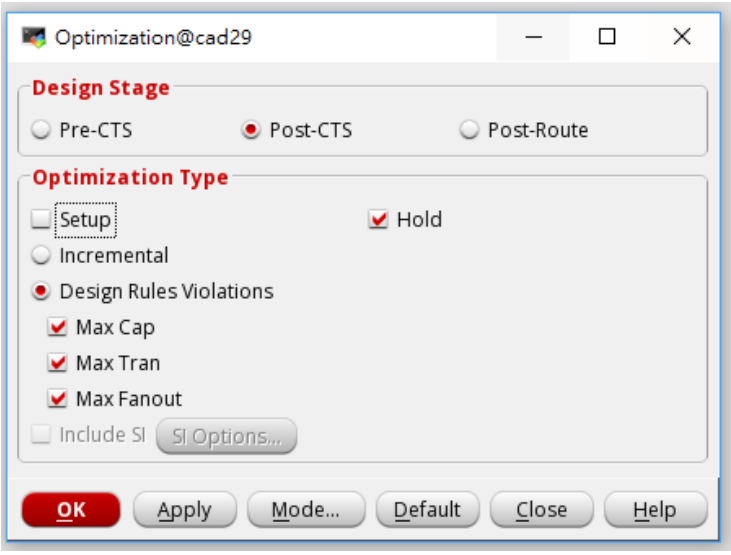
8.5 Verify if the hold time constraint is satisfied or not. Open ***Timing → Report Timing…***

- Design Stage ◆ post-CTS
- Analysis Type ◆ Hold
- Click OK button

8.6 If hold time slack is negative, open ***ECO → Optimize Design…***

8.7 Perform post-CTS IPO

- Design Stage ◆ post-CTS
- Optimization Type
  - **Hold**
  - Design Rule Violations
  - Max Cap
  - Max Tran
  - Max Fanout
- Click OK button

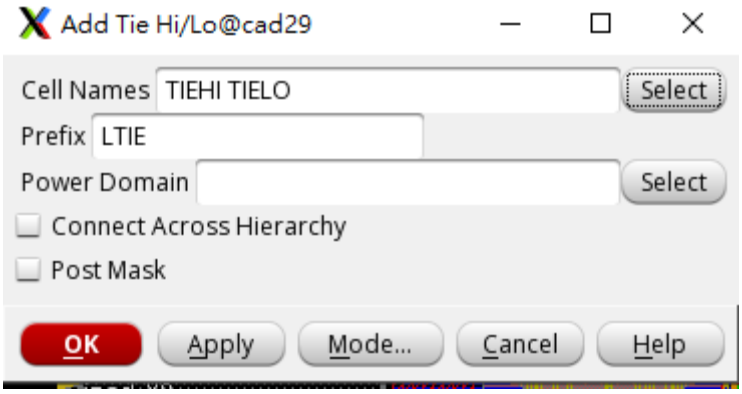


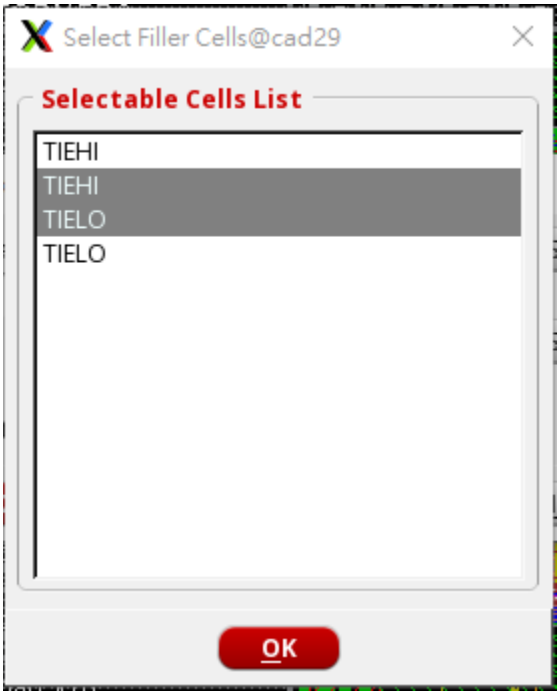
8.8 See timing reports in **timingReports** directory. For detail path report, see **CHIP_postCTS_reg2reg.tarpt.gz** (setup time check) and **CHIP_postCTS_reg2reg_hold.tarpt.gz** (hold time check).
DRV violations report files: ***.cap.gz** , ***.fanout.gz** , and ***.tran.gz**

9. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/cts

Add Tie Hi/Lo cell

1. Open ***Place → Tie HI/LO → Add…***
2. Click Select button next to Cell Names
3. Choose one **TIEHI** and one **TIELO**, click OK button
4. Click OK button





Routing

1. Open ***Route*** → ***NanoRoute*** → ***Route***
2. Nanoroute can prevent crosstalk effects and fix antenna rule violations, also it routes design to meet timing constraints

   2.1 Routing Phase

   - Add ◆ **Optimize Via** and ◆ **Optimize Wire**

   2.2 Concurrent routing features

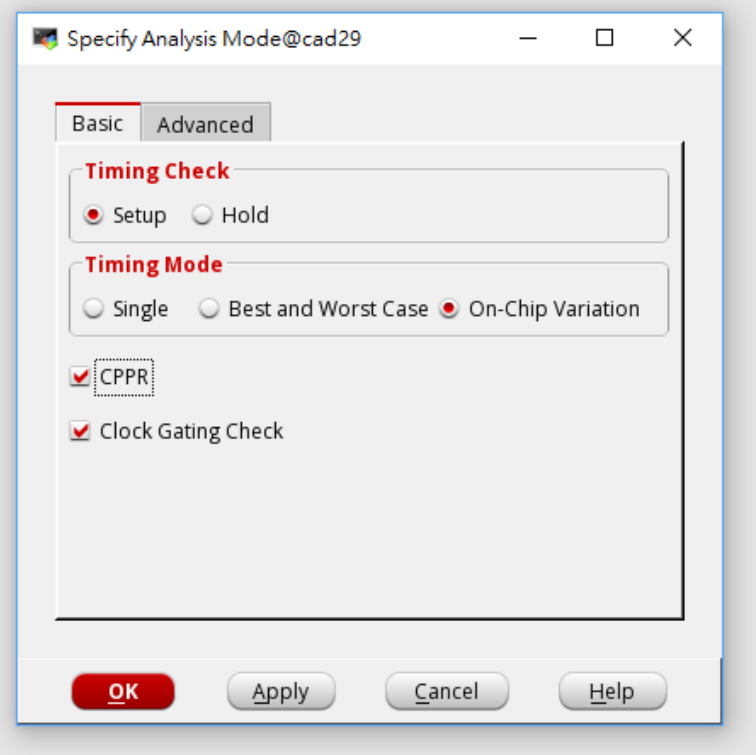
   - ◆ Fix Antenna
   - ◆ Insert Diodes — Diode Cell Name: **ANTENNA**
   - ◆ Timing Driven — Effort: **10**
   - ◆ SI Driven

   2.3 Click OK button

If Innovus crash, cancel **Timing Driven**.

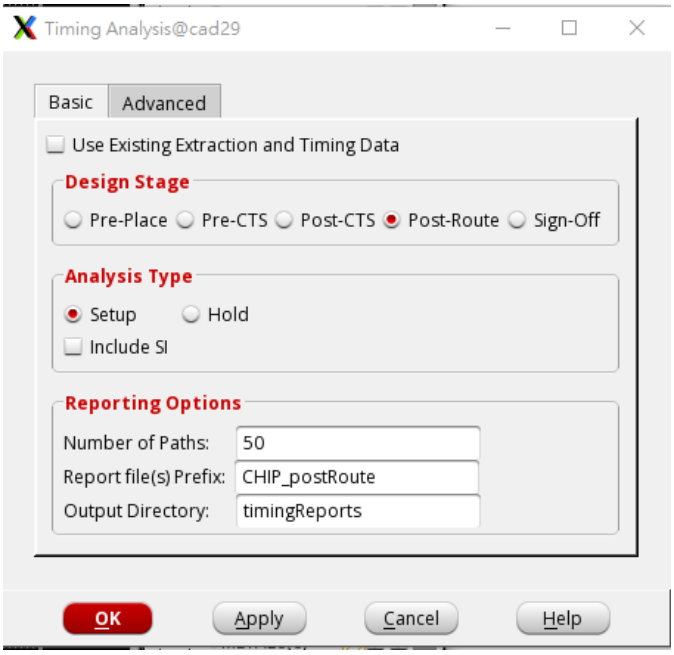
3. Save file
   - Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/route
4. In-Place Optimization – After Detail Route

   4.1 Open ***Tools → set Mode → Specify Analysis Mode…***
   - Timing Mode ◆ On-Chip Variation
   - ◆ CPPR
   - Click OK button



   4.2 Open ***Timing → Report Timing…***

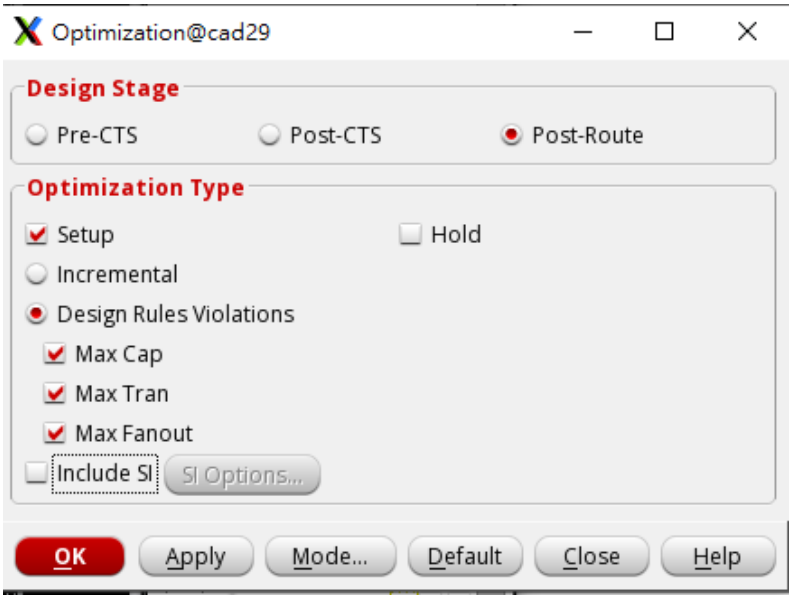
   4.3 Perform First Encounter trial route to model the interconnection RC effects
   - Design Stage ◆ Post-Route
   - Analysis Type ◆ Setup
   - Click OK button



4.4 Further timing optimization is performed to meet timing constraints if there is negative timing slack or DRVs. Open ***ECO → Optimize Design…***

4.5 Perform post-Route IPO

- Design Stage ◆ post-Route
- Optimization Type
  - Setup
  - Design Rule Violations
  - Max Cap
  - Max Tran
  - Max Fanout
- Click OK button



4.6 Verify if the hold time constraint is satisfied or not. Open ***Timing → Report Timing…***

- ➢ Design Stage ◆ Post-Route
- ➢ Analysis Type ◆ Hold
- ➢ Click OK button

4.7 If hold time slack is negative, open ***ECO → Optimize Design…***

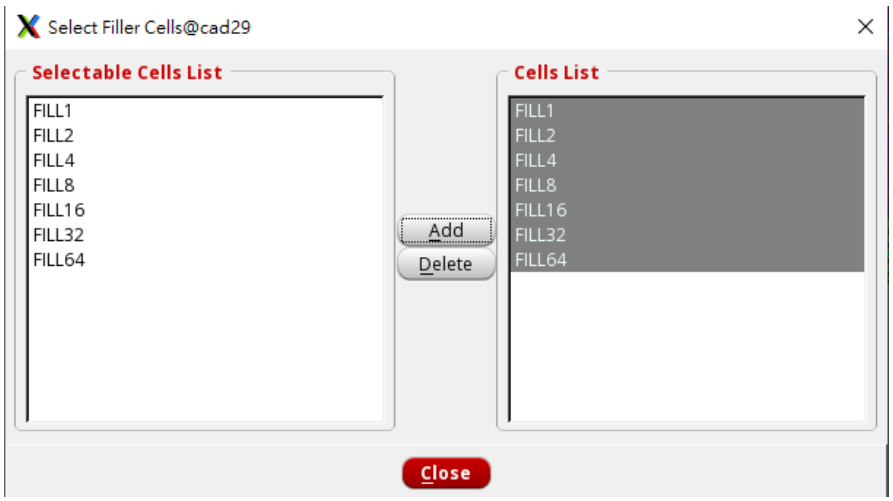
4.8 Perform post-Route IPO

- ➢ Design Stage ◆ post-Route
- ➢ Optimization Type
  - ◆ **Hold**
  - ◆ Design Rule Violations
  - ◆ Max Cap
  - ◆ Max Tran
  - ◆ Max Fanout
- ➢ Click OK button

5. Save file
   - ➢ Open ***File → Save Design…***
   - ➢ Choose ◆ Innovus
   - ➢ File Name: DBS/route

Add Core Filler cells

1. Open ***Place → Physical Cell → Add Filler…***
2. Add core filler to improve electric effects of NWELL and PWELL:
   2.1 Click Select button
   2.2 Select all core filler cells
   2.3 Click Add button
   2.4 Click Close button
3. 2.5 Click OK button



```
*INFO: Adding fillers to top-module.
*INFO:   Added 17 filler insts (cell FILL64 / prefix FILLER).
*INFO:   Added 50 filler insts (cell FILL32 / prefix FILLER).
*INFO:   Added 156 filler insts (cell FILL16 / prefix FILLER).
*INFO:   Added 553 filler insts (cell FILL8 / prefix FILLER).
*INFO:   Added 1319 filler insts (cell FILL4 / prefix FILLER).
*INFO:   Added 1438 filler insts (cell FILL2 / prefix FILLER).
*INFO:   Added 1494 filler insts (cell FILL1 / prefix FILLER).
*INFO: Total 5027 filler insts added - prefix FILLER (CPU: 0:00:00.3).
For 5027 new insts, *** Applied 2 GNC rules (cpu = 0:00:00.0)
```

Verify Geometry & Connectivity & Process Antenna

1. Verify geometry
   1.1 innovus # > **verify_drc**
2. Verify connectivity
   2.1 Open ***Verify → Verify Connectivity …***
   2.2 Net Type ◆ **All**
   2.3 Nets ◆ **All**
   2.4 Click OK button
3. Verify process antenna
   3.1 Open ***Verify → Verify Process Antenna…***
   3.2 Click OK button

If there are dangling wires, use hot key T (shift + t) to fix it.

Output Data

1. Open ***File → Save → Netlist…***
   - ⬥Include Intermediate Cell Definition
   - ⬥Include Leaf Cell Definition
   - Netlist File: CHIP_pr.v
   - Click OK button
2. Open ***File → Save Design…***
   - Choose ◆ Innovus
   - File Name: DBS/final
3. In innovus command prompt, execute the following commands:
   - **setAnalysisMode -analysisType bcwc**
   - **write_sdf -max_view av_func_mode_max **
     **-min_view av_func_mode_min **
     **-edges noedge **
     **-splitsetuphold **
     **-remashold **
     **-splitrecrem **
     **-min_period_edges none **
     CHIP.sdf

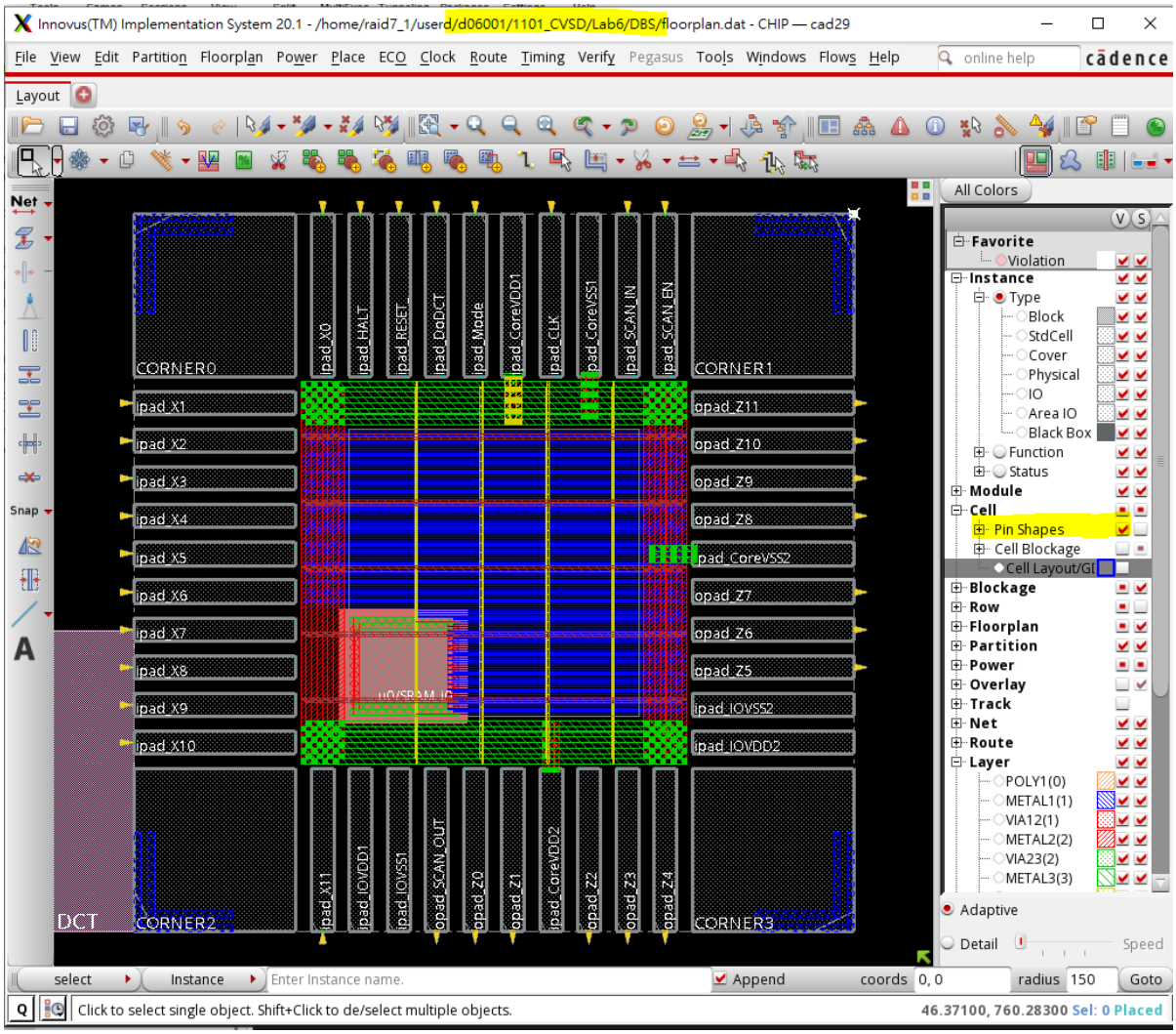
4. In innovus command prompt, execute the following commands:
   - **setStreamOutMode -specifyViaName default -SEvianames false -virtualConnection false -uniquifyCellNamesPrefix false -snapToMGrid false -textSize 1 -version 3**
   - **streamOut CHIP.gds -mapFile library/streamOut.map **
     **-merge {library/gds/tsmc13gfsg_fram.gds **
     **library/gds/tpz013g3_v1.1.gds } **
     **-stripes 1 **
     **-units 1000 **
     -mode ALL

Checkpoints

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Show your final results as follows. (Please make sure your screenshots can show your student ID with the server or you will not be graded)

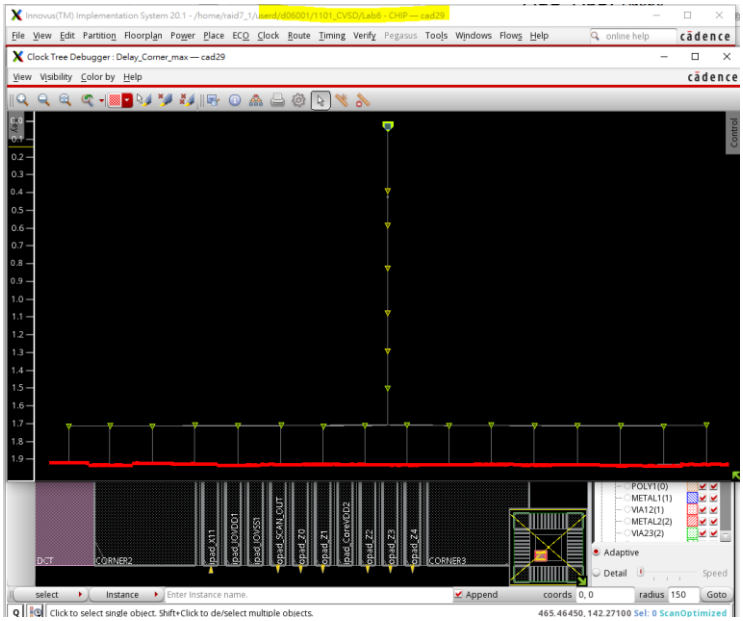
a. Placement result after adding follow pins



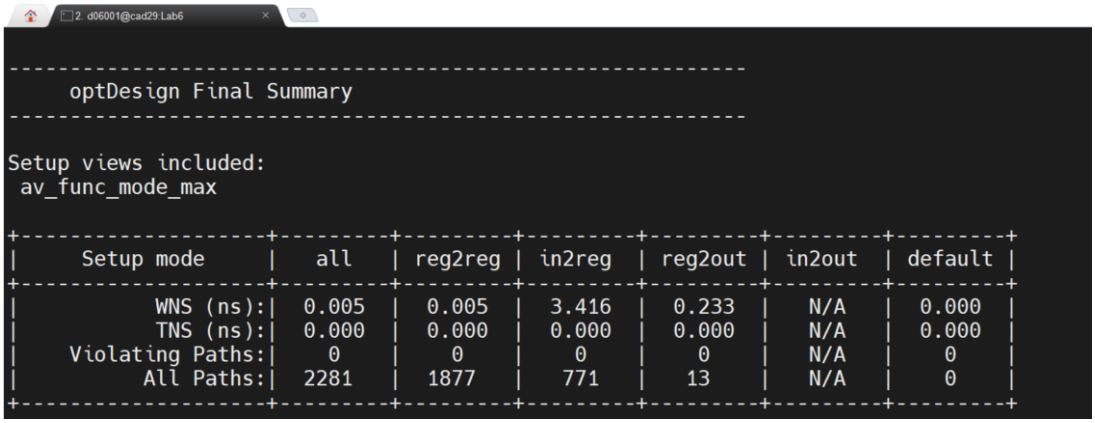
b. Verify geometry and connectivity after power planning

```
  VERIFY DRC ..... Sub-Area: {0.000 884.000 176.800 1058.620} 31 of 36
  VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 884.000 353.600 1058.620} 32 of 36
  VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 884.000 530.400 1058.620} 33 of 36
  VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 884.000 707.200 1058.620} 34 of 36
  VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {707.200 884.000 884.000 1058.620} 35 of 36
  VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {884.000 884.000 1058.820 1058.620} 36 of 36
  VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.2  ELAPSED TIME: 1.00  MEM: 6.0M) ***

1
innovus 6> VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Tue Nov 23 11:27:53 2021

Design Name: CHIP
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (1058.8200, 1058.6200)
Error Limit = 1000; Warning Limit = 50
Check specified nets
*** Checking Net VDD
*** Checking Net VSS

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Tue Nov 23 11:27:53 2021
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)

innovus 6>
```

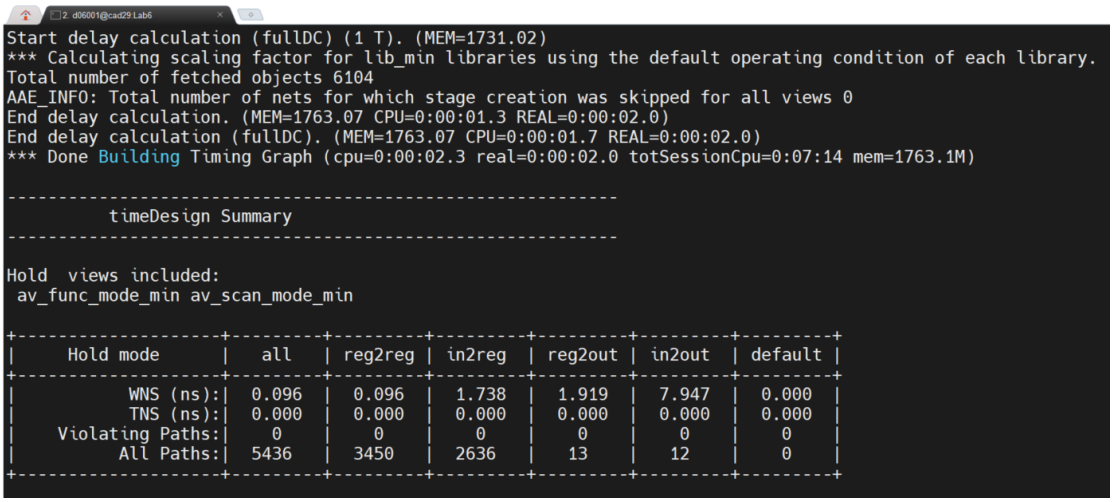
c. Clock -> CCopt Clock Tree Debugger



d. Post-routing timing analysis of setup time and hold time (ensure the slack of hold time and the slack of setup time >= 0)



```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.005  |  0.005  |  3.416  |  0.233  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  2281   |  1877   |   771   |   13    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+
```



```
Start delay calculation (fullDC) (1 T). (MEM=1731.02)
*** Calculating scaling factor for lib_min libraries using the default operating condition of each library.
Total number of fetched objects 6104
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=1763.07 CPU=0:00:01.3 REAL=0:00:02.0)
End delay calculation (fullDC). (MEM=1763.07 CPU=0:00:01.7 REAL=0:00:02.0)
*** Done Building Timing Graph (cpu=0:00:02.3 real=0:00:02.0 totSessionCpu=0:07:14 mem=1763.1M)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_min av_scan_mode_min

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.096  |  0.096  |  1.738  |  1.919  |  7.947  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |    0    |    0    |
|          All Paths:|  5436   |  3450   |  2636   |   13    |   12    |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+
```

Submission

1. **Due Tuesday, Dec. 21, 23:59**

2. Put the snapshots mentioned in the previous section (5 images in total) in a .tar and name the .tar with the format: **studentID_lab7_v*k***
   Note1: Use **lower case** for the letter in your student ID. (Ex. d06943027_lab7_v1)
   Note2: TA will only check the last version of your result.

3. Submit to FTP
   - IP: 140.112.175.68
   - Port: 21
   - Account: 1101cvsd_student
   - Password: ilovecvsd