Computer-Aided VLSI System Design
Lab5: STA Lab: Static Timing Analysis

TA: 蔡宇軒 f07943171@ntu.edu.tw

Introduction

In this lab, you will learn:

1. How to use STA tools to analyze the timing of synchronous digital ASICs.
2. How to fix these problems of the timing violations.

Environmental Setup

1. Source the license file.

```
source /usr/cad/synopsys/CIC/primetime.cshrc
```

2. Make a working directory

```
mkdir sta_lab
```

```
cd sta_lab
```

Copy Files from NTU Cool

1. Upload all the files downloaded from NTU Cool to your working directory (Lab4.zip)

2. Check if you have these files (including hidden files)

Files/Folder	Description
`.synopsys_dc.setup`	Synopsys DFT Compiler setup file (same format as Design Vision). Define search paths, library name etc.
`ALU_syn.v`	Gate level Verilog code for the simple ALU
`ALU.spef`	Time and RC information file for the simple ALU
`ALU_pt.script`	Script to run PrimeTime
`ALU_syn.script`	Script to run Design Vision (including generating ALU.spef)

Invoke PrimeTime STA tool

1. To invoke PrimeTime, you can do either one
   - pt_shell (command mode)
   - primetime & (GUI mode)

2. We encourage everybody to use command mode because:
   a. The command mode helps you to keep a record of what you have done.

b. The command mode runs more efficiently than GUI mode.
c. The command mode helps you to lookup the manual/reference quickly.

In spite of the above advantages, command mode sometimes is not as good as GUI mode in terms of debugging the schematic problem. We will use command mode throughout this Lab. You are welcome to try the GUI mode by yourself.

Start Operating PrimeTime STA tool

STA Environment Setting for TSMC 0.13um Technology

1. Set search path (If it has not been set up yet)

```
set search_path ".
/home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db"
```

2. Set link library

```
set link_path "* typical.db fast.db slow.db"
```

Read Gate level Netlist Files and Link design

1. Type these lines to read in CIC .18 library and your gate level netlist

```
read_verilog ./ALU_syn.v
```

2. Link all designs

```
link_design ALU
```

Note, you have to check the search path and include library, if you get the error message after step 2.

Read Timing and RC information

Reads leaf cell and net timing and RC information from a file in SPEF Format and uses that information to annotate the current design.

```
read_parasitics ALU.spef
```

Note: The file can be get during synthesis with “write_parasitics” comment.

Set Operating Conditions

```
set_operating_conditions typical -library typical
```

Set Design Constraints:

1. Specify the clock name, period, and clock characteristic

```
create_clock -period 10 -waveform {0 5} [get_ports clk]
set design_clock [get_clock clk]
set_clock_uncertainty 0.5 $design_clock
set_clock_latency -min 1.5 $design_clock
set_clock_latency -max 2.5 $design_clock
set_clock_transition -min 0.25 $design_clock
set_clock_transition -max 0.30 $design_clock
set_propagated_clock $design_clock
```

2. Set wire load model

```
set_wire_load_model -name "ForQA" -library "typical"
```

3. Set wire load mode

```
set_wire_load_mode top
```

4. Report

```
report_design
report_reference
```

Questions:

How many reference cells will you have? _____.

And total area size = _____

Timing analysis and report possible problems:

Please type the following commands to set the input/output delay:

```
set_input_delay 1.5 [get_ports inputA] -clock $design_clock
set_input_delay 1.5 [get_ports inputB] -clock $design_clock
set_input_delay 1.5 [get_ports instruction] -clock $design_clock
set_input_delay 1.5 [get_ports reset] -clock $design_clock
set_output_delay 1.5 [get_ports alu_out] -clock $design_clock
```

And then check the timing:

```
check_timing
report_timing
report_bottleneck
```

Questions:

Does the design meet the timing requirement? _____.

Find the critical path: Start-point = _____

End-point = _____

Change the setting and check the timing again:

```
create_clock -period 2 -waveform {0 1.0} [get_ports clk]
report_timing
```

Questions:

Now, does the design meet the timing requirement? _____.

Is it the setup time violation or the hold time violation? _____.

If all other setting is the same, what is the maximum clock period for the design to meet the timing requirement? _____ ns.

Try to modify the setting and verify the number you get with STA tool.

Do you succeed? _____

Change the setting and check the timing again:

```
create_clock -period 10 -waveform {0 5.0} [get_ports clk]
set_output_delay 8 [get_ports alu_out] -clock $design_clock
report_timing
```

Questions:

Now, does the design meet the timing requirement? _____.

Where is the new critical path:

Start-point = _____

End-point = _____

Reports:

1. Show the types of checks being done (setup, hold, min pulse width, recovery, removal and so forth)

```
report_constraint
report_constraint -all_violators
report_analysis_coverage
```

Questions:

How many timing violations are there in the design? _____

2. Change the setting and check the report again:

```
set_clock_uncertainty 0.0 $design_clock
report_constraint
report_constraint -all_violators
report_analysis_coverage
```

Questions:

Why are the hold-time violations fixed? Think about the change in clock setting.

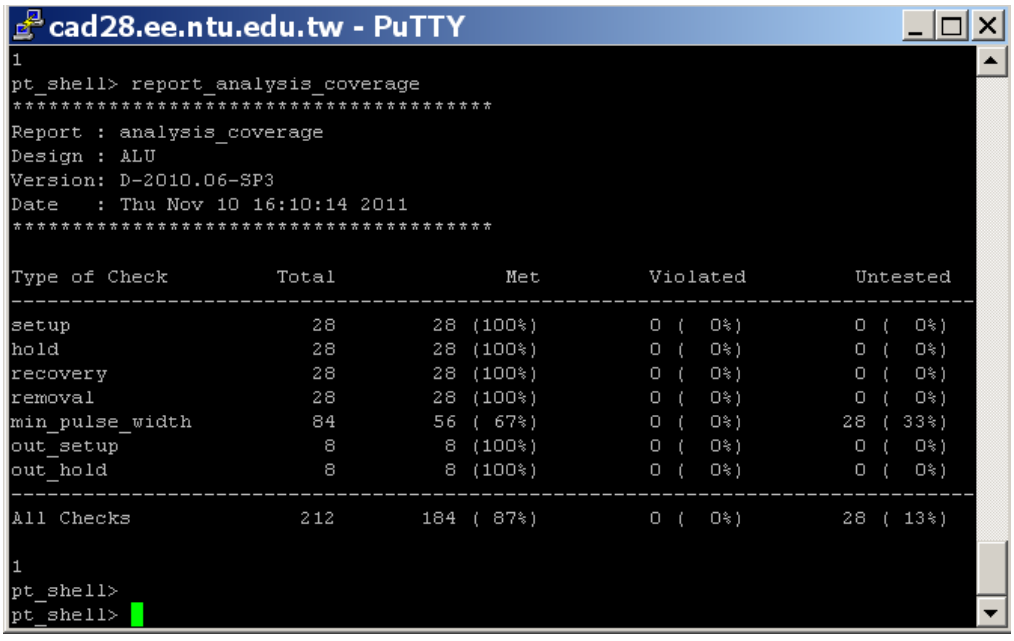
_____

_____

Checkpoints:

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Show your final STA results as follows.



2. Show your answers of the questions in this lab document.

Submission

1. **Due Tuesday, Nov. 23, 19:00**

2. Put the snapshots mentioned in the previous section in a .tar and name the .tar with the format: **studentID_lab5_v*k***
   Note1: Use **lower case** for the letter in your student ID. (Ex. d06943027_lab5_v1)
   Note2: TA will only check the last version of your result.

3. Submit to FTP
   - IP: 140.112.175.68
   - Port: 21
   - Account: 1101cvsd_student
   - Password: ilovecvsd