Computer-Aided VLSI System Design
Homework 4 Report

Due Tuesday, Dec. 21, 14:00

Student IDs: d10943013

Student Names: 姜承佑

Questions and Discussion

1. Fill in the blanks

Physical category		
Design Stage	Description	Value
Gate-level Simulation	Cycle time for Gate-level Simulation (ex. 10ns)	10ns
	Gate-level Simulation Time for f1	15410
	Gate-level Simulation Time for f2	15410
	Gate-level Simulation Time for f3	15410
	Gate-level Simulation Time for f4	15390
	Gate-level Simulation Time for f5	15410
	Gate-level Simulation Time for f6	15390
	Gate-level Simulation Time for f7	15390

2. Specify the methods you adopted for low-power design. (10pts)
   少用乘法器、較大的加法器，減少不必要的 register 值變動。