Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Jan. 4, 14:00

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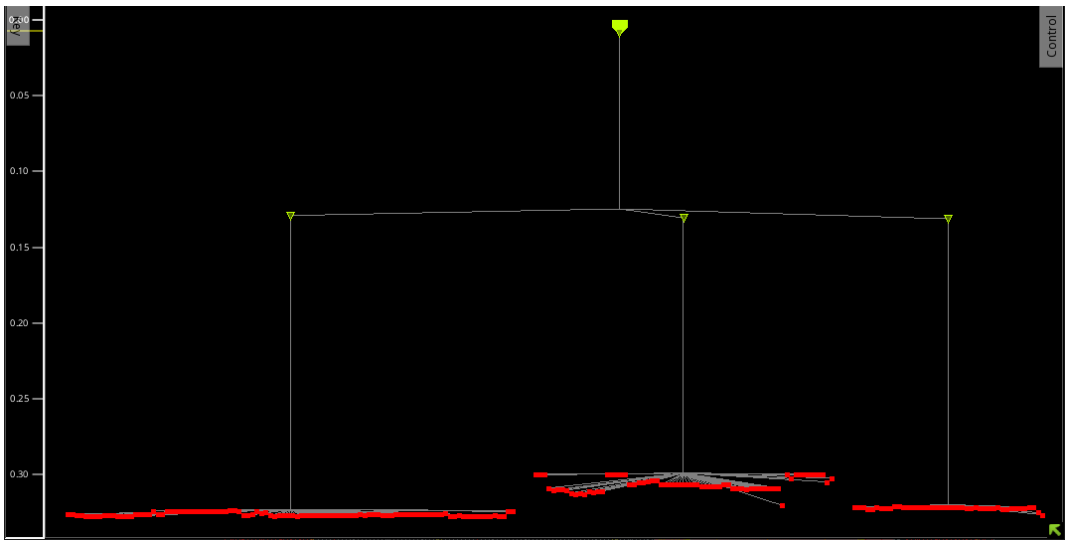
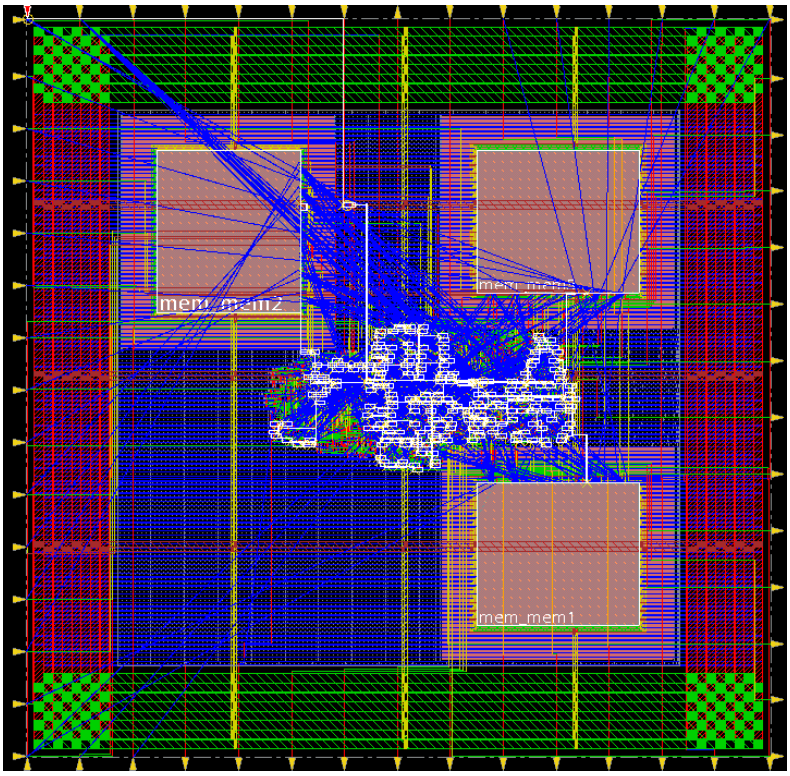
Questions and Discussion

1. Fill in the blanks

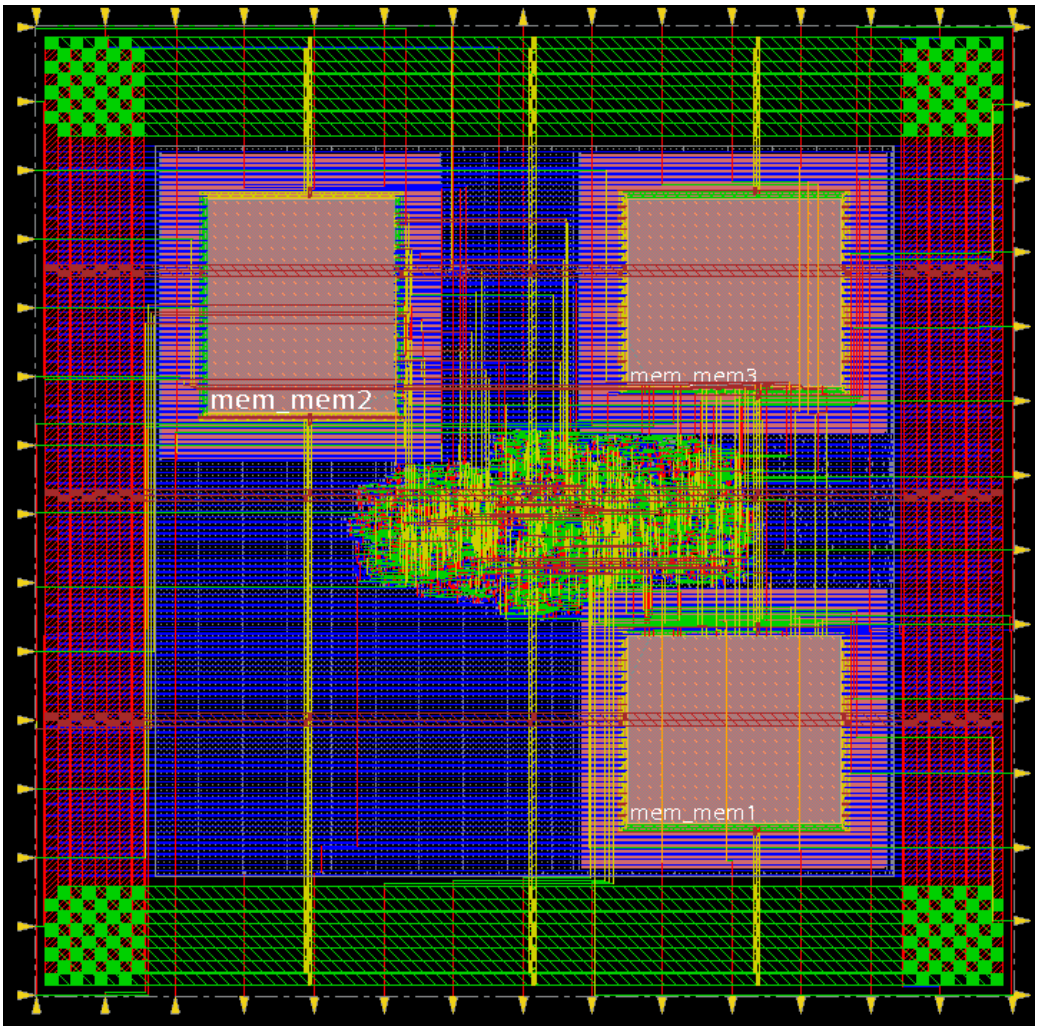
Physical category (10%)		
Design Stage	Description	Value
P&R	Number of DRC violation (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violation (ex: 0) (Verify -> Verify Connectivity…)	0
	Core area (um^2)	240412.95
	Die area (um^2)	423440.95
Prost-layout Gate-level Seimulation	Cycle time for Post-layout Simulation (ex. 10ns)	6.8ns
N/A	Follow your design in HW3? (If not, write down the student ID of the designer)	TA

2. Attach the snapshot of CCOpt Clock Tree Debugger result, and show the routing result in the layout (10%).





3. Attach the snapshot of your final layout **after adding core filler** (10%).



4. Show one of the critical paths (reg2reg) after post-route optimization (5%)

```
Path 1: MET Setup Check with Pin mem_mem2/CLK
Endpoint:   mem_mem2/A[7]    (^) checked with  leading edge of 'i_clk'
Beginpoint: ftr_row_reg_0_/Q (^) triggered by  leading edge of 'i_clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.316
- Setup                         0.539
+ Phase Shift                   6.800
+ CPPR Adjustment               0.000
= Required Time                 6.577
- Arrival Time                  5.619
= Slack Time                    0.957
     Clock Rise Edge                     0.000
     + Source Insertion Delay           -0.321
     = Beginpoint Arrival Time          -0.321
     Timing Path:
     +-------------------------------------------------------------------------------------------+
     |          Pin          | Edge |    Net     |    Cell    | Delay | Arrival | Required |
     |                       |      |            |            |       |  Time   |   Time   |
     |-----------------------+------+------------+------------+-------+---------+----------|
     | i_clk                 |  ^   | i_clk      |            |       |  -0.321 |    0.636 |
     | CTS_ccl_a_buf_00024/A |  ^   | i_clk      | CLKBUFX16  | 0.004 |  -0.317 |    0.640 |
     | CTS_ccl_a_buf_00024/Y |  ^   | CTS_2      | CLKBUFX16  | 0.116 |  -0.201 |    0.756 |
     | CTS_ccl_a_buf_00019/A |  ^   | CTS_2      | CLKBUFX20  | 0.006 |  -0.195 |    0.762 |
     | CTS_ccl_a_buf_00019/Y |  ^   | CTS_4      | CLKBUFX20  | 0.168 |  -0.027 |    0.931 |
     | ftr_row_reg_0_/CK     |  ^   | CTS_4      | DFFQX1     | 0.014 |  -0.013 |    0.944 |
     | ftr_row_reg_0_/Q      |  ^   | ftr_row[0] | DFFQX1     | 0.548 |   0.535 |    1.492 |
     | U1303/A               |  ^   | ftr_row[0] | ADDHXL     | 0.000 |   0.535 |    1.492 |
     | U1303/S               |  ^   | n8190      | ADDHXL     | 0.332 |   0.867 |    1.824 |
     | U1072/A               |  ^   | n8190      | CLKINVX1   | 0.000 |   0.867 |    1.824 |
     | U1072/Y               |  v   | n8310      | CLKINVX1   | 0.178 |   1.044 |    2.002 |
     | U1233/A1              |  v   | n8310      | OAI22XL    | 0.000 |   1.044 |    2.002 |
     | U1233/Y               |  ^   | n1065      | OAI22XL    | 0.236 |   1.280 |    2.237 |
     | U1215/A               |  ^   | n1065      | ADDHXL     | 0.000 |   1.280 |    2.237 |
     | U1215/S               |  ^   | n8320      | ADDHXL     | 0.286 |   1.566 |    2.523 |
     | U1079/A               |  ^   | n8320      | AND2X1     | 0.000 |   1.566 |    2.523 |
     | U1079/Y               |  ^   | n1068      | AND2X1     | 0.197 |   1.763 |    2.720 |
     | U1722/B               |  ^   | n1068      | ADDFXL     | 0.000 |   1.763 |    2.720 |
     | U1722/CO              |  ^   | n1076      | ADDFXL     | 0.673 |   2.436 |    3.393 |
     | U1276/CI              |  ^   | n1076      | ADDFXL     | 0.000 |   2.436 |    3.393 |
     | U1276/S               |  v   | n1087      | ADDFXL     | 0.290 |   2.726 |    3.684 |
     | U1588/B               |  v   | n1087      | ADDFXL     | 0.000 |   2.726 |    3.684 |
     | U1588/CO              |  v   | n1109      | ADDFXL     | 0.661 |   3.387 |    4.345 |
     | U1270/CI              |  v   | n1109      | ADDFXL     | 0.000 |   3.387 |    4.345 |
     | U1270/CO              |  v   | n1102      | ADDFXL     | 0.408 |   3.795 |    4.753 |
     | U1268/CI              |  v   | n1102      | ADDFXL     | 0.000 |   3.795 |    4.753 |
     | U1268/S               |  ^   | n1114      | ADDFXL     | 0.484 |   4.279 |    5.236 |
     | U1748/B               |  ^   | n1114      | OR2X1      | 0.000 |   4.279 |    5.236 |
     | U1748/Y               |  ^   | n799       | OR2X1      | 0.236 |   4.515 |    5.473 |
     | U1020/A               |  ^   | n799       | NAND2X1    | 0.000 |   4.515 |    5.473 |
     | U1020/Y               |  v   | n1118      | NAND2X1    | 0.072 |   4.587 |    5.545 |
     | U1256/A1              |  v   | n1118      | OAI21XL    | 0.000 |   4.587 |    5.545 |
     | U1256/Y               |  ^   | n1869      | OAI21XL    | 0.336 |   4.923 |    5.881 |
     | U1720/A0              |  ^   | n1869      | AOI21X1    | 0.000 |   4.923 |    5.881 |
     | U1720/Y               |  v   | n1915      | AOI21X1    | 0.151 |   5.074 |    6.031 |
     | U1721/A               |  v   | n1915      | XOR2X1     | 0.000 |   5.074 |    6.031 |
     | U1721/Y               |  ^   | n1918      | XOR2X1     | 0.149 |   5.223 |    6.181 |
     | U1719/A0              |  ^   | n1918      | AO22X4     | 0.000 |   5.223 |    6.181 |
     | U1719/Y               |  ^   | mem_addr[7]| AO22X4     | 0.394 |   5.617 |    6.575 |
     | mem_mem2/A[7]         |  ^   | mem_addr[7]| sram_256x8 | 0.002 |   5.619 |    6.577 |
     +-------------------------------------------------------------------------------------------+
```

5. Attach the snapshot of timing report for setup time with no timing violation (post-route) (5%).

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.651  |  0.957  |  2.048  |  0.651  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   481   |   231   |   247   |   26    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000     |      0 (0)       |
|   max_fanout   |      0 (0)       |     0       |      0 (0)       |
|   max_length   |      0 (0)       |     0       |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 14.658%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

6. Attach the snapshot of timing report for hold time with no timing violation (post-route) (5%).

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.816  |  0.816  |  3.402  |  4.572  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   481   |   231   |   247   |   26    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 14.658%
       (100.000% with Fillers)
------------------------------------------------------------
```

7. Attach the snapshot of DRC checking after routing (5%).

```
innovus 2> verify_drc
#-check_ndr_spacing auto                # enums={true false auto}, default=auto,  user setting
#-report ipdc.drc.rpt                   # string, default="", user setting
 *** Starting Verify DRC (MEM: 1291.3) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 165.920 163.200} 1 of 16
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {165.920 0.000 331.840 163.200} 2 of 16
  VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {331.840 0.000 497.760 163.200} 3 of 16
  VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {497.760 0.000 653.660 163.200} 4 of 16
  VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 163.200 165.920 326.400} 5 of 16
  VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {165.920 163.200 331.840 326.400} 6 of 16
  VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {331.840 163.200 497.760 326.400} 7 of 16
  VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {497.760 163.200 653.660 326.400} 8 of 16
  VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 326.400 165.920 489.600} 9 of 16
  VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {165.920 326.400 331.840 489.600} 10 of 16
  VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {331.840 326.400 497.760 489.600} 11 of 16
  VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {497.760 326.400 653.660 489.600} 12 of 16
  VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 489.600 165.920 647.800} 13 of 16
  VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {165.920 489.600 331.840 647.800} 14 of 16
  VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {331.840 489.600 497.760 647.800} 15 of 16
  VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {497.760 489.600 653.660 647.800} 16 of 16
  VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.5  ELAPSED TIME: 0.00  MEM: 1.0M) ***
```

8. Attach the snapshot of LVS checking after routing (5%).

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Wed Dec 29 00:29:00 2021

Design Name: ipdc
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (653.6600, 647.8000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Dec 29 00:29:00 2021
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.1  MEM: 0.000M)
```

9. Attach the snapshot of final area result (5%).

```
************************ Analyze Floorplan **************************
    Die Area(um^2)             : 423440.95
    Core Area(um^2)            : 240412.95
    Chip Density (Counting Std Cells and MACROs and IOs): 42.325%
    Core Density (Counting Std Cells and MACROs): 74.547%
    Average utilization        : 100.000%
    Number of instance(s)      : 5042
    Number of Macro(s)         : 3
    Number of IO Pin(s)        : 59
    Number of Power Domain(s) : 0
************************ Estimation Results ************************
********************************************************************
```