

# IST8310 3D Magnetometer

# **Preliminary Datasheet**



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# 1 General Description

iSentek IST8310 is a 3-axis digital magnetometer with 3.0x3.0x1.0mm<sup>3</sup>, 16-pin LGA package. It is an integrated chip with 3-axis magnetic sensors, digital control logic, built-in temperature compensation circuit and self-test function. IST8310 provides an I<sup>2</sup>C digital output with fast mode up to 400kHz. The ultra-low hysteresis features, excellent temperature drift and low noise performance make it a perfect candidate for high accuracy applications.

### **Features**

- Single chip 3-axis magnetic sensor
- 3.0x3.0x1.0mm<sup>3</sup>, 16-pin LGA package
- I<sup>2</sup>C slave, Fast Mode up to 400kHz
- 14 bits data output
- Wide dynamic range of  $\pm 1600 \text{uT}$  (x, y-axis) and  $\pm 2500 \text{uT}$  (z-axis)
- Ultra-low hysteresis (<0.1%FS)
- Ultra-low sensitivity temperature drift (±0.016 %/°K)
- Ultra-low offset temperature drift (0.024uT/°K)
- Low noise performance of 0.1uT (x-axis), 0.2uT (y-axis) and 0.3uT (z-axis)
- Wide operating temperature range
- High precision temperature compensation
- Built-in self-test function
- Software and algorithm support available (For tilt compensation, cross-axis compensation and noise suppression)

### **Applications**

Quadcopter/Drone Applications

**Augmented Reality Applications** 

Virtual Reality Applications

**Location Based Services** 

**Navigation Applications** 

**Industrial Applications** 

Magnetometry

IOT devices

**Pointing** 

Gaming



# 2 Block Diagram, Package Dimension and Application Circuit

# 2.1 Block diagram

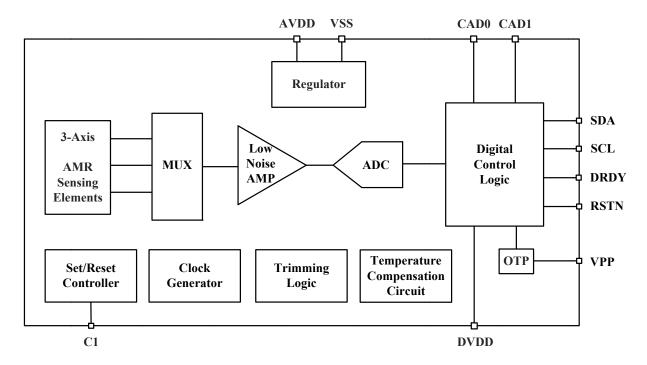
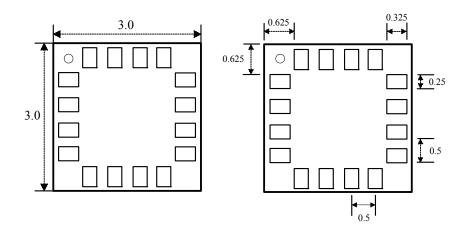


Figure 1. Block Diagram

# 2.2 Package Dimensions and Pin Description

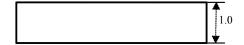
# IST8310 LGA Top View (Looking Through)



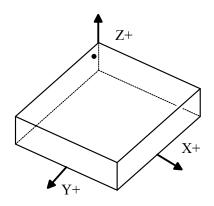
Unit: mm Tolerance: ±0.1mm



# IST8310 LGA Side View



# IST8310 3D Top View



Unit: mm Tolerance: ±0.1mm

Pin	Name	Function
1	SCL	I <sup>2</sup> C serial clock
2	AVDD	Analog supply voltage, 1.72~3.6V
3	NC	Not use
4	NC	Not use
5	CAD0	I <sup>2</sup> C slave address
6	CAD1	I <sup>2</sup> C slave address
7	VPP	Test pin, floating connection is suggested
8	NC	Not use
9	VSS	GND
10	C1	Set/Reset function, 4.7uF
11	VSS	GND
12	NC	Not use
13	DVDD	Digital supply voltage, 1.72~3.6V
14	RSTN	Reset pin, resets registers by setting it to "Low"
15	DRDY	Data ready indication, output pin only
16	SDA	I <sup>2</sup> C serial data

<sup>\*</sup>please refer to Figure 2.



# 2.3 Application Circuit

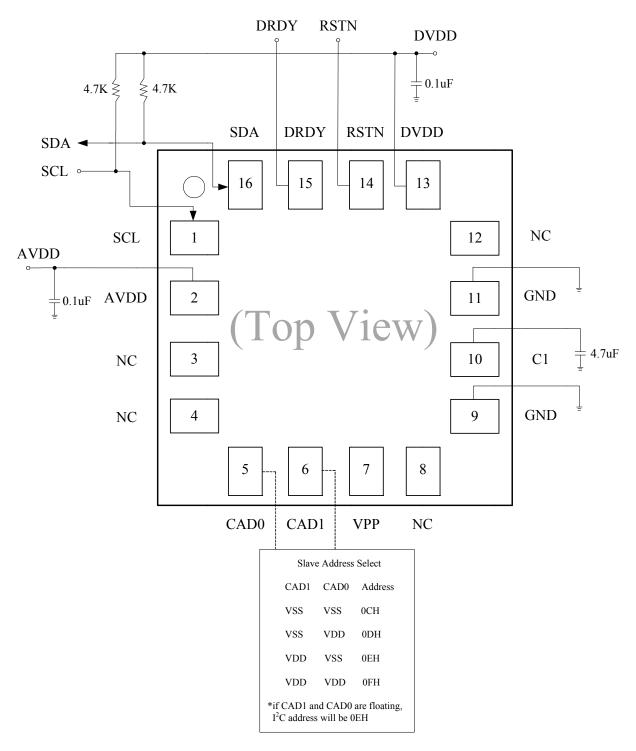


Figure 2. Application Circuit



# 3 Operational Modes and Functional Descriptions

### 3.1 Operation modes

IST8310 has following operation modes:

- (1) Stand-By Mode
- (2) Single Measurement Mode
- (3) Self-Test Mode

### 3.1.1 Stand-By Mode

The initial mode (after power on) of IST8310 is Stand-By Mode. In Stand-By Mode, all internal circuits are off (except oscillator and regulator). All registers can be accessed in Stand-By Mode. Data stored in Read/Write registers remains as last state. Registers can be reset by soft reset.

### 3.1.2 Single Measurement Mode

In Single Measurement Mode, the measured data is stored in data registers then IST8310 transits to Stand-By Mode automatically. On transition to Stand-By Mode, Control register 1(CNTL1[3:0]) turns to "0000". At the same time, DRDY bit in STAT1 register turns to "1". This is called "data ready". When any of the measurement data registers or STAT2 register is read, DRDY bit turns to "0". For the next measurement, user needs to set Control register 1(CNTL1[3:0]) to "0001" again.

Please noted in IST8310, the default operation includes soft-averaging in driver, please contact iSentek for the technical support.

### 3.1.3 Self-Test Mode

Self-Test mode is used to check if the 3-axis outputs read in Single Measurement Mode are correct. It is activated by setting Self-Test Register (0x0C) to 40h; then all 3-axis outputs will change their polarity. User can check the 3-axis output values before and after activating Self-Test Mode; if the absolute values are the same, then the IC is working correctly. It can be turned off by setting Self-Test Register (0x0C) to 00h.

### 3.2 Interrupt Function

Interrupt function is used when there is a huge external magnetic field in the surrounding. When the absolute sum of measured 3-axis output value exceeds 1600 uT, the INT flag is activated. The INT flag can be found in STAT2 register.



### 3.3 DRDY Function

DRDY function is used when the output data is updated. The DRDY pin is used to monitor the data ready output. DRDY is changed to low after reading data from the output register.

### 3.4 IST8310 Read Process

- (1) Read STAT1 register:
  - Polling STAT1 register bit 0
  - DRDY: shows if the data is ready or not
    - 0: no data ready
    - 1: data ready
  - DOR: shows if any data has been skipped before the current data
    - 0: no skipped data
    - 1: data skipped.

# (2) Read Measurement Data:

Read Register 0x03h~0x08h for X, Y and Z axis data. When data reading starts, DRDY bit and DOR bit turn to "0".



# **4 Electrical Specifications**

# 4.1 Extreme Rating

Parameter	Symbol	Limits	Unit		
Storage Temperature	TSTG	-40 to +125	°C		
Operating Temperature	TA	-40 to +85	°C		
Analog Supply Voltage	AVDD	-0.5 to +3.6	V		
Digital Supply Voltage	DVDD	-0.5 to +3.6	V		
Digital Input Voltage	VIN	-0.3 to DVDD+0.3	V		
Electrostatic Discharge Voltage*1	VESD_HBM	-4000 to 4000	V		
Electrostatic Discharge Voltage*2	VESD_MM	-350 to 350	V		
Reflow Classification	JESD22-A113 with 260 °C Peak Temperature				

<sup>1.</sup> Human Body Model (HBM)

# **4.2 Recommended Operating Conditions**

Parameter	Symbol	Min.	Тур.	Max.	Unit
Operating Temperature	TA	-40		+85	°C
Analog Supply Voltage	AVDD	1.72	2.8	3.6	V
Digital Supply Voltage	DVDD	1.72	1.8	3.6	V

# 4.3 Electrical Specifications

(Operating conditions: TA=+25 $^{\circ}$ C; AVDD=2.8V; DVDD=1.8V; 0.1 $\mu$ F ceramic capacitors **tied closely** to AVDD/DVDD and GND respectively.)

Parameter	Symbol	Conditions	Min.	Тур.	Max	Unit
Operating Current	IDD3A	Full operation, at				uA
(including 4 times		0.25 sps		20		
averaging in driver)		2 sps		72		
		2.5 sps		80		
		5 sps		140		
		12.5 sps		320		
		25 sps		600		
		50 sps		1200		
Standby Current	ISTB			10		uA

<sup>2.</sup> Machine Model (MM)



Output Data Rate	ODR		0.25	50	Hz
(ODR)					
Input Low Voltage	VIL		0	DVDD	V
				*30%	
Input High Voltage	VIH		DVDD	DVDD	V
			*70%		
Output Low Voltage	VOL	IOL= +4 mA	0	DVDD	V
				*20%	
Output High Voltage	VOH	IOH= -100 uA	DVDD	DVDD	V
		(Except SCL and	*80%		
		SDA)			

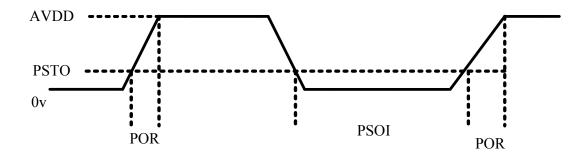
# **4.4 Magnetic Sensor Specifications**

(Operating conditions: Ta=+25°C; AVDD=2.8V; DVDD=1.8V; 4.7 $\mu$ F ceramic capacitors **tied closely** to C1 and GND respectively.)

Parameter	Symbol	Condition	Min.	Тур.	Max	Unit
Damania Dama	MDR_XY	TA=25 °C		±1600		T
Dynamic Range	MDR_Z	TA=25 °C		±2500		uТ
Linearity	LIN	X-axis		1	1.5	%FS
Linearity	LIN	Y, Z-axis		0.1	0.5	70F3
Resolution	RESO			0.3		uT/LSB
Sensitivity	SEN			3.3		LSB/uT
Zero Gauss Offset	ZGD	RMS value		±0.3		uТ
Hysteresis	HS			0.1		%FS
	NRMS	X-axis		0.10		
RMS Noise		Y-axis		0.20	uT	
		Z-axis		0.30		
Heading Accuracy	НА	30uT horizontal geomagnetic field, component level, TA=25 °C		±1		Degree
Sensitivity Temperature Drift	TD_S	-40 ~ 85 °C		±0.016		%/°K
Zero-B Offset Temperature Drift	TD_O	-40 ~ 85 °C		0.024		uT/°K



# 4.5 Power On Reset (POR) Specifications



PSTO: Power Supply Turn Off voltage PSOI: Power Supply Turn Off Interval

POR: Power On Reset

PSTO: max=0.1volt PSOI: min=10ms POR: max:50ms

When POR circuit detects the rise of AVDD voltage, it resets all internal circuits and initializes all registers. After reset, IST8310 transits to Stand-By mode.



# 5 Digital Interface and Registers

# 5.1 I<sup>2</sup>C Interface

The interface of IST8310 follows the standard I<sup>2</sup>C definition guidelines with some additional protocol definitions. IST8310 supports standard speed (100kHz) and fast speed (400kHz). Pull-up resistors of 4.7kohm for both SDA and SCL lines should be used.

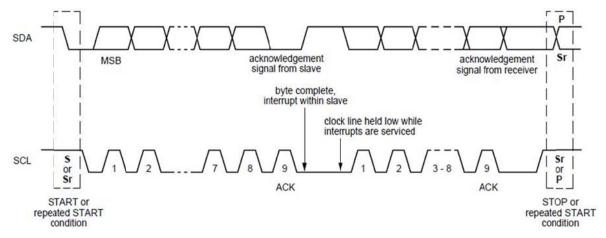


Figure 3. I<sup>2</sup>C Operation

# 5.2 I<sup>2</sup>C Read Operation

Single Byte Read:

SA	Slave	ACK	Reg	ACK	SP	Slave Address+RW	ACK	DATA	NA	ST
	Address+ RW		Address							

Figure 4. I<sup>2</sup>C Single Byte Read Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

Multiple Byte Read:

SA	Slave	ACK	Reg	ACK	SP	Slave	ACK	DATA	ACK	DATA	NA	ST
	Address+		Address			Address+RW						
	RW											

Figure 5. I<sup>2</sup>C Multiple Byte Read Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master ■: Master to Slave



# 5.3 I<sup>2</sup>C Write Operation

Single Byte Write:

SA	Slave Address +RW	ACK	Reg Address	ACK	DATA	ACK	ST	

Figure 6. I<sup>2</sup>C Single Byte Write Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

Multiple Byte Write:

SA	Slave Address	ACK	Reg Adderss	ACK	DATA	ACK	DATA	NA	ST
	+RW								

Figure 7. I<sup>2</sup>C Multiple Byte Write Operation

ACK: Acknowledge, NA: Not Acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■: Slave to Master □: Master to Slave

# 5.4 Registers

# 5.4.1 Customer Defined Registers

Register name	Тур	I <sup>2</sup> C	Size	Info
		Addr	(bit)	
Who am I	R	00h	8	Device ID
Status Register 1	R	02h	8	Data Status
Output Value X_L	R	03h	8	Low byte for X-axis data
Output Value X_H	R	04h	8	High byte for X-axis data
Output Value Y_L	R	05h	8	Low byte for Y-axis data
Output Value Y_H	R	06h	8	High byte for Y-axis data
Output Value Z_L	R	07h	8	Low byte for Z-axis data
Output Value Z_H	R	08h	8	High byte for Z-axis data
Status Register 2	R	09h	8	Data Status
Control Register 1	R/W	0Ah	8	Chip Control setting 1
Control Register 2	R/W	0Bh	8	Chip Control setting 2
Output Value T_L	R	1Ch	8	Low byte for Temperature data
Output Value T_H	R	1Dh	8	High byte for Temperature data



# 5.4.2 Who Am I Register

# This Register provides device ID information

	WAI (0x00)		
Bit	Description	Attr	Default
7:0	Device ID	R	10

# 5.4.3 Status Register 1

# This Register provides status information of IST8310

	STAT1 (0x02)				
Bit	Description	Attr	Default		
7:2	Reserved				
1	DOR: Turns to 1 when data has been skipped. Bit is released	R	0		
	after any output data register read				
	0: no data overrun				
	1: data overrun				
0	DRDY: Data ready pin	R	0		
	0: no data ready				
	1: data is ready				
	This status bit follows physical signal appearance, expect the				
	polarity control (refer to DRP bit in CNTL2 register)				
	If data ready function enable bit is not set (refer to DREN bit in				
	CNTL2 register), this bit is zero				

# 5.4.4 Output Data Registers

The Output Registers (from  $0x03h\sim0x08h$ ) contain X, Y and Z axis measurement data. Measurement data are stored in 2's complement format.

	DATAXL(0x03)		
Bit	Description	Attr	Default
7:0	Low Byte of X-axis data	R	0



	DATAXH(0x04)		
Bit	Description	Attr	Default
7:0	High Byte of X-axis data	R	0

	DATAYL(0x05)		
Bit	Description	Attr	Default
7:0	Low Byte of Y-axis data	R	0

	DATAYH(0x06)		
Bit	Description	Attr	Default
7:0	High Byte of Y-axis data	R	0

	DATAZL(0x07)		
Bit	Description	Attr	Default
7:0	Low Byte of Z-axis data	R	0

	DATAZH(0x08)		
Bit	Description	Attr	Default
7:0	High Byte of Z-axis data	R	0

# 5.4.5 Status Register 2

In this register, there is an INT flag for customer use.

	STAT2(0x09)			
Bit	Description	Attr	Default	
7:4	Reserved			
3	INT: Interrupt bit. When interrupt event occurs, this bit will be	R	0	
	set to 1			
2:0	Reserved			

# 5.4.6 Control Setting Register 1



This Register controls and adjusts the main parameters.

	CNTL1(0x0A)			
Bit	Description	Attr	Default	
7:4	Reserved			
3:0	Mode: Operating mode setting	R/W	0	
	0000: Stand-By mode			
	0001: Single Measurement Mode			
	Others: Reserved			

# 5.4.7 Control Setting Register 2

This Register controls and adjusts the main parameters.

	CNTL2(0x0B)			
Bit	Description	Attr	Default	
7:4	Reserved			
3	DREN : Data ready enable control:	R/W	1	
	0: disable			
	1: enable			
	Master switch for DRDY output pin			
2	DRP: DRDY pin polarity control	R/W	1	
	0: active low			
	1: active high			
1	Reserved			
0	SRST: Soft reset, perform Power On Reset (POR) routine	R/W	0	
	0: no action			
	1: start immediately POR routine			
	This bit will be set to zero after POR routine			

# 5.4.8 Self-Test Register

	STR(0x0C)			
Bit	Description	Attr	Default	
7	Reserved			
6	SELF_TEST: When this bit set to 1, chip enters self-test mode	R	0	
5:0	Reserved			



# 5.4.9 Temperature Sensor Output Registers

The Output Data Registers use 2's complement format.

TEMPL(0x1C)						
Bit	Description	Attr	Default			
7:0	Low Byte of Temperature data	R	0			

TEMPH(0x1D)						
Bit	Description	Attr	Default			
7:0	High Byte of Temperature data	R	0			

# **6 Ordering Information**

Order	Package Type	Packaging	Temperature	Marking Information
Number			Range	
IST8310	LGA – 16 pin	Tape and Reel: 5k	-40 to +85 °C	$X_1 X_2 X_3 0$
		pieces per reel		010●
				X <sub>1</sub> : Last number of the year
				X <sub>2</sub> X <sub>3</sub> : Week number
				010: Product code of IST8310

For more information on iSentek's Magnetic Sensors, please contact us at +86-177-1262-7208 (China), +886-2-2698-3306 ext:110 (Taiwan), via e-mail:sales@isentek.com or visit us online at www.isentek.com.

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Taiwanese Patents I437249, I420128 and I463160 apply to our magnetic sensor technology described.