School of Computer, Wuhan University

2019-2020 Second Semester *Digital Logic and Digital Circuit*

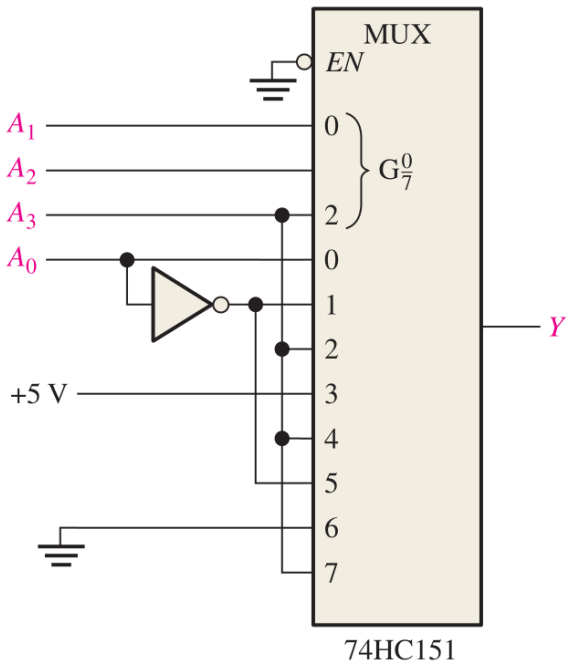
Term Exam Paper A（Open book）

Student No._____ Name_____

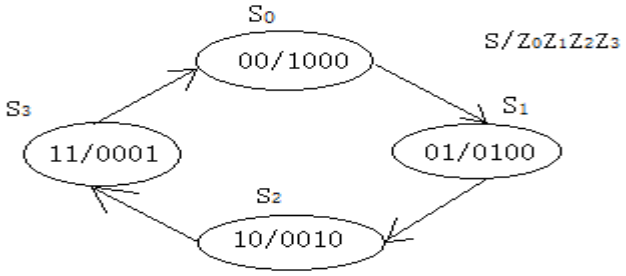
Note: All answers are required to be written on the answer sheet.

1. Combinational Logic Circuit Analysis (18')

1. Produce the logic function expression. (6')
2. Produce the truth table. (6')
3. Describe the function of the circuit. (6')



2. Using Verilog HDL to design a beat generator (节拍脉冲发生器) circuit. The circuit has 4 outputs of Z_0, Z_1, Z_2 and Z_3, corresponding to 4 states S_0, S_1, S_2 and S_3. For each clock pulse, one of the four outputs is 1, and the other three outputs are 0, and then the state will be transferred to the next state. Under the action of sequential clock pulse, the 4 output ports output 1 in turn. The state diagram is as follows. (16')



3. Design a synchronous sequential circuit to realize the following state table using D flip-flops. （16‘）

1. Derive logic expressions for the inputs of D flip-flops(10’)
2. Produce the logic circuit diagram(6’)

Present State		Next State							
		$x_2x_1 = 00$		$x_2x_1 = 01$		$x_2x_1 = 11$		$x_2x_1 = 10$	
Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Q_1^{n+1}	Q_0^{n+1}
0	0	0	0	1	0	0	1	0	0
0	1	0	0	1	0	1	1	1	0
1	0	0	1	1	1	1	1	1	0
1	1	0	1	1	1	0	1	0	0

4. Please make a summary for our course *Digital Logic and Digital Circuit* (including but not limited to the basic knowledge, key and difficult contents, principles, definitions, structural features, analysis and design methods, logic symbols, function tables, classifications of digital circuit, application fields and prospects). (50’)