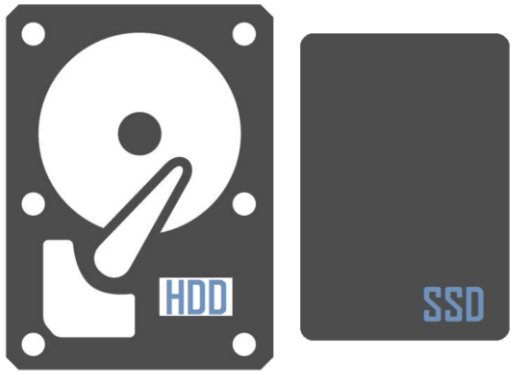
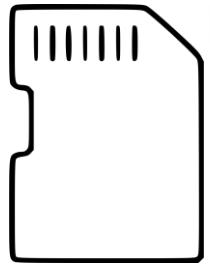
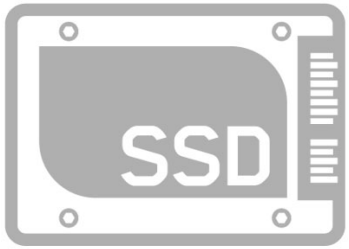


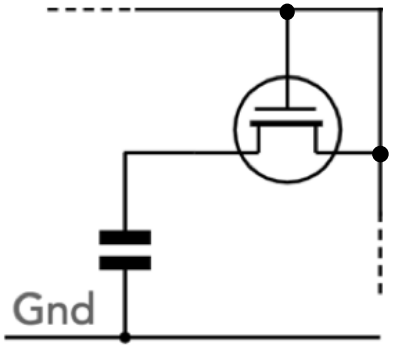


Architectures des Systèmes de Bases de Données

HDD to SSD

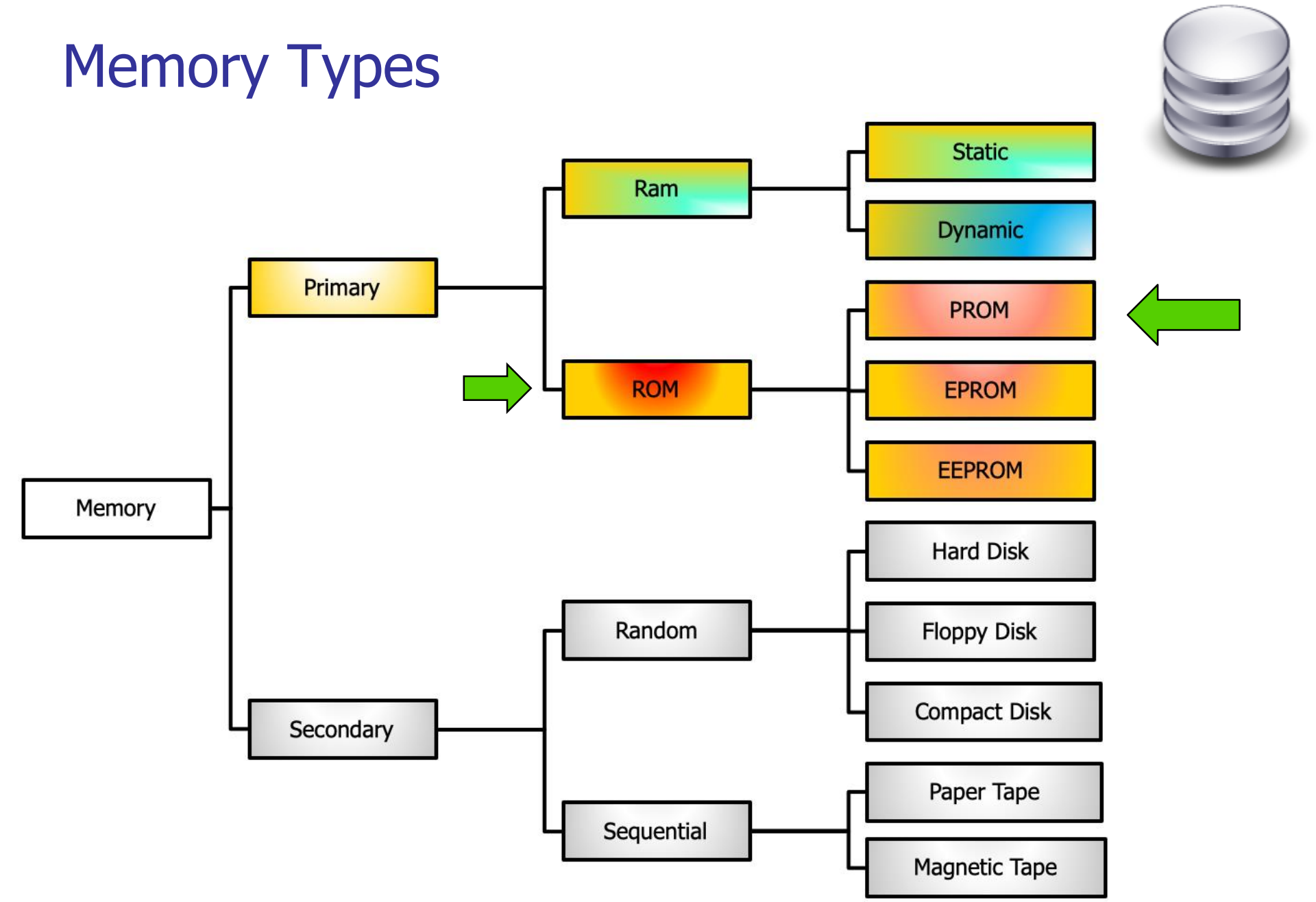
Flash Memory



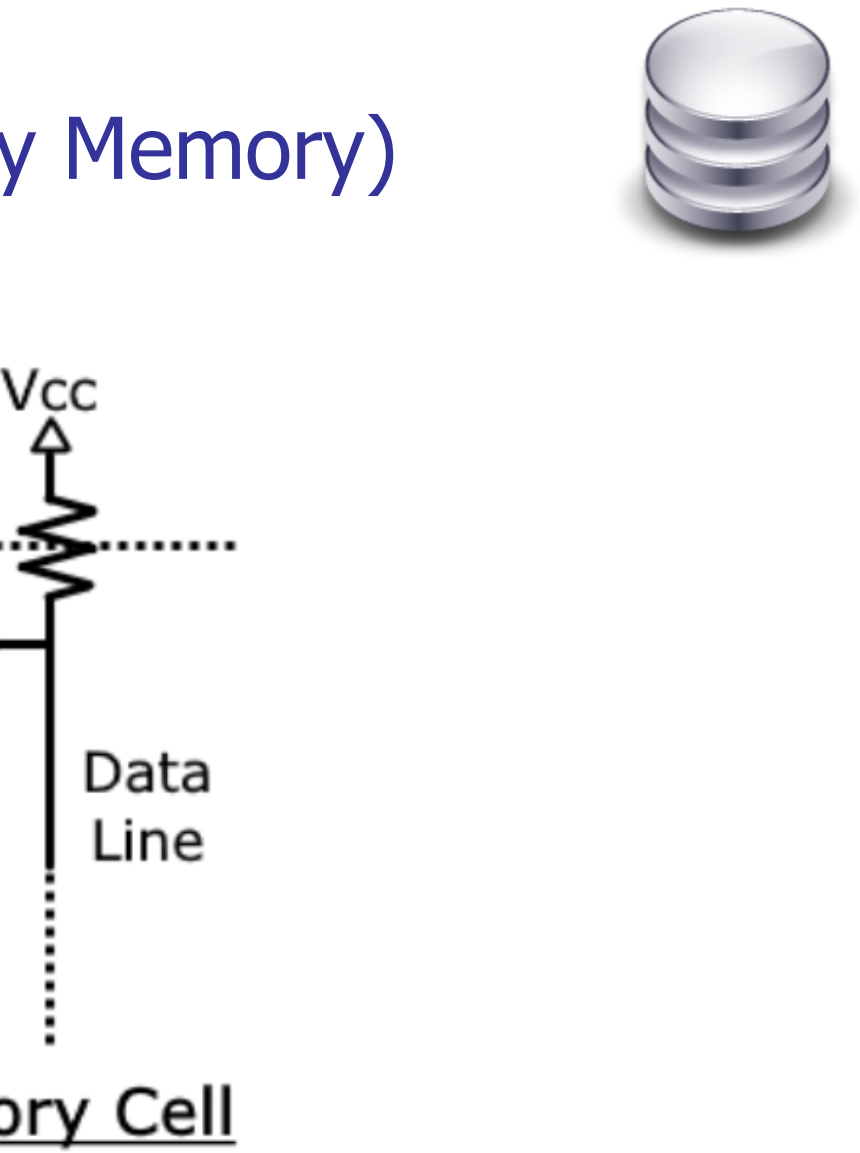


Traduction en cours

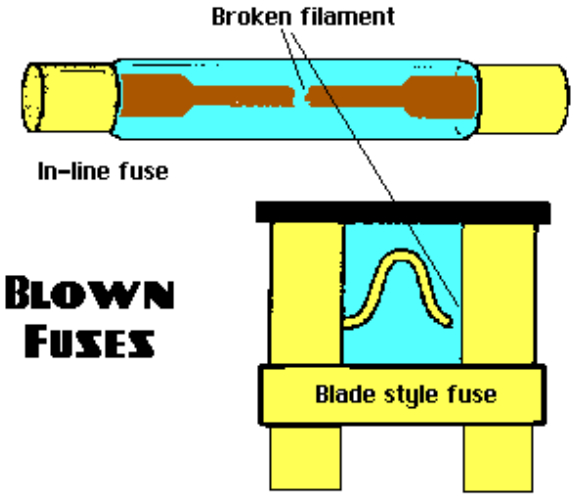
Memory Types



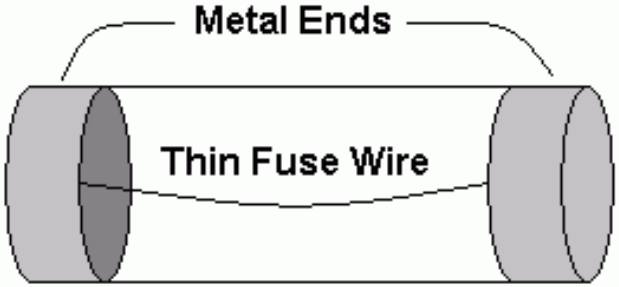
PROM
(Programmable Read-Only Memory)



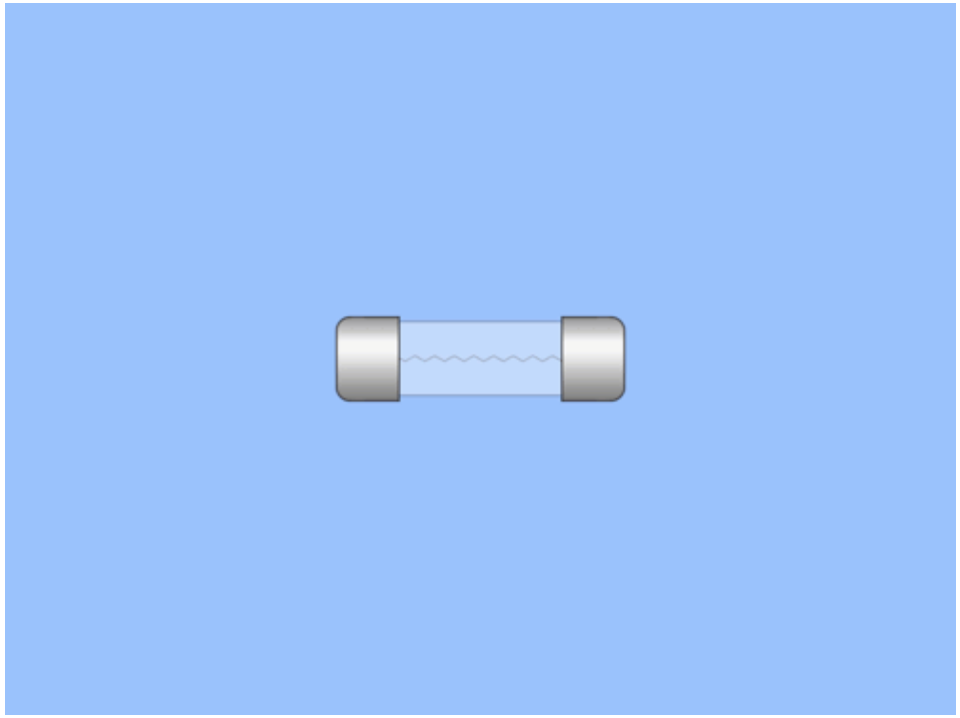
PROM : Fuse Cell



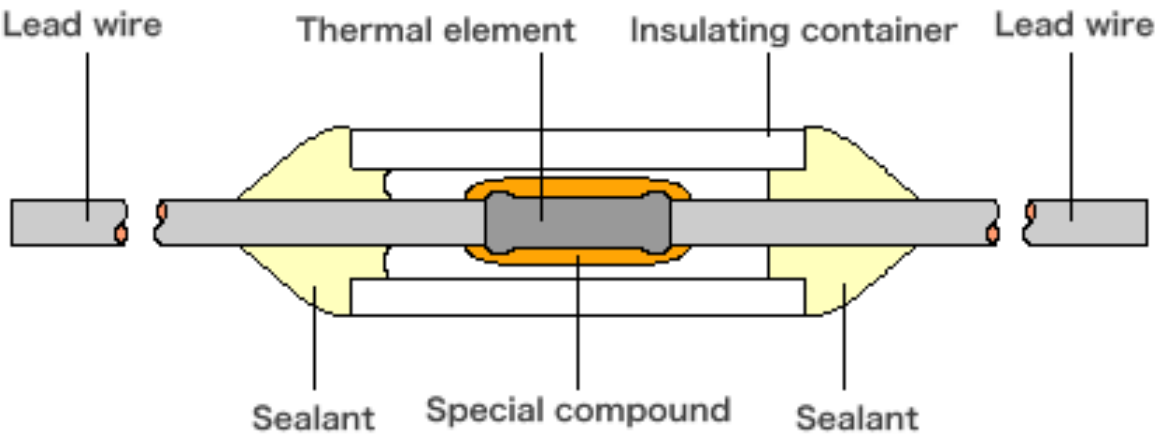
Blown Fuses



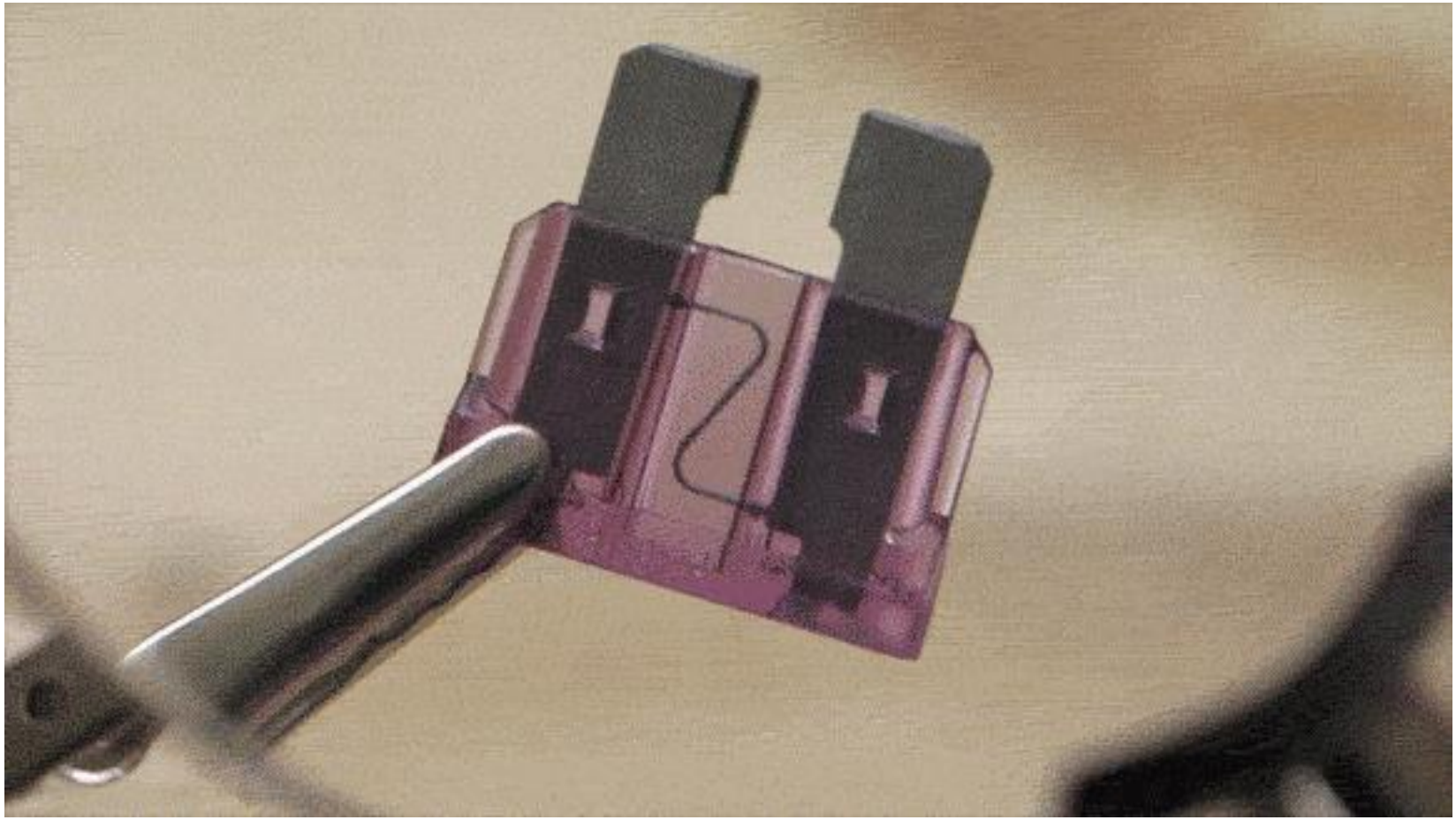
PROM : Fuse Cell



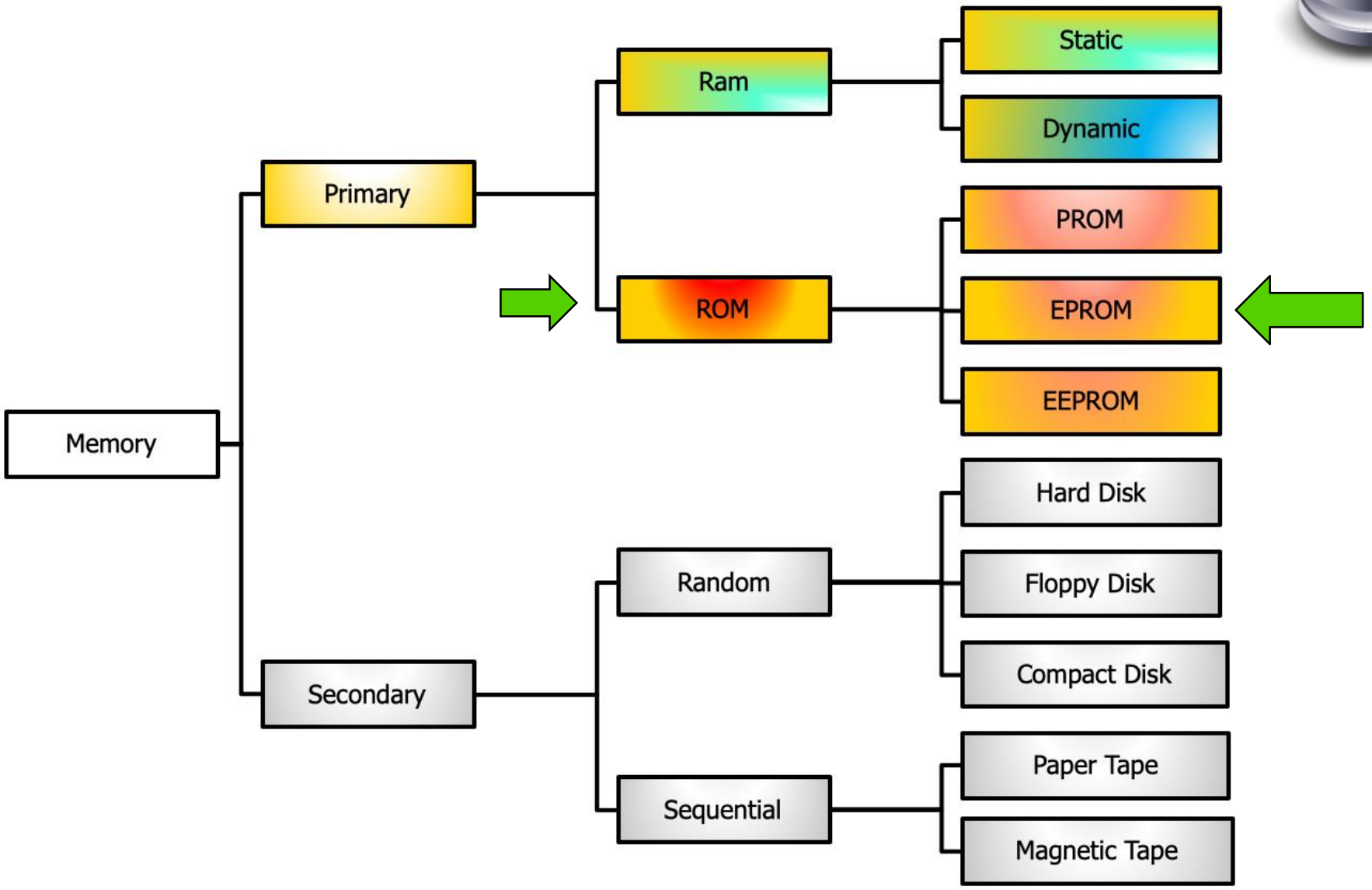
PROM : Fuse Cell



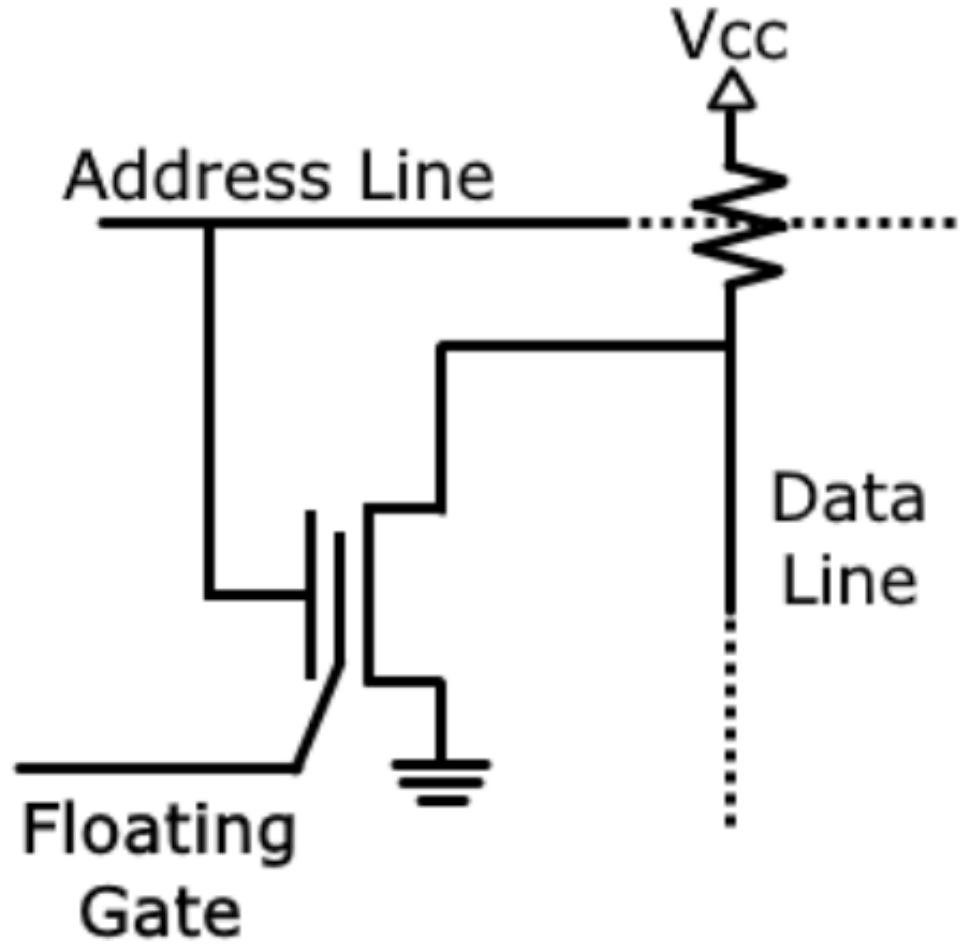
PROM : Fuse Cell



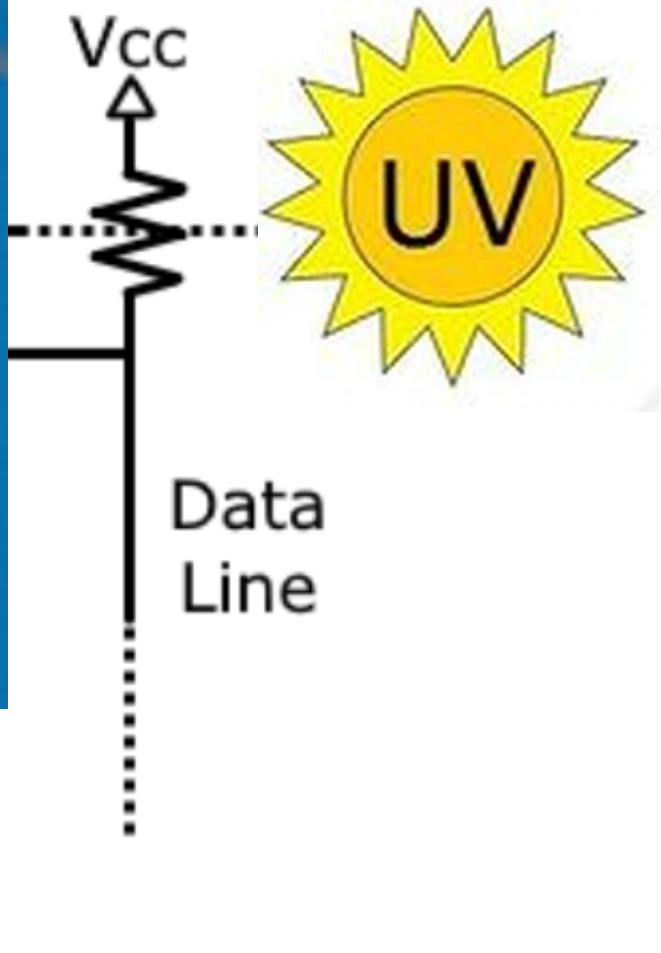
Memory Types



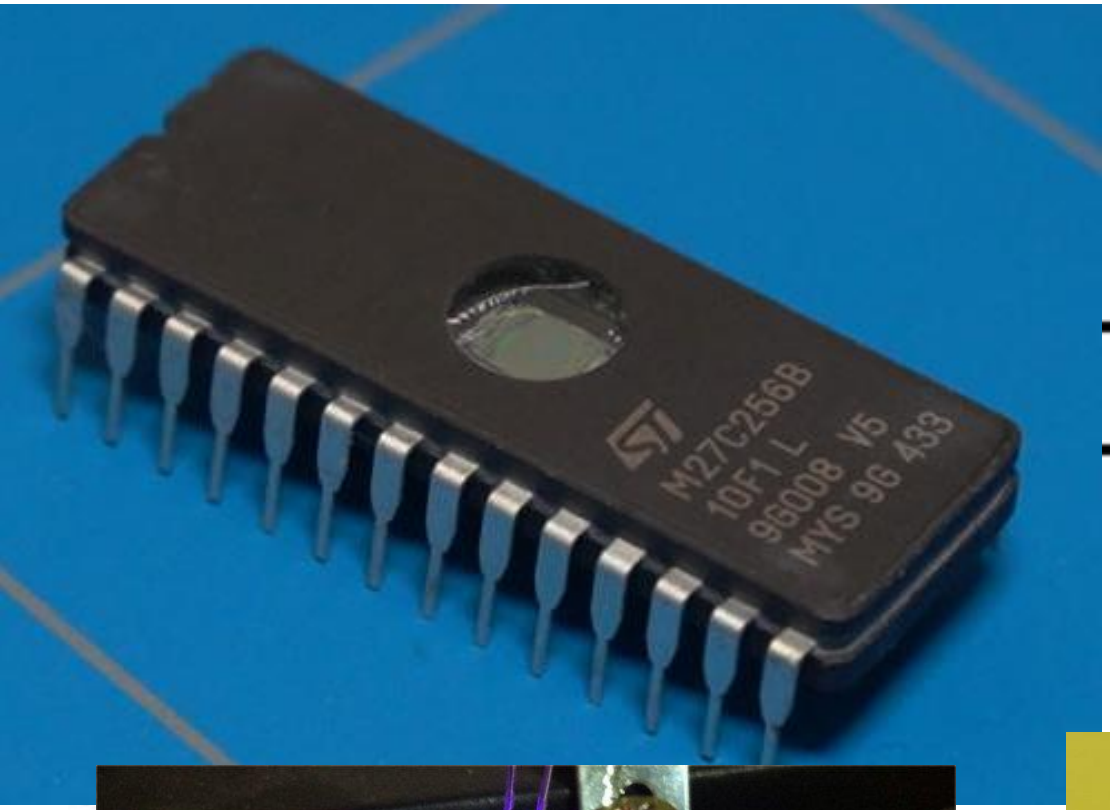
EPROM
(Erasable Programmable Read-Only Memory)

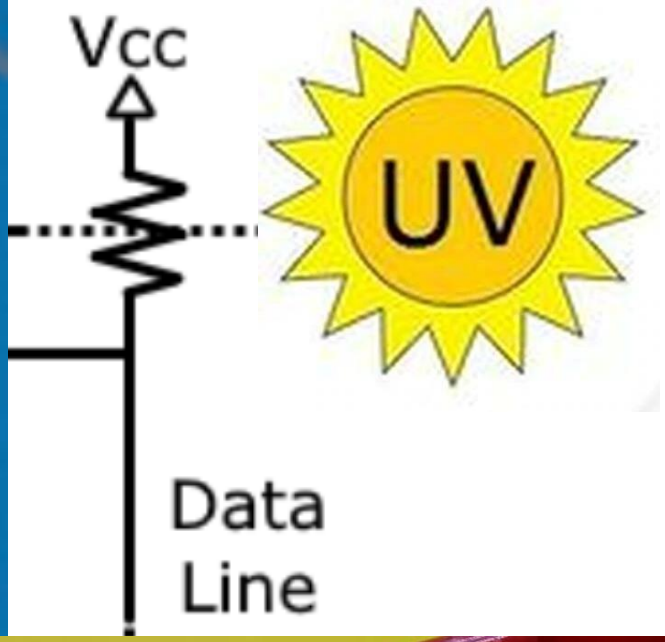


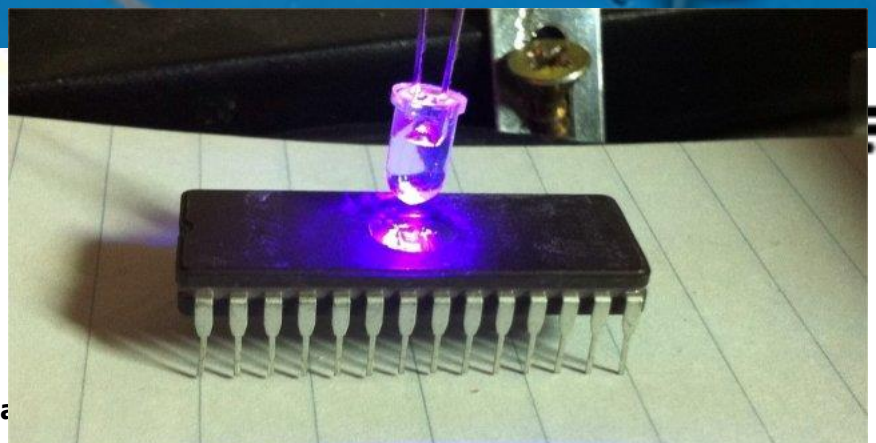
EPROM
(Erasable Programmable Read-Only Memory)

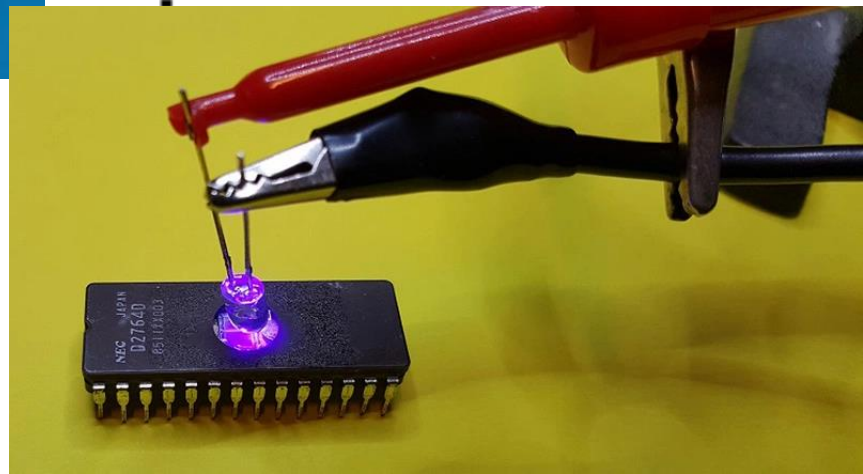


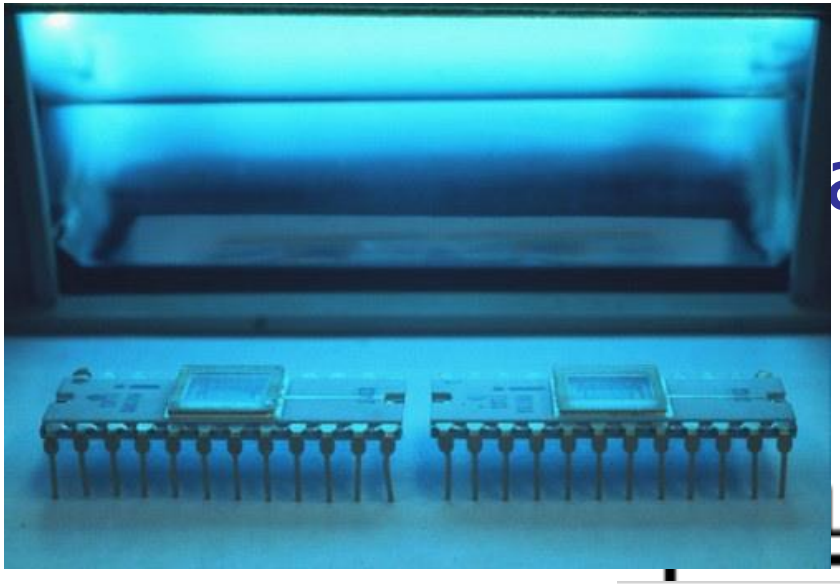
EPROM
(Erasable Programmable Read-Only Memory)



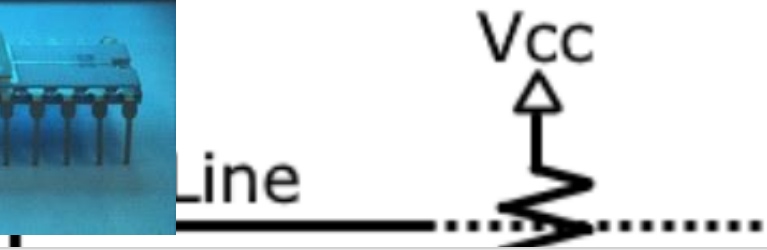


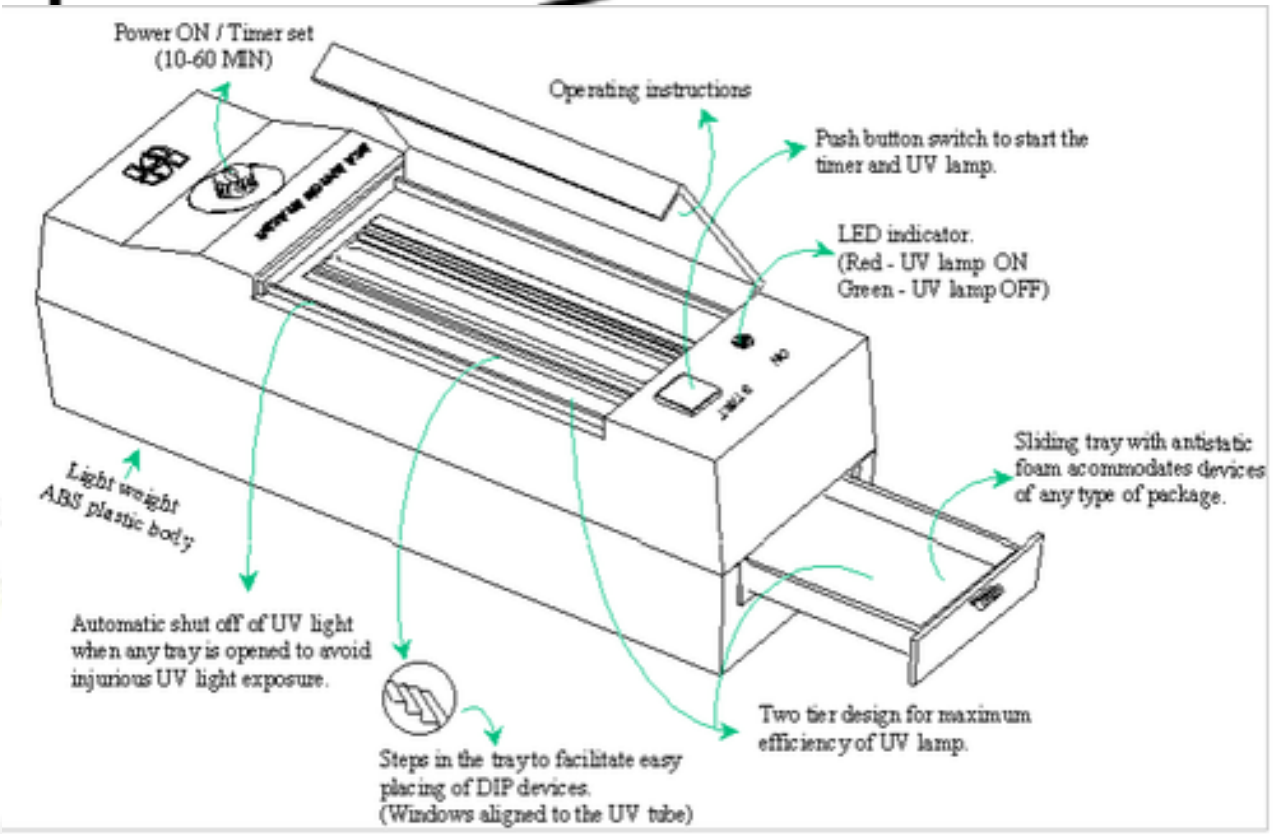






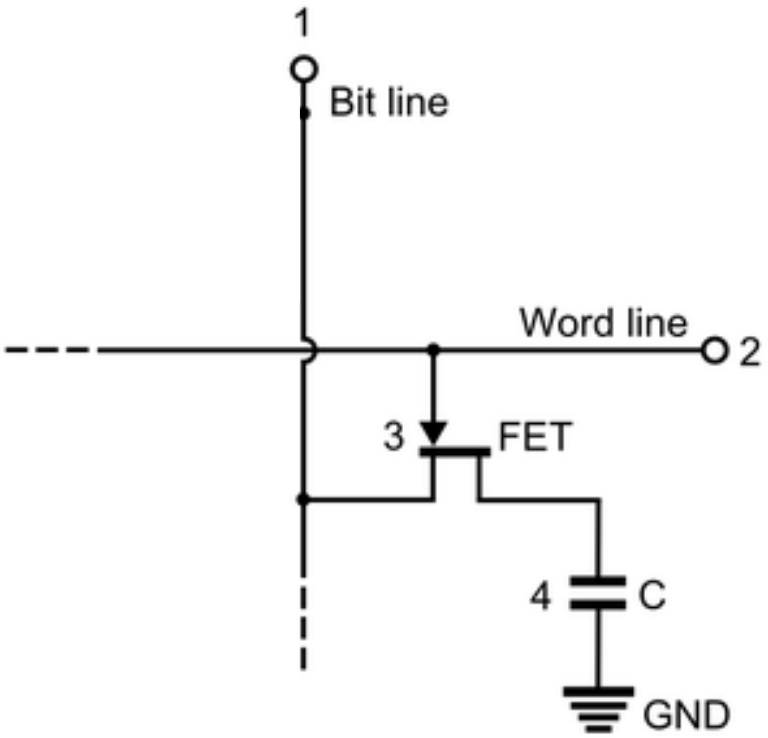
able Read-Only Memory)





Emmanuel

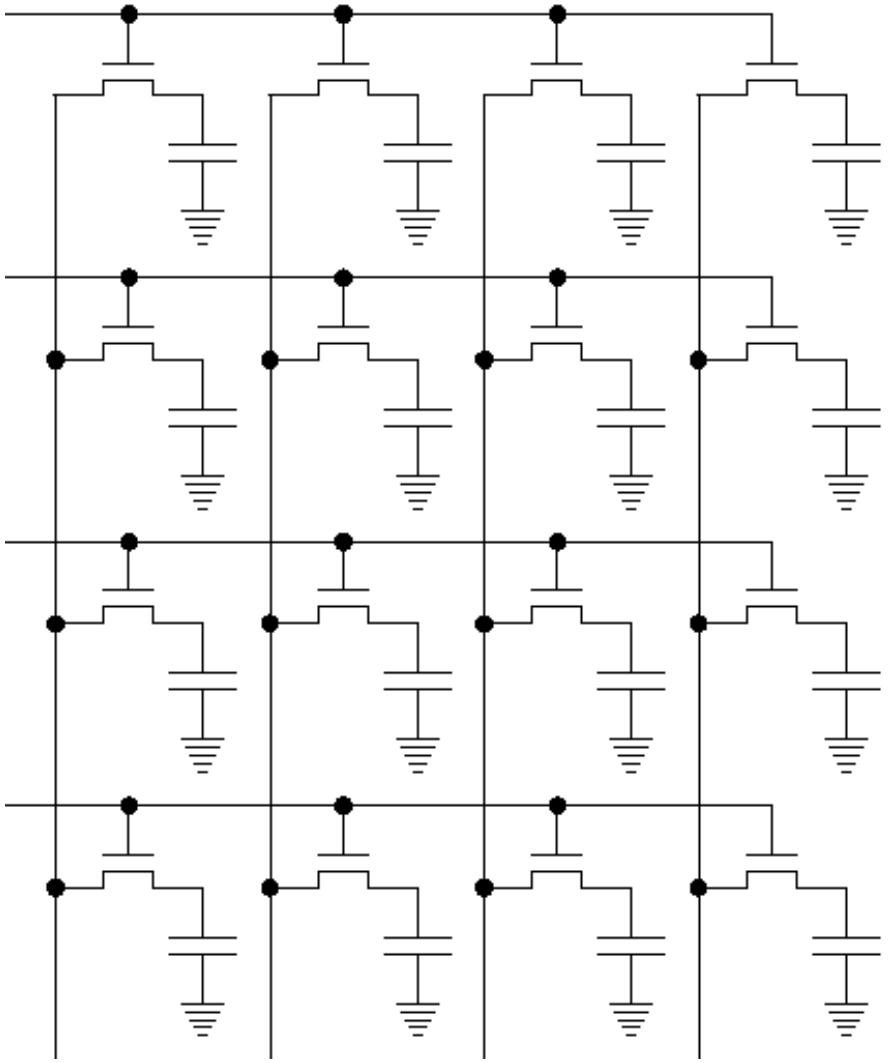
Memory Cells Address



FET : Field-Effect Transistor

https://en.wikipedia.org/wiki/Dynamic_random-access_memory

Memory Cells and words



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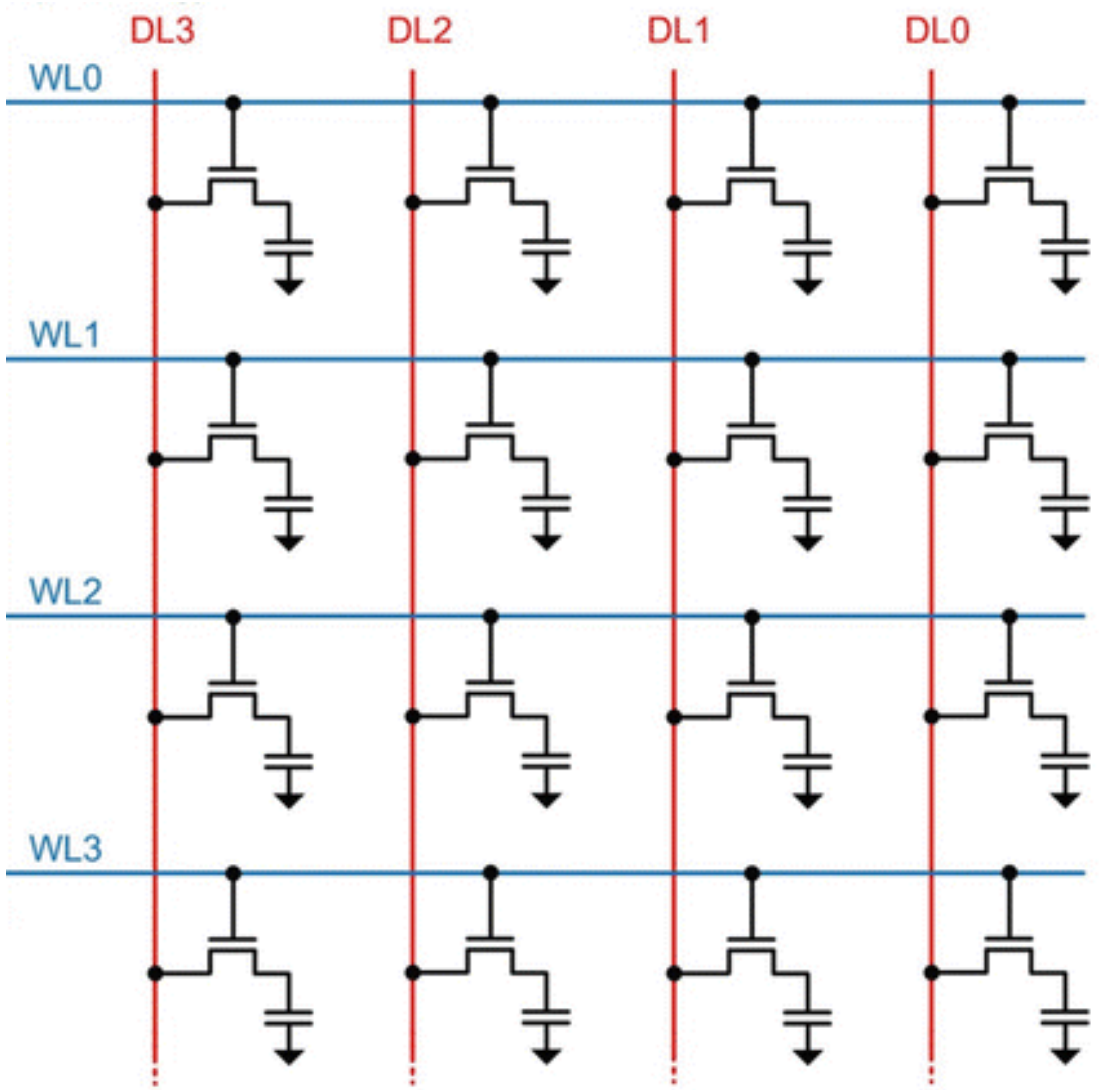
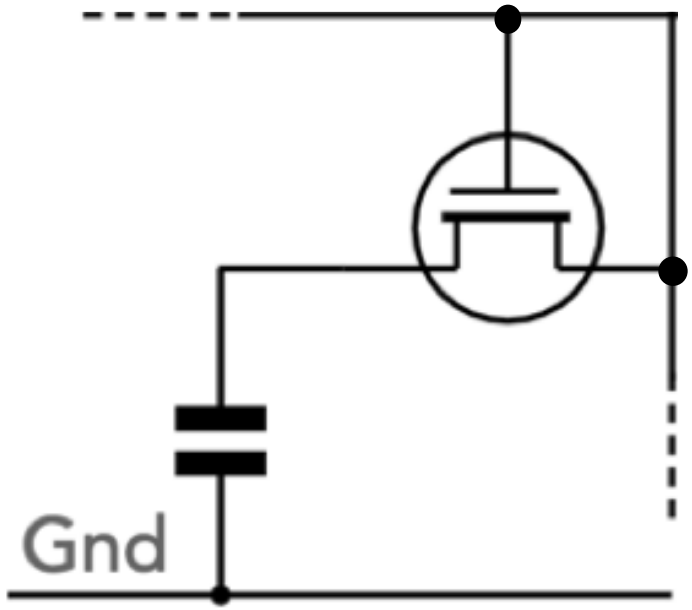
Memory Cells and words



Memory Cell Address



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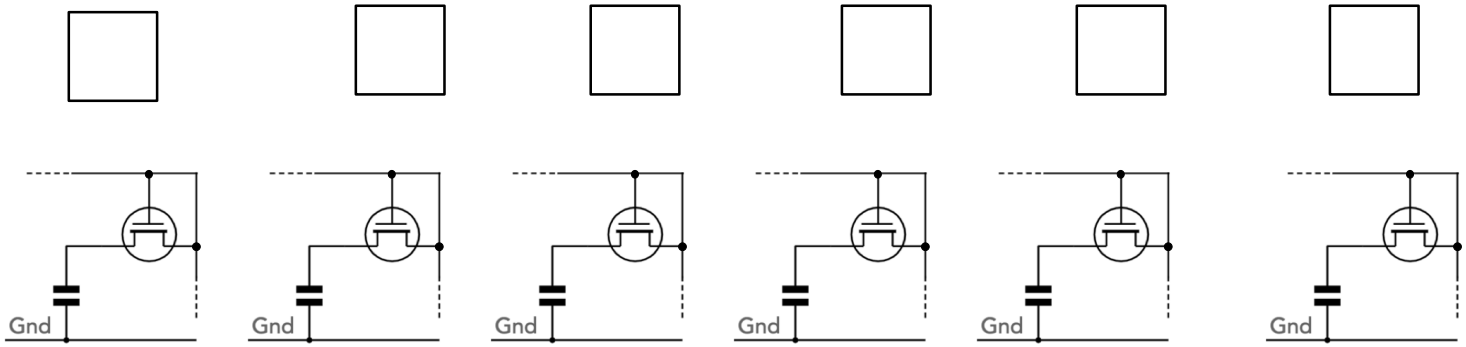

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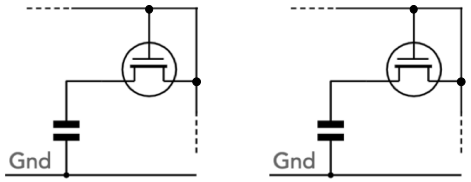

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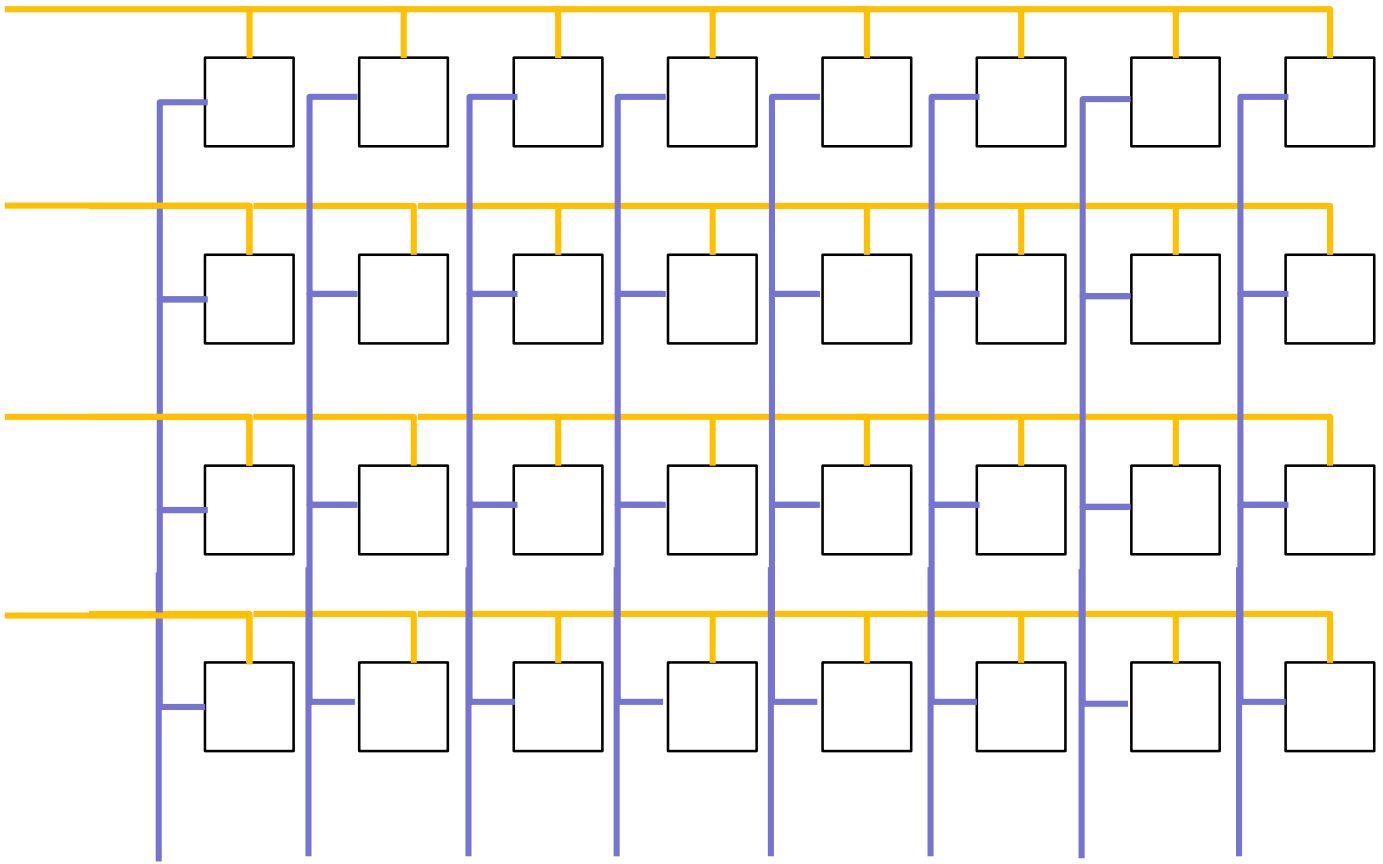

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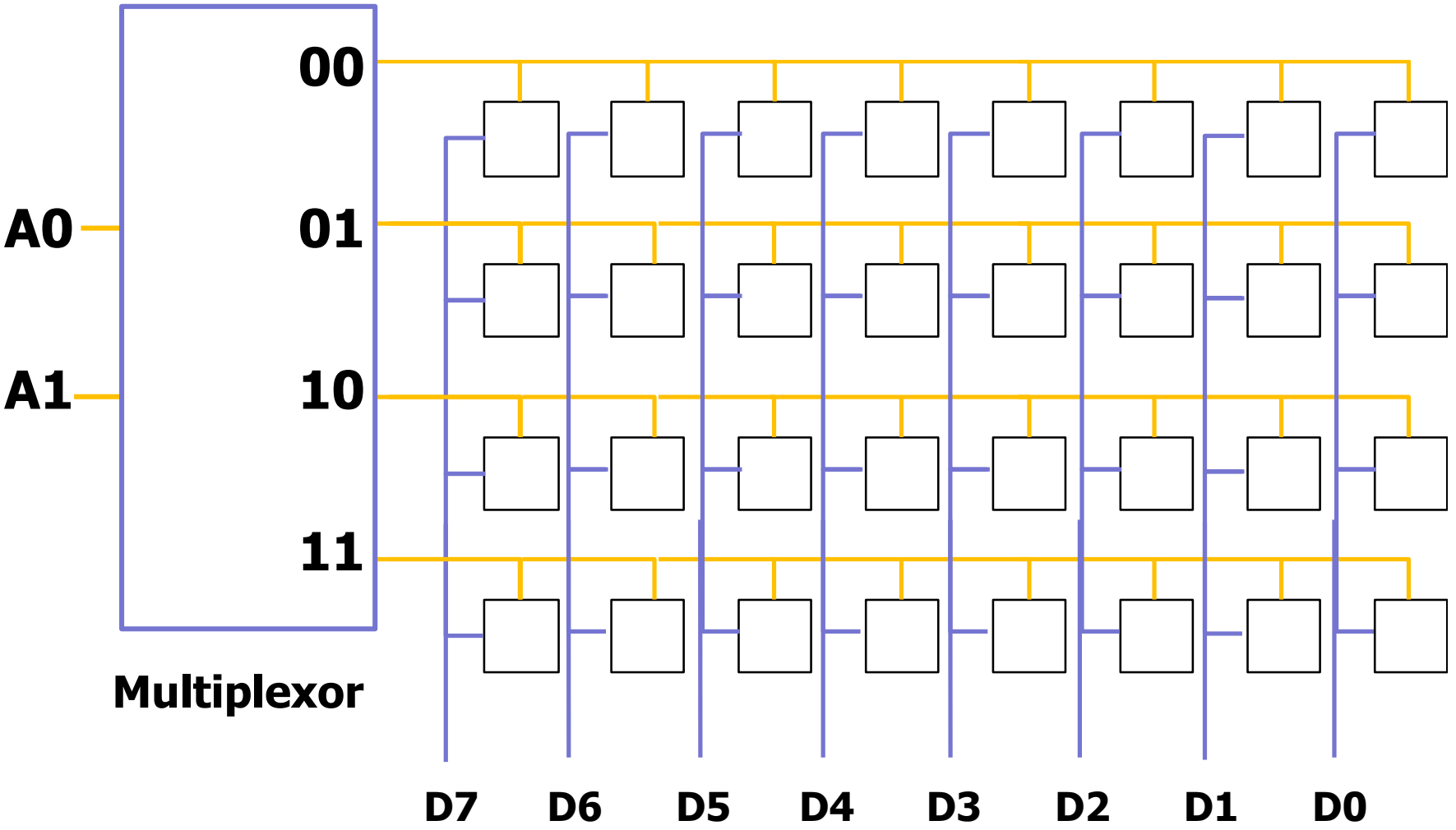
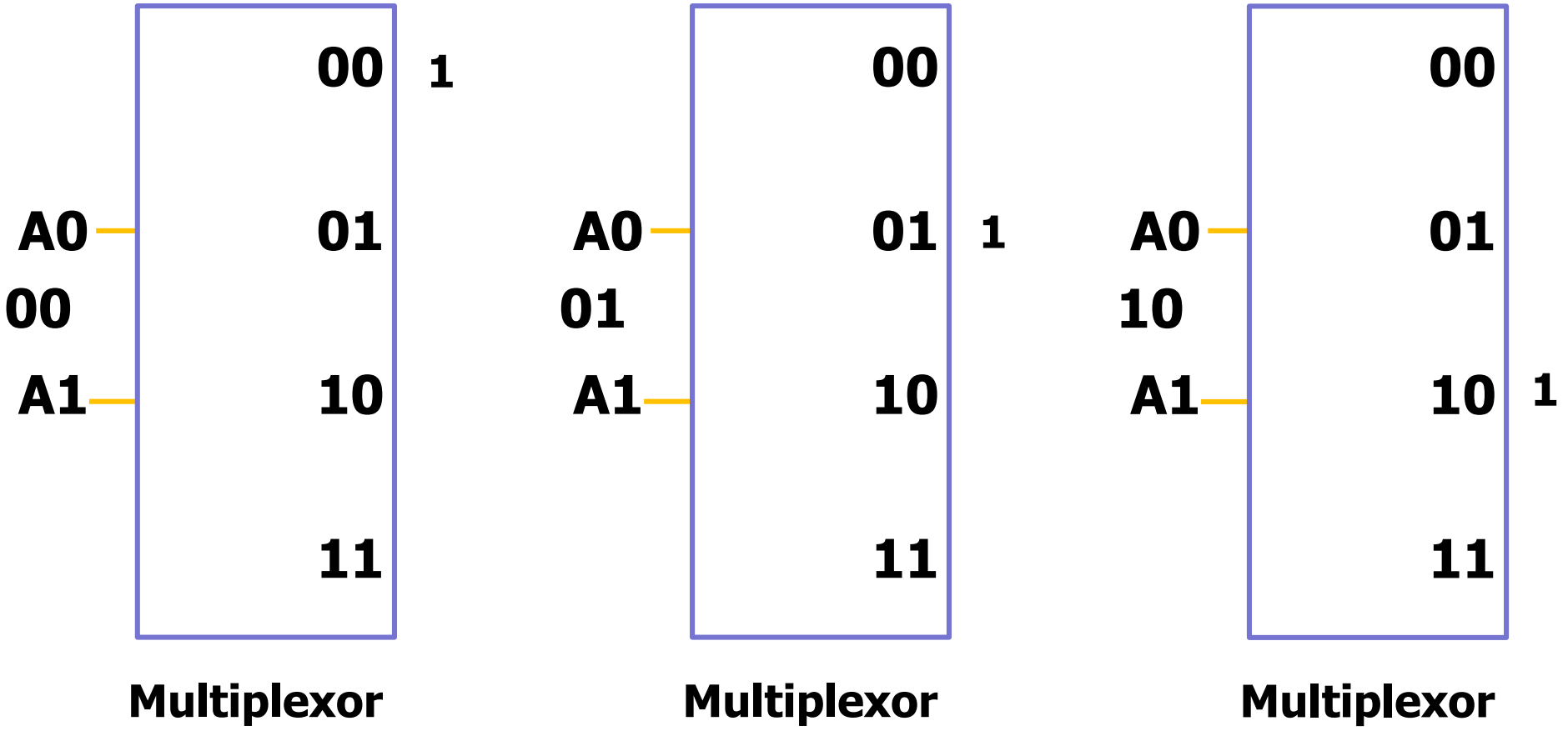
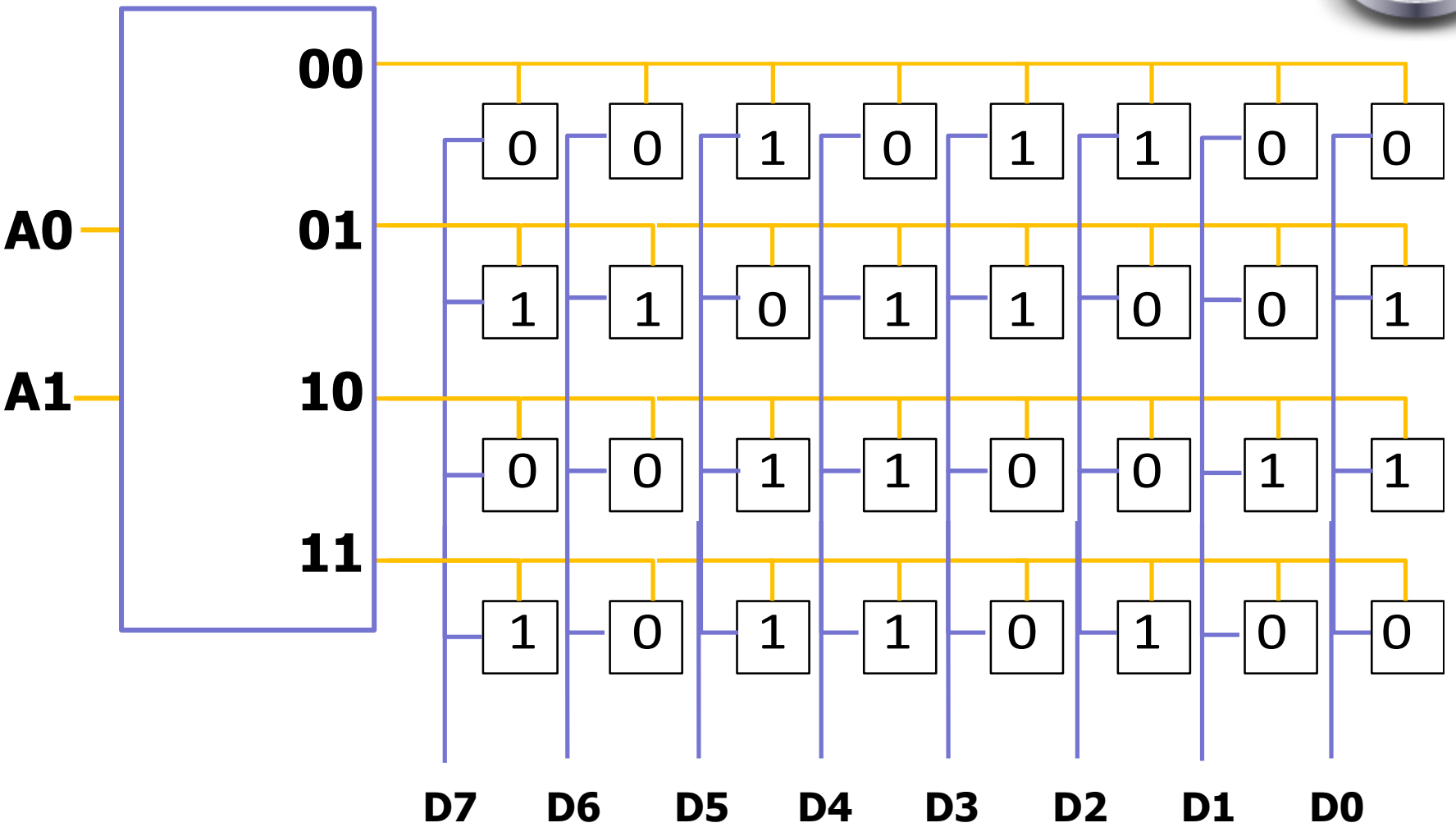


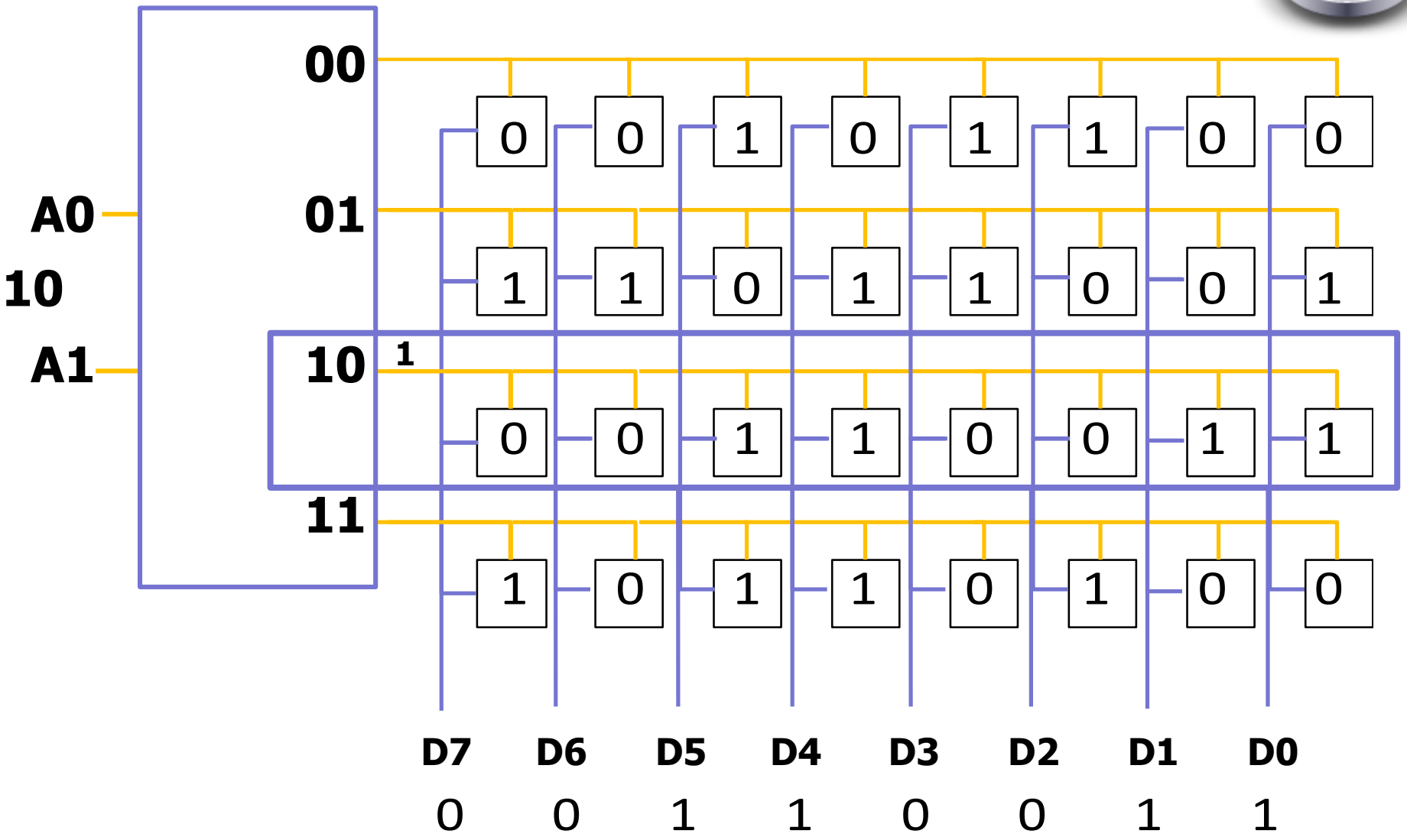
Memory Address : Multiplexor



Memory Address



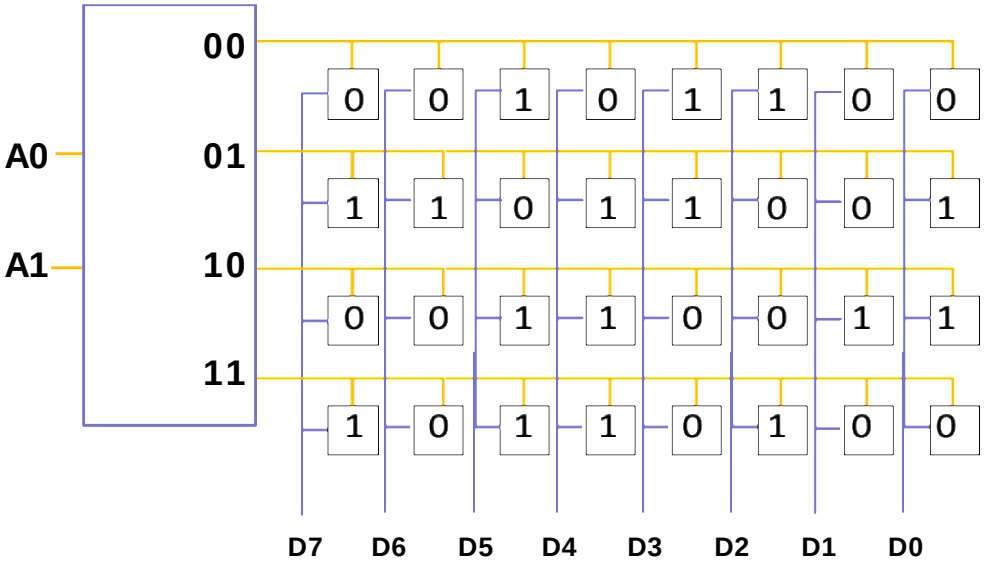
Memory Address



Memory Address

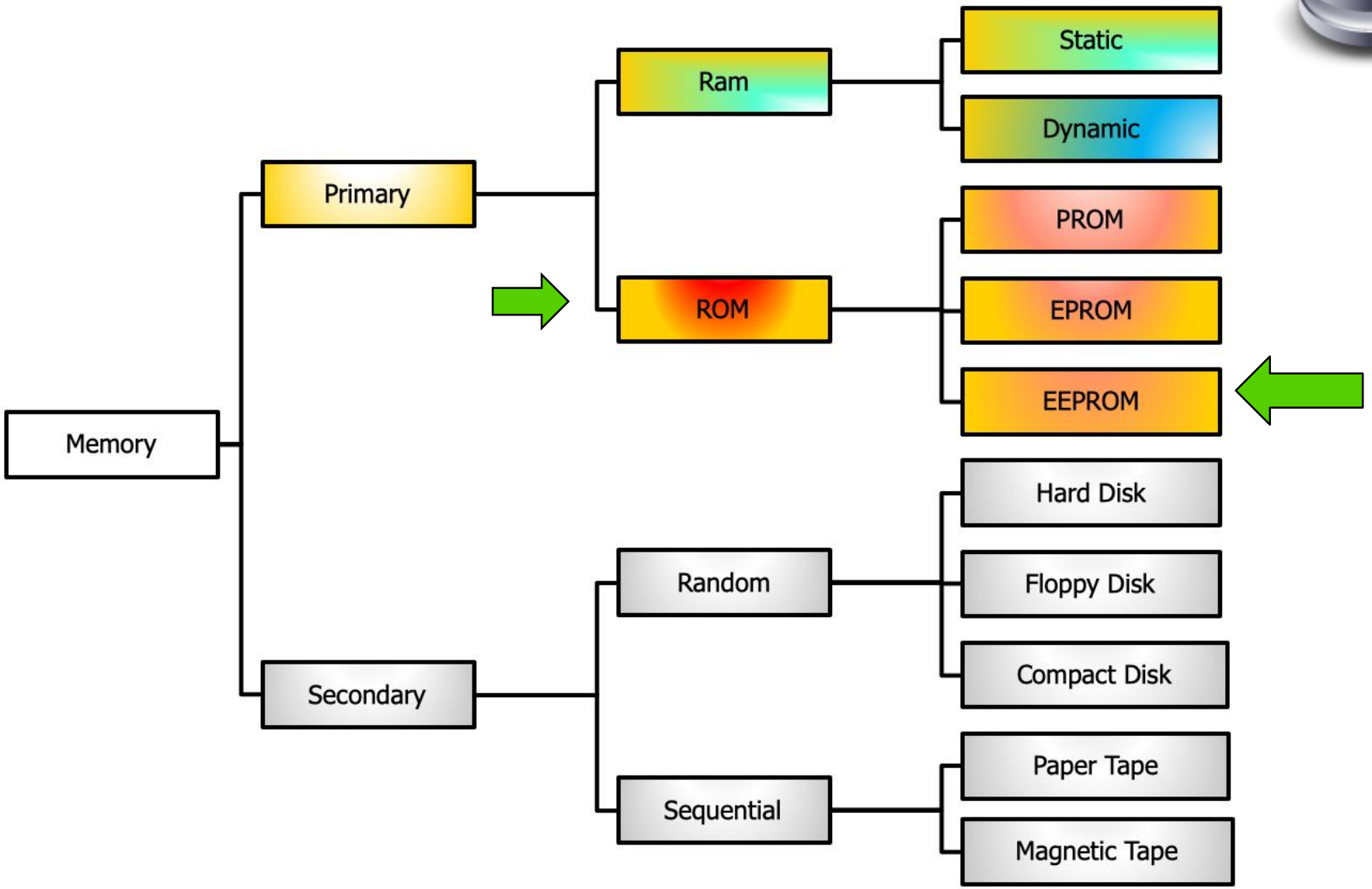
	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	1	0	1	1	0	0
01	1	1	0	1	1	0	0	1
11	0	0	1	1	0	0	1	1
10	1	0	1	1	0	1	0	0

Memory Address

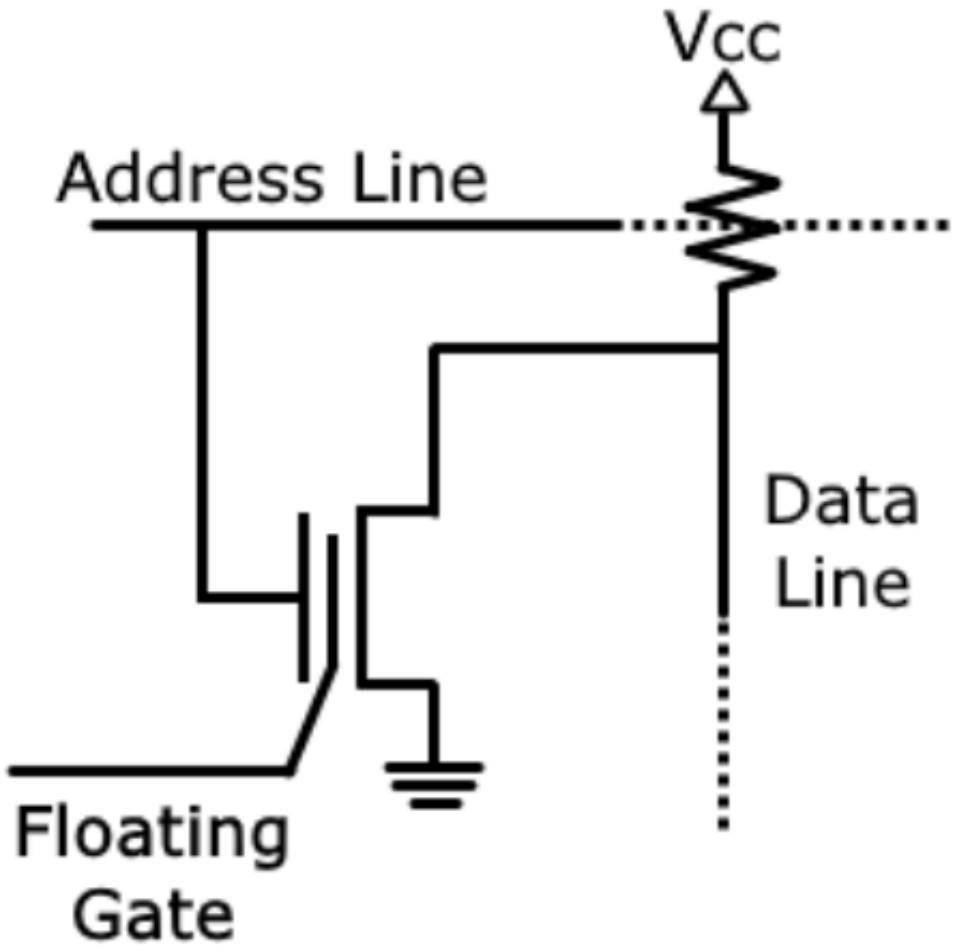


	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	1	0	1	1	0	0
01	1	1	0	1	1	0	0	1
11	0	0	1	1	0	0	1	1
10	1	0	1	1	0	1	0	0

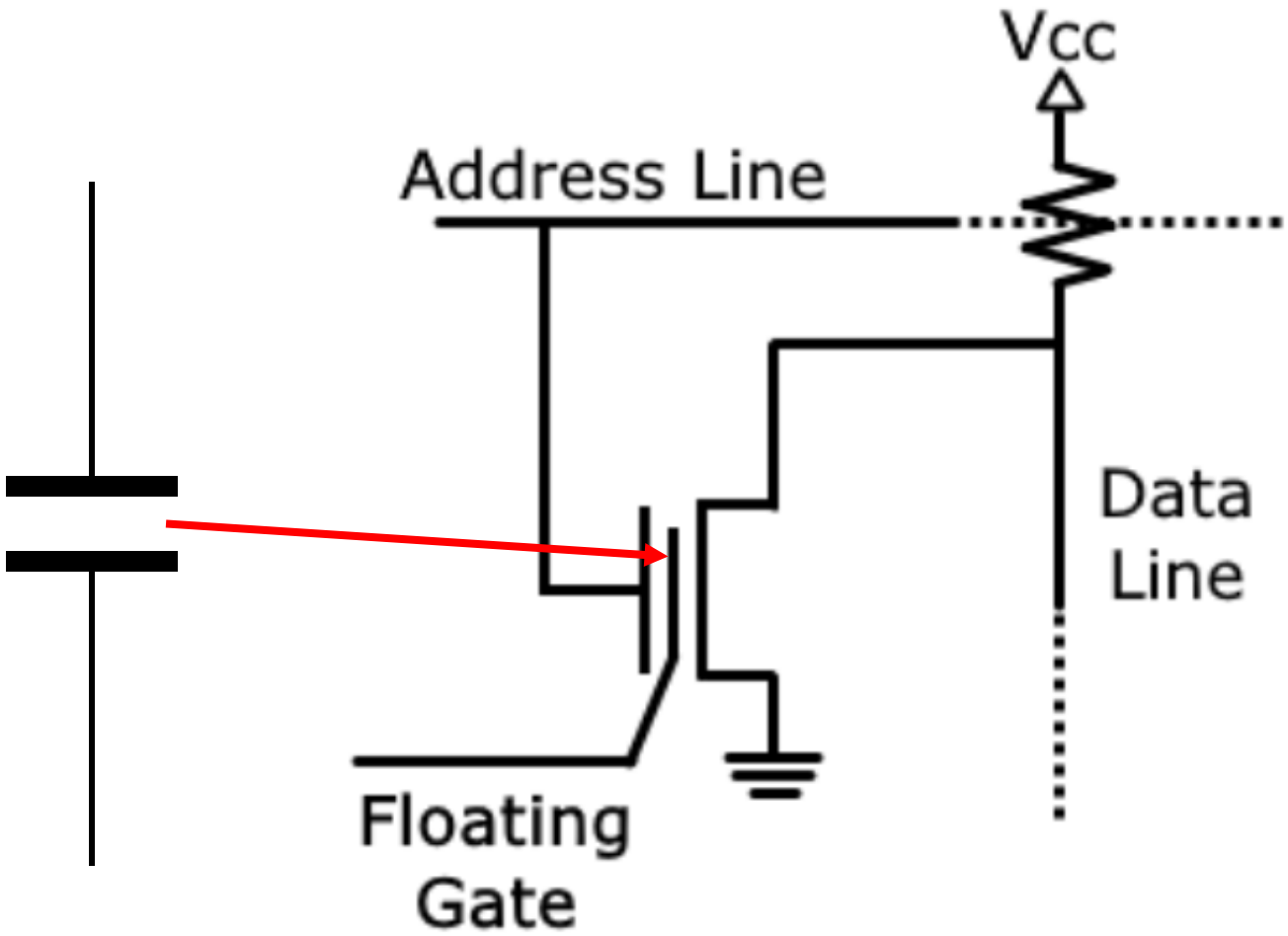
Memory Types



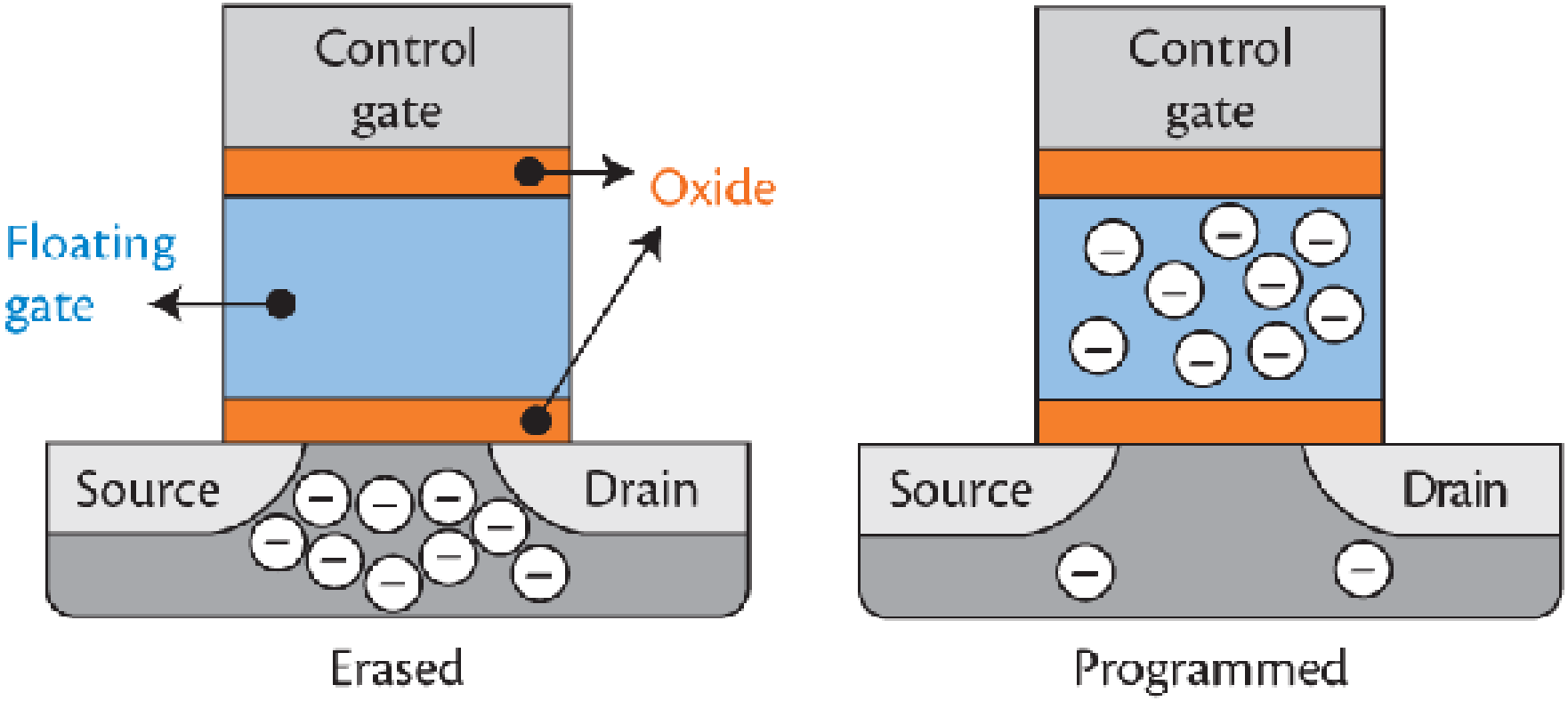
EEPROM
(Electrically Erasable Programmable Read-Only Memory)



EEPROM
(Electrically Erasable Programmable Read-Only Memory)



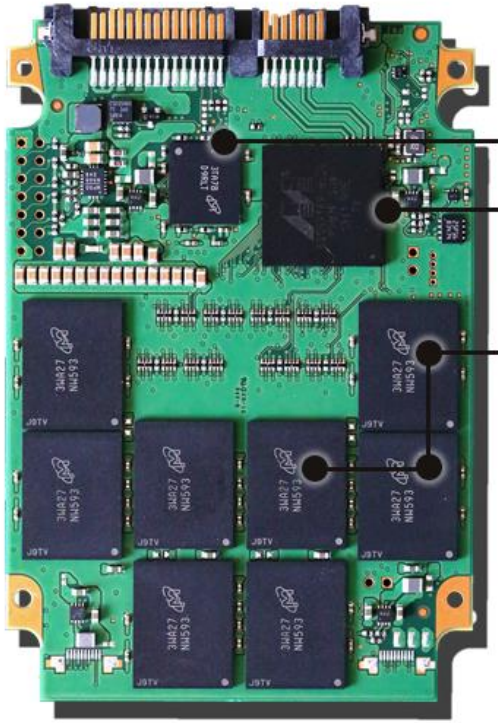
Floating gate



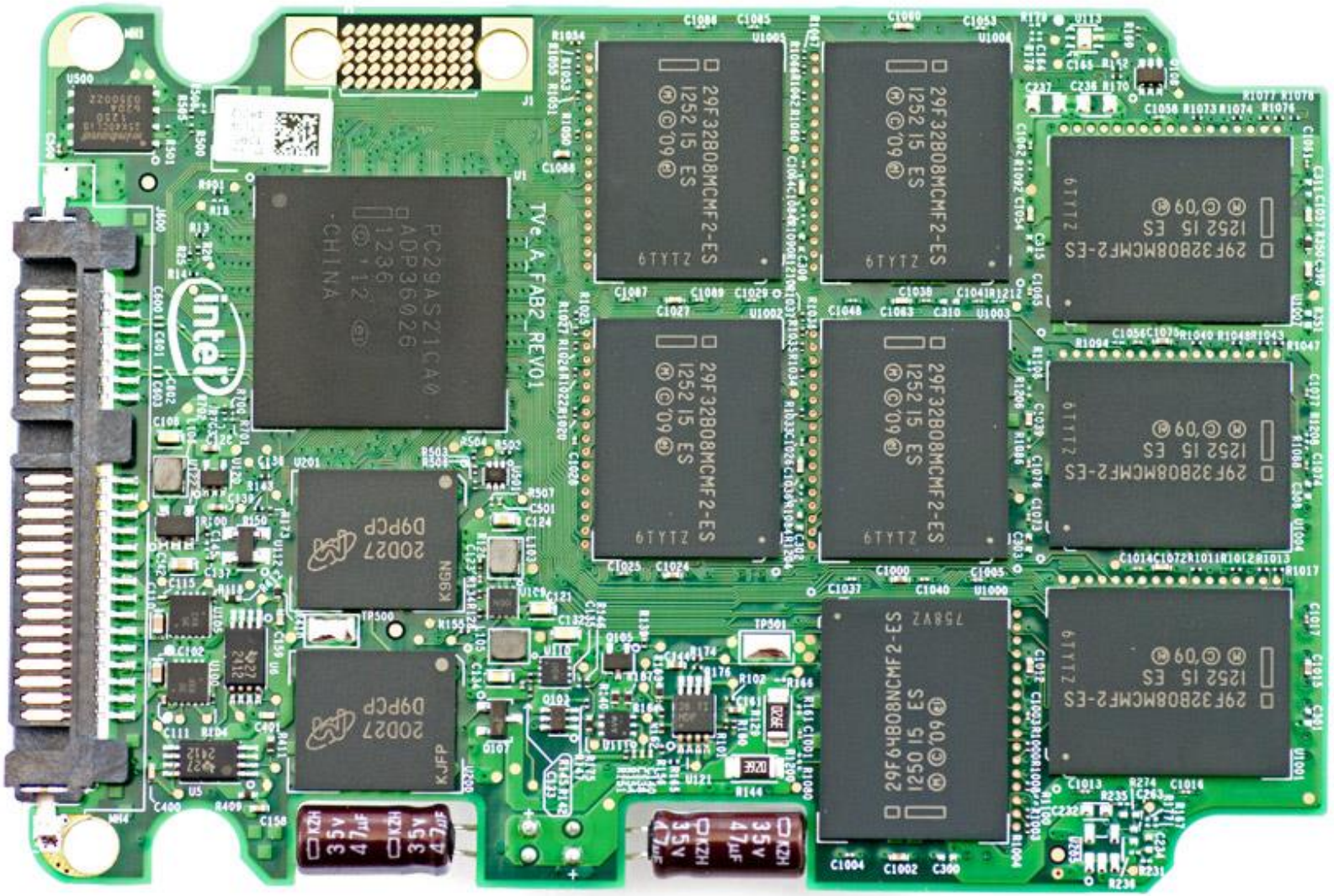
SSD

HDD
3.5″

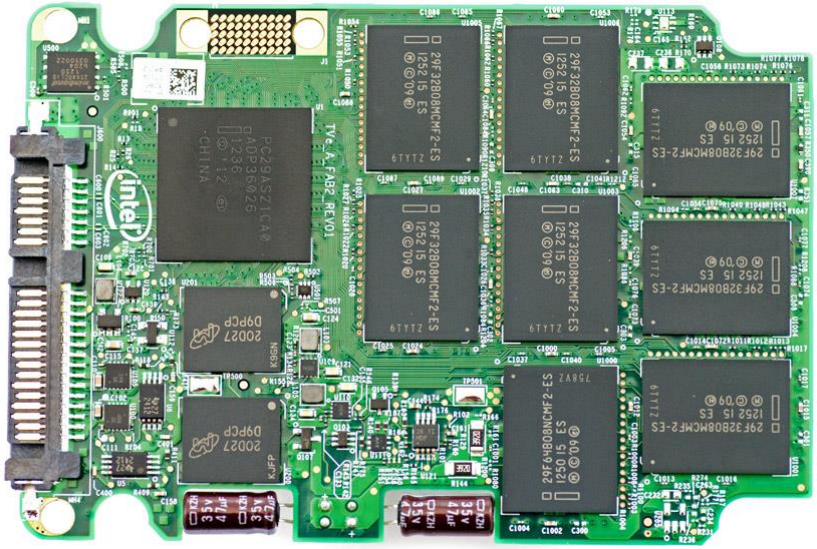
SSD
2.5″

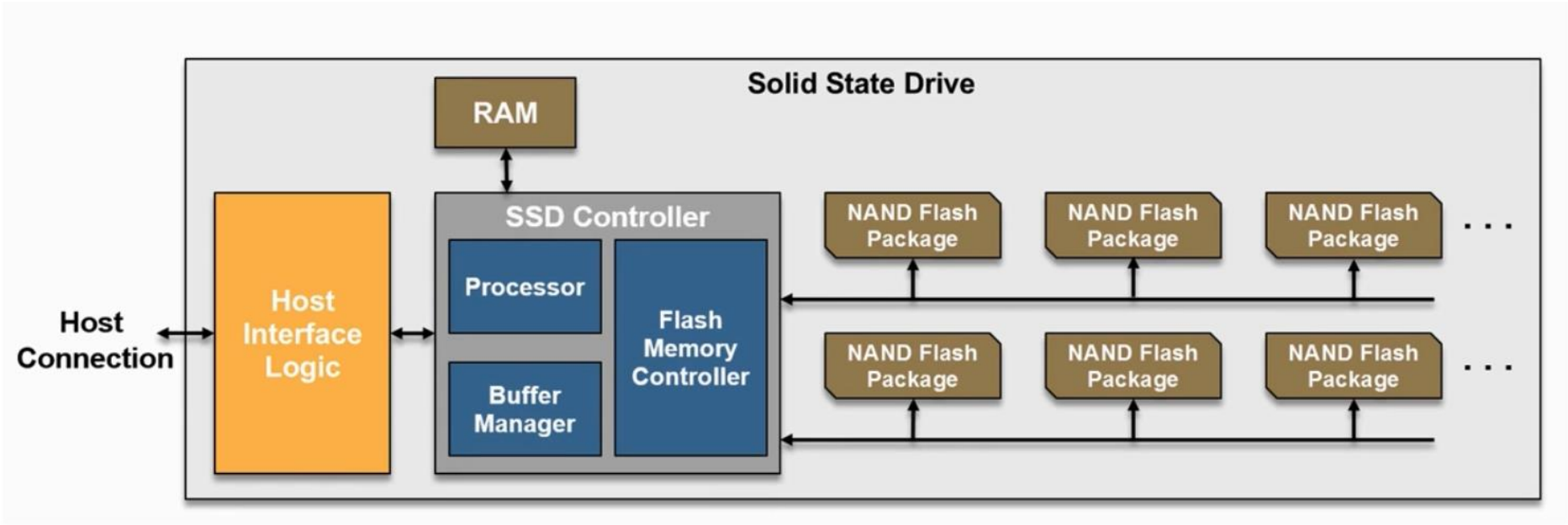


SSD


29F32B08MCMF2-ES
I252 15 ES
6TYTZ
TVc_A_FAB2_REV01
intel
20027
D9PCP
K9GN
KJFP

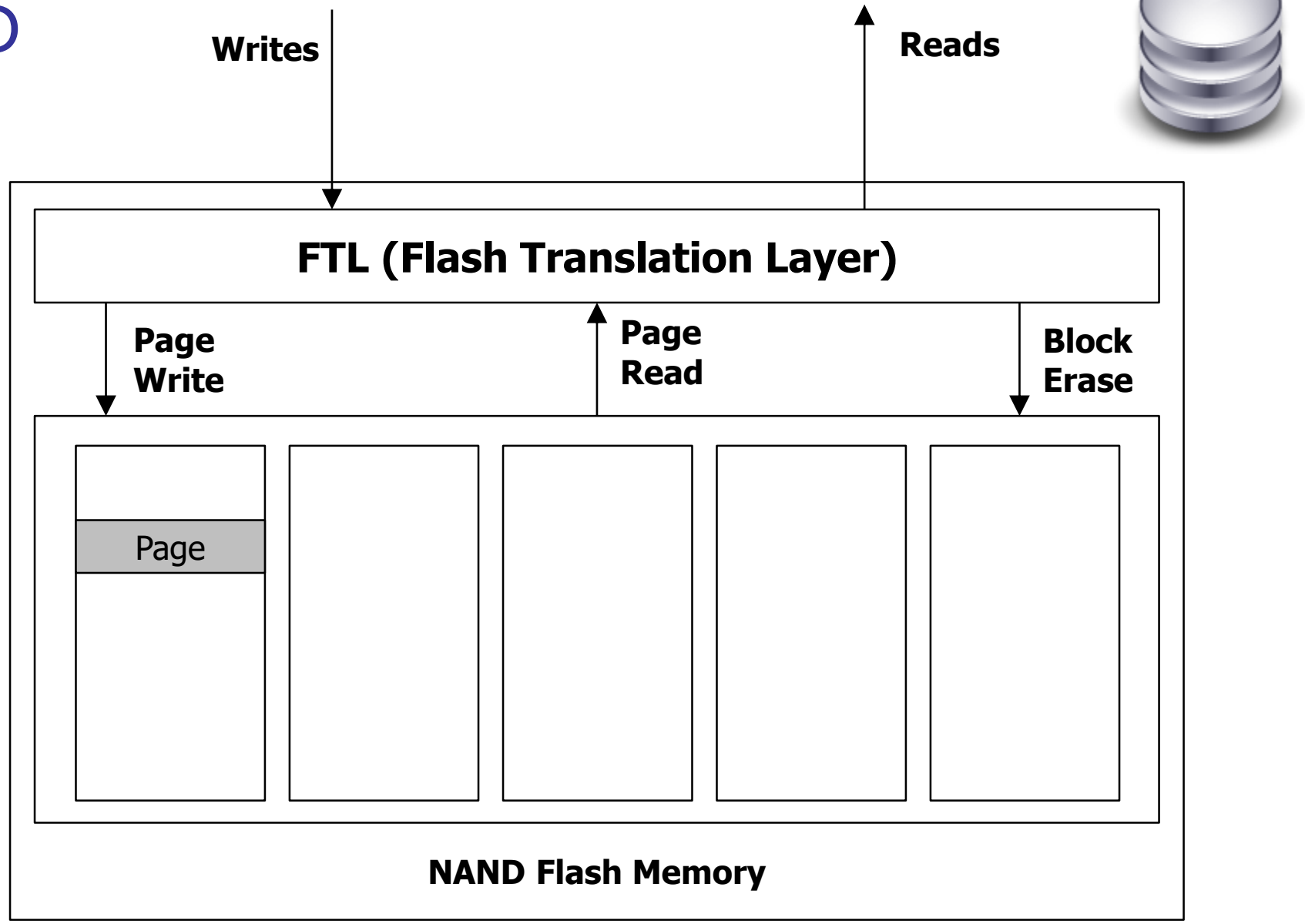
SSD





https://c4cloudguru.wordpress.com/2-6-solid-state-drive-part-1/

SSD


Writes
Reads
FTL (Flash Translation Layer)
Page
Write
Page
Read
Block
Erase
Page
NAND Flash Memory

FTL (Flash Translation Layer)

- A software layer emulating standard block device interface Read/Write
- Features :
  - Sector mapping
  - Garbage collection
  - Bad block management
  - Wear-leveling
  - Error Correction Code (ECC)

FTL : Wear Leveling

- Due to its architecture, data can be written to an address on a NAND flash memory only a finite number of times.
- NAND flash memory wears out if data is written too often to the same address, so wear leveling is used to help prolong the life of the NAND flash device.
- It ensures that data erasures and writes are distributed evenly across the NAND Flash storage medium, so that NAND memory blocks don't fail prematurely due to a high number of erase cycles.

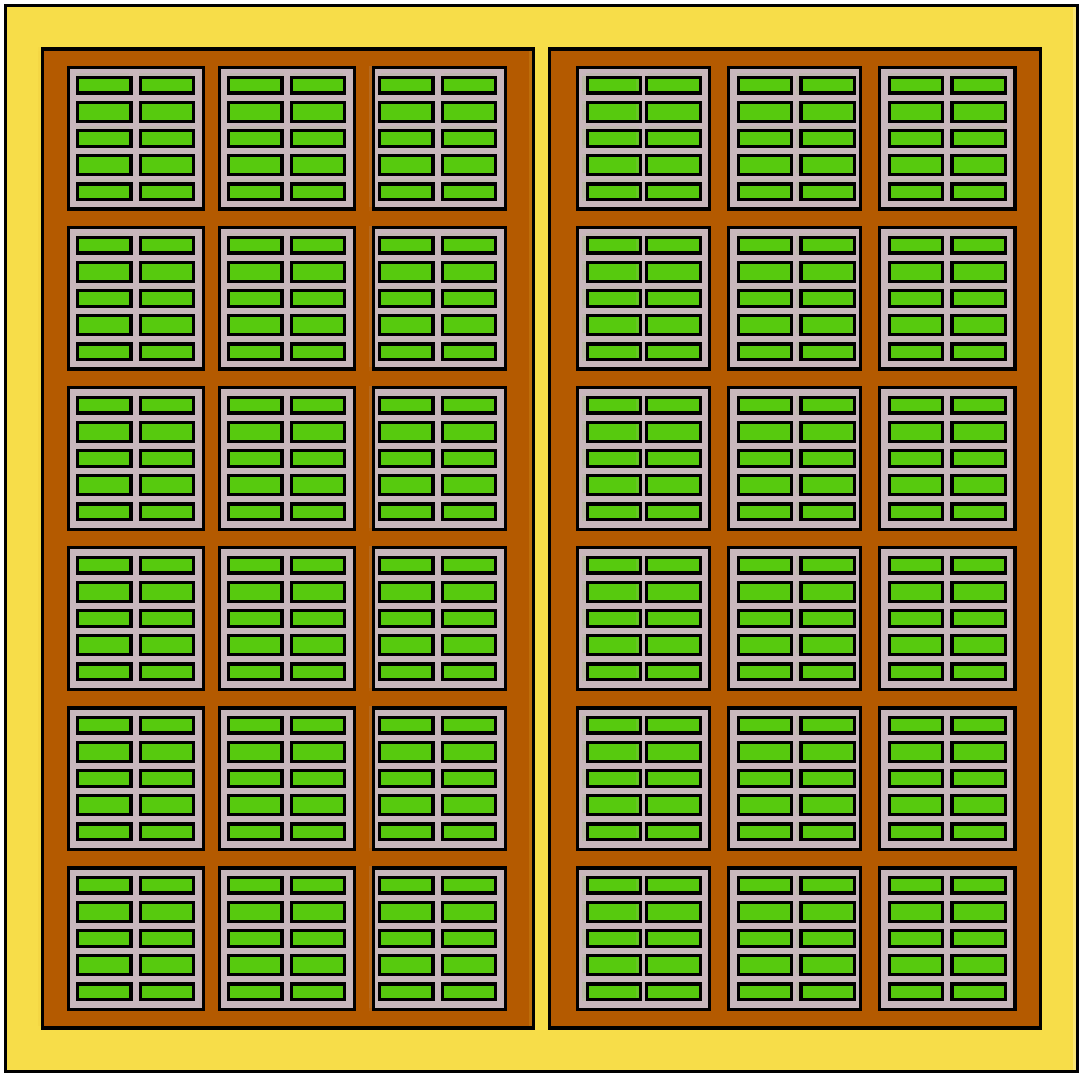
Page write operations and Block Erase

- Page write operations in a flash memory must be preceded by an erase operation and within a block, pages need be to written sequentially.
- The in-place update problem becomes complicated as write operations are performed in the page granularity, while erase operations are performed in the block granularity

Block Erase

- Groups of pages are called blocks.
- There are over 100 pages in each block.
- Because multiple pages are contained in each block, blocks can store a large amount of data.
- When it is necessary to erase part of the data stored in the NAND flash memory, it can only be erased by block.
- It is not possible to erase smaller or larger groups of data within a NAND flash die.

Flash Lay out



Die

Plane

Block

Page

https://flashdba.com/2014/06/20/understanding-flash-blocks-pages-and-program-erases/

Memory Types