西安电子科技大学

电子线路实验 II 课程实验报告

实验名称 大规模集成数字电路设计

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龚志豪 杨卓程

成 绩

实验日期 2021 年 11 月 21 日

指导教师评语: 指导教师: _____年____月____日
实验报告内容基本要求及参考格式 一、实验目的 二、实验所用仪器（或实验环境） 三、实验基本原理及步骤（或方案设计及理论计算） 四、实验数据记录（或仿真及软件设计） 五、实验结果分析及回答问题（或测试环境及测试结果）

实验七　定时报时数字钟

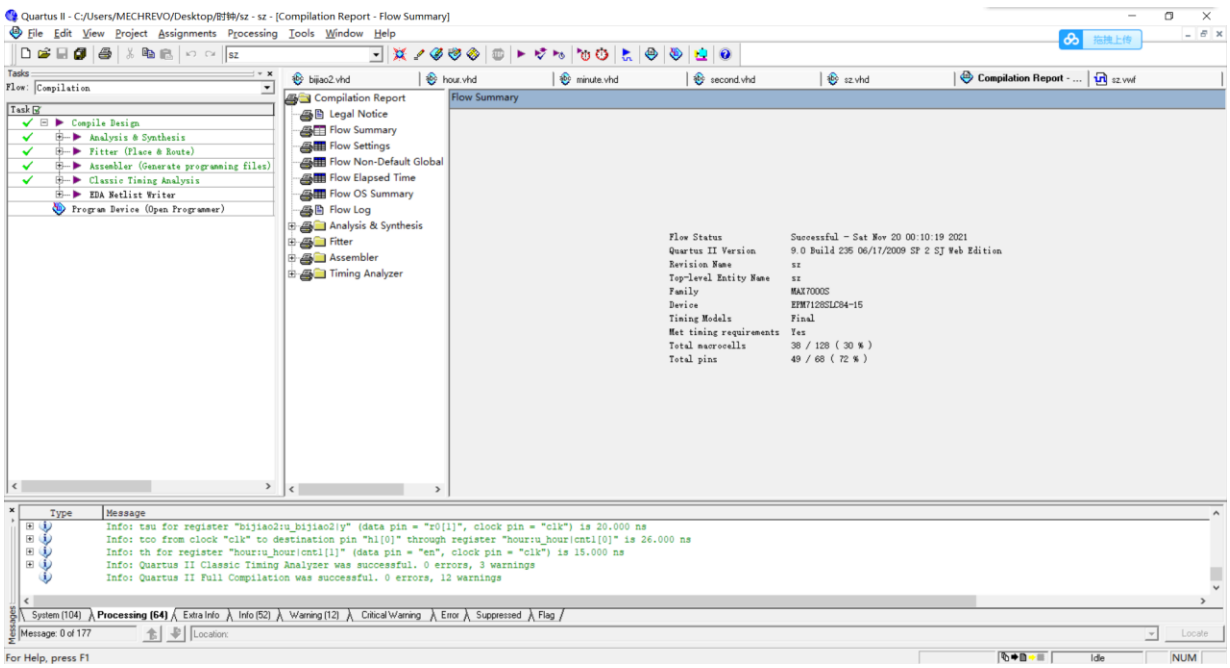
一，设计概述

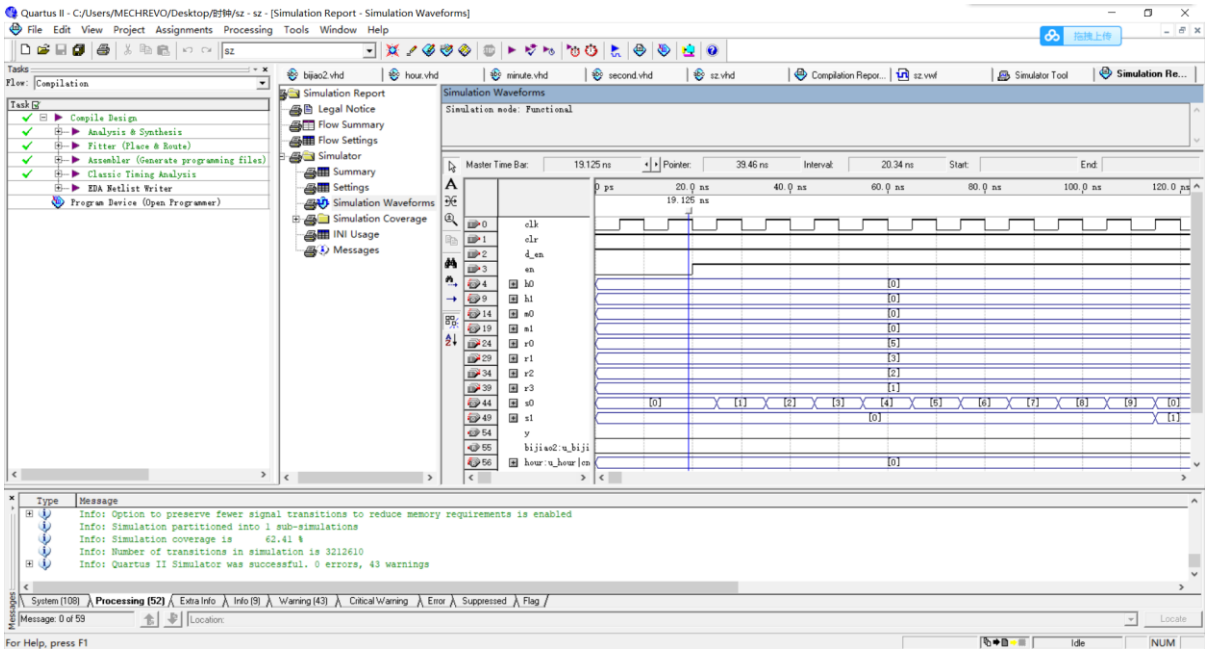
本设计是一个带有定时报时功能的数字钟，总的分为 4 个模块，时计数模块，分计数模块，秒计数模块以及定时模块。能够实现 0-24 小时下的任意时间显示以及定时提醒。

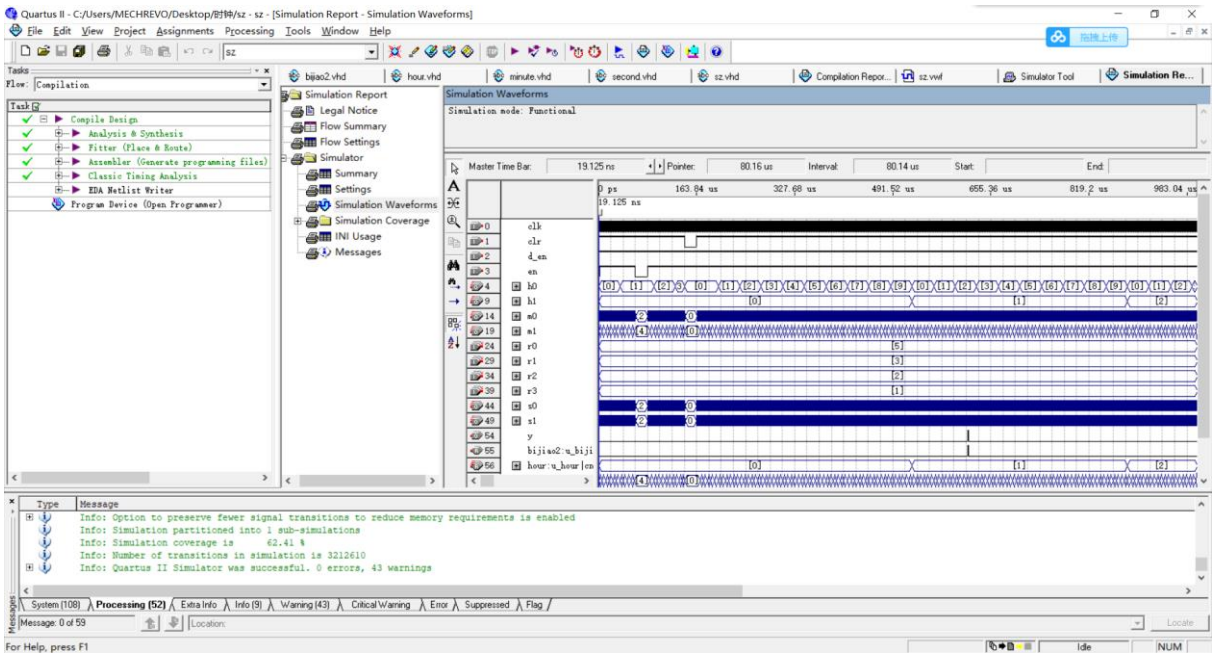
二，功能说明

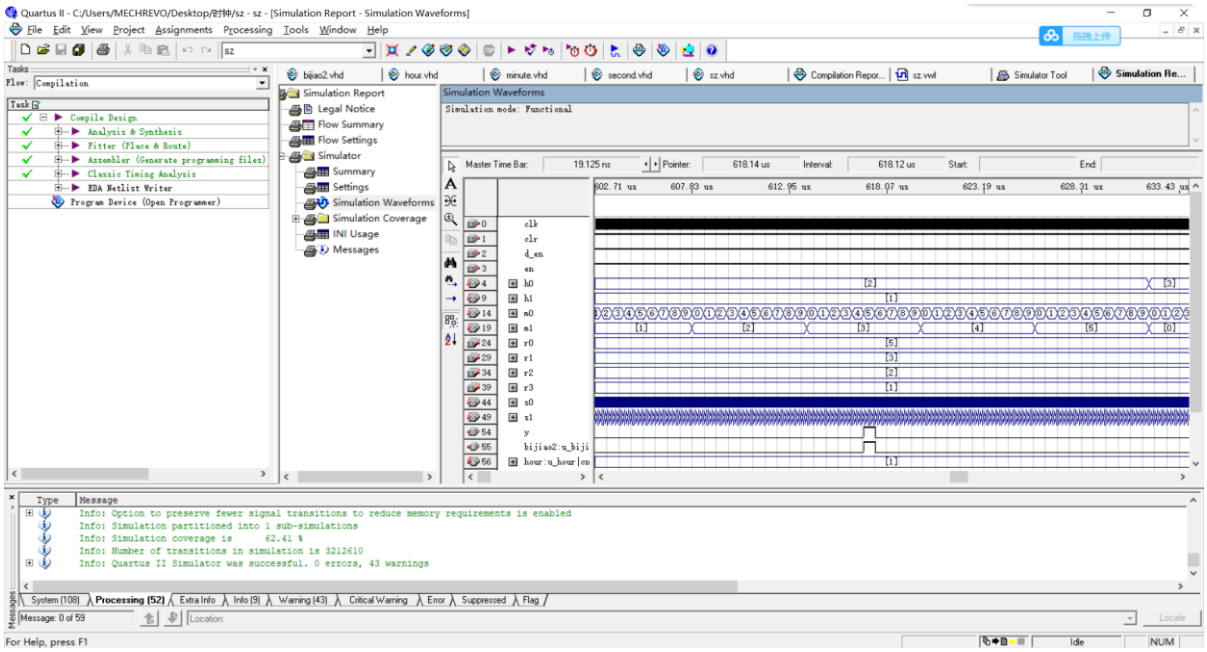
本设计功能说明如下：定时模块与秒计数模块使用同一个时钟 clr，分，时计数模块分别使用时钟 cs，cm。秒，分，时计数模块都采取两位显示，每次时钟上升沿来到时计数。秒计数模块低位逢 10 进 1，高位逢 6 进 1；分计数模块低位逢 10 进 1，高位逢 6 进 1；时计数模块低位逢 10 进 1，当高位为 2，低位为 4 时，进行清零。定时模块可以预设时间，每次时钟上升沿来到时逐位比较，当计数时间与预设时间相同时输出闹钟信号。

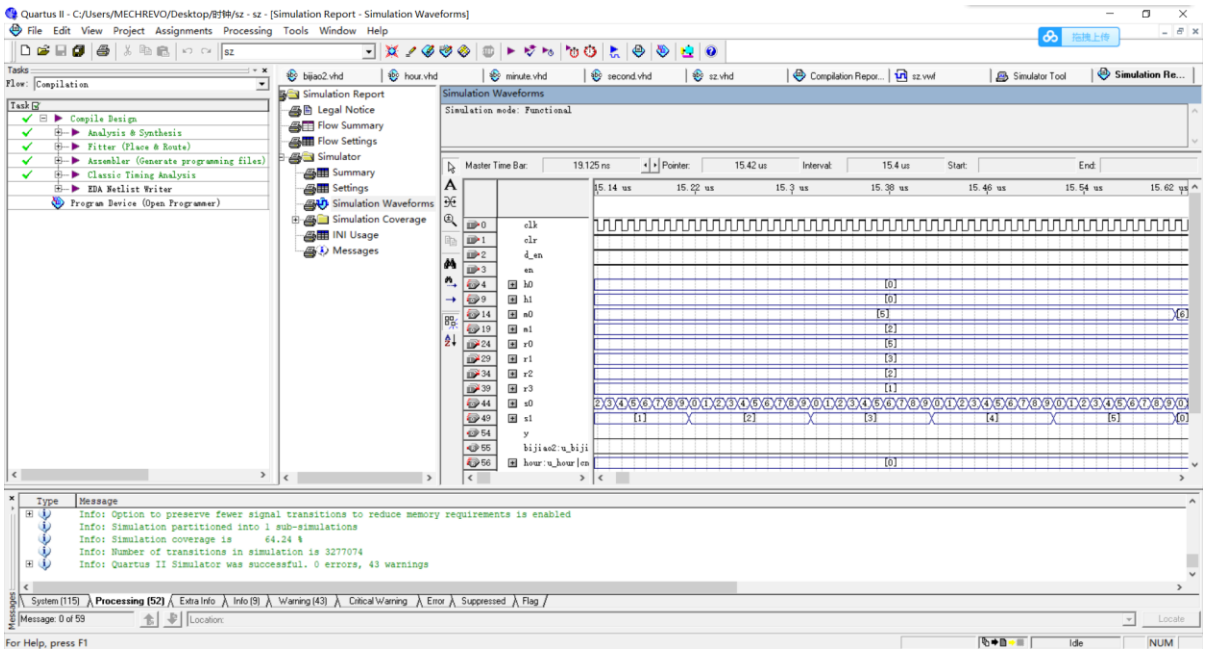
三，功能仿真

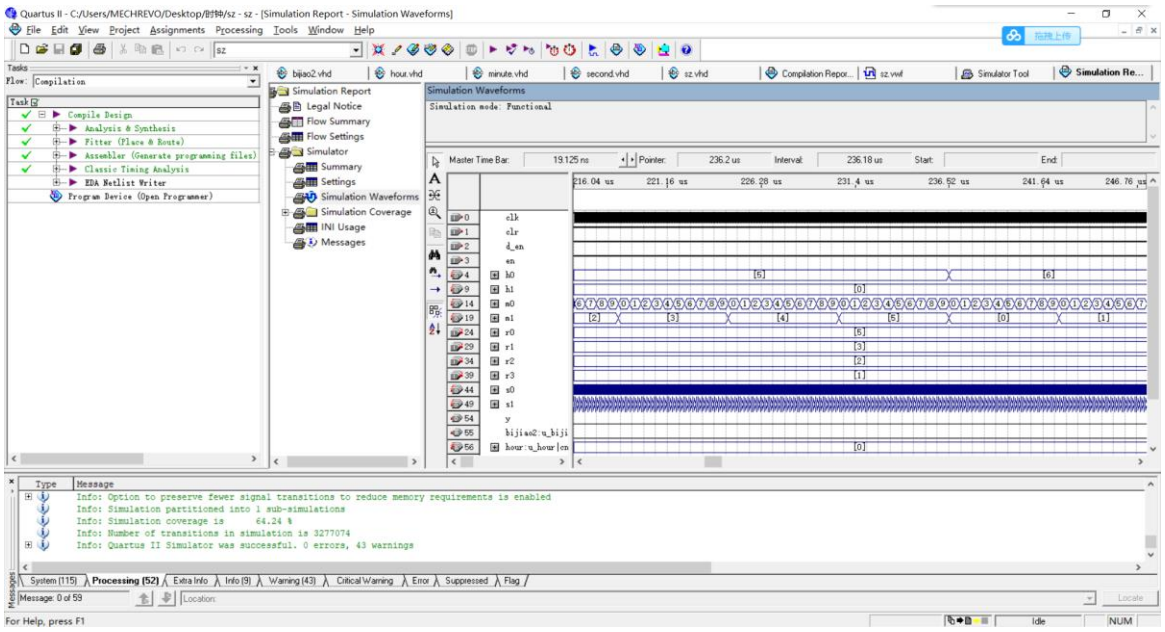


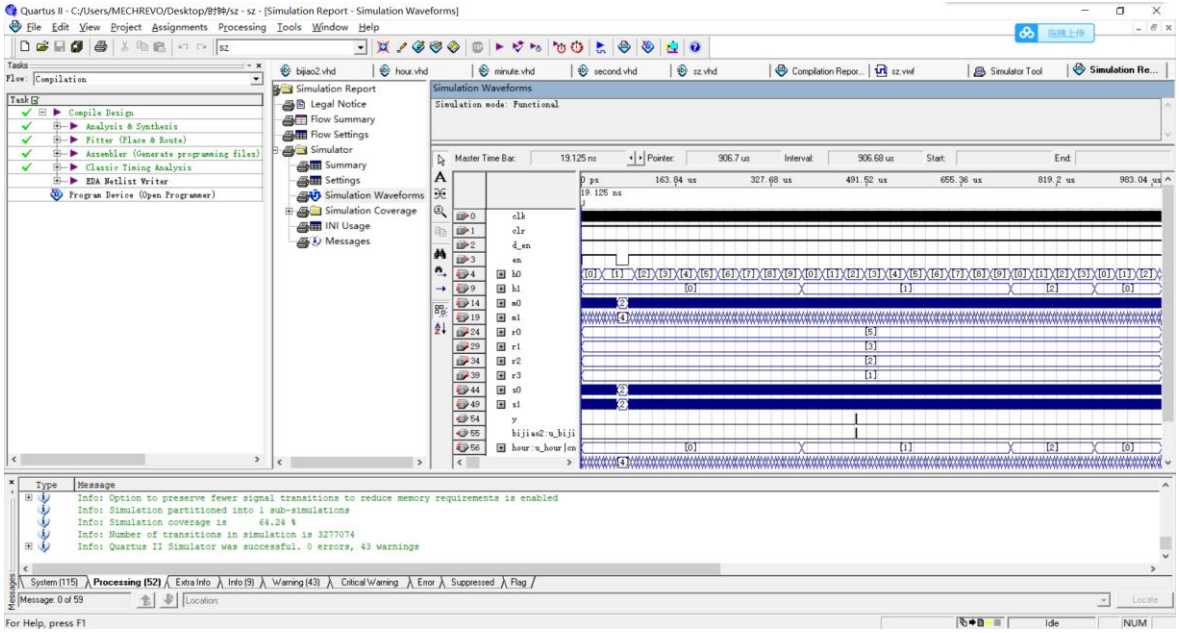

Quartus II - C:/Users/MECHREVO/Desktop/时钟/sz - sz - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.125 ns Pointer: 39.46 ns Interval: 20.34 ns Start: End:
clk
clr
d_en
en
h0
h1
m0
m1
r0
r1
r2
r3
s0
s1
y
bijiao2:u_biji
hour:u_hour|en
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 62.41 %
Info: Number of transitions in simulation is 3212610
Info: Quartus II Simulator was successful. 0 errors, 43 warnings
For Help, press F1


Quartus II - C:/Users/MECHREVO/Desktop/时钟/sz - sz - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.125 ns Pointer: 80.16 us Interval: 80.14 us Start: End:
clk
clr
d_en
en
h0
h1
m0
m1
r0
r1
r2
r3
s0
s1
y
bijiao2:u_biji
hour:u_hour|en
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 62.41 %
Info: Number of transitions in simulation is 3212610
Info: Quartus II Simulator was successful. 0 errors, 43 warnings
For Help, press F1


Quartus II - C:/Users/MECHREVO/Desktop/时钟/sz - sz - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.125 ns Pointer: 618.14 us Interval: 618.12 us Start: End:
clk
clr
d_en
en
h0
h1
m0
m1
r0
r1
r2
r3
s0
s1
y
bijiao2:u_biji
hour:u_hour|en
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 62.41 %
Info: Number of transitions in simulation is 3212610
Info: Quartus II Simulator was successful. 0 errors, 43 warnings
For Help, press F1


Quartus II - C:/Users/MECHREVO/Desktop/时钟/sz - sz - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.125 ns Pointer: 15.42 us Interval: 15.4 us Start: End:
clk
clr
d_en
en
h0
h1
m0
m1
r0
r1
r2
r3
s0
s1
y
bijiao2:u_biji
hour:u_hour|en
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 64.24 %
Info: Number of transitions in simulation is 3277074
Info: Quartus II Simulator was successful. 0 errors, 43 warnings
For Help, press F1





三，小组自评

白浩禹 19069100172 100 分

马真 19040300008 76 分

苟虎劲 20049200384 76 分

王曦瑶 20049200161 76 分

杨卓程 20049200356 76 分

龚志豪 20049200361 76 分

四，各模块源代码

1，顶层文件 sz

```
library ieee;

use ieee.std_logic_1164.all;

use ieee.std_logic_unsigned.all;

entity sz is

port(clk,d_en,clr,en:in std_logic;

s0,s1:out std_logic_vector(3 downto 0);

h1,h0:out std_logic_vector(3 downto 0);

r0,r1,r2,r3:in std_logic_vector(3 downto 0);

m1,m0:out std_logic_vector(3 downto 0);

y:out std_logic

);

end sz;

architecture shizhong of sz is

component second IS Port(
clk,clr,en:in std_logic;
sec0,sec1:out std_logic_vector(3 downto 0);
co:out std_logic
);
END component;

component minute IS Port(
clk,clr,en:in std_logic;
min0,min1:out std_logic_vector(3 downto 0);
co:out std_logic
);
END component;
```

```
component hour IS Port(
clk,clr,en:in std_logic;
h0,h1:out std_logic_vector(3 downto 0)
);
END component;

component bijiao2 IS Port(
clk,d_en:in std_logic;
h0,h1,h2,h3,s0,s1,s2,s3:in std_logic_vector(3 downto 0);
y:out std_logic
);
END component;


signal cs:std_logic;
signal cm:std_logic;
signal sec0,sec1,min0,min1,hour0,hour1:std_logic_vector(3 downto 0);
begin
    u_second:second port map(clk,clr,en,sec0,sec1,cs);
    u_minute:minute port map(cs,clr,en,min0,min1,cm);
    u_hour:hour port map(cm,clr,en,hour0,hour1);
    u_bijiao2:bijiao2 port map(clk,d_en,min0,min1,hour0,hour1,r0,r1,r2,r3,y);

s1<=sec1;
s0<=sec0;
m1<=min1;
m0<=min0;
h1<=hour1;
h0<=hour0;


end shizhong;
```

2，时计数模块 hour

```
library ieee;

use ieee.std_logic_1164.all;

use ieee.std_logic_unsigned.all;

entity hour is

port(clk,clr,en:in std_logic;
```

```
h0,h1:out std_logic_vector(3 downto 0));
end hour;
architecture beha of hour is
signal cnt1,cnt0:std_logic_vector(3 downto 0);
begin
process(clk)
begin
if(clr='0')then
cnt0<="0000";
cnt1<="0000";
elsif(clk'event and clk='1') then
if en='1' then
if cnt1="0010" and cnt0="0011" then
cnt1<="0000";
cnt0<="0000";
elsif cnt0<"1001" then
cnt0<=cnt0+1;
else
cnt0<="0000";
cnt1<=cnt1+1;
end if;
end if;
```

```
end if;
h1<=cnt1;
h0<=cnt0;
end process;
end beha;
```

3，分计数模块

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity minute is
port (clk,clr,en:in std_logic;
        min0,min1:out std_logic_vector(3 downto 0);
      co:out std_logic);
end minute;
architecture min of minute is
SIGNAL cnt1,cnt0:std_logic_vector(3 downto 0);
begin
      process(clk)
      begin
      if(clr='0')then
      cnt0<="0000";
      cnt1<="0000";
      elsif(clk'event and clk='1')then
```

```
        if   en='1' then
            if cnt1="0101" and cnt0="1001" then
                co<='1';
                cnt0<="0000";
                cnt1<="0000";
            elsif cnt0<"1001" then
                cnt0<=(cnt0+1);
            else
                cnt0<="0000";
                cnt1<=cnt1+1;
                co<='0';
            end if;
        end if;
    end if;
    min1<=cnt1;
    min0<=cnt0;
    end process;
end min;
```

4，秒计数模块

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
```

```
entity second is
port (clk,clr,en:in std_logic;
      sec0,sec1:out std_logic_vector(3 downto 0);
      co:out std_logic);
end second;
architecture sec of second is
SIGNAL cnt1,cnt0:std_logic_vector(3 downto 0);
begin
       process(clk)
       begin
       if(clr='0')then
       cnt0<="0000";
       cnt1<="0000";
       elsif(clk'event and clk='1')then

            if   en='1' then
                 if cnt1="0101" and cnt0="1001" then
                      co<='1';
                      cnt0<="0000";
                      cnt1<="0000";
                 elsif cnt0<"1001" then
                      cnt0<=(cnt0+1);
                 else
```

```
                    cnt0<="0000";
                        cnt1<=cnt1+1;
                        co<='0';
                end if;
            end if;
        end if;

        sec1<=cnt1;
        sec0<=cnt0;
        end process;
end sec;
```

5，定时模块 bijiao2

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity second is
port (clk,clr,en:in std_logic;
      sec0,sec1:out std_logic_vector(3 downto 0);
      co:out std_logic);
end second;
architecture sec of second is
SIGNAL cnt1,cnt0:std_logic_vector(3 downto 0);
begin
```

```
process(clk)
begin
if(clr='0')then
cnt0<="0000";
cnt1<="0000";
elsif(clk'event and clk='1')then

        if   en='1' then
                if cnt1="0101" and cnt0="1001" then
                        co<='1';
                        cnt0<="0000";
                        cnt1<="0000";
                elsif cnt0<"1001" then
                        cnt0<=(cnt0+1);
                else
                     cnt0<="0000";
                        cnt1<=cnt1+1;
                        co<='0';
                end if;
        end if;
end if;

sec1<=cnt1;
```

```
        sec0<=cnt0;

        end process;

end sec;
```