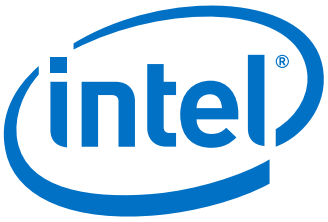
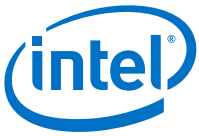


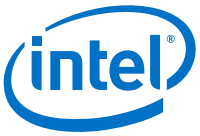
Intel® Firmware Support Package (Intel® FSP) for Intel Atom® Processor C2000 Product Family for Communications Infrastructure Post-Gold 6

Release Notes

April 2017

Order Number: 333408-003





Revision History

Date	Revision	Description
April 2017	003	Post-Gold 6 Release
June 15, 2016	002	Post-Gold 005 Release
September 24, 2015	001	Initial public release. Post-Gold 004 Release
April 9, 2015	1.3	Post-Gold 003 Release
April 2, 2014	1.2	Post-Gold 002 Release
December 18, 2013	1.1	Post-Gold 001 Release – first public release

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1.0 Introduction

This package contains the required binary image(s) and collateral for the Intel® Firmware Support Package (Intel® FSP) for Intel® Atom™ Processor C2000 Product Family for Communications Infrastructure Post-Gold 6.

This document provides system requirements, installation instructions, issues and limitations, and legal information.

To learn more about this product, see:

- New features listed in Section 2.0 "New in This Release", or in the help.
- Reference documentation listed in Section 4.0 "Related Documentation, Tools, and Packages" below.
- Installation instructions listed in Section 5.1 "How to Install this Release" below.

1.1 Component Information

The software in this release has been developed and validated using the following in Table 1.

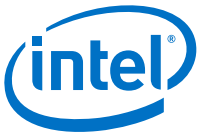
Table 1. Intel® FSP Component Information

FSP Binary Version	POSTGOLD4
Reference Code Version	49.R00
Memory Reference Code Version	1.0.0.49
Microcode Update C2xx0 A1	M01406D000E
Microcode Update C2xx0 B0	M01406D8129

1.2 Limitations

The following are the limitations for the Intel® FSP:

- The serial console base address of Intel® Atom™ Processor C2000 Product Family FSP is 0x2F8.
- The boot loader must ensure that FspInitEntry Application Programming Interface (API) is called within one second of returning from TempRamInitEntry API. Intel® FSP for Intel Atom® Processor C2000 Post-Gold 6.



1.3 Acronyms and Terms

Table 2 shows the acronyms and terms used in this document (arranged in alphabetic order).

Table 2. Acronyms and Terms

Acronym/Term	Description
API	Application Programming Interface
BCT	Binary Configuration Tool
BSF	Binary Settings File
CRB	Customer Reference Board
FSP	Firmware Support Package
IBL	Intel® Business Link
RMT	Rank Margining Tool
SoC	System on a Chip
UPD	Updatable Product Data
VPD	Vital Product Data

1.4 Intended Audience

Platform and system developers who intend to use an Intel® Firmware Support Package-based boot loader for the firmware solution for their overall design based on the Intel® Atom™ Processor C2000 Product Family. This group includes, but is not limited to, system BIOS developers, boot loader developers, and system integrators.

1.5 Customer Support

Intel offers support for this software at the API level only, defined in the FSP Integration guide and reference manuals listed in Section 4.0 “Related Documentation, Tools, and Packages”. If your field representative has created an account for you, support requests can be submitted at https://premier.intel.com.

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2.0 New in This Release

2.1 New Features

This release includes the following new features and product changes:

- Updated platform reference code to Reference Code Release (49.R00)
- Updated USB Workaround for detection issue found in certain configurations.

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3.0 Known Issues

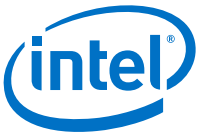
Known and resolved issues relating to Intel® Firmware Support Package are described in this section.

3.1 Known Issues for the Intel® Atom™ Processor C2000 Product Family

Table 3 lists known issues for the Intel® Atom™ Processor C2000 Product Family.

Table 3. Known Issues

Title	Certain boards exhibit intermittent boot and MCE errors.
Problem	Boards with DDR trace lengths longer than the CRBs, see MCE Errors at 1333/1600 MT.
Workaround	Set PcdEnableRelaxedTurnaroundTiming to Enabled in order to enable the relaxed DDR Turnaround timing.
Impact of Workaround	Enabling this PCD will cause ~1% performance loss on the platform.
Title	FSP disables the TCO Watchdog Timer after the boot loader re-enables the WDT.
Problem	There is a coverage gap for boot loaders that utilize the WDT to address system hangs.
Workaround	Set the PcdTcoEnable to 1 in order for FSP to bypass disabling the WDT.
Impact of Workaround	None.
Title	Reboot occurring when PUNIT watchdog timer times out.
Problem	The PUNIT has a watchdog timer that provides a window of approximately 1 second to complete initial programming of power management related registers. Failure to feedback the status to the PUNIT within 1 second of a microcode update will result in the system requesting a reboot.
Workaround	The boot loader must ensure that FspInitEntry API is called within one second of returning from TempRamInitEntry API. For designs that do not use an RTC battery, it is recommended that the RtcPowerFailureHandler() routine should be executed after the call to FspInitEntry API to ensure that the 1 second PUNIT timeout window is not violated.
Impact of Workaround	None.



3.2 Resolved Issues for the Intel® Atom™ Processor C2000 Product Family

Table 4. Resolved Software-Related Issues

Title	USB 2.0 device may not be detected at system power-on.
Problem	Certain internal conditions may cause one or more USB ports to fail at system power-on.
Implication	When this erratum occurs, a USB device attached to the affected port will not function. In addition, the OS may report problems with the USB port.
Title	USB devices not being detected in certain configuration
Workaround	Enabling workaround in early stage and using sideband transaction to program WA for USB Lane 0 to USB Lane 3. USB_IP Port ID:0xA4, write command: 0x7 Register: 0x4113 (Lane 0), 0x4123 (Lan0_Pull_down) 0x4213 (Lane 1), 0x4223 (Lan1_Pull_down) 0x4313 (Lane 2), 0x4323 (Lan2_Pull_down) 0x4413 (Lane 3), 0x4423 (Lan3_Pull_down) For Lane 0 and Lan0_Pull_down, Repeat steps for Lan1 and Lan3. Step1. Offset: 0x4113=0x08 Step2. Offset: 0x4123=0x7F13 Step3. Offset: 0x4123=0x13 Step4. Offset: 0x4123=0x4011 Step5. Offset: 0x4113=0
Implication	None

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4.0 Related Documentation, Tools, and Packages

Table 5 lists Intel® FSP for Intel® Atom™ Processor C2000 Product Family Platform documentation.

Table 5. Intel® Firmware Support Package Documentation

Document Name	Document No./Location
Intel® Firmware Support Package for Intel® Atom™ Processor C2000 Product Family Integration Guide	https://github.com/IntelFsp/FSP
Intel® Atom™ Processor C2000 Product Family Custom Reference Board Platform Guide	www.intel.com/fsp
Binary Configuration Tool (BCT) for Intel® FSP	*https://github.com/IntelFsp/BCT*
Intel® Firmware Support Package External Architecture Specification	*http://www.intel.com/content/dam/www/public/us/en/documents/technical-specifications/fsp-architecture-spec.pdf*

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5.0 Where to Find the Release

This package can be found on www.intel.com/fsp.

5.1 How to Install this Release

This release can be installed on a Linux* system using the following:

Download the Linux* files from https://github.com/IntelFsp/FSP

Note: For the guide to adding the Intel® FSP APIs into the boot loader code, refer to the *Intel® Atom™ Processor C2000 Product FSP Integration Guide.* (See Section 4.0, "Related Documentation, Tools, and Packages" on page 10.)

Note: For the guide to compiling the boot loader together with the Intel® FSP binary, refer to the *Intel® Atom™ Processor C2000 Product Family Custom Reference Board Platform Guide.* (See Section 4.0, "Related Documentation, Tools, and Packages" on page 10.)

5.2 Microcode Update

Since the introduction of the Intel® Pentium® Pro processor, IA-32 processors have had the capability to correct specific errata through the loading of an Intel-supplied data block. This data block is referred to as a microcode update or system configuration data.

Each unique processor stepping/package combination has an associated microcode update that, when applied, constitutes a supported processor (that is, Specified Processor = Processor Stepping + Microcode Update). The proper microcode update must be loaded on each processor in a system. The proper microcode update is defined as the latest microcode update available from Intel for a given family, model, and stepping of the processor. Any processor that does not have the correct microcode update loaded is considered to be operating out of specification.

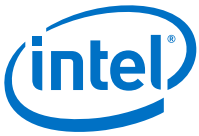
The microcode update included in this release is the latest update at this particular time. Intel recommends that future microcode updates are done as soon as the latest ones are released.

Note: Intel recommends subscribing to the *Intel Atom® Processor C2000 Product Family for Microserver and Communications Infrastructure Platforms (Edisonville/Rangeley) - Message of the Week (MoW)* (see Section 4.0, "Related Documentation, Tools, and Packages" on page 10) for latest news on Processor Microcode Updates.

The steps for updating the microcode for a sample boot loader can be found under "Microcode Update" in the *Intel Atom® Processor C2000 Product Family Custom Reference Board Platform Guide.* (See Section 4.0, "Related Documentation, Tools, and Packages" on page 10.)

5.3 Debug

Debug messages are the primary way of debugging the Intel® FSP. This requires enabling the debug messages into the serial port. The steps to enable the serial debug messages can be found in How to Enable Serial Debug Messages in the Intel Atom® Processor C2000 Product Family Custom Reference Board Platform Guide. (See Section 4.0, "Related Documentation, Tools, and Packages" on page 10.)



5.4 Validation

The Rank Margining Tool (RMT) can flag areas of concern for platform developers. The steps to enable RMT is described in detail under "How to Enable the Rank Margining Tool" in the *Intel® Atom™ Processor C2000 Product Family Custom Reference Board Platform Guide*. (See Section 4.0, "Related Documentation, Tools, and Packages" on page 10.)

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6.0 Release Content

This release package contains the following:

Table 6. Package Contents

Description	Filename	Path
FSP Kit License File	FSP Kit Production RULAC click-through License.pdf	RANGELEY_FSP_KIT
FSP Binary File	RangeleyFsp.fd	RANGELEY_FSP_KIT/FSP
Boot Setting File (BSF)	RangeleyFsp.bsf	RANGELEY_FSP_KIT/FSP
Text file copy of FSP kit license file (Linux* only)	license.txt	RANGELEY_FSP_KIT/ DOCUMENTATION
*.h	FSP header files	RANGELEY_FSP_KIT/FSP/include
*.c	FSP source files	RANGELEY_FSP_KIT/FSP/srx

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7.0 Hardware and Software Compatibility

7.1 Supported Hardware

The FSP included in this release is specifically targeted for the Intel Atom® Processor C2000 Product Family System on a Chip (SoC).

7.2 Supported Operating Systems

This release installs on either a Windows* or a Linux* system. However, the FSP binary itself can be used with any software development environment to generate a complete boot loader solution.

The software in this release has been validated against the operating systems given in the following table on the Customer Reference Boards (CRBs) for the following products:

- Intel Atom® Processor C2000 Product Family

Note: While the Intel® Firmware Support Package is validated on Coreboot* and Yocto* on the respective platforms, it is designed to work without change on some other boot loaders and operating systems.

Table 7. Operating System/Boot Loader/Tools Support

Software Type	Name	Version
Boot loader	Coreboot	4.3
Payload Boot loader	u-boot Payload	u-boot-2013.01.01
Firmware Component	FSP	Gold 006
Operating System	Yocto*	Poky* 9.0 (Yocto Project* 1.4 Reference Distro) 1.4.1
Tool	Binary Configuration Tool	3.2.0

Note: Validation done on C0 Stepping Intel Atom® C2000 Product Family.

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8.0 Configuration

A Binary Configuration Tool (BCT) for the Intel® FSP is provided as a companion tool and is intended to be used to do the following:

- Customize the FSP binary configuration options based on the Boot Setting File (BSF).
- Rebase the FSP binary to a different base address. (The default base address of the Intel® FSP for Intel Atom® Processor C2000 Product Family is 0xFFF80000.)

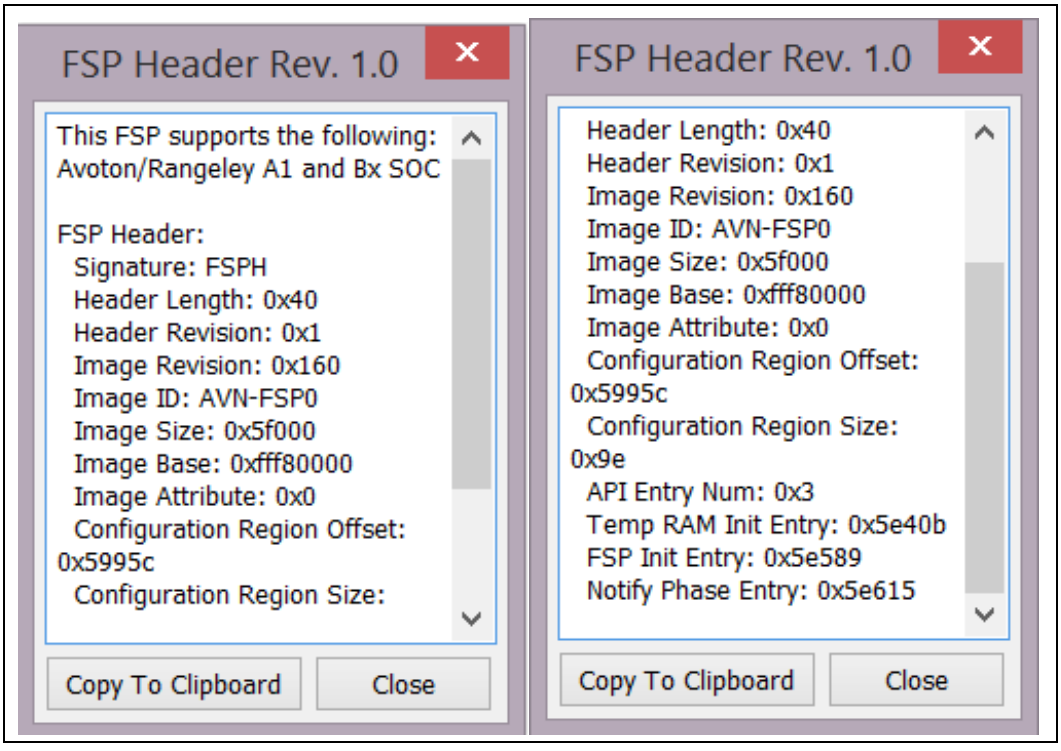
Refer to the BCT User Guide for the usage instructions. See Section 4.0 "Related Documentation, Tools, and Packages" to obtain the BCT.

8.1 Intel® Firmware Support Package Information

To obtain the Intel® FSP binary information:

1. Run the `Binary Configuration Tool` as an Administrator.
2. Click the `Show Binary Description command` button.
3. Select the Intel® FSP binary. For this release, the binary included is named as RangeleyFsp.fd.
4. Click Open. Another window, shown in Figure 1, will pop out to show the Intel® FSP binary information.
5. Click OK to close the window.

Figure 1. Intel® FSP Binary Information



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9.0 Legal Information

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