**DSD Final Checkpoint Scores**

**1. Baseline**

(1) Area: (um2)

Total Cell Area =

截圖:一張含有 文字, 螢幕擷取畫面, 軟體, 電腦 的圖片

自動產生的描述

(2) Total Simulation Time of given noHazard testbench: (ns)

截圖:

(3) Total Simulation Time of given hasHazard testbench: (ns)

finish at simulation time: 814ns

一張含有 文字, 螢幕擷取畫面, 軟體, 電腦 的圖片

自動產生的描述截圖:

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

CYCLE = 4ns

post-syn simulation command used:

* vcs Final\_tb.v slow\_memory.v ../Syn/CHIP\_syn.v -v /home/raid7\_2/course/cvsd/CBDK\_IC\_Contest/CIC/Verilog/tsmc13.v -full64 -R -debug\_access+all +v2k +define+hasHazard \

+define+SDF +define+SDF\_FILE=\"../Syn/CHIP\_syn.sdf\" +define+CYCLE=4 +neg\_tchk