清大實作專題

7/8/2023

Jiin Lai

Agenda

- TA Session
- Guidelines for Posting in Forum
- Q/A & Logistics
- Verilog Critical Concepts Explained

Study Plan

Will update when presentation schedule confirmed

wk	Date	Meeting (Q&A + Presentation)	Area	Reading Assignment	Lab
-1	6/20	Summer program introduction	Verilog	L3 + NTU Verilog / Lint / Gotchas	Lab1: Tool installation: Vitis HLS/ Vivado Tool
0				L4 + NTU Verilog / Lint / Gotchas, PYNQ Video	Lab#2 - PYNQ Lab - GCD (xsim)
1	7/5	Verilog/Lint	Logic Design	L#5(CL I), L#6(CL II), L#21 (FF), Script, Udemy (Com)	Lab - combinational (1.5 w)
2	7/12	Verilog/Lint		L#18 (Adders), L#19(Multiplier), L#20 (Multiplier II) Udemy(Comb), Script: Perl	Lab - Combinational + Sequential (2.5 w)
3	7/19	Lab - combinational		L#22, L#23 SRAM, Udemy(Seq), Script: Perl	Lab - Sequential
4	7/26	Lab - combinational, Script	RISCV	L#7, L#8 - RISCV	Lab - Sequential
5	8/2	Lab - Sequential, Script		L#9, L#10 - RISCV , Script: Tcl	Lab - RISCV HLS/Verilog (1/5w)
6	8/9	Lab - Sequential + Lint + Script		L#10 - RISCV, Script: Tcl	Lab - RISCV (2/5w)
7	8/16	Logic Design/ Vaibbhav	VLSI Physics	L#13 - CMOS Transistor / Logic Gate L#14 - Inverter-Delay L#15 - Inverter Chain Delay	Lab - RISCV (3/5w)
8	8/23	Lab-RISCV		L#16 - Logical Effort L#17 - Wire Energy, Static / Dynamic Power	Lab - RISCV (4/5w)
9	8/30	Lab - RISCV	Computer System	Chap8 - Memory (Cache, Virtual Memory)	Lab - RISCV (5/5w)
10	9/6	Computer System		Chap 9: Embedded IO	

Logistics

- TA - 王立皓, 張育碩, 謝明翰, 陳冠晞
- Logistics & Status
  - Team / Team leader / TA
  - Topic selection
  - Lab1 & Lab2 Status ?
- **Post Questions to be answered in class**
  - https://docs.google.com/forms/d/e/1FAIpQLSeExQQQVT0Gy8FpZVe1YNlh3jxx8d-h0qYBCuI3PgeiB9gteQ/viewform?usp=sharing
- HackMD – everyone maintain a study_record.md
  - Simulation issue studied: https://hackmd.io/@TonyHo/BkhFOUe_n
  - Sequential logic that requires blocking assignments https://hackmd.io/@TonyHo/rJwPNuIu3
  - Intra-delay and Inter-delay Assignments https://hackmd.io/@TonyHo/S1nmbWuOh