

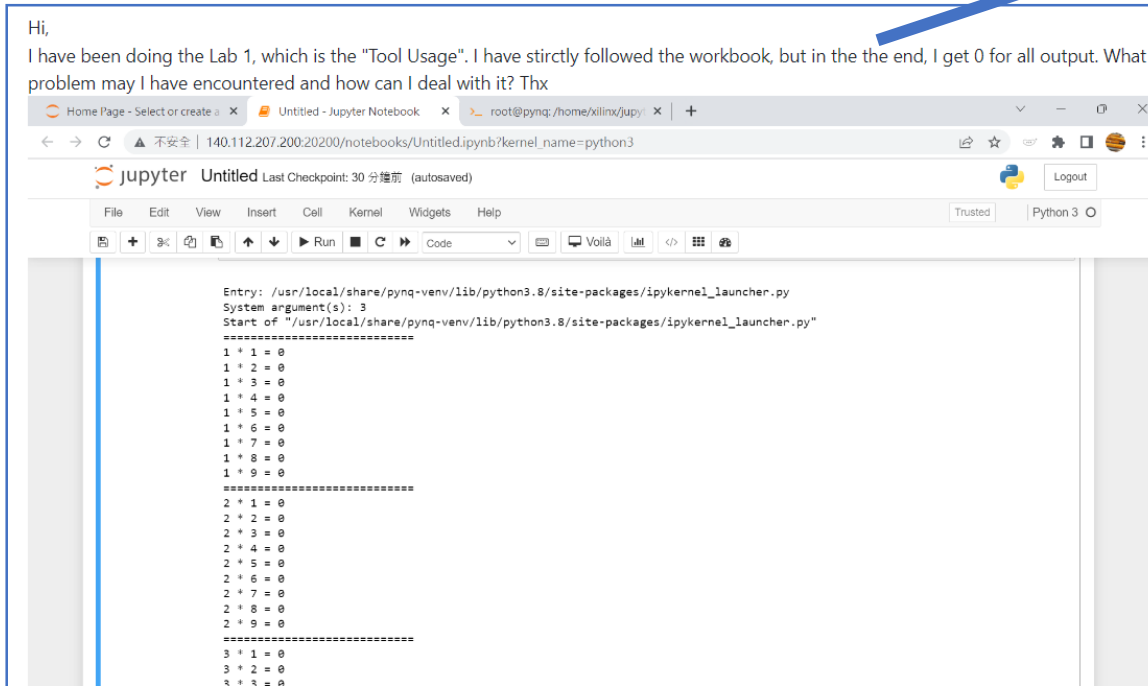


Bridge of Life
Education

Guidelines for Posting in Forum

Let's look at a post in the Github HLS Discussion

Subject: course-1-lab question



The screenshot shows a Jupyter Notebook interface. At the top, there is a text input area with the following text: "Hi, I have been doing the Lab 1, which is the 'Tool Usage'. I have strictly followed the workbook, but in the the end, I get 0 for all output. What problem may I have encountered and how can I deal with it? Thx". Below this, there is a code cell with the following output:

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
=====
1 * 1 = 0
1 * 2 = 0
1 * 3 = 0
1 * 4 = 0
1 * 5 = 0
1 * 6 = 0
1 * 7 = 0
1 * 8 = 0
1 * 9 = 0
=====
2 * 1 = 0
2 * 2 = 0
2 * 3 = 0
2 * 4 = 0
2 * 5 = 0
2 * 6 = 0
2 * 7 = 0
2 * 8 = 0
2 * 9 = 0
=====
3 * 1 = 0
3 * 2 = 0
3 * 3 = 0
```

Hi,
I have been doing the Lab 1, which is the "Tool Usage". I have strictly followed the workbook, but in the the end, I get 0 for all output. What problem may I have encountered and how can I deal with it? Thx

How can people help him based on the above description ?

Guidelines

- Picking the right forum
- The Subject – Offer the Clue to your problem
- Search online solutions, e.g. Google
- State what you have already tried
- Steps to Re-create your Problem
- Provide Information about what errors you get
- Show the portion of the code that is failing
- Others

Picking the Right Forum

- Participate in Github HLS Discussion:

<https://github.com/bol-edu/HLS-Discussions/discussions>

- Submit question to Xilinx HLS Forum:

https://support.xilinx.com/s/topic/OTO2E000000YKXtWA0/hls?language=en_US

The screenshot displays the 'Welcome to HLS Discussions! (& some usage guides)' forum page. At the top, a blue header bar contains the forum title and the 'boledulab' logo. Below the header is a search bar labeled 'Search all discussions' and navigation buttons for 'New', 'Top: All', 'Label', 'Filter', and a 'New discussion' button. The main content area is divided into two columns. The left column, titled 'Categories', lists 'Announcements', 'General', 'Ideas', 'Polls', and 'Q&A', with a 'View all' button for each. Below this is a 'Most helpful' section with a tip about marking answers and a link to 'Community guidelines'. The right column, titled 'Discussions', shows a list of topics with icons for replies, status, and user avatars. The topics include 'course-1-lab question', 'C/RTL co-simulation hang', 'References for HLS Project Idea', 'RTL kernel flow: undefined reference to xrt::<>', 'Winners of Xilinx Adaptive Computing Challenge 2021', and 'Welcome to HLS Discussions! (& some usage guides)'. Below the discussions list is a 'Sort by' dropdown menu set to 'Top Questions'. The bottom section of the screenshot shows a list of search results for 'Vitis HLS Design Hub', including topics like 'Export IP Invalid Argument / Revision Number Overflow Issue', 'AXI Tutorials', 'Does the new versions of Vitis HLS/Vivado HLS not support KCU1500?', 'C simulation fails with no specific message', 'Vitis HLS stopped working just after opening', 'Vitis HLS 2022.1 crashes on startup Ubuntu 22.04', 'Enquiry on sorting algo api usage.', and 'i am using these interfaces in HLS design. what are the ip's are used in testing(vivado) to connect ip generted from HLS. #pragma HLS INTERFACE...'. Each result shows the topic title, user, date, and engagement metrics like views, likes, and replies.

The Subject – Offer the Clue to your problem

Subject: course-1-lab question

Subject: Problem with Course-1-lab - getting all zero in the result

Search online solution first, e.g. Google

- Search Google with error number
- If can not find what you want on Google or you don't understand what you have seen, then, post the question

State what you have already tried

vitis his 2020.2 Pre-synthesis failed, but it didn't prompt any errors. How can I find out the cause of the error and fix it?

```
void read_data(kern_colmeta *colmeta
, int ncols
, HeapTupleHeaderData *htup
, cl_char tup_dclass[READ_COL]
, cl_long tup_values[READ_COL])
{
    char *addr; //__attribute__((unused));
    EXTRACT_HEAP_TUPLE_BEGIN(addr, colmeta, ncols, htup); /*(cl_uint*)addr == 4
    EXTRACT_HEAP_TUPLE_NEXT(addr); /*(cl_uint*)addr == 1085693
    EXTRACT_HEAP_READ_32BIT(addr, tup_dclass[3], tup_values[3]); /*(cl_uint*)addr == 85694
    EXTRACT_HEAP_TUPLE_NEXT(addr); /*(cl_uint*)addr == 1
    EXTRACT_HEAP_TUPLE_NEXT(addr);
    EXTRACT_HEAP_TUPLE_NEXT(addr);
    //EXTRACT_HEAP_READ_POINTER(addr, tup_dclass[1], tup_values[1]);
    EXTRACT_HEAP_TUPLE_NEXT(addr);
    //EXTRACT_HEAP_READ_POINTER(addr, tup_dclass[2], tup_values[2]);
    EXTRACT_HEAP_TUPLE_END();
}

extern "C"
void accel(char *a, kern_colmeta *b)
{
    #pragma HLS INTERFACE m_axi depth=125 port=a
    #pragma HLS INTERFACE m_axi depth=1984 port=b
    #pragma HLS INTERFACE m_axi depth=16 port=b
    //kern_colmeta col[16];
    //memcpy(col, b, sizeof(kern_colmeta)*16);
    HeapTupleHeaderData *htup;
    htup = (HeapTupleHeaderData *)a;
    cl_char tup_dclass[READ_COL];
    cl_long tup_values[READ_COL];
    read_data(b, 16, htup, tup_dclass, tup_values);
}
}
```

The top function is accel(), error occurs in the code when calling EXTRACT_HEAP_READ_32BIT(). C simulation results are normal, but as once try to run synthesis, it failed, error log just like as follows:
INFO: [HLS 200-111] Running synth_design
INFO: [HLS 200-111] Finished File checks and directory preparation: CPU user time: 0 seconds. CPU system time: 0 seconds. Elapsed time: 0 seconds; current allocated

By the way, It's an interesting phenomenon. When changing the code as below, it works fine!

```
void read_data(kern_colmeta *colmeta
, int ncols
, HeapTupleHeaderData *htup
, cl_char tup_dclass[READ_COL]
, cl_long tup_values[READ_COL])
{
    char *addr; //__attribute__((unused));
    EXTRACT_HEAP_TUPLE_BEGIN(addr, colmeta, ncols, htup); /*(cl_uint*)addr == 4
    EXTRACT_HEAP_READ_32BIT(addr, tup_dclass[3], tup_values[3]);
    EXTRACT_HEAP_TUPLE_NEXT(addr); /*(cl_uint*)addr == 1085693
    EXTRACT_HEAP_TUPLE_NEXT(addr);
    EXTRACT_HEAP_TUPLE_NEXT(addr);
    /*(cl_uint*)addr == 85694
    EXTRACT_HEAP_TUPLE_NEXT(addr); /*(cl_uint*)addr == 1
    ...
```

When changing the code as below, it's still normal..

```
void read_data(kern_colmeta *colmeta
, int ncols
, HeapTupleHeaderData *htup
, cl_char tup_dclass[READ_COL]
, cl_long tup_values[READ_COL])
```

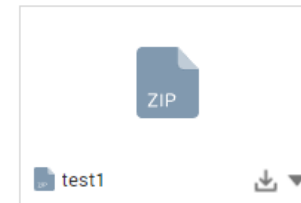
When changing the code as below, it's still normal..

```
void read_data(kern_colmeta *colmeta
, int ncols
, HeapTupleHeaderData *htup
, cl_char tup_dclass[READ_COL]
, cl_long tup_values[READ_COL])
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    char *addr; //__attribute__((unused));
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    EXTRACT_HEAP_TUPLE_NEXT(addr); /*(cl_uint*)addr == 1085693
    EXTRACT_HEAP_READ_32BIT(addr, tup_dclass[3], tup_values[3]);
    EXTRACT_HEAP_TUPLE_NEXT(addr);
    /*(cl_uint*)addr == 85694
    EXTRACT_HEAP_TUPLE_NEXT(addr); /*(cl_uint*)addr == 1;
```

But it fails when the code is as follows. Why?

```
void read_data(kern_colmeta *colmeta
, int ncols
, HeapTupleHeaderData *htup
, cl_char tup_dclass[READ_COL]
, cl_long tup_values[READ_COL])
{
    char *addr; //__attribute__((unused));
    EXTRACT_HEAP_TUPLE_BEGIN(addr, colmeta, ncols, htup); /*(cl_uint*)addr == 4
    EXTRACT_HEAP_TUPLE_NEXT(addr); /*(cl_uint*)addr == 1085693
    EXTRACT_HEAP_TUPLE_NEXT(addr);
    EXTRACT_HEAP_READ_32BIT(addr, tup_dclass[3], tup_values[3]);
    /*(cl_uint*)addr == 85694
    EXTRACT_HEAP_TUPLE_NEXT(addr); /*(cl_uint*)addr == 1
    ...
```

The sample code zip package has been uploaded. How can I fix it ? thanks



Steps to Re-create your Problem

Vitis HLS 2022.1 crashes on startup Ubuntu 22.04

Hello,

Vitis HLS crashes on Ubuntu 22.04, also crashes on my other machine running Ubuntu 21.04. I can see splash screen pop up but it then exits:

```
tian@tianmsi:~$ source /tools/Xilinx/Vitis_HLS/2022.1/settings64.sh
tian@tianmsi:~$ vitis_hls
```

```
***** Vitis HLS - High-Level Synthesis from C, C++ and OpenCL v2022.1 (64-bit)
**** SW Build 3526262 on Mon Apr 18 15:47:01 MDT 2022
**** IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022
** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
```

```
source /tools/Xilinx/Vitis_HLS/2022.1/scripts/vitis_hls/hls.tcl -notrace
INFO: [HLS 200-10] Running '/tools/Xilinx/Vitis_HLS/2022.1/bin/unwrapped/lnx64.o/vitis_hls'
INFO: [HLS 200-10] For user 'tian' on host 'tianmsi' (Linux_x86_64 version 5.15.0-47-generic) on Tue Sep 13 15:19:50 PDT 2022
INFO: [HLS 200-10] On os Ubuntu 22.04 LTS
INFO: [HLS 200-10] In directory '/home/tian'
INFO: [HLS 200-10] Bringing up Vitis HLS GUI ...
INFO: [HLS 200-112] Total CPU user time: 12.24 seconds. Total CPU system time: 0.59 seconds. Total elapsed time: 4.11 seconds; peak allocated memory: 19.289 MB.
INFO: [Common 17-206] Exiting vitis_hls at Tue Sep 13 15:19:54 2022...
```

Does not crash on my windows 11 machine.

The following post has a similar issue and suggests it might be caused by a memory issue but I have 25G of free memory when I launched Vitis_hls:

https://support.xilinx.com/s/question/0D52E00006IMPOqSAO/vitis-hls-20211-crash-when-start?language=en_US

Any help is appreciated!

Tian

https://support.xilinx.com/s/question/0D54U00005aqaytSAA/vitis-hls-20221-crashes-on-startup-ubuntu-2204?language=en_US

Provide Information about what errors you get

vivado giving error when getting ip from Vivado hls ...

i am synthesizing TPG hls ip , but i am getting error with newly installed Vivado 2020.1

```
***** Vivado v2020.1 (64-bit)
**** SW Build 2902540 on Wed May 27 19:54:35 MDT 2020
**** IP Build 2902112 on Wed May 27 22:43:36 MDT 2020
** Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

source run_ippack.tcl -notrace
bad lexical cast: source type value could not be interpreted as target
while executing
"rdi::set_property core_revision 2205041141 {component component_1}"
invoked from within
"set_property core_revision $Revision $core"
(file "run_ippack.tcl" line 940)
INFO: [Common 17-206] Exiting Vivado at Wed May 4 11:41:14 2022...
ERROR: [IMPL 213-28] Failed to generate IP.
command 'ap_source' returned error code
while executing
"source /home/chaitusvk/Documents/sdi/sdi_tx/sdi_tx.runs/design_1_v_tpg_0_0_synth_1/runhls.tcl"
("uplevel" body line 1)
invoked from within
"uplevel \#0 [list source $arg] "
```

INFO: [HLS 200-112] Total elapsed time: 54.06 seconds; peak allocated memory: 400.766 MB.
INFO: [Common 17-206] Exiting vivado_hls at Wed May 4 11:41:17 2022...



https://support.xilinx.com/s/question/0D52E000079rt7fSAA/vivado-giving-error-when-getting-ip-from-vivado-hls-?language=en_US

Show the portion of the code that is failing



mash-knit (Member) asked a question.
March 30, 2020 at 6:13 PM

Malfunction of ap_int on ofstream's insertion operator with hexadecimal format

I'm new to Vivado HLS and trying to write a test code, and I found a strange behavior about 'ap_int' as follows.
It makes inconvenience on writing test code, since I should handle a lot of long stream data with hex format.

```
1 // io manipulation error
2 int main(){
3     using namespace std;
4     int int_val = 256;
5     ap_int<16> ap_int_val = int_val;
6     cout << hex << setw(4) << setfill('0') << int_val << endl; // 0100 -> OK
7     cout << hex << setw(4) << setfill('0') << ap_int_val << endl; // 0x100 -> NG, setfill is ignored
8 }
```

```
1 // ofstream error
2 int main(){
3     using namespace std;
4     ofstream ofile("result.txt");
5     int int_val = 256;
6     ap_int<16> ap_int_val = int_val;
7     ofile << hex << setw(4) << setfill('0') << int_val << endl; // 0100 -> OK
8     ofile << hex << setw(4) << setfill('0') << ap_int_val << endl; // 0256 -> NG, hex is ignored
9     ofile.close();
10 }
```

I'm already aware that the reason is in the header files that are provided with Vivado HLS 2019.2 ('ap_int_base.h' and 'ap_private.h').
Is there anyone who knows if there is a plan to fix this problem, or good work around?
Thank you.

https://support.xilinx.com/s/question/0D52E00006hprN8SAI/malfunction-of-apint-on-ofstreams-insertion-operator-with-hexadecimal-format?language=en_US

Others

- Don't write a novel. Be specific and concise.
- Questions that are obviously basic probably aren't going to get helpful replies.
- We aren't here to do your work for you. You should have your due diligence