Senior Design: Week Three Progress Report

Team 3: Micheal Frith, David Larribas, Devin Moore, Benjamin Smith

1 Group Time Synopsis

1.1 Team efforts and overall status

Current Group Leader: Ben Smith

THE group spent about half of its bandwidth on developing the work breakdown structure (WBS) and documentation. The WBS gave the group an opportunity to clarify a feature set after last weeks Design Document review. The Design Document revisions for this week reflect our changes of expectation in accordance with last week's review.

Three development boards have been purchased by the group for Verilog development and testing. These boards come equipped with the Analog Devices ADXL345 accelerometer that is configurable for SPI or I2C. This accelerometer is extremely common and the most likely to be used in the final production design. Having the accelerometer on board will prove invaluable for the breadboard proof.

The development board supports JTAG over USB and does not require an external power supply. It will provide hardware based verification in a small, easy to use form factor. The board is also based on the Altera Cyclone IV FPGA. This allows the use of development tools familiar to the group members. The FPGA is also large enough to use Signaltap, Alteras embedded logic analyzer.

1.2 Review after Meeting with Professor Tatro

We revised the punch list, particularly the motor control modes, after design document review. This lead to the elimination of all operational modes except biometric feedback. The biometric feedback scheme's definition was made more broad to allow for change over span of the project.

TABLE 1
Weekly Team Meetings

Topic	Hours
Tuesday: Review after Meeting with Professor Tatro	1.0
Thursday: WBS assignment review and section assignment	3.0
Sunday : Finalization of WBS and Design Document Review	5.0
Monday : Weekly Report drafting	5.0
Monday : WBS typesetting and final review	5.0

1.3 WBS assignment review and section assignment

Group members took responsibility for individual sections in the WBS related to their technical expertise. A diagrammatic representation of the WBS was constructed to ensure mutual exclusivity of the individual sections.

1.4 Finalization of WBS and Design Document Review

The group met on line to compile and review their individual sections of the WBS they worked on over the week. Final draft was prepared for typesetting on Monday.

1.5 Weekly Report drafting and weekly debrief

Group assembled to review progress over the last week. Expectations of next week's time expenditure were drafted from the lecture notes for the week. The group was brought up to speed with Mike's motor research from last week.

1.6 WBS typesetting and final review

Document was typeset and reviewed by the group to catch spelling and grammatical errors.

2 Individual Activity Synopsis

2.1 Micheal Frith

Synopsis of past week's work

I spent considerable time researching various hub motors as well as preliminarily selecting a speed controller after getting in touch with Richard Lyen, a custom motor controller designer in San Francisco. He steered me towards some potential motor suppliers as well as made some recommendations for motors themselves. I'm waiting on contact back after some initial conversation with a potential supplier about getting a discounted motor. Other than motor and speed controller research, I spent time investigating integrating audio into our design. Generating sound at the FPGA level may be a good preliminary implementation. Additionally I worked on my sections of WBS document, weekly report, and design contract.

TABLE 2
Micheal Frith: Tasks Assigned - Last Week

Task	Hours Worked	Status
Component Research/Selection	6.0	60%
Work Breakdown Structure	6.0	100%
Researched implementing FPGA audio	2.0	20%
Design Contract Finalization	4.0	100%
Gantt Chart	0	10%

TABLE 3
Micheal Frith: Tasks Assigned - This Week

Task	Hours Worked	Status
Component research/selection	6.0	80%
PERT/TeamGantt	6.0	90%
Start FPGA Dev: Screen, User inputs	3	10%

2.2 David Larribas

Synopsis of past week's work

For the first task of this week, my group and I met up with Professor Tatro to realign our focus. This led to some rewording that altered the scope of our project including changing specifications in my part of the design document. I researched over a dozen lighting systems and their reviews to estimate which LEDs to use. I researched three power conversion methods and settled on a buck converter to be the ideal method because of its minimal power loss. I then wrote up the safety and power system sections of the WBS diagram. I also wrote my sections of the WBS document including the lighting and power systems. I had to research the various components of these sections by searching through half a dozen websites to price these items.

TABLE 4
David Larribas: Tasks Assigned - Last Week

Task	Hours Worked	Status
Work breakdown Structure	8.0	100%
Develop Gantt Chart	1.0	5%
Component research and selection for lighting	3.0	50%
Component research and selection for Voltage Regulator	2.0	25%
Weekly Report - Week 3	2.0	100%
Editing Design Document	2.0	100%

TABLE 5
David Larribas: Tasks Assigned - Next Week

Task	Hours Worked	Status
Develop Gantt Chart	4.0	5%
Component research and selection for Lighting	2.0	50%
Component research and selection for Voltage Regulator	6.0	25%
"Breadboard" Voltage Regulator	4.0	0%

2.3 Devin Moore

Synopsis of past week's work

The beginning of the week consisted of researching and discussing possible features for the system. Once they had been compiled we broke them up into groups to research and report the various aspects of each feature including why it is relevant, what has been done before, how it would be implemented, and resources needed. After we had finished, we began typesetting the document in LaTeX and refining our desired layout. There was a substantial amount of discussion on required features and possible parts to order.

TABLE 6
Devin Moore: Tasks Assigned - Last Week

Task	Hours Worked	Status
Refine Problem Statement	2.0	80%
Refined Design Contract	4.0	100%
Selected and Ordered FPGA dev kit	3.0	70%
Wrote Work Breakdown Structure	15.0	100%
Started IMU I2C Interface	4.0	15%
Started Cell Phone App	2.0	10%

TABLE 7
Devin Moore: Tasks Assigned - Next Week

Task	Hours Worked	Status
Scheduling and Gantt Chart	10.0	90%
IMU I2C interface	25.0	80%

2.4 Ben Smith

Synopsis of past week's work

I spent a good deal of time learning how use Mentor's Modelsim application and learning to write a proper System Verilog test bench. Until now I have largely used Signaltap to validate design, this was effective for small projects but is ineffective for large designs. A proper test bench allows the use of automated debugging constructs like random generation and assertion which ensure adherence to a much more rigorous specification and allow a more rapid verification-development cycle. I averaged a 5 minute synthesis time average with the Cyclone over my summer internship. This weeks compilations with Modelsim averaged under 5 seconds. The advantage of simulator use is clear, more code, better code, less time.

The analysis of the open cores module brought the group up to speed with I2C. We have a clear understanding of how the I2C protocol works. This understanding allows us to write a specification for what we need our module to do. We need a Master controller that will operate in single master mode at the 100kHz I2C spec. We know both the accelerometer and gyroscope operate at this speed.

Devin and I have begun to write the HDL for our implementation of a I2C master controller. This week setup the skeleton of the State machine to control data transmission. The Input/Output port were defined in the top level module with support for the bidirectional SDA port.

A different interface type for the heart rate strap was investigated. ANT+ is a open standard for personal area networks that already include a specification for a heart rate monitor. ANT+ is being adopted as the defacto standard for consumer biometric devices. Garmin and Polar both use this standard for their newer models of heart rate straps. A dual Bluetooth ANT+ module was ordered for experimentation. I already use a Garmin system and own a ANT+ heart rate strap and a speed/cadence module. Using Bluetooth to connect to both the heart rate and cellphone requires the bluetooth adapter to operate in master mode which will cause some implementation headaches. Using ANT+ allows the bluetooth adapter to operate in slave mode to connect to the cellphone and ANT+ for devices that need to communicate with the FPGA alone.

TABLE 8
Ben Smith: Tasks Assigned - Last Week

Task	Hours Worked	Status
Refine Problem Statement	2.0	80%
Revising Design Contract	10.0	80%
Work Breakdown Structure	10.0	100%
Verilog I2C interface	15.0	15%

TABLE 9
Ben Smith: Tasks Assigned - Next Week

Task	Hours Worked	Status
Scheduling and Gantt Chart	10.0	90%
IMU I2C interface	25.0	80%
ANT+ experimentation	10.0	10%