相对简单CPU设计

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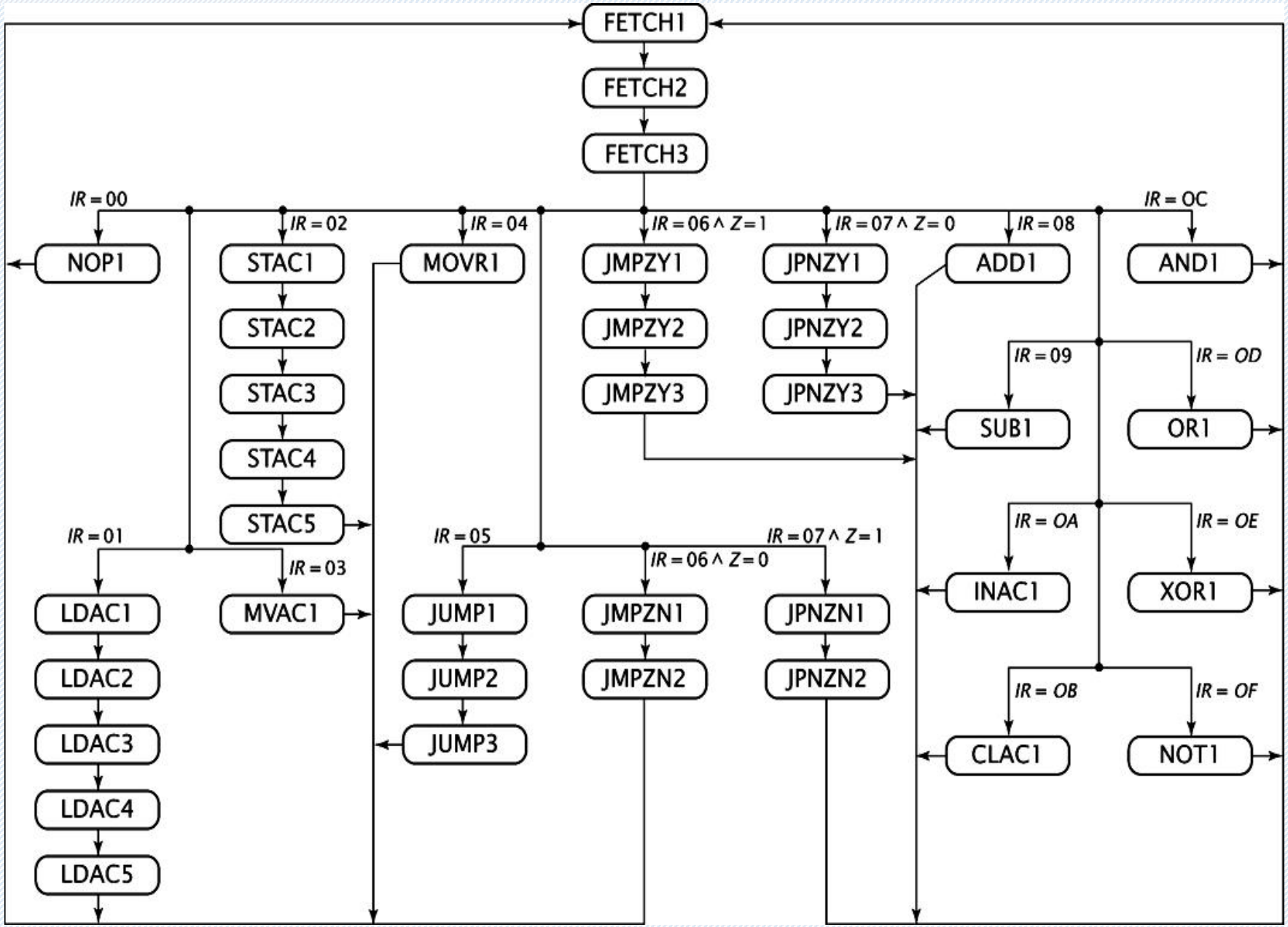

FETCH1
FETCH2
FETCH3
IR = 00
NOP1
IR = 02
STAC1
STAC2
STAC3
STAC4
STAC5
IR = 04
MOVR1
IR = 06 ∧ Z = 1
JMPZY1
JMPZY2
JMPZY3
IR = 07 ∧ Z = 0
JPNZY1
JPNZY2
JPNZY3
IR = 08
ADD1
IR = 09
SUB1
IR = OA
INAC1
IR = OB
CLAC1
IR = OC
AND1
IR = OD
OR1
IR = OE
XOR1
IR = OF
NOT1
IR = 01
LDAC1
LDAC2
LDAC3
LDAC4
LDAC5
IR = 03
MVAC1
IR = 05
JUMP1
JUMP2
JUMP3
IR = 06 ∧ Z = 0
JMPZN1
JMPZN2
IR = 07 ∧ Z = 1
JPNZN1
JPNZN2

一、指令与状态

第一个状态：

LDAC1: DR←M，PC←PC＋1，AR←AR＋1

第二个状态：

LDAC2: TR←DR，DR←M，PC←PC＋1

LDAC3: AR←DR，TR

LDAC4: DR←M

LDAC5: AC←DR

STAC1: DR←M，PC←PC＋1，AR←AR＋1

STAC2: TR←DR，DR←M，PC←PC＋1

STAC3: AR←DR，TR

STAC4: DR←AC

STAC5: M←DR

ADD1: AC←AC＋R，IF（AC＋R＝0）THEN Z←1 ELSE Z←0

SUB1: AC←AC－R，IF（AC－R＝0）THEN Z←1 ELSE Z←0

INAC1: AC←AC＋1，IF（AC＋1＝0）THEN Z←1 ELSE Z←0

CLAC1: AC←0，Z←1

AND1: AC←AC∧R，IF（AC∧R＝0）THEN Z←1 ELSE Z←0

OR1: AC←AC∨R，IF（AC∨R＝0）THEN Z←1 ELSE Z←0

XOR1: AC←AC⊕ R，IF（AC⊕ R＝0）THEN Z←1 ELSE Z←0

NOT1: AC←AC'，IF（AC'＝0）THEN Z←1 ELSE Z←0

MVAC1: R←AC

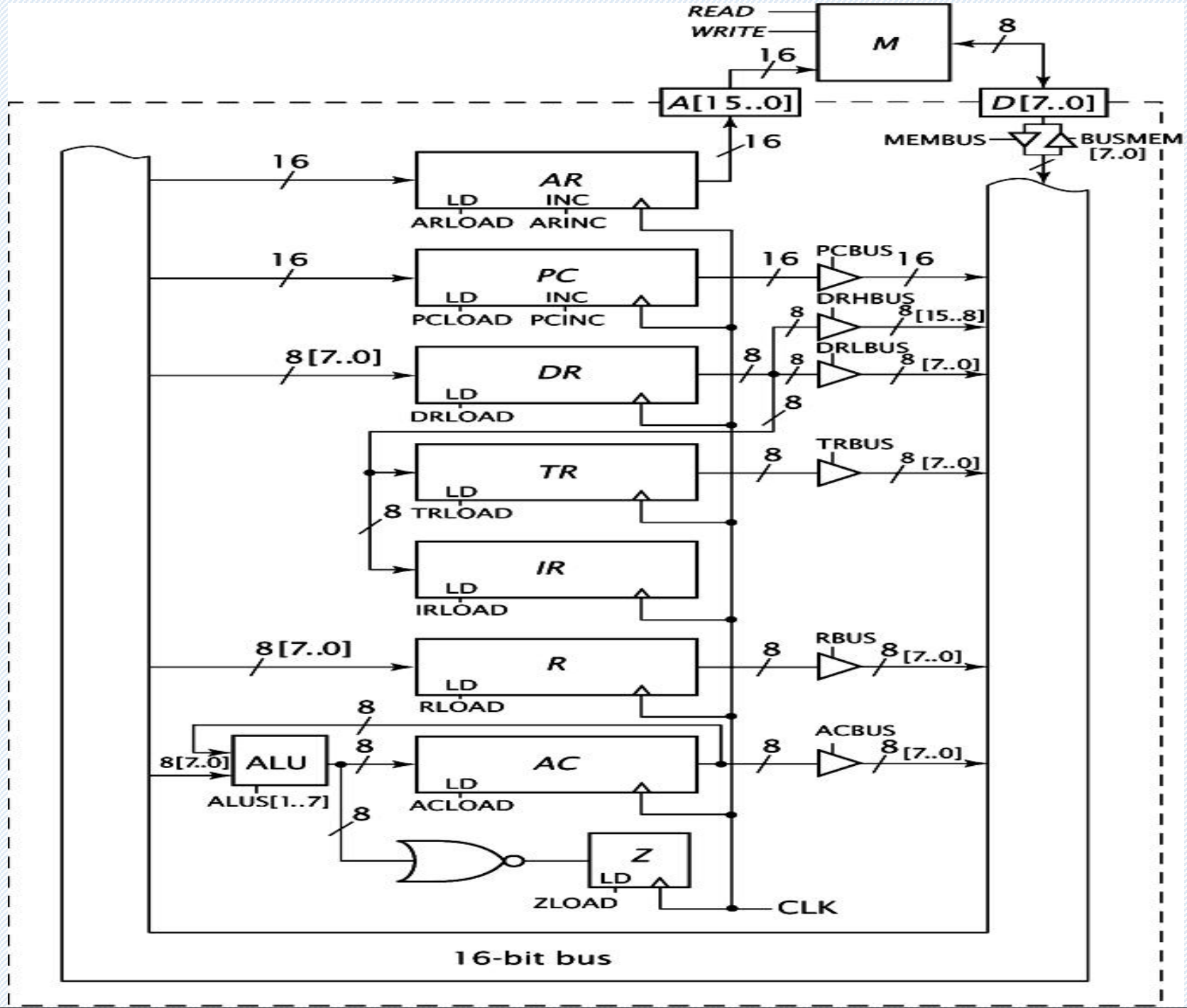
MOVR1: AC←R

JUMP1: DR←M，AR←AR+1

JUMP2: TR←DR，DR←M

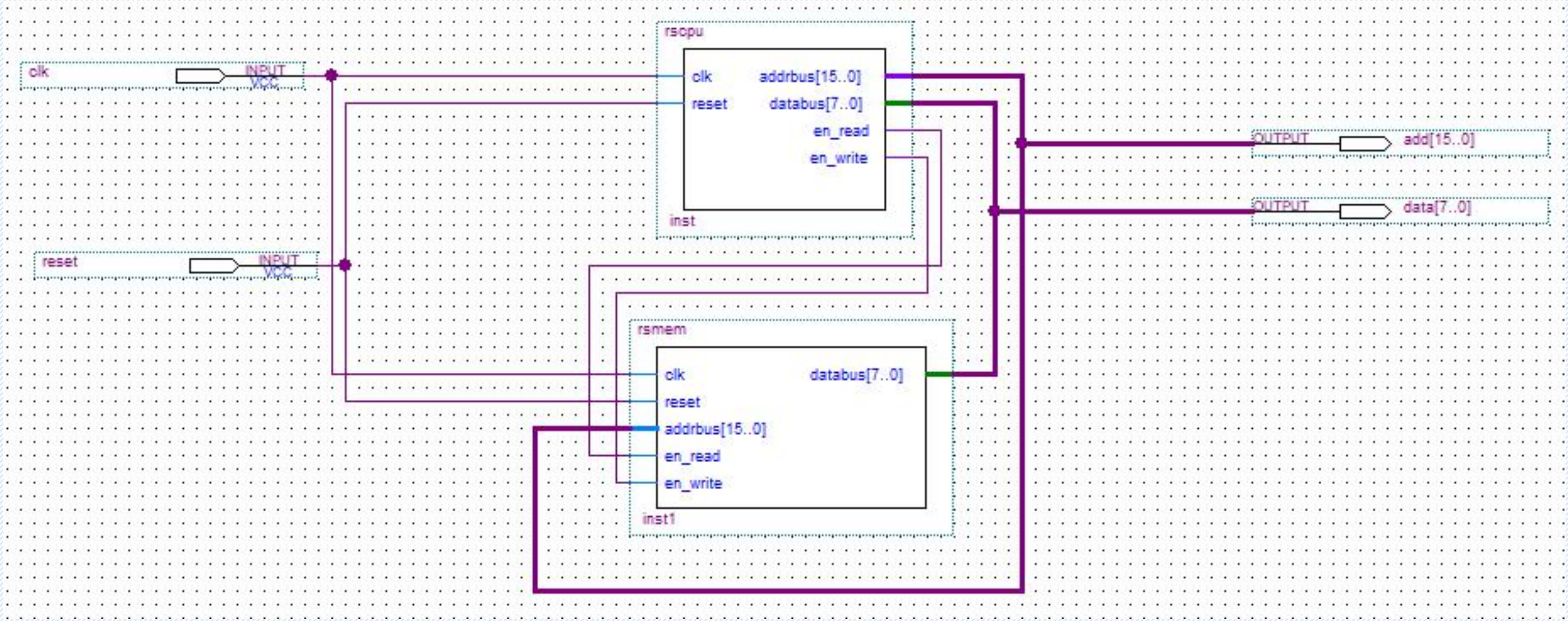
JUMP3: PC←DR，TR

一、数据通路

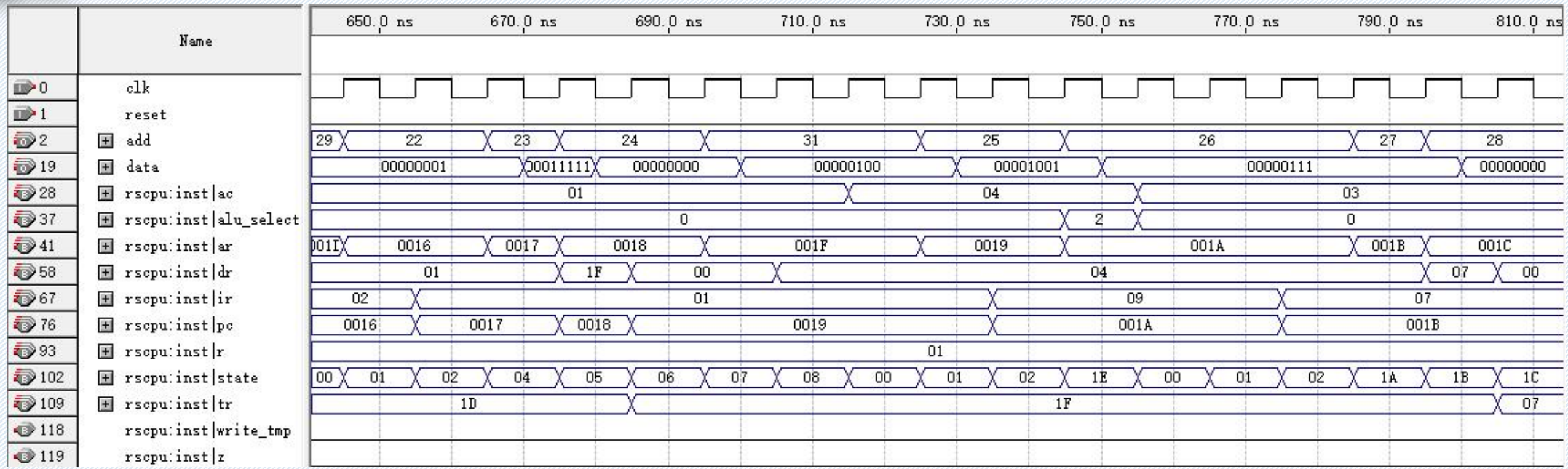

READ
WRITE
M
16
8
A[15..0]
D[7..0]
MEMBUS
BUSMEM
[7..0]
16
AR
LD
INC
ARLOAD
ARINC
PC
PCLOAD
PCINC
PCBUS
DRHBUS
DRLBUS
8[7..0]
DR
DRLOAD
[15..8]
[7..0]
TR
TRLOAD
TRBUS
IR
IRLOAD
R
RLOAD
RBUS
ALU
ALUS[1..7]
AC
ACLOAD
ACBUS
Z
ZLOAD
CLK
16-bit bus

PART 02
仿真结果

一、仿真结果

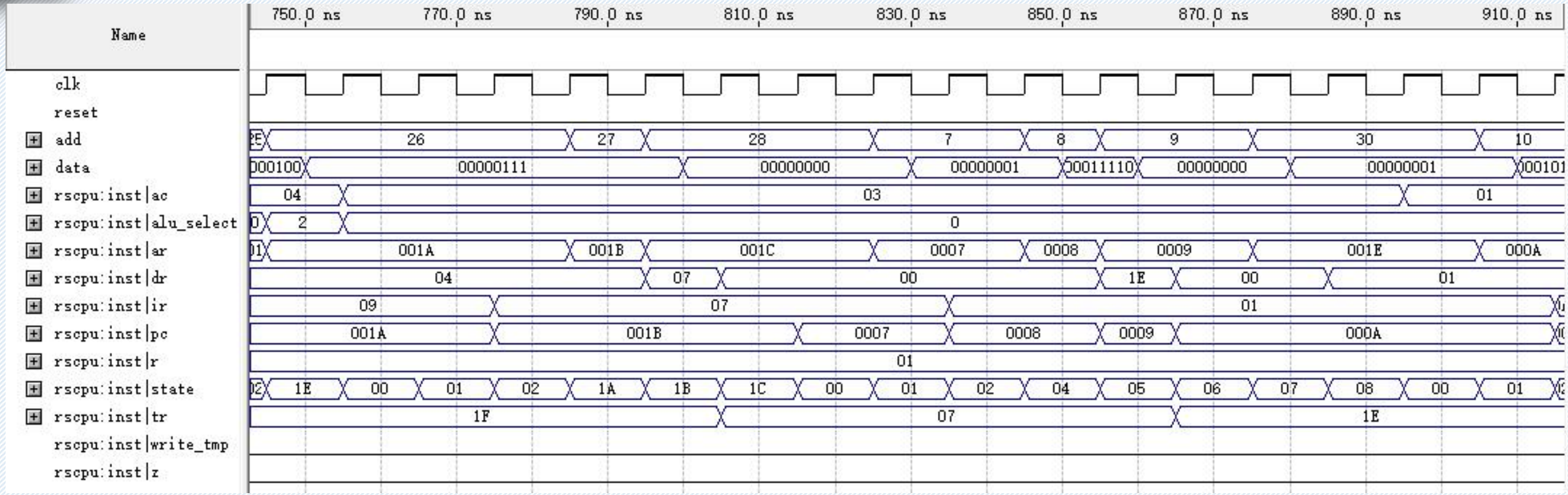

clk
INPUT
reset
INPUT
rscpu
clk
reset
addrbus[15..0]
databus[7..0]
en_read
en_write
inst
OUTPUT
add[15..0]
OUTPUT
data[7..0]
rsmem
clk
reset
addrbus[15..0]
en_read
en_write
databus[7..0]
inst1

一、仿真结果




```
22 => RSLDAC,
23 => std_logic_vector(to_unsigned(n_addr, 8)),
24 => X"00",
25 => RSSUB,
26 => RSJPNZ,
```

一、仿真结果




```
25 => RSSUB,
26 => RSJPNZ,
27 => std_logic_vector(to_unsigned(loop_addr, 8)),
28 => X"00",
7 => RSLDAC,        -- loop
8 => std_logic_vector(to_unsigned(i_addr, 8)),
9 => X"00",
```