相对简单CPU设计

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PART 01

数据通路与指令

一、指令与状态

第一个状态：

LDAC1: DR←M，PC←PC＋1，AR←AR＋1

第二个状态：

LDAC2: TR←DR，DR←M，PC←PC＋1

LDAC3: AR←DR，TR

LDAC4: DR←M

LDAC5: AC←DR

STAC1: DR←M，PC←PC＋1，AR←AR＋1

STAC2: TR←DR，DR←M，PC←PC＋1

STAC3: AR←DR，TR

STAC4: DR←AC

STAC5: M←DR

ADD1: AC←AC＋R，IF（AC＋R＝0）THEN Z←1 ELSE Z←0

SUB1: AC←AC－R，IF（AC－R＝0）THEN Z←1 ELSE Z←0

INAC1: AC←AC＋1，IF（AC＋1＝0）THEN Z←1 ELSE Z←0

CLAC1: AC←0，Z←1

AND1: AC←AC∧R，IF（AC∧R＝0）THEN Z←1 ELSE Z←0

OR1: AC←AC∨R，IF（AC∨R＝0）THEN Z←1 ELSE Z←0

XOR1: AC←AC⊕ R，IF（AC⊕ R＝0）THEN Z←1 ELSE Z←0

NOT1: AC←AC'，IF（AC'＝0）THEN Z←1 ELSE Z←0

MVAC1: R←AC

MOVR1: AC←R

JUMP1: DR←M，AR←AR+1

JUMP2: TR←DR，DR←M

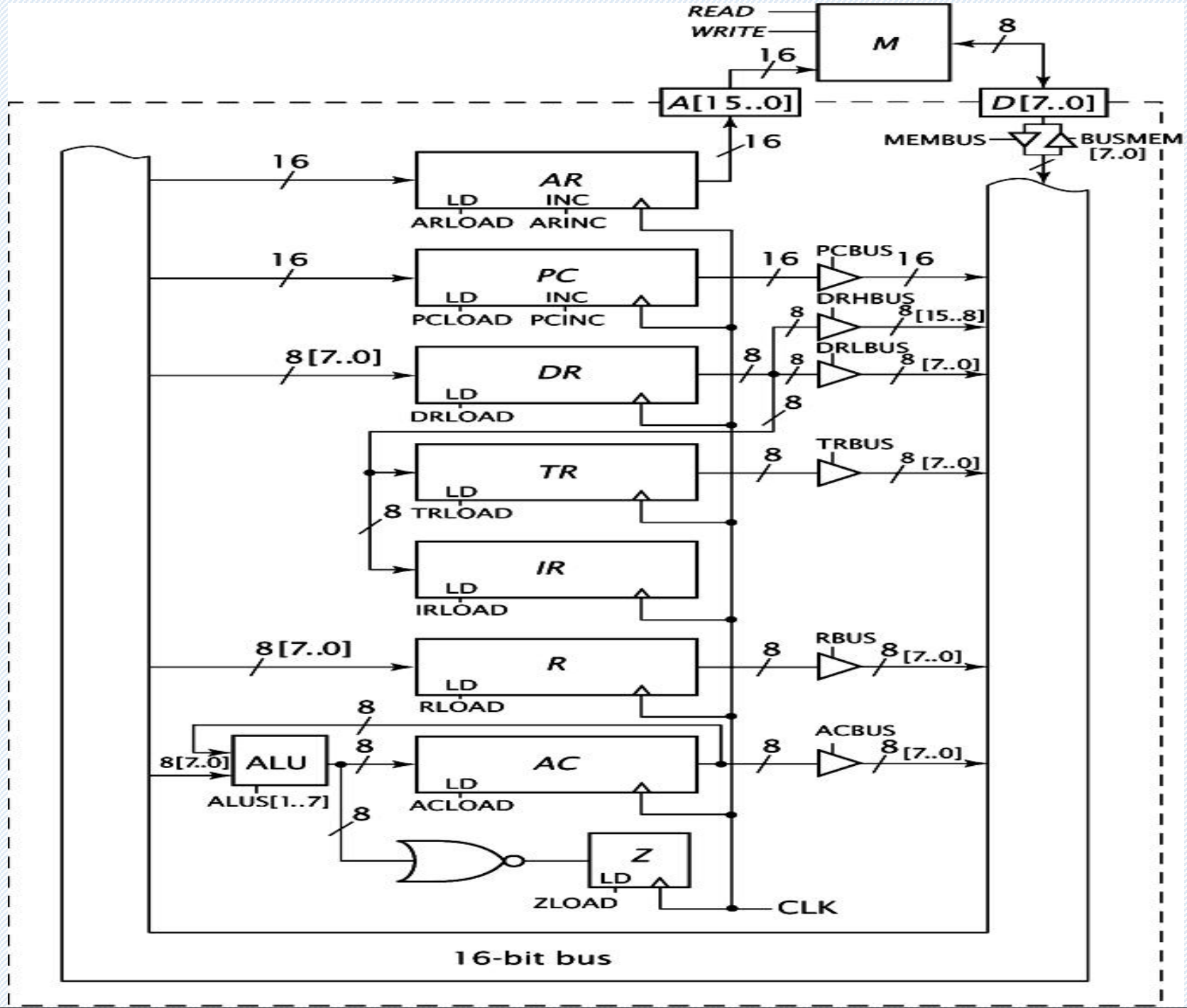
JUMP3: PC←DR，TR

一、数据通路

FETCH1: AR←PC

FETCH2: DR←M，
PC←PC＋1

FETCH3: IR←BUS，
AR←PC



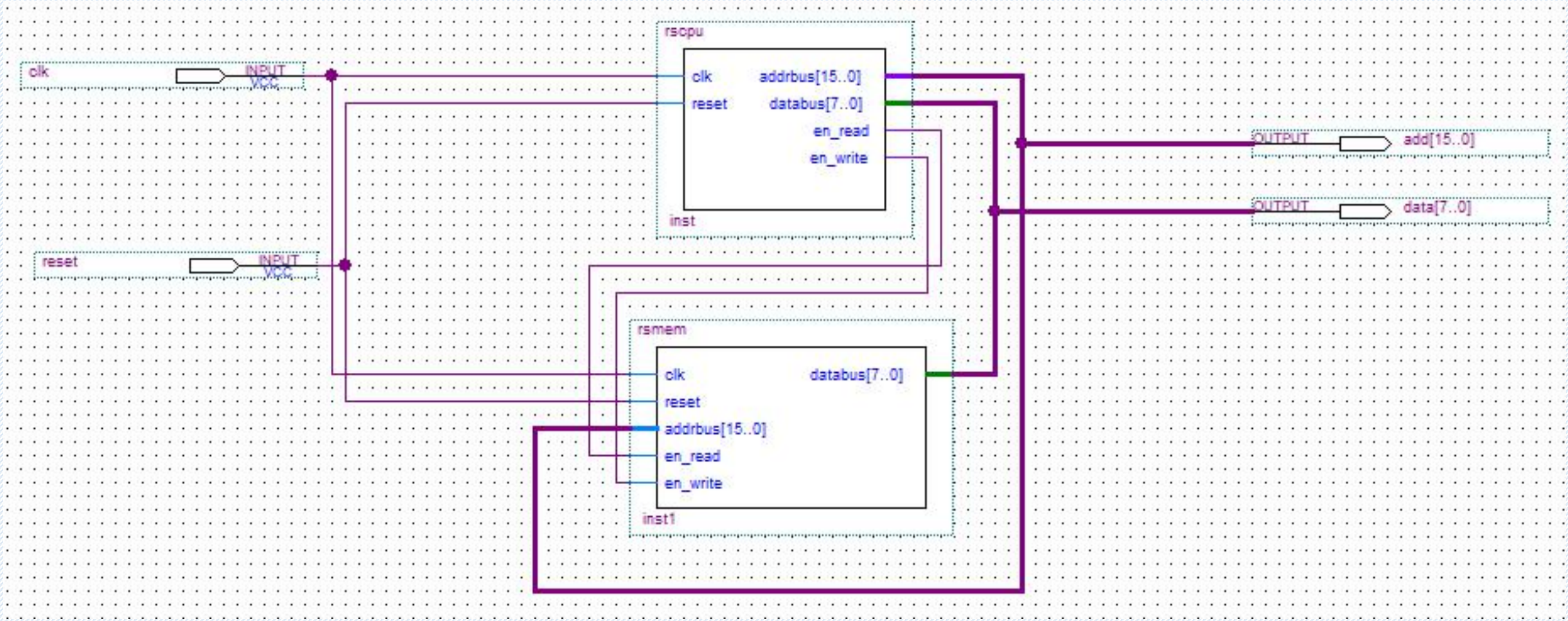
一、内存指令执行过程

0、将AC清0
1、将AC存到29号地址
2、将AC存到30号地址
3、将30号地址的值传到AC
4、AC++
5、将AC存到30号地址
6、AC——>R
7、将29号地址的值传到AC
8、AC=R+AC
9、将AC存到29号地址
10、将31号地址的值传到AC
11、AC=AC-R
12、IF AC！=0 跳转到第3步

最终实现1累加到n

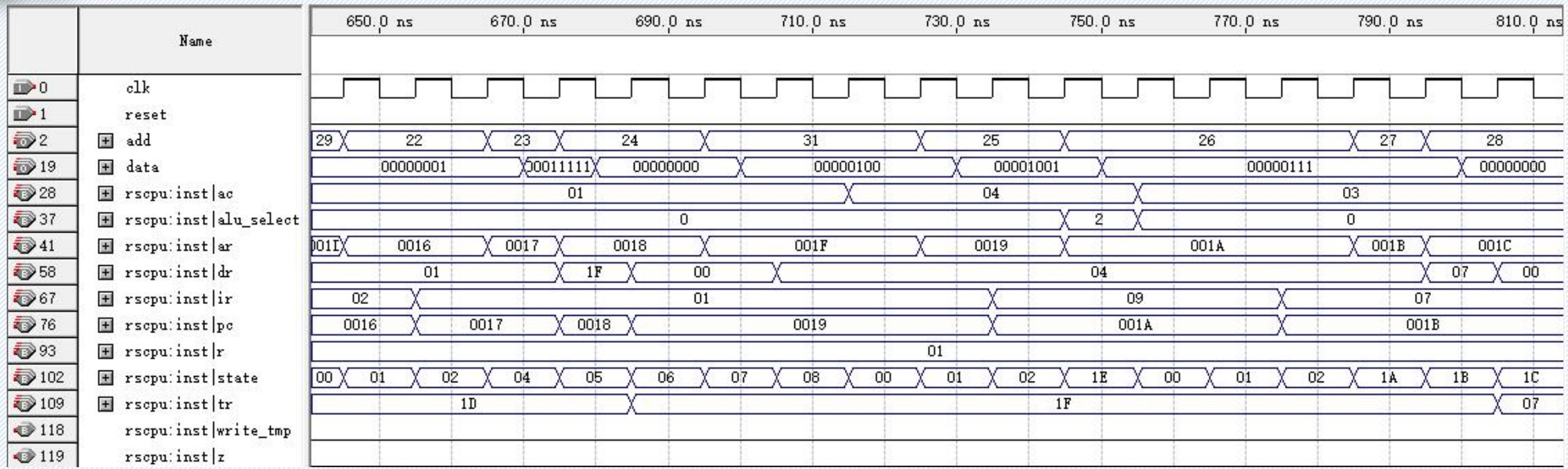
```
0 => RSCLAC,
1 => RSSTAC,
2 => std_logic_vector(to_unsigned(total_addr, 8)),
3 => X"00",
4 => RSSTAC,
5 => std_logic_vector(to_unsigned(i_addr, 8)),
6 => X"00",
7 => RSLDAC,  -- loop
8 => std_logic_vector(to_unsigned(i_addr, 8)),
9 => X"00",
10 => RSINAC,
11 => RSSTAC,
12 => std_logic_vector(to_unsigned(i_addr, 8)),
13 => X"00",
14 => RSMVAC,
15 => RSLDAC,
16 => std_logic_vector(to_unsigned(total_addr, 8)),
17 => X"00",
18 => RSADD,
19 => RSSTAC,
20 => std_logic_vector(to_unsigned(total_addr, 8)),
21 => X"00",
22 => RSLDAC,
23 => std_logic_vector(to_unsigned(n_addr, 8)),
24 => X"00",
25 => RSSUB,
26 => RSJPNZ,
27 => std_logic_vector(to_unsigned(loop_addr, 8)),
28 => X"00",
29 => X"00",  -- total
30 => X"00",  -- i
31 => X"04",  -- n
```

一、顶层文件


clk
INPUT
reset
INPUT
rscpu
clk
reset
addrbus[15..0]
databus[7..0]
en_read
en_write
inst
OUTPUT
add[15..0]
OUTPUT
data[7..0]
rsmem
clk
reset
addrbus[15..0]
en_read
en_write
databus[7..0]
inst1

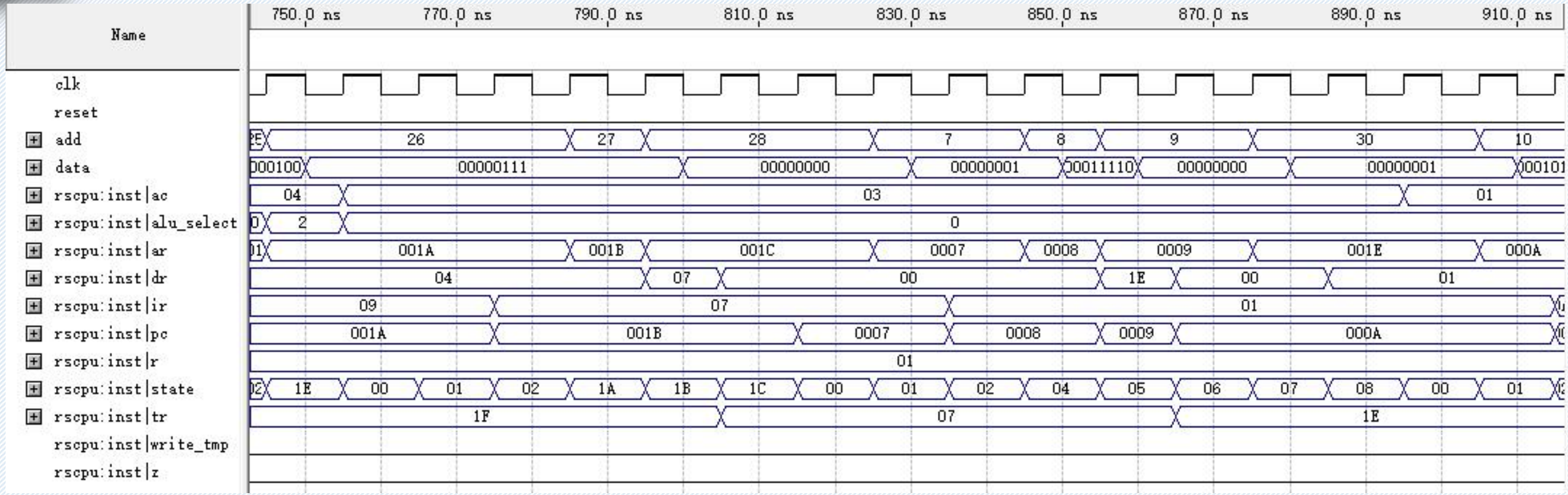
PART 02
仿真结果

一、仿真结果




```
22 => RSLDAC,
23 => std_logic_vector(to_unsigned(n_addr, 8)),
24 => X"00",
25 => RSSUB,
26 => RSJPNZ,
```

一、仿真结果




```
25 => RSSUB,
26 => RSJPNZ,
27 => std_logic_vector(to_unsigned(loop_addr, 8)),
28 => X"00",
7 => RSLDAC,        -- loop
8 => std_logic_vector(to_unsigned(i_addr, 8)),
9 => X"00",
```

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谢谢观看