计算机系统设计

相对简单CPU设计报告

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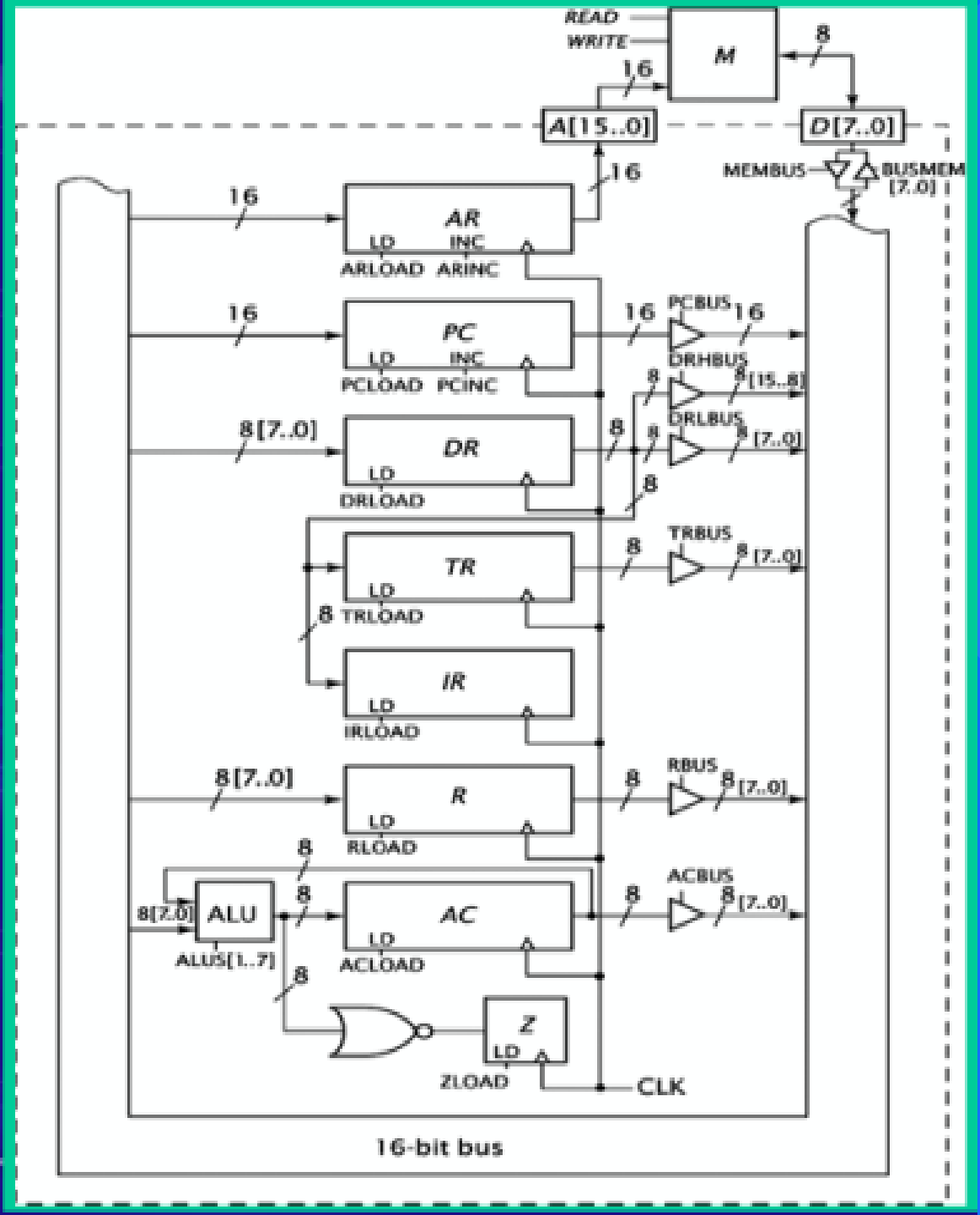
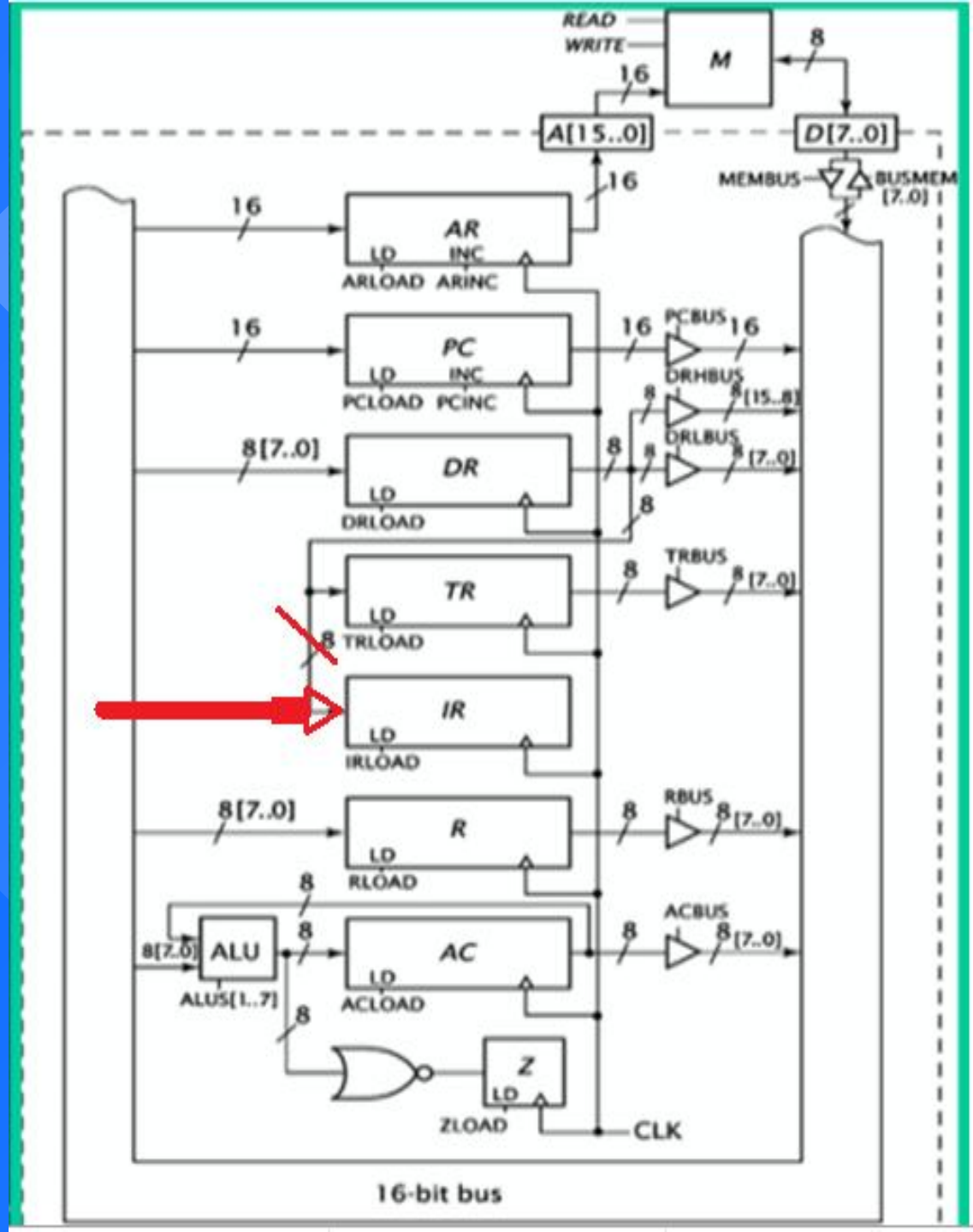
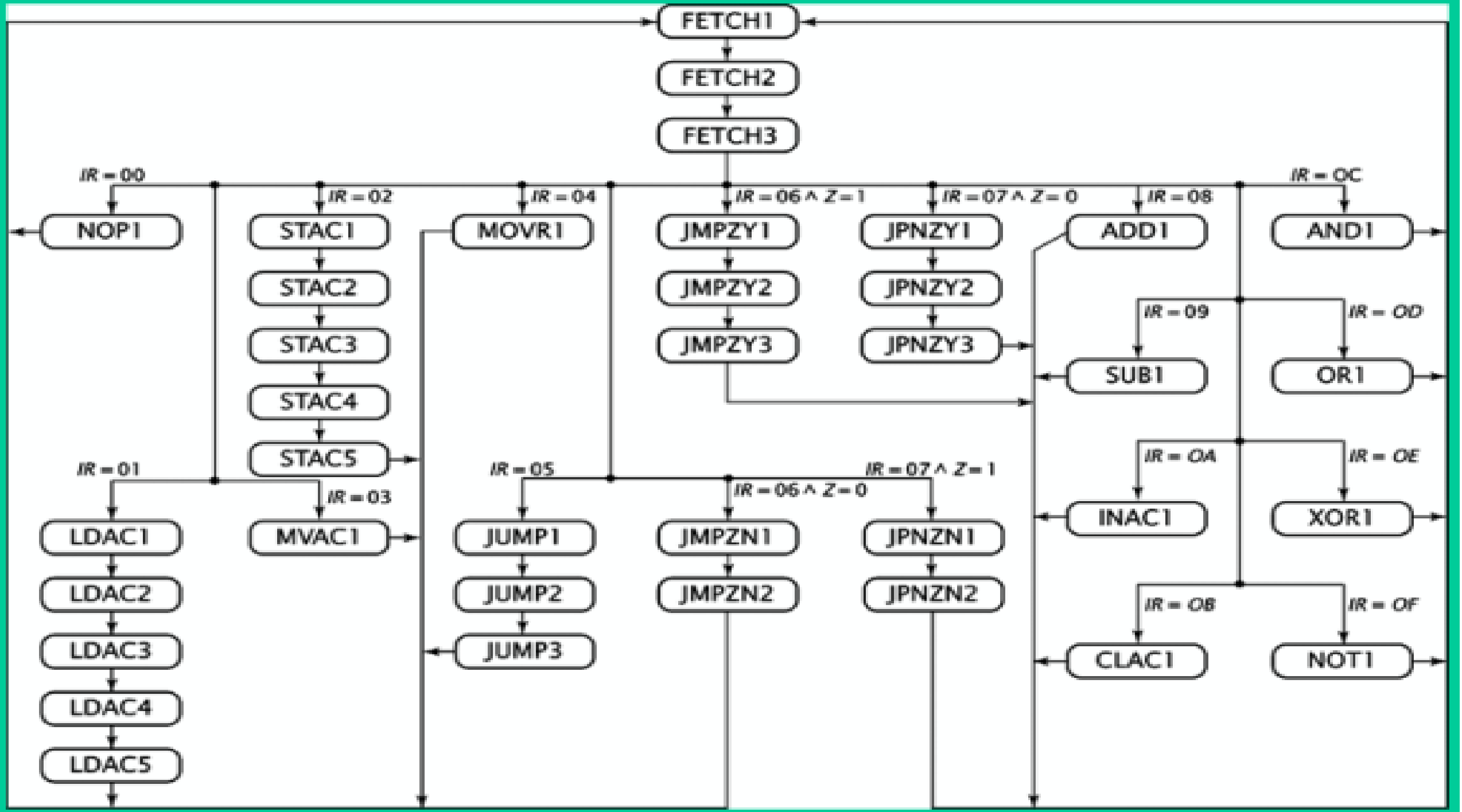
01

PART ONE

数据通路与指令状态划分


READ
WRITE
M
16
8
A[15..0]
D[7..0]
MEMBUS
BUSMEM
[7..0]
AR
LD
INC
ARLOAD
ARINC
PC
PCLOAD
PCINC
PCBUS
DRHBUS
[15..8]
DR
DRLOAD
DRLBUS
[7..0]
TR
TRLOAD
TRBUS
IR
IRLOAD
R
RLOAD
RBUS
ALU
ALUS[1..7]
AC
ACLOAD
ACBUS
Z
ZLOAD
CLK
16-bit bus


READ
WRITE
M
16
8
A[15..0]
D[7..0]
MEMBUS
BUSMEM
[7..0]
AR
LD
INC
ARLOAD
ARINC
PC
PCLOAD
PCINC
PCBUS
DRHBUS
[15..8]
DR
DRLOAD
DRLBUS
[7..0]
TR
TRLOAD
TRBUS
IR
IRLOAD
R
RLOAD
RBUS
ALU
ALUS[1..7]
AC
ACLOAD
ACBUS
Z
ZLOAD
CLK
16-bit bus


FETCH1
FETCH2
FETCH3
IR = 00
NOP1
IR = 02
STAC1
STAC2
STAC3
STAC4
STAC5
IR = 04
MOVR1
IR = 06 ^ Z = 1
JMPZY1
JMPZY2
JMPZY3
IR = 07 ^ Z = 0
JPNZY1
JPNZY2
JPNZY3
IR = 08
ADD1
IR = 09
SUB1
IR = 0C
AND1
IR = 0D
OR1
IR = 0A
INAC1
IR = 0E
XOR1
IR = 0B
CLAC1
IR = 0F
NOT1
IR = 01
LDAC1
LDAC2
LDAC3
LDAC4
LDAC5
IR = 03
MVAC1
IR = 05
JUMP1
JUMP2
JUMP3
IR = 06 ^ Z = 0
JMPZN1
JMPZN2
IR = 07 ^ Z = 1
JPNZN1
JPNZN2

Fetch 1: AR <- PC

Fetch2: IR <- M, PC++

Fetch3: AR <- PC

Fetch 1: AR <- PC

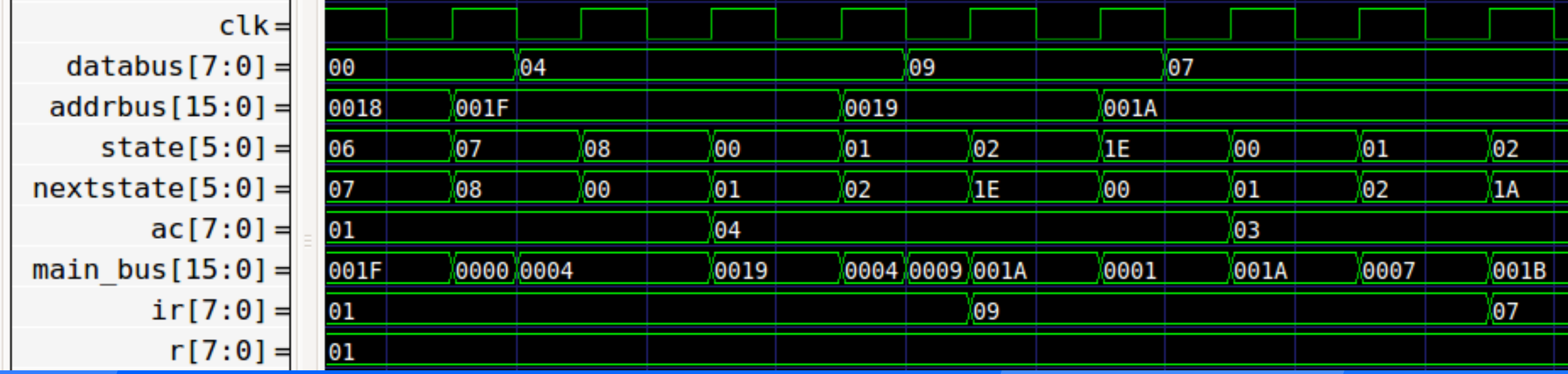
Fetch2: DR <- M, PC++

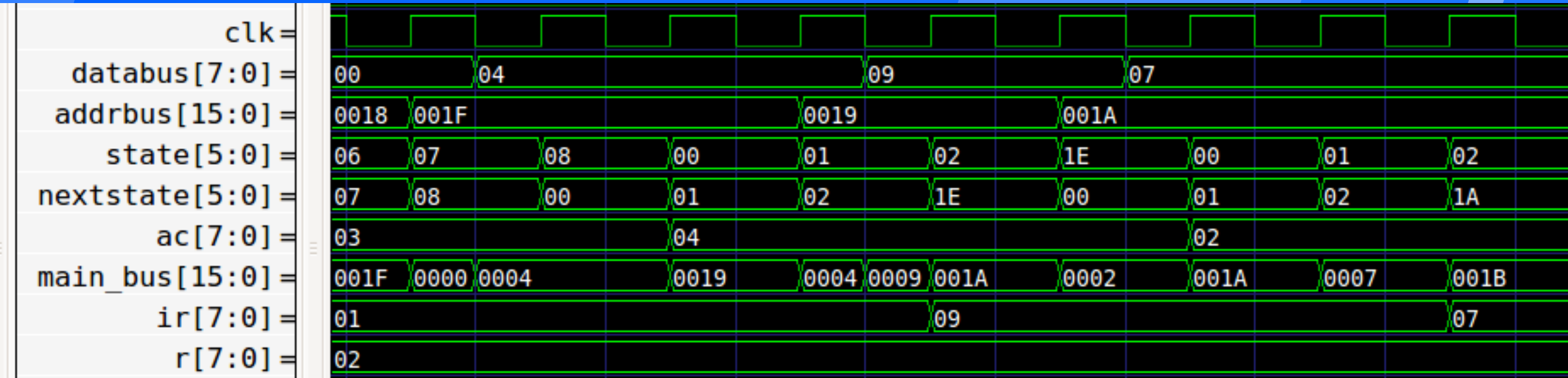
Fetch3: IR <- DR,AR <- PC

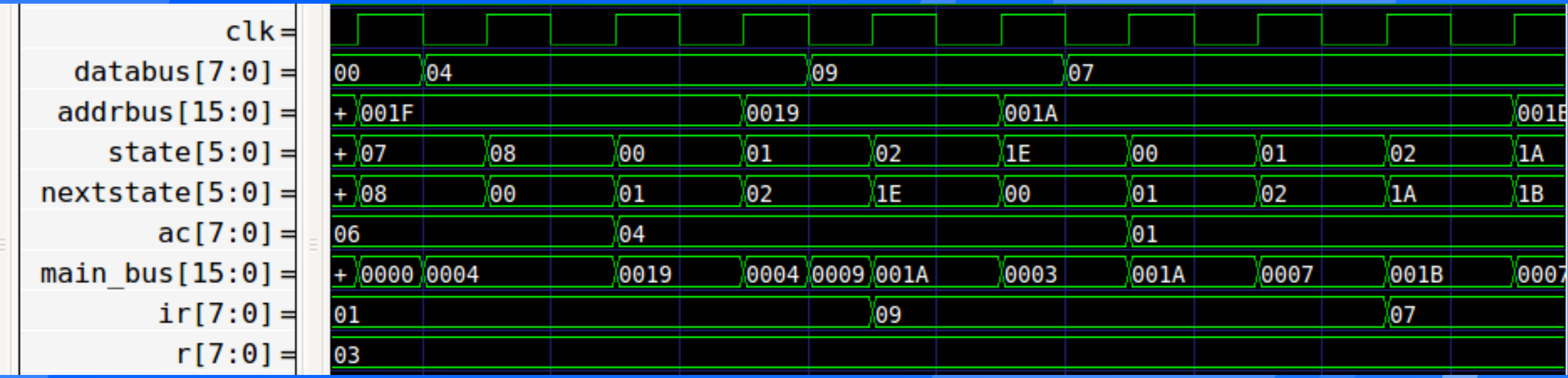
02

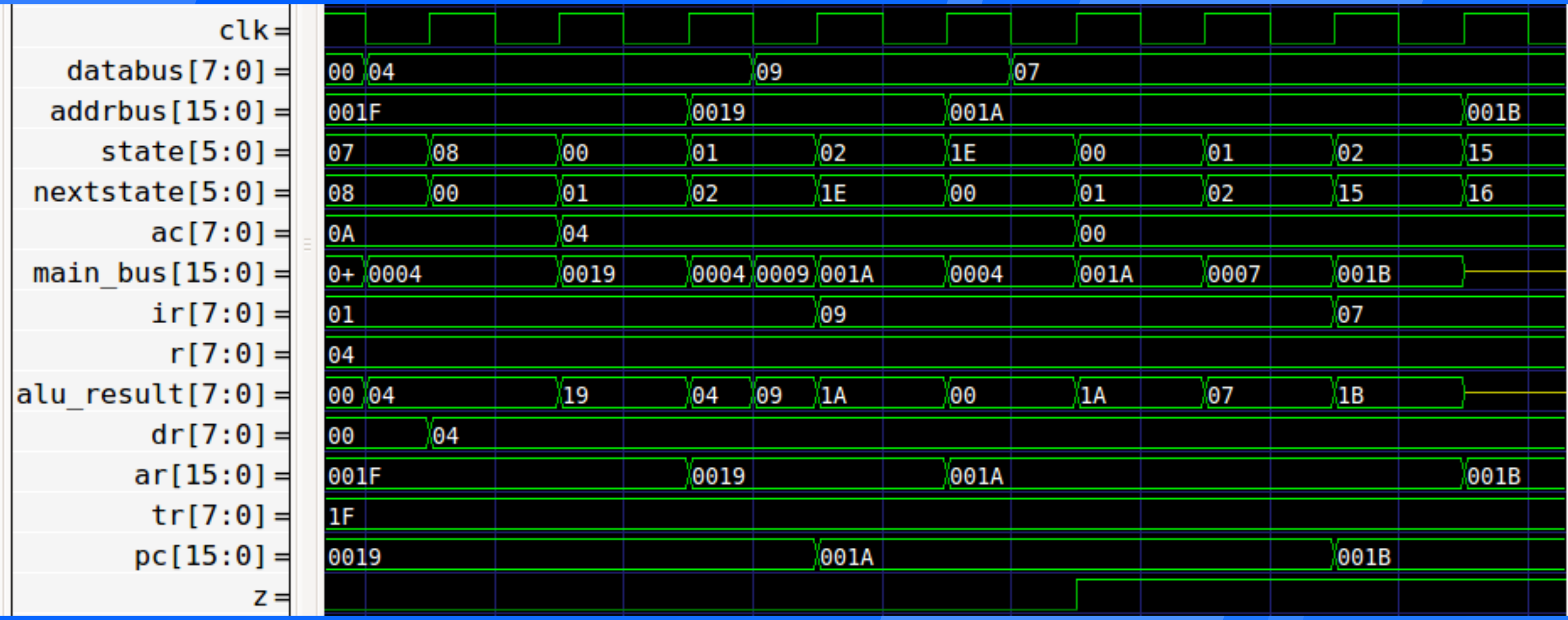
PART TWO

仿真结果与遇到的问题


clk
databus[7:0]
00 04 09 07
addrbus[15:0]
0018 001F 0019 001A
state[5:0]
06 07 08 00 01 02 1E 00 01 02
nextstate[5:0]
07 08 00 01 02 1E 00 01 02 1A
ac[7:0]
01 04 03
main_bus[15:0]
001F 0000 0004 0019 0004 0009 001A 0001 001A 0007 001B
ir[7:0]
01 09 07
r[7:0]
01


clk
databus[7:0]
00 04 09 07
addrbus[15:0]
0018 001F 0019 001A
state[5:0]
06 07 08 00 01 02 1E 00 01 02
nextstate[5:0]
07 08 00 01 02 1E 00 01 02 1A
ac[7:0]
03 04 02
main_bus[15:0]
001F 0000 0004 0019 0004 0009 001A 0002 001A 0007 001B
ir[7:0]
01 09 07
r[7:0]
02


clk
databus[7:0]
00
04
09
07
addrbus[15:0]
001F
0019
001A
001E
state[5:0]
07
08
00
01
02
1E
00
01
02
1A
nextstate[5:0]
08
00
01
02
1E
00
01
02
1A
1B
ac[7:0]
06
04
01
main_bus[15:0]
0000
0004
0019
0004
0009
001A
0003
001A
0007
001B
0007
ir[7:0]
01
09
07
r[7:0]
03


clk
databus[7:0]
00 04 09 07
addrbus[15:0]
001F 0019 001A 001B
state[5:0]
07 08 00 01 02 1E 00 01 02 15
nextstate[5:0]
08 00 01 02 1E 00 01 02 15 16
ac[7:0]
0A 04 00
main_bus[15:0]
0+ 0004 0019 0004 0009 001A 0004 001A 0007 001B
ir[7:0]
01 09 07
r[7:0]
04
alu_result[7:0]
00 04 19 04 09 1A 00 1A 07 1B
dr[7:0]
00 04
ar[15:0]
001F 0019 001A 001B
tr[7:0]
1F
pc[15:0]
0019 001A 001B
z

```
user@ubuntuvm:~/Documents/winter2018/rscpu_M-ir$ ./rscomp --wave=simu07.ghw
../../../src/ieee/numeric_std-body.v93:2098:7:@50ns:(assertion warning): NUMERIC
_STD.TO_INTEGER: metavalue detected, returning 0
./rscomp:error: bound check failure at rsmem.vhd:81
./rscomp:error: simulation failed
```

T A H N K S