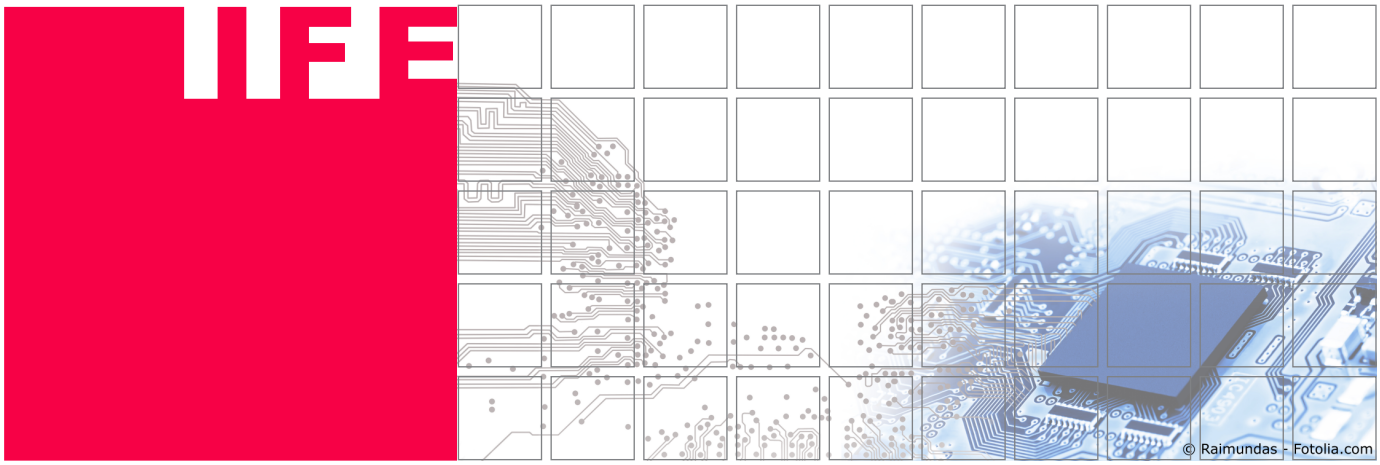
TU Graz

Institute of Electronics



Circuit Simulation

Delivery 4

Dominik Zupan

May 26, 2020

Contents

General Information

Please make a written documentation (in English or in German, PDF type preferred) of your results and upload this document and a single Workspace-Archive, containing all your simulation files to the TeachCenter.
Please upload both documents separately. As we will use the grading guidelines defined in TeachCenter, this will ease our work being able to directly comment the PDF. The **submission deadline** is **Monday, 22. June 2020**.

Exercise 1: ABM Modelling

The first exercise deals with analog behavioural model (ABM) modelling of components in PSpice. You can choose **one** of the given exercises

- Exercise 1.1: ABM Modelling of NMOS Transistor and
- Exercise 1.2: ABM Modelling of Operational Amplifier.

Exercise 1.1: ABM Modelling of NMOS Transistor

In a very simple model the drain current depending on the region of operation of an NMOS transistor could be modelled as described by Equation 1.

$$I_D = \begin{cases} 0 & V_{GS} < V_{TH}, \text{cutoff} \\ K \cdot \frac{W}{L} \cdot \left((V_{GS} - V_{TH}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right) & V_{GS} \geq V_{TH} \text{ and } V_{DS} < V_{GS} - V_{TH}, \text{ohmic} \\ \frac{K}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 & V_{GS} \geq V_{TH} \text{ and } V_{DS} \geq V_{GS} - V_{TH}, \text{saturation} \end{cases} \quad (1)$$

The goal of this exercise is to implement this simplified model using ABMs that are provided by PSpice. The constant $\beta = K \cdot \frac{W}{L}$ and V_{TH}, should be deduced from the transfer and output characteristic plots shown in Figure 1, Figure 2.

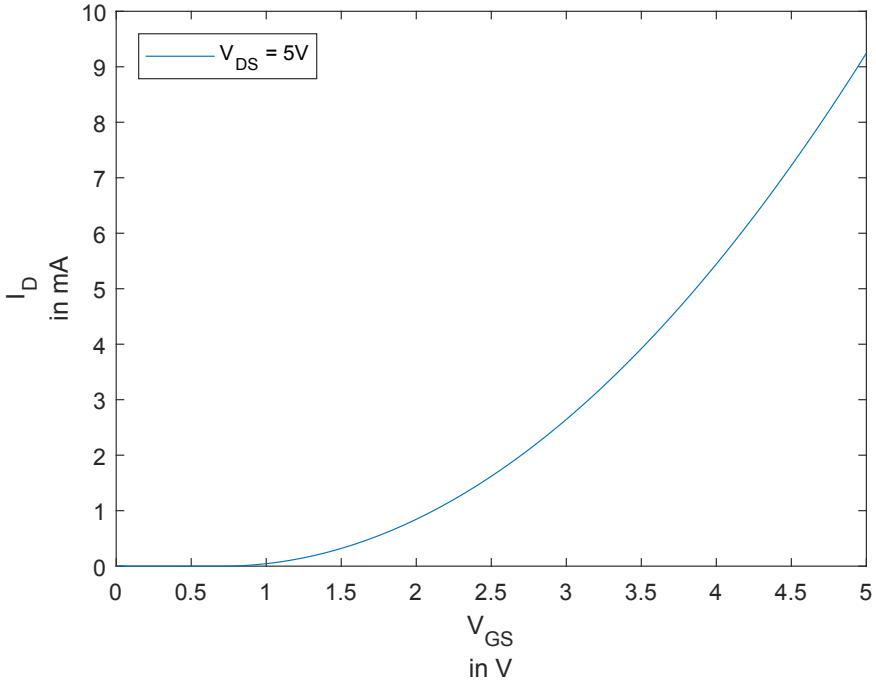


Figure 1: Transfer characteristic.

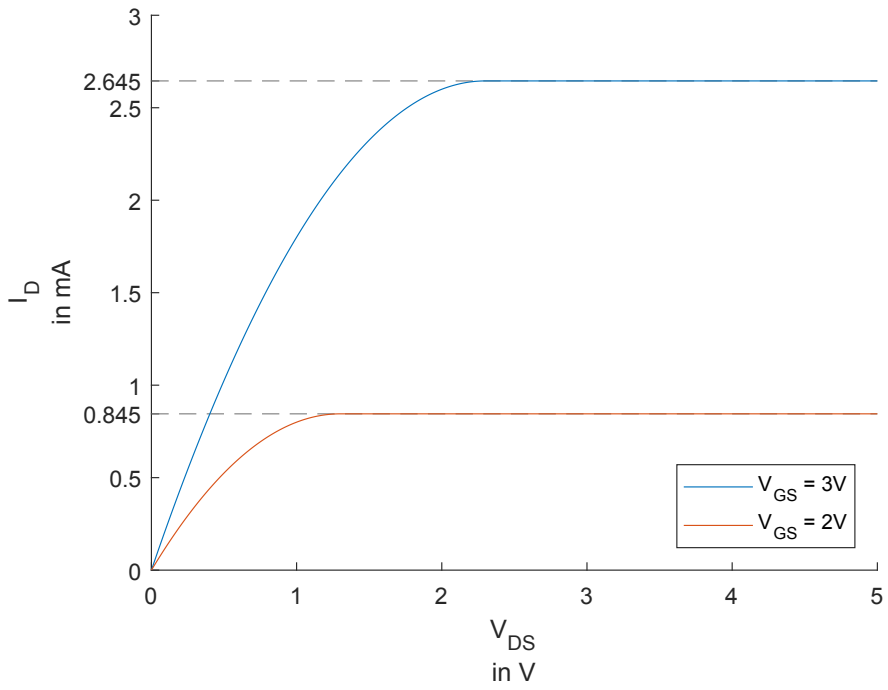


Figure 2: Output characteristic.

Complete the following tasks:

- Are the plotted characteristics and the model equations accounting for channel length modulation (CLM)? Why (not)?
- How large are the constants β and V_{TH}?
- Model the given NMOS characteristics using ABMs that are provided by PSpice. Hint: To model the conditional you could use the **GLIMIT** part.
- Show your schematic and the transfer and output characteristic plots, obtained by your models.

Exercise 1.2: ABM Modelling of Operational Amplifier

The goal of this exercise is to design an ABM for the operational amplifier (opamp) LF155/LT, in which the frequency response of the open loop gain is modeled. The macro model of the operational amplifier (OpAmp), is given in the library `biblio.zip` ▸ **`lin_tech.lib`**, that was already provided for Delivery 3.

Complete the following tasks:

- Derive the necessary characteristic values by means of simulation from the macro model.
- Which simulations are needed to achieve this? Which operating point should the circuit be in?
- Compare and plot the frequency and phase characteristics for the ABM and the macro model in one probe plot.

Exercise 2: Tracking ADC

In this exercise the digital part of a tracking analog-to-digital converter (ADC) should be designed. The analog part of the ADC is given in Figure 3. The reference voltage should be set to 5 V.

- First, the timing constraints for the already given part need to investigated. How large is the delay time of the inverter buffers for the different timing modes *Typical*, *Minimum*, *Maximum* and *Worst Case*. What is the difference between these timing models?
- Taking the analog part into account: How large is the delay time from a change in digital value to a new result on the output of the comparator? Can this value be clearly defined? Why (not)?
- Extend the circuit with TTL logic (74xx) gates, such that a 3-bit tracking ADC is resulting. You do not need to implement mechanisms to prevent underflowing or overflowing of the counter.
- Which range should the analog input signal be in, such that definitely no underflow or overflow is occuring.
- Show the proper operation of the tracking ADC, taking the previously defined constraints for the analog input signal into account. Use a clocking signal of 1 MHz at timing mode of *Typical*.
- Does the Tracking ADC still work properly for timing modes *Minimum*, *Maximum*, *Worst Case*. Why (not)?

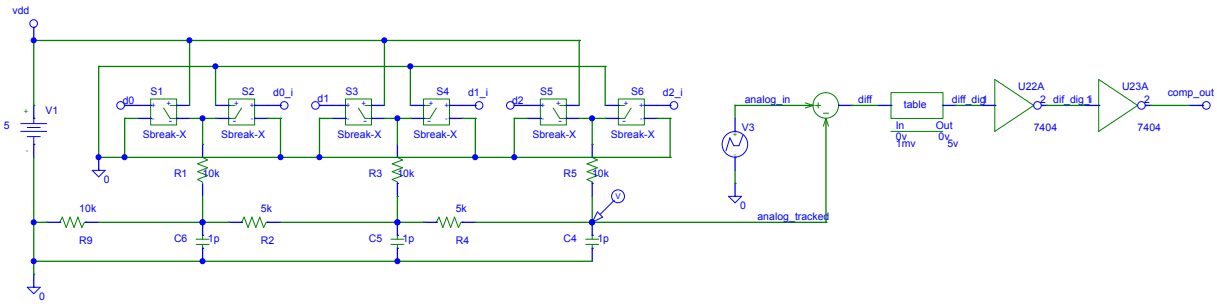


Figure 3: Analog part of tracking ADC.

Exercise 3: Individual Circuit

Design and simulate a(n) (small) electronic circuit of your free choice, which is of any interest to you!