Line Tracer 08

- Interrupt -

This lecture is based on

- [Timers]
- [Real-Time Systems]

1. Interrupt

How to Handle Hardware Events

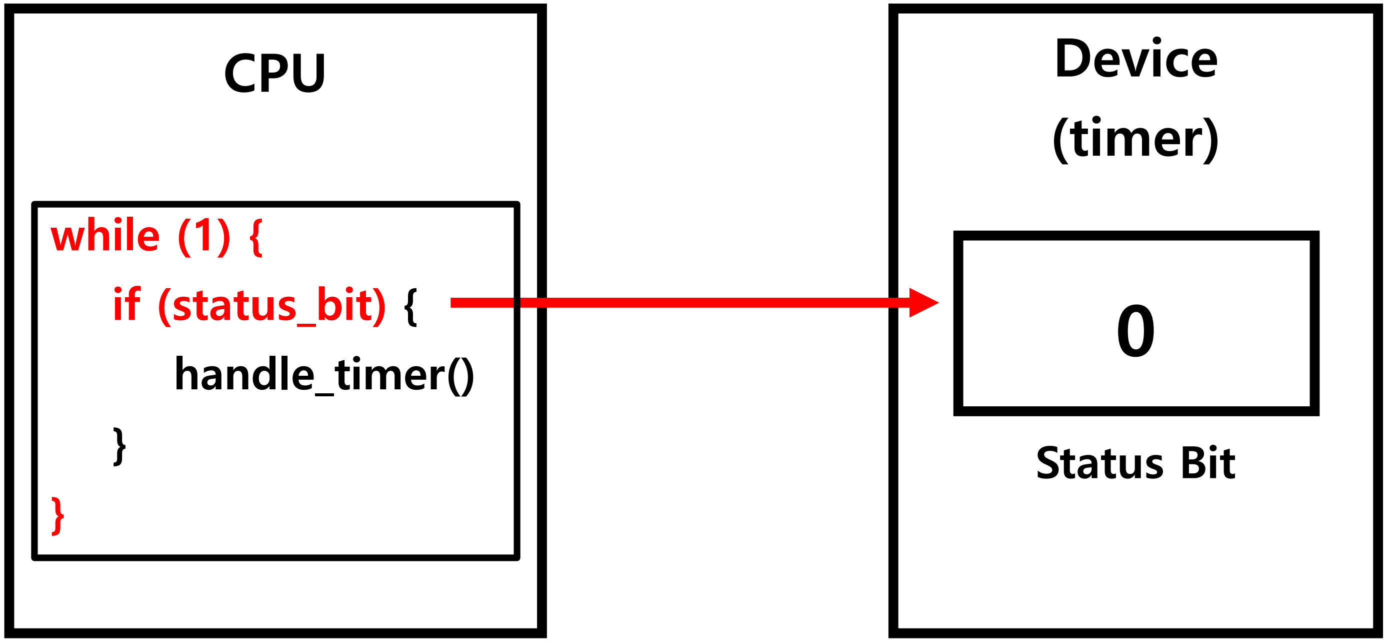
Polling

- CPU (Program) steadily checks whether event occurs
- Not hardware mechanism SW 방법으로 hw 상태체크

Interrupt

- Devices notice the CPU when event occurs
- Hardware mechanism

Polling



CPU

```
while (1) {
    if (status_bit) {
        handle_timer()
    }
}
```

Device

(timer)

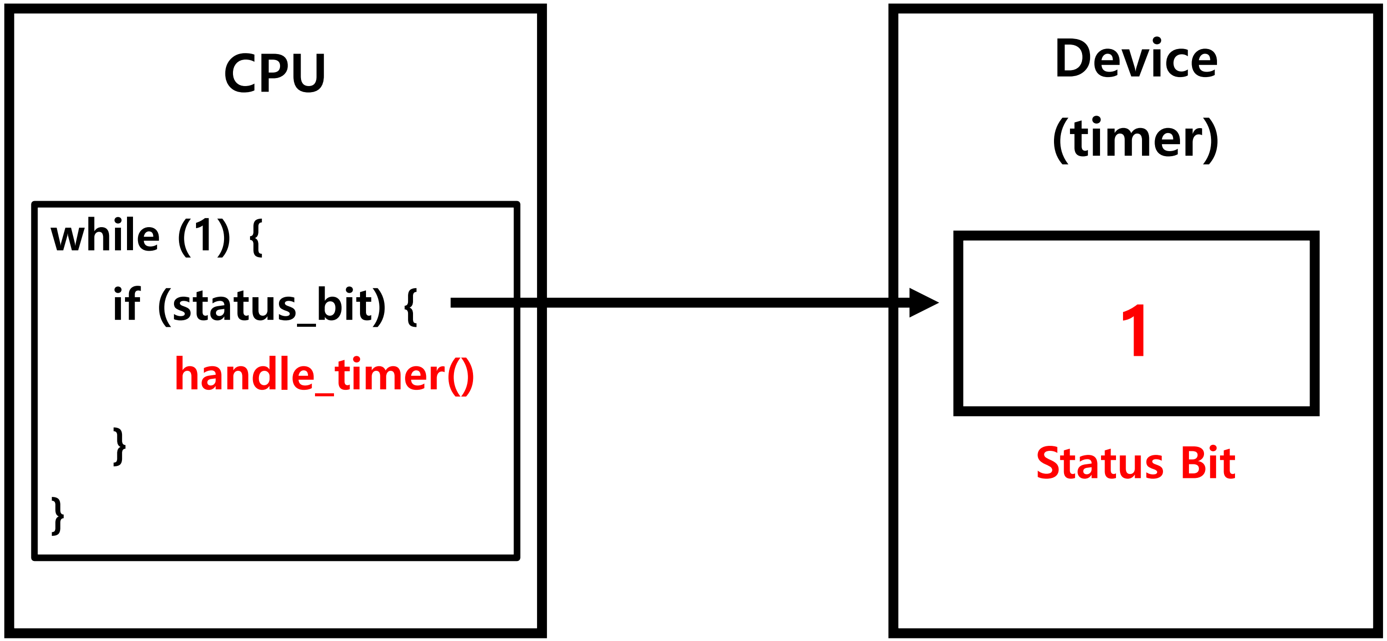
0

Status Bit

check device’s
status bit repeatedly

counter decreased

Polling



CPU

```
while (1) {
    if (status_bit) {
        handle_timer()
    }
}
```

Device (timer)

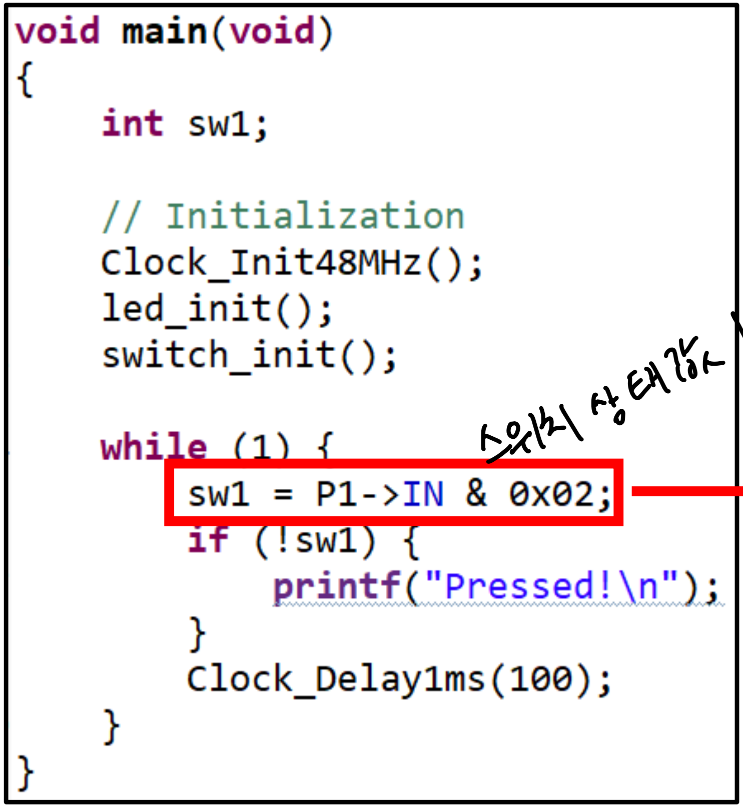
Status Bit

handle timer event

set status bit

when counter reaches 0

Polling Example

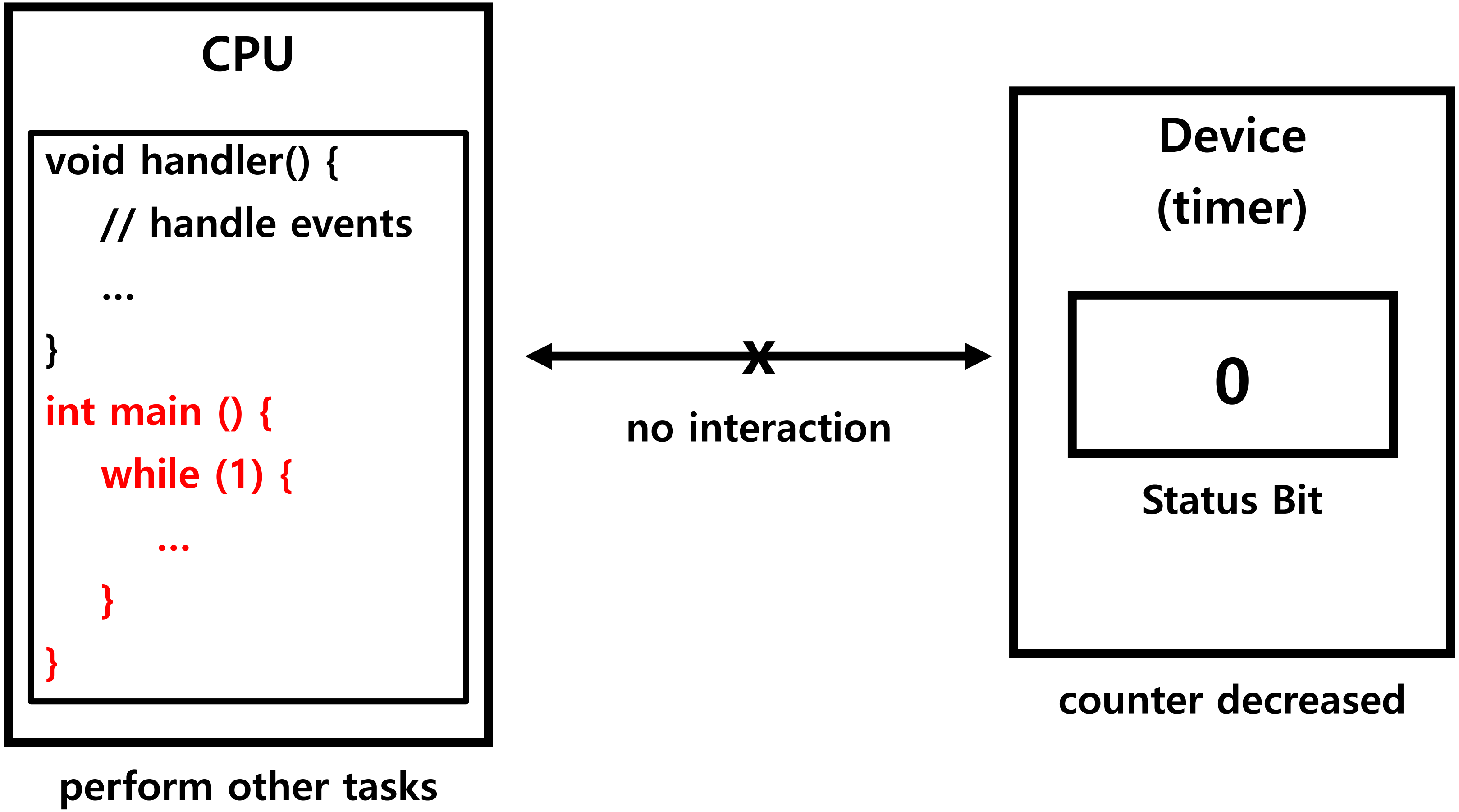


```c
void main(void)
{
    int sw1;

    // Initialization
    Clock_Init48MHz();
    led_init();
    switch_init();

    while (1) {
        sw1 = P1->IN & 0x02;
        if (!sw1) {
            printf("Pressed!\n");
        }
        Clock_Delay1ms(100);
    }
}
```

스위치 상태값 1→0 : 눌림

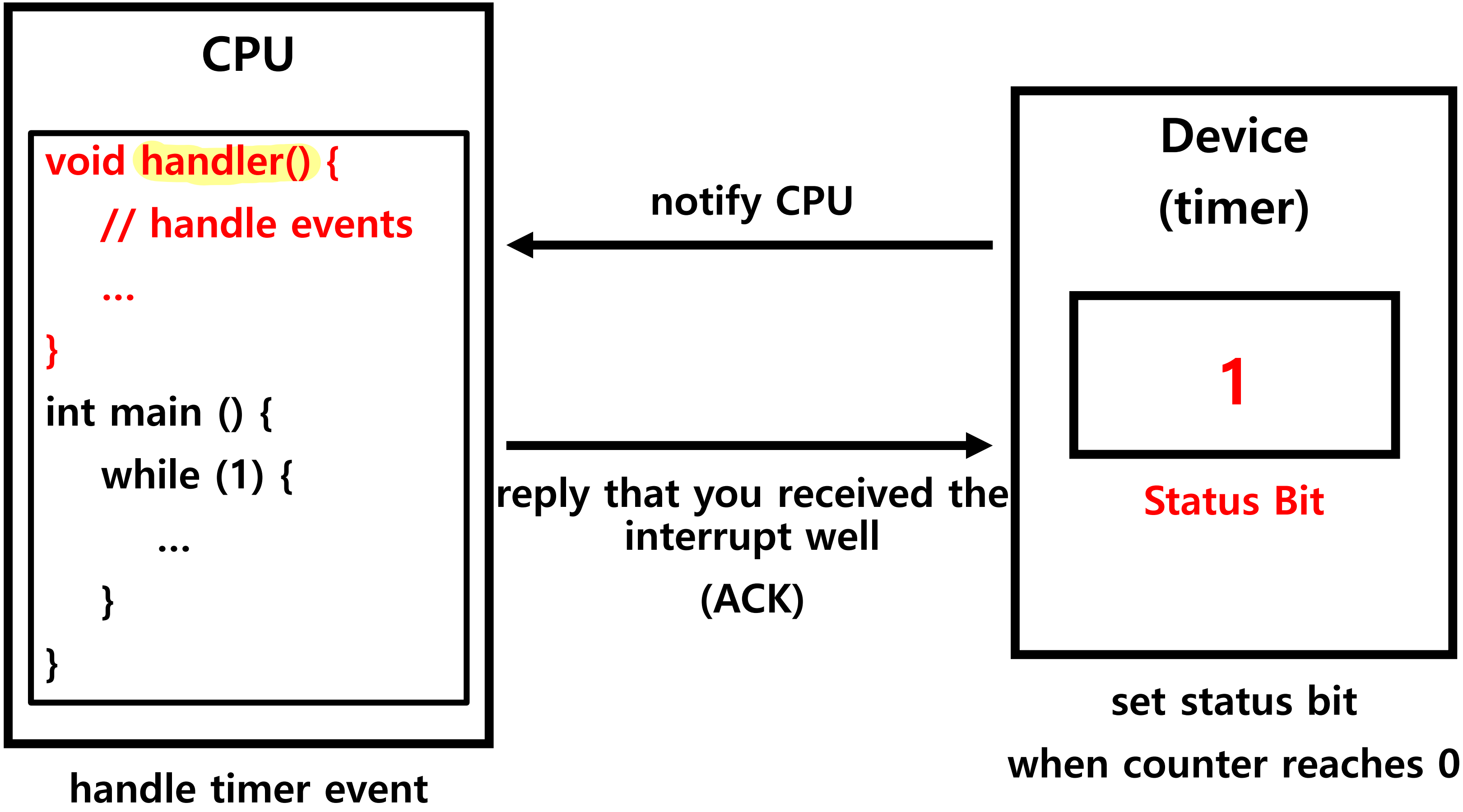
CPU checks the status of the switch periodically

Interrupt



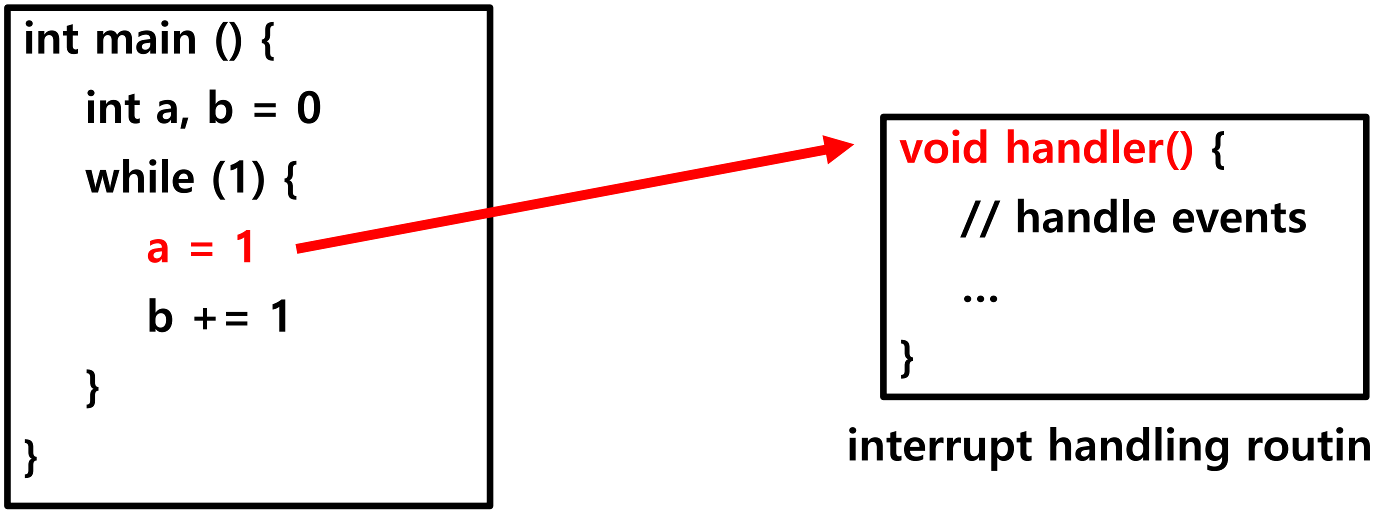
```
void handler() {
    // handle events
    …
}
int main () {
    while (1) {
        …
    }
}
```

Interrupt



```
void handler() {
    // handle events
    ...
}
int main () {
    while (1) {
        ...
    }
}
```

Interrupt Handling



```
int main () {
    int a, b = 0
    while (1) {
        a = 1
        b += 1
    }
}
```

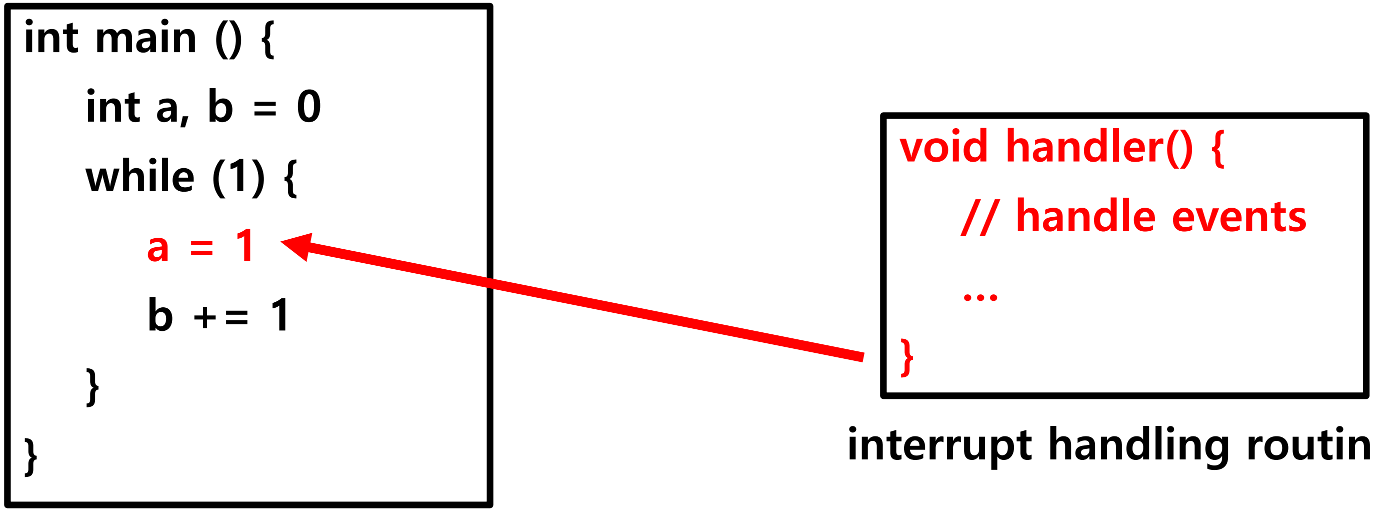
main routine

```
void handler() {
    // handle events
    ...
}
```

interrupt handling routine

when interrupt occurs while executing a= 1,
save main routine’s state and jump to the handler

Interrupt Handling



```
int main () {
    int a, b = 0
    while (1) {
        a = 1
        b += 1
    }
}
```

main routine

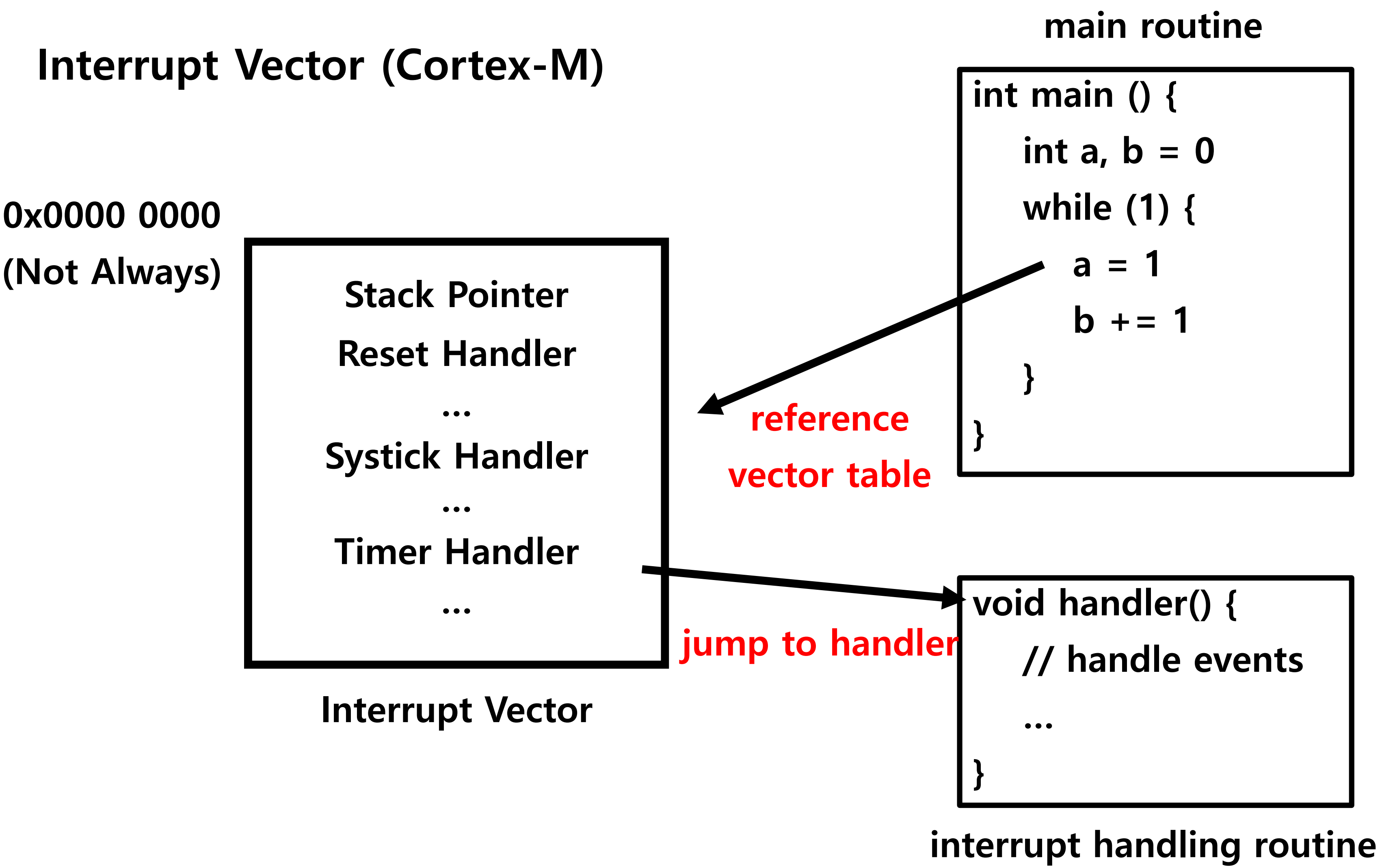
```
void handler() {
    // handle events
    ...
}
```

interrupt handling routine

after executing handler,

go back to the location previously executed

Interrupt Vector (Cortex-M)



0x0000 0000

(Not Always)

Stack Pointer

Reset Handler

...

Systick Handler

...

Timer Handler

...

Interrupt Vector

main routine

```
int main () {
    int a, b = 0
    while (1) {
        a = 1
        b += 1
    }
}
```

reference

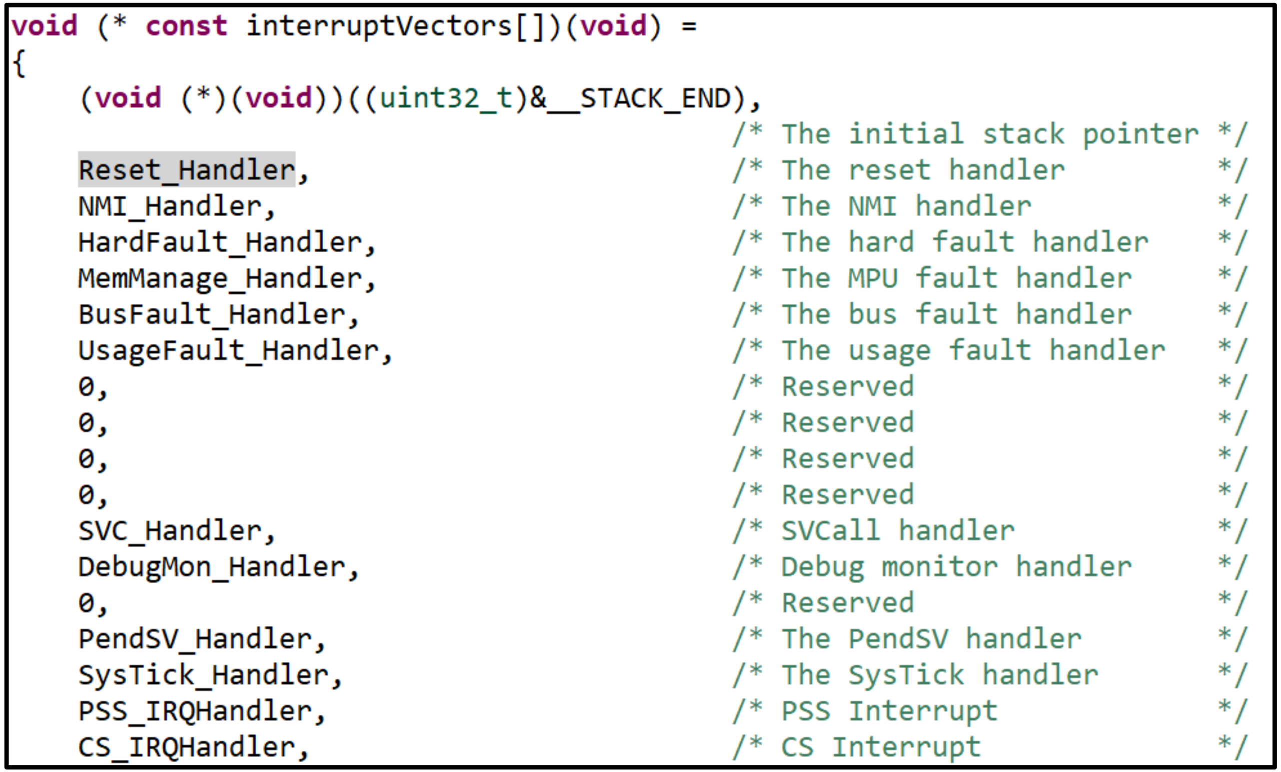
vector table

jump to handler

```
void handler() {
    // handle events
    ...
}
```

interrupt handling routine

Interrupt Vector (Cortex-M)



```
void (* const interruptVectors[])(void) =
{
    (void (*)(void))((uint32_t)&__STACK_END),
                                           /* The initial stack pointer */
    Reset_Handler,                         /* The reset handler         */
    NMI_Handler,                           /* The NMI handler           */
    HardFault_Handler,                     /* The hard fault handler    */
    MemManage_Handler,                     /* The MPU fault handler     */
    BusFault_Handler,                      /* The bus fault handler     */
    UsageFault_Handler,                    /* The usage fault handler   */
    0,                                     /* Reserved                  */
    0,                                     /* Reserved                  */
    0,                                     /* Reserved                  */
    0,                                     /* Reserved                  */
    SVC_Handler,                           /* SVCall handler            */
    DebugMon_Handler,                      /* Debug monitor handler     */
    0,                                     /* Reserved                  */
    PendSV_Handler,                        /* The PendSV handler        */
    SysTick_Handler,                       /* The SysTick handler       */
    PSS_IRQHandler,                        /* PSS Interrupt             */
    CS_IRQHandler,                         /* CS Interrupt              */
```

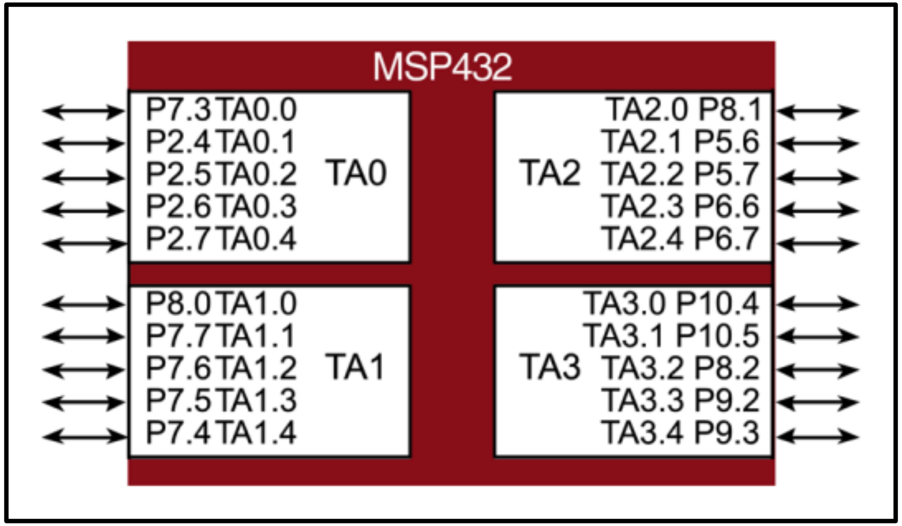
startup_msp432p401r_ccs.c, line 112

2. Timer Interrupt

MSP432 Timer A

MSP432 Timer A consists of

- 4 Timers TA0, TA1, TA2, TA3
- Each timer has submodules

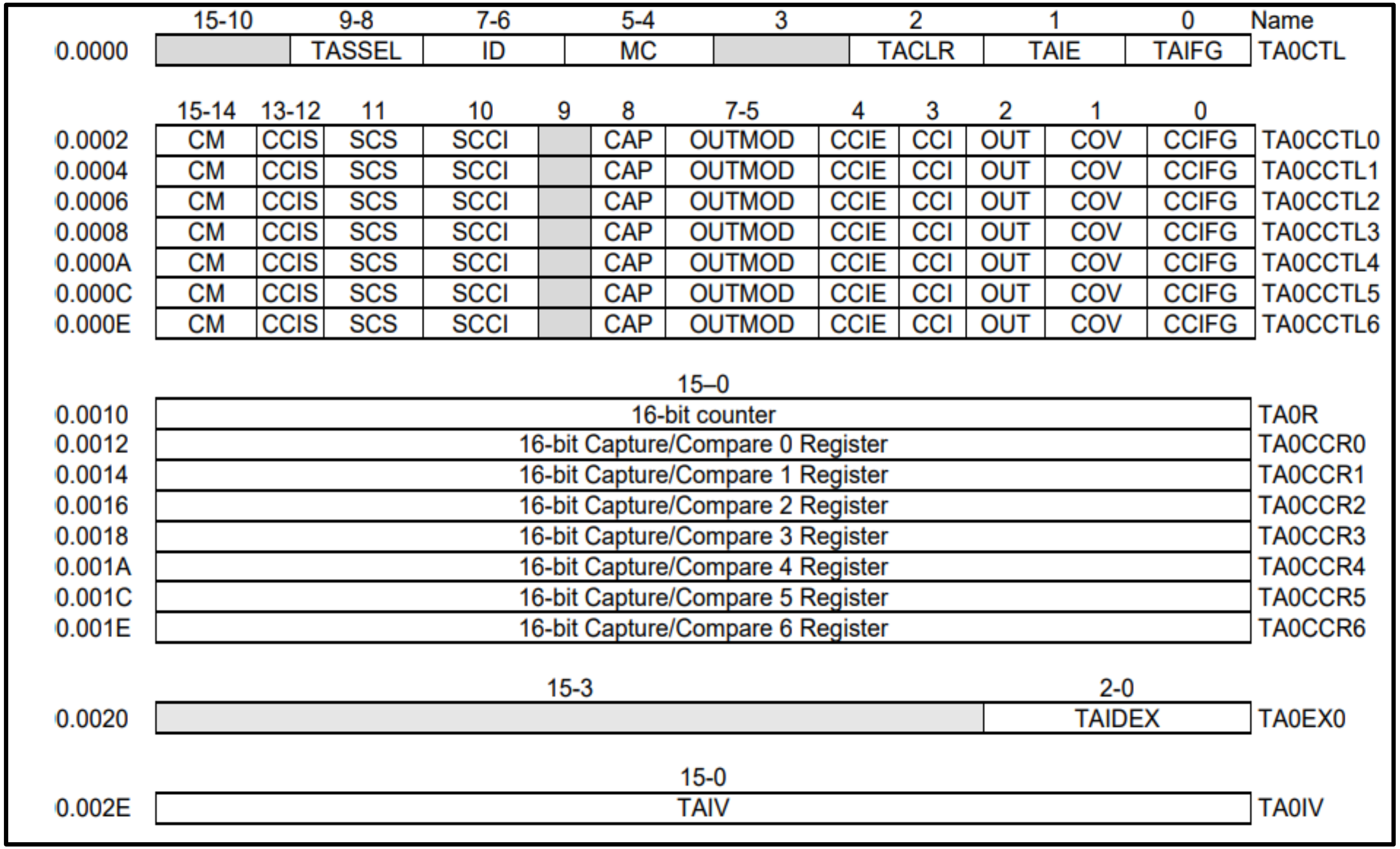


MSP432

TA0		TA2	
P7.3	TA0.0	TA2.0	P8.1
P2.4	TA0.1	TA2.1	P5.6
P2.5	TA0.2	TA2.2	P5.7
P2.6	TA0.3	TA2.3	P6.6
P2.7	TA0.4	TA2.4	P6.7

TA1		TA3	
P8.0	TA1.0	TA3.0	P10.4
P7.7	TA1.1	TA3.1	P10.5
P7.6	TA1.2	TA3.2	P8.2
P7.5	TA1.3	TA3.3	P9.2
P7.4	TA1.4	TA3.4	P9.3

Timer A Registers



	15-10	9-8	7-6	5-4	3	2	1	0	Name
0.0000		TASSEL	ID	MC		TACLR	TAIE	TAIFG	TA0CTL

	15-14	13-12	11	10	9	8	7-5	4	3	2	1	0	
0.0002	CM	CCIS	SCS	SCCI		CAP	OUTMOD	CCIE	CCI	OUT	COV	CCIFG	TA0CCTL0
0.0004	CM	CCIS	SCS	SCCI		CAP	OUTMOD	CCIE	CCI	OUT	COV	CCIFG	TA0CCTL1
0.0006	CM	CCIS	SCS	SCCI		CAP	OUTMOD	CCIE	CCI	OUT	COV	CCIFG	TA0CCTL2
0.0008	CM	CCIS	SCS	SCCI		CAP	OUTMOD	CCIE	CCI	OUT	COV	CCIFG	TA0CCTL3
0.000A	CM	CCIS	SCS	SCCI		CAP	OUTMOD	CCIE	CCI	OUT	COV	CCIFG	TA0CCTL4
0.000C	CM	CCIS	SCS	SCCI		CAP	OUTMOD	CCIE	CCI	OUT	COV	CCIFG	TA0CCTL5
0.000E	CM	CCIS	SCS	SCCI		CAP	OUTMOD	CCIE	CCI	OUT	COV	CCIFG	TA0CCTL6

	15–0	
0.0010	16-bit counter	TA0R
0.0012	16-bit Capture/Compare 0 Register	TA0CCR0
0.0014	16-bit Capture/Compare 1 Register	TA0CCR1
0.0016	16-bit Capture/Compare 2 Register	TA0CCR2
0.0018	16-bit Capture/Compare 3 Register	TA0CCR3
0.001A	16-bit Capture/Compare 4 Register	TA0CCR4
0.001C	16-bit Capture/Compare 5 Register	TA0CCR5
0.001E	16-bit Capture/Compare 6 Register	TA0CCR6

	15-3	2-0	
0.0020		TAIDEX	TA0EX0

	15-0	
0.002E	TAIV	TA0IV

Timer A Register – CTL

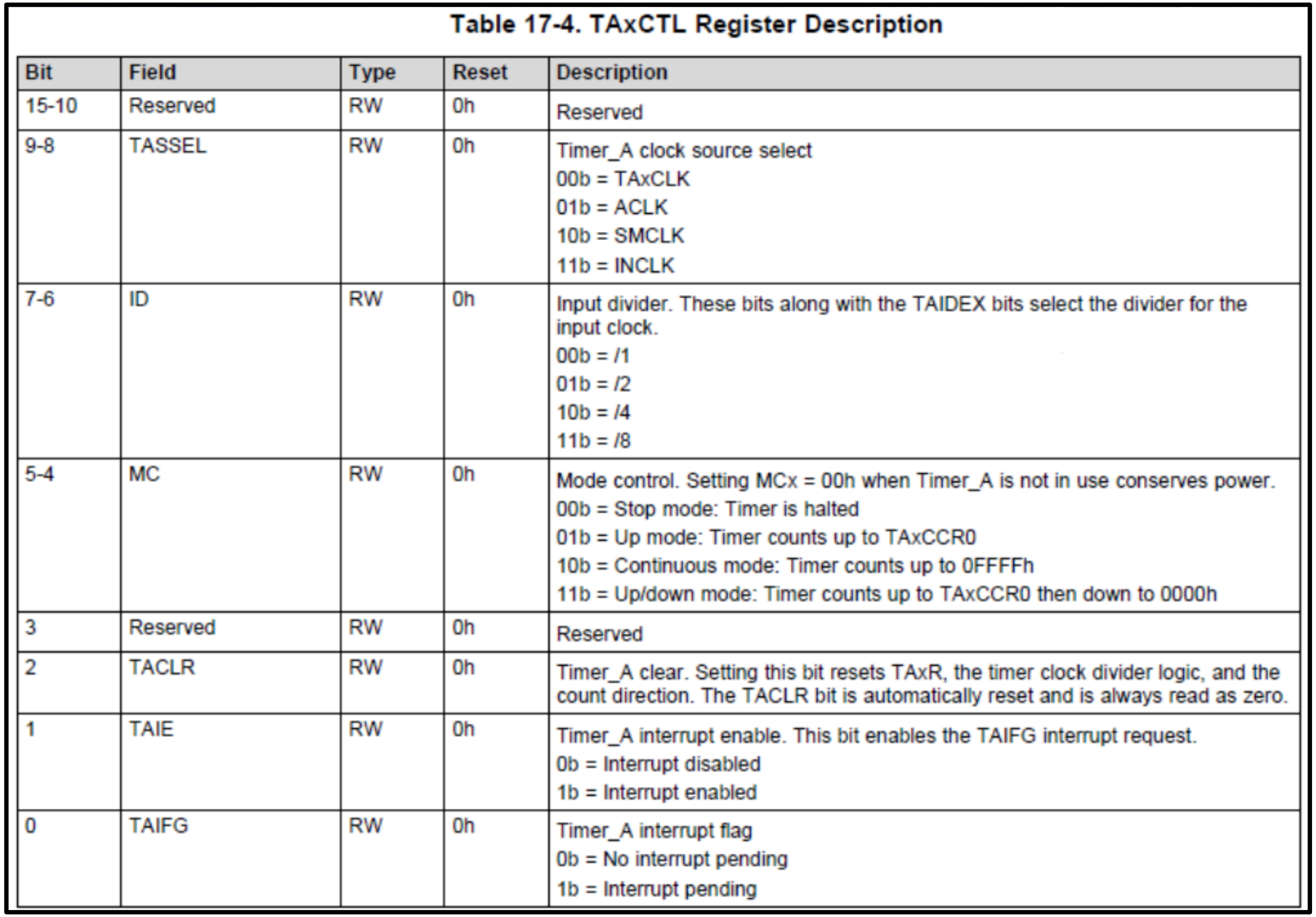
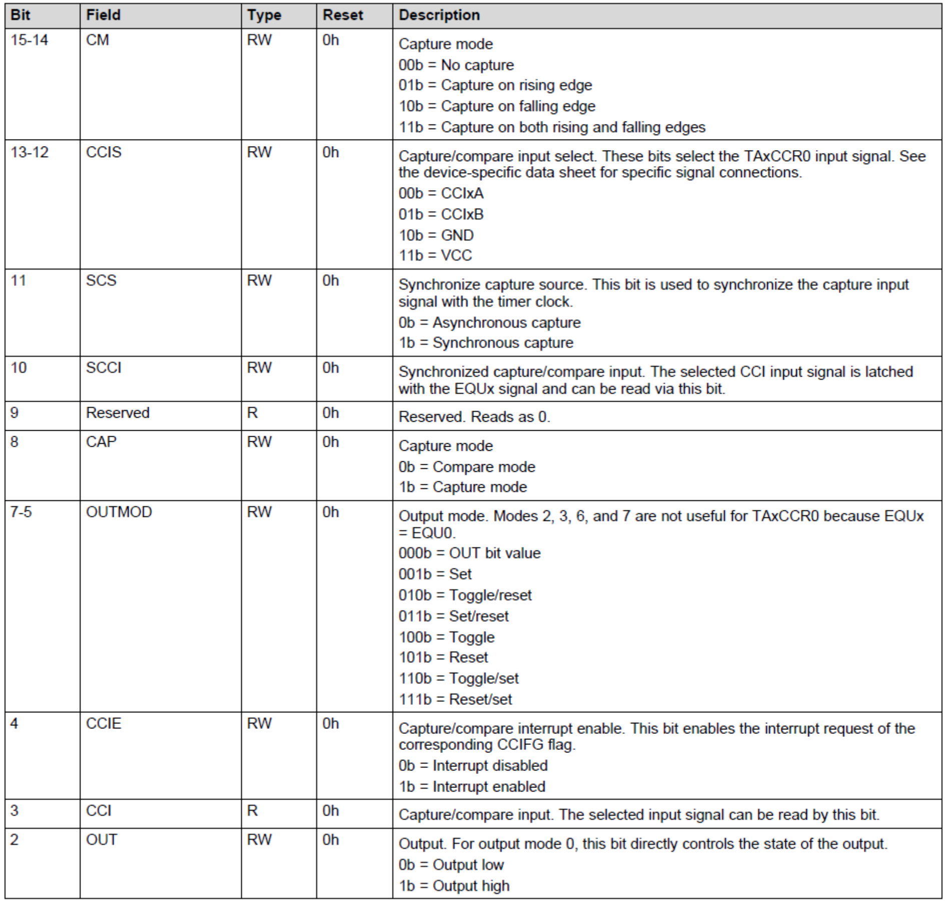
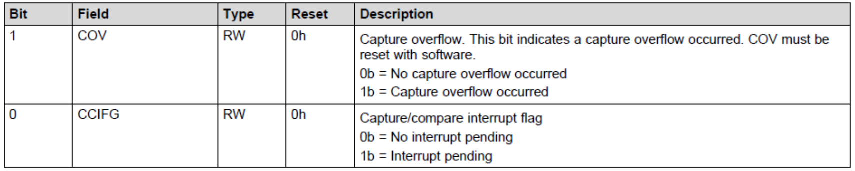


Table 17-4. TAxCTL Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	RW	0h	Reserved
9-8	TASSEL	RW	0h	Timer_A clock source select 00b = TAxCLK 01b = ACLK 10b = SMCLK 11b = INCLK
7-6	ID	RW	0h	Input divider. These bits along with the TAIDEX bits select the divider for the input clock. 00b = /1 01b = /2 10b = /4 11b = /8
5-4	MC	RW	0h	Mode control. Setting MCx = 00h when Timer_A is not in use conserves power. 00b = Stop mode: Timer is halted 01b = Up mode: Timer counts up to TAxCCR0 10b = Continuous mode: Timer counts up to 0FFFFh 11b = Up/down mode: Timer counts up to TAxCCR0 then down to 0000h
3	Reserved	RW	0h	Reserved
2	TACLR	RW	0h	Timer_A clear. Setting this bit resets TAxR, the timer clock divider logic, and the count direction. The TACLR bit is automatically reset and is always read as zero.
1	TAIE	RW	0h	Timer_A interrupt enable. This bit enables the TAIFG interrupt request. 0b = Interrupt disabled 1b = Interrupt enabled
0	TAIFG	RW	0h	Timer_A interrupt flag 0b = No interrupt pending 1b = Interrupt pending

Timer A Register – CCTL





Bit	Field	Type	Reset	Description
15-14	CM	RW	0h	Capture mode 00b = No capture 01b = Capture on rising edge 10b = Capture on falling edge 11b = Capture on both rising and falling edges
13-12	CCIS	RW	0h	Capture/compare input select. These bits select the TAxCCR0 input signal. See the device-specific data sheet for specific signal connections. 00b = CCIxA 01b = CCIxB 10b = GND 11b = VCC
11	SCS	RW	0h	Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock. 0b = Asynchronous capture 1b = Synchronous capture
10	SCCI	RW	0h	Synchronized capture/compare input. The selected CCI input signal is latched with the EQUx signal and can be read via this bit.
9	Reserved	R	0h	Reserved. Reads as 0.
8	CAP	RW	0h	Capture mode 0b = Compare mode 1b = Capture mode
7-5	OUTMOD	RW	0h	Output mode. Modes 2, 3, 6, and 7 are not useful for TAxCCR0 because EQUx = EQU0. 000b = OUT bit value 001b = Set 010b = Toggle/reset 011b = Set/reset 100b = Toggle 101b = Reset 110b = Toggle/set 111b = Reset/set
4	CCIE	RW	0h	Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag. 0b = Interrupt disabled 1b = Interrupt enabled
3	CCI	R	0h	Capture/compare input. The selected input signal can be read by this bit.
2	OUT	RW	0h	Output. For output mode 0, this bit directly controls the state of the output. 0b = Output low 1b = Output high
1	COV	RW	0h	Capture overflow. This bit indicates a capture overflow occurred. COV must be reset with software. 0b = No capture overflow occurred 1b = Capture overflow occurred
0	CCIFG	RW	0h	Capture/compare interrupt flag 0b = No interrupt pending 1b = Interrupt pending

Timer A Register – TAxEX0

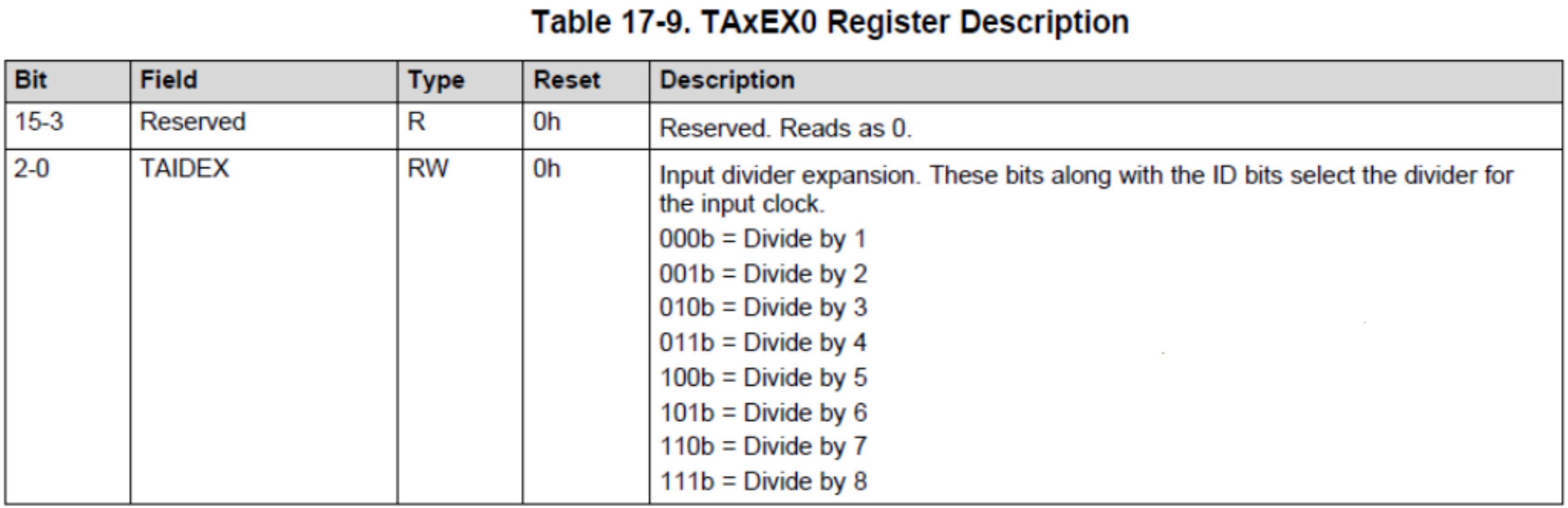
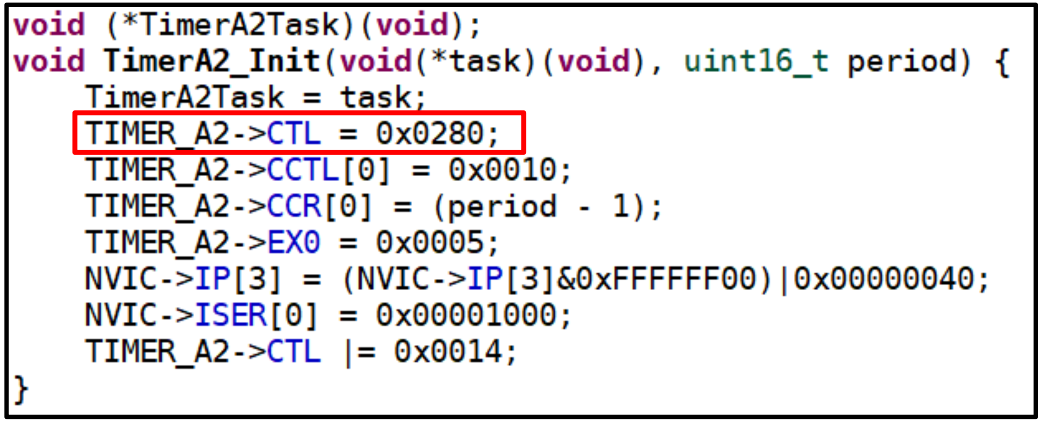


Table 17-9. TAxEX0 Register Description

Bit	Field	Type	Reset	Description
15-3	Reserved	R	0h	Reserved. Reads as 0.
2-0	TAIDEX	RW	0h	Input divider expansion. These bits along with the ID bits select the divider for the input clock. 000b = Divide by 1 001b = Divide by 2 010b = Divide by 3 011b = Divide by 4 100b = Divide by 5 101b = Divide by 6 110b = Divide by 7 111b = Divide by 8

Timer Interrupt Initialization



```
void (*TimerA2Task)(void);
void TimerA2_Init(void(*task)(void), uint16_t period) {
    TimerA2Task = task;
    TIMER_A2->CTL = 0x0280;
    TIMER_A2->CCTL[0] = 0x0010;
    TIMER_A2->CCR[0] = (period - 1);
    TIMER_A2->EX0 = 0x0005;
    NVIC->IP[3] = (NVIC->IP[3]&0xFFFFFF00)|0x00000040;
    NVIC->ISER[0] = 0x00001000;
    TIMER_A2->CTL |= 0x0014;
}
```

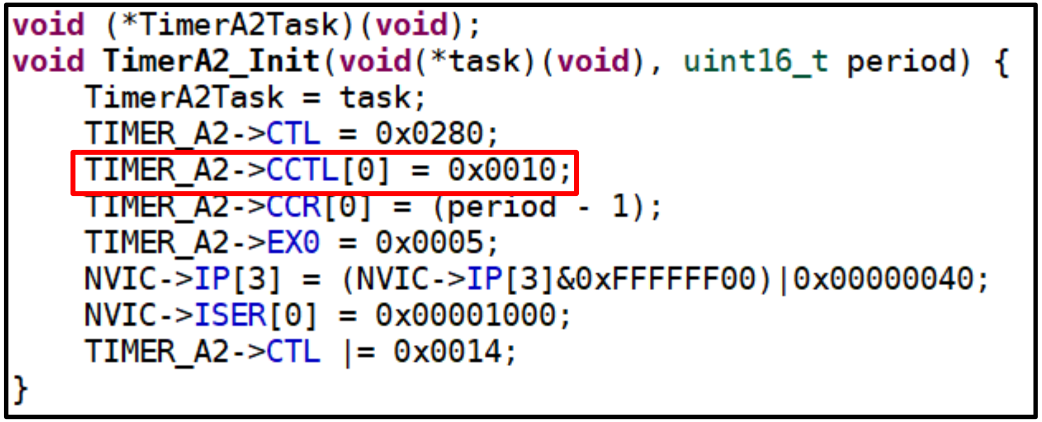
TIMER_A2->CTL = 0x0280

-> TIMER_A2->CTL = 0b 0000 0010 1000 0000

7~6 bit : 1/4 input divider

9~8 bit : timer clock source, SMCLK = 12MHz

Timer Interrupt Initialization



```
void (*TimerA2Task)(void);
void TimerA2_Init(void(*task)(void), uint16_t period) {
    TimerA2Task = task;
    TIMER_A2->CTL = 0x0280;
    TIMER_A2->CCTL[0] = 0x0010;
    TIMER_A2->CCR[0] = (period - 1);
    TIMER_A2->EX0 = 0x0005;
    NVIC->IP[3] = (NVIC->IP[3]&0xFFFFFF00)|0x00000040;
    NVIC->ISER[0] = 0x00001000;
    TIMER_A2->CTL |= 0x0014;
}
```

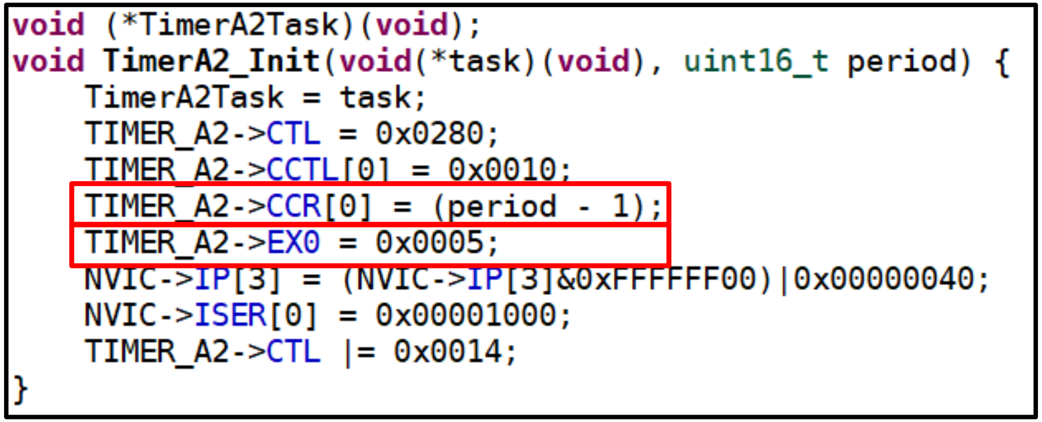
TIMER_A2->CCTL = 0x0010

-> TIMER_A2->CCTL = 0b 0000 0000 0001 0000

8 bit : compare mode

4 bit : enable compare interrupt

Timer Interrupt Initialization



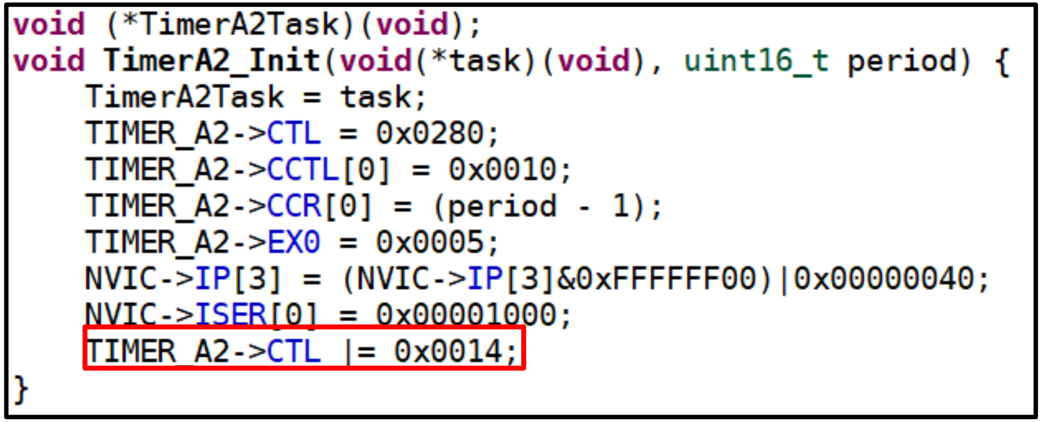
```
void (*TimerA2Task)(void);
void TimerA2_Init(void(*task)(void), uint16_t period) {
    TimerA2Task = task;
    TIMER_A2->CTL = 0x0280;
    TIMER_A2->CCTL[0] = 0x0010;
    TIMER_A2->CCR[0] = (period - 1);
    TIMER_A2->EX0 = 0x0005;
    NVIC->IP[3] = (NVIC->IP[3]&0xFFFFFF00)|0x00000040;
    NVIC->ISER[0] = 0x00001000;
    TIMER_A2->CTL |= 0x0014;
}
```

TIMER_A2->CCR[0] : compare match value

when the counter meets CCR[0], interrupt occurs

TIMER_A2->EX0 : input divider 2

Timer Interrupt Initialization



```
void (*TimerA2Task)(void);
void TimerA2_Init(void(*task)(void), uint16_t period) {
    TimerA2Task = task;
    TIMER_A2->CTL = 0x0280;
    TIMER_A2->CCTL[0] = 0x0010;
    TIMER_A2->CCR[0] = (period - 1);
    TIMER_A2->EX0 = 0x0005;
    NVIC->IP[3] = (NVIC->IP[3]&0xFFFFFF00)|0x00000040;
    NVIC->ISER[0] = 0x00001000;
    TIMER_A2->CTL |= 0x0014;
}
```

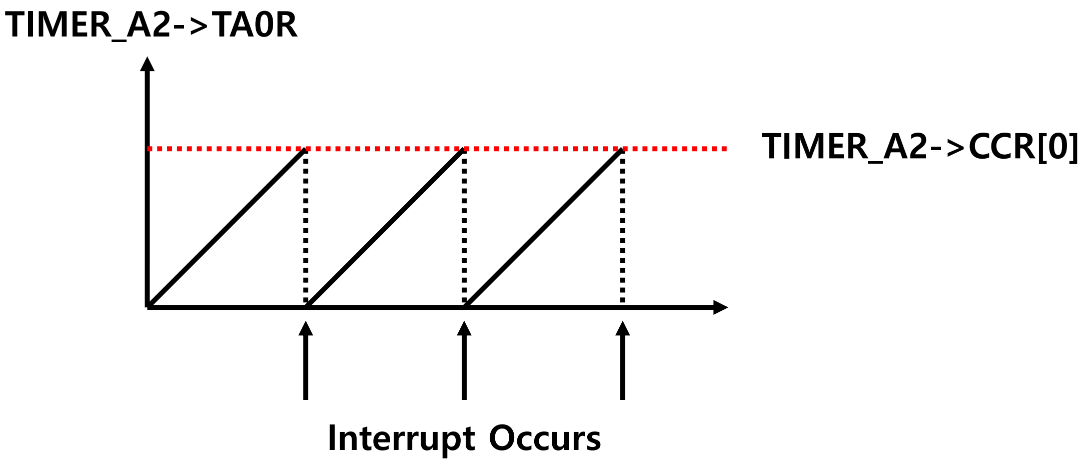
TIMER_A2->CTL |= 0x0014

-> TIMER_A2->CTL |= 0b 0000 0000 0001 0100

5~4 bit : up mode, increment counter

2 bit : clear TA0R register

Timer Interrupt Initialization



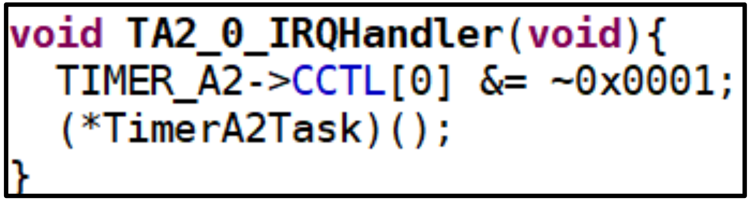
period = 50,000

-> 0.1s

$$\text{Resolution} = \frac{1}{\text{Clock Source}} * (\text{input divider}) * (\text{EX0} + 1)$$

$$= \frac{1}{12\text{MHz}} * (4) * (5 + 1) = 2\text{us}$$

Timer Interrupt Handler

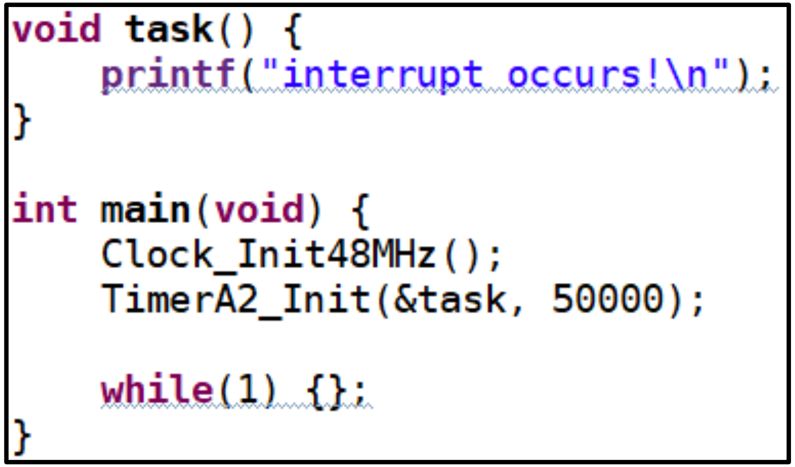


```
void TA2_0_IRQHandler(void){
  TIMER_A2->CCTL[0] &= ~0x0001;
  (*TimerA2Task)();
}
```

TIMER_A2->CCTL[0] &= ~0x0001;

-> send ack to the timer

-> If the timer does not receive an ack,
the timer continuously send an interrupt



```
void task() {
    printf("interrupt occurs!\n");
}

int main(void) {
    Clock_Init48MHz();
    TimerA2_Init(&task, 50000);

    while(1) {};
}
```

Notice

- The final exam is on 12/5.
- You can take the device from today.
  - If you took it, you have to bring it in next week's
- But if you lose it, you get an F. Please take good care of it so that it doesn't get lost.
  - (Please take care of it after consultation with the team, and if you lose it, all the team members are responsible.)
- If you find it difficult to store or manage it, you can return it to the teaching assistant.
- If you do not understand or have any difficulties, or if you have any other questions, please feel free to contact the teaching assistant via e-mail.
- Likewise, if you want to use it separately, you can contact the assistant by email.
  - In this case, we need to adjust the schedule, so please tell us the date and time you want to use it.
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