**EE-599B:** SoC Verification in System-Verilog



**Assignment:** Verification Plan for AHB

Lite Memory

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## **Verification Plan for AMBA AHB-Lite Compliant Memory**

| No. | Feature   | Test Description  | Ref.  | Type | Result | Comments  |
|-----|---|---|-------|------|--------|---|
| 1   | Write transfers at random locations                           | HWRITE signal will be high and Master will broadcast the data packets on the HWDATA [31:0] bus.   | 3.1   | TR   |        | Successful write transfers at random locations. Then Slave must give OKAY response by low HRESP signal.                             |
| 2   | Read Transfers at random locations                            | HWRITE is low then the slave must generate the data packets on the HRDATA [31:0] bus.   | 3.1   | TR   |        | Successful read transfers at random locations. Then Slave must give OKAY response by low HRESP signal.                              |
| 3   | Write-Read Transfer<br>at same address                        | Write transfer followed by Read transfer at an address.   | 3.1   | TR   |        | When HRESP is low, HREADY is high then particular address location must have the updated value which will be read in next transfer. |
| 4   | Transfer Type<br>HTRANS [1:0]:<br>IDLE                        | IDLE transfer is inserted   | 3.2   | TR   |        | IDLE transfer must be ignored by the slave and must provide zero wait state OKAY response.  |
| 5   | Burst Termination with BUSY transfer                          | Burst Termination with BUSY Transfer for fixed length burst. (It must terminate with SEQ transfer.)   | 3.5.1 | A    |        | Slave must give an ERROR response.  |
| 6   | BUSY transfer after<br>SINGLE Burst                           | BUSY transfer immediately after SINGLE<br>Burst (It must followed by IDLE or NONSEQ<br>transfer)  | 3.5.1 | A    |        | Slave must give an ERROR response.  |
| 7   | Waited states:<br>Transfer type and<br>Address change         | Transfer type and address changed from IDLE to NONSEQ during waited states. These will be held constant untill HREADY is high                     | 3.6.1 | A    |        | Successfully transfer type and address changed. Slave must give OKAY response.  |
| 8   | Waited States`: Transfer type changed for fixed length burst. | Transfer type changes from BUSY to SEQ during waited states for fixed length bursts. The HTRANS signal must be kept constant until HREADY is high | 3.6.1 | A    |        | Successfully transfer type changed. Slave must give OKAY response.  |

| 9  | Transfer type changed during waited states             | Transfer type changes from BUSY to any other type during waited states for undefined length burst. The burst continues if a SEQ transfer is performed but terminates if and IDLE or NONSEQ transfer is performed. | 3.6.1 | A  | Successfully transfer type changed. Slave must give OKAY response.   |
|----|--|---|-------|----|--|
| 10 | Transfer type<br>changed during<br>waited states       | Transfer type changed from IDLE to SEQ.   |       |    | Slave will give an ERROR response.   |
| 11 | Address change<br>after an ERROR<br>response by slave  | Master can change the address if slave responds with an ERROR during waited states  | 3.6.2 | TR | Successfully address changed. Slave must give OKAY response.   |
| 11 | Slave Transfer<br>response:<br>Transfer done           | Transfer is successfully completed by the Slave   | 5.1.1 | TR | HREADY will be high whereas HRESP will be low  |
| 12 | Slave Transfer<br>response:<br>Transfer pending        | Slave inserted waited states to enable time to complete the transfer  | 5.1.2 | TR | Both signals HREADY & HRESP will be low  |
| 13 | Slave Transfer<br>response:<br>Transfer failed         | Slave signal an ERROR to indicate the transfer failure  | 5.1.3 | TR | Slave give an ERROR response in two cycles Cycle I: HREADY will be low whereas HRESP will be high  Cycle II: HREADY will be high whereas HRESP will also be high |
| 14 | Transfer attempted to non-existential address location | NONSEQ or SEQ transfer attempted at non-<br>existential address location  | 4.1.1 | TR | Slave must give an ERROR response.   |
| 15 | Global Signal:<br>HRESTn<br>(Active Low Signal)        | Reset all bus elements. Slaves will have HREADYOUT signal high while transfer type HTRANS [1:0] must be IDLE.   | 7.1.2 | TR | All bus element must be resetted.  |

## **Explanation of Different Fields**

**No.** The serial number of the test.

**Feature** The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user.

**Test Description** A detailed description of the test case being performed. You can be as verbose as you want.

**Ref.** Reference to the section in the related standard document. The section number as well as page numbers should be

described here.

**Type** Type of the test. Whether the test is an assertion (A) or a transaction (T) type.

**Result** Pass (P) or Fail (F).

**Comments** Any other comments about the test or its results that you want to mention.