EE-599B: SoC Verification in System-Verilog

Assignment: Verification Plan for AHB Lite Memory

Submitted To: **Dr. Ubaid Ullah Fayyaz**

Submitted By: **Muhammad Usman Tahir**
Reg. No: **2019-MS-EE-40**

UNIVERSITY OF ENGINEERING AND TECHNOLOGY LAHORE

Verification Plan for AMBA AHB-Lite Compliant Memory

No.	Feature	Test Description	Ref.	Type	Result	Expected Result	Comments
1	Single Write Transaction from Master to Slave at one address	The address will be broadcasted on the write data bus which will be sampled on 1st rising edge.	3.1	TR		The slave will sample the address when HREADY is high. When the Data will be successfully written at particular address then HRESP signal will be low while HRADY will be high.	HWRITE signal will be high and Master will broadcast the data packets on the HWDATA [31:0] bus.
2	Single Read Transaction from slave to Master from one address	The address will be broadcasted on the read data bus which will be sampled on 1st rising edge	3.1	TR		The slave will sample the address when HREADY is high. When the Data will be successfully read from particular address then HRESP signal will be low while HRADY will be high.	HWRITE is low then the slave must generate the data packets on the HRDATA [31:0] bus.
3	Multiple Read / Write Transaction at Random locations	Random addresses will be broadcasted on the particular bus depending upon whether Read / Write Transactions which will be sampled on 1st rising edge.	3.1	TR		When the Data will be successfully write/read to/from particular address then HRESP signal will be low while HRADY will be high.	HWRITE is low / high depending upon whether Read / Write Transactions is performed
4	Write then Read Transfer at same address	The address will be broadcasted on the write data bus which will be sampled on 1st rising edge. Further, the same address will be broadcasted on the read data bus which will be sampled on 2st rising edge.	3.1	TR		During Write Transaction: HWRITE signal will be high and Master will broadcast the data packets on the HWDATA [31:0] bus.\n\nDuring Read Transaction: HWRITE will be low then the slave must generate the data packets on the HRDATA [31:0] bus.	Upon successful Write Transaction, HRESP is low, HREADY is high then particular address will be written.\n\nSimilarly, upon successful Read Transaction, HRESP is low, HREADY is high and the updated value at this particular address will be read.

5	Read then Write Transfer at same address	The address will be broadcasted on the read data bus which will be sampled on 1st rising edge. Further, the same address will be broadcasted on the write data bus which will be sampled on 2st rising edge.	3.1	TR		During Read Transaction: HWRITE will be low then the slave must generate the data packets on the HRDATA [31:0] bus. During Write Transaction: HWRITE signal will be high and Master will broadcast the data packets on the HWDATA [31:0] bus.	Upon successful Read Transaction, HRESP is low, HREADY is high on 2nd Rising edge. Then, upon successful Write Transaction, HRESP is low, HREADY is high and that particular address will have the updated.
6	Transfer Type HTRANS [1:0]: IDLE	IDLE transfer is inserted	3.2	A			IDLE transfer must be ignored by the slave and must provide zero wait state OKAY response.
7	Burst Termination with BUSY transfer	Burst Termination with BUSY Transfer for fixed length burst. *(It must terminate with SEQ transfer.)*	3.5.1	A			Slave must give an ERROR response.
8	BUSY transfer after SINGLE Burst	BUSY transfer immediately after SINGLE Burst *(It must followed by IDLE or NONSEQ transfer)*	3.5.1	A			Slave must give an ERROR response.
9	**Waited states:** Transfer type change from IDLE to NONSEQ	Transfer type changed from IDLE to NONSEQ during waited states. These will be held constant untill HREADY is high	3.6.1	A			Successfully transfer type and address changed. Slave must give OKAY response.
10	**Waited States:** Transfer type change for fixed length burst.	Transfer type changes from BUSY to SEQ during waited states for fixed length bursts. The HTRANS signal must be kept constant until HREADY is high	3.6.1	A			Successfully transfer type changed. Slave must give OKAY response.
11	**Waited States:** Transfer type change during waited states for	Transfer type changes from BUSY to any other type during waited states for undefined length burst. The burst continues if a SEQ transfer is performed	3.6.1	A			Successfully transfer type changed. Slave must give OKAY response.

	undefined length burst.	but terminates if and IDLE or NONSEQ transfer is performed.					
12	**Waited States:** Address change after an ERROR response by slave	Master can change the address if slave responds with an ERROR during waited states	3.6.2	TR			Successfully address changed. Slave must give OKAY response.
13	Slave Transfer response: Transfer done	Transfer is successfully completed by the Slave	5.1.1	TR			HREADY will be high whereas HRESP will be low
14	Slave Transfer response: Transfer pending	Slave inserted waited states to enable time to complete the transfer	5.1.2	TR			Both signals HREADY & HRESP will be low
15	Slave Transfer response: Transfer failed	Slave signal an ERROR to indicate the transfer failure	5.1.3	TR			Slave give an ERROR response in two cycles Cycle I: HREADY will be low whereas HRESP will be high Cycle II: HREADY will be high whereas HRESP will also be high
16	Transfer attempted to non-existential address location	NONSEQ or SEQ transfer attempted at non-existential address location	4.1.1	TR			Slave must give an ERROR response.
17	**Incrementing Bursts:** (INCR4, INCR8, INCR16)	For HSIZE [2:0] signal is 010 or 32 bit (4byte) and Slave Memory is byte aligned: INCR4, INCR8, INCR16 are 4,8 & 16 beats burst and from starting address the burst will have incrementing addresses.	3.5.3	TR			The address in the incrementing burst are incremented from the started address depending upon the HSIZE of date and Slave specifications i.e. byte aligned memory etc.
18	**Wrapping Burst:** (WRAP4, WRAP8, WRAP16)	For 32 bit (4byte) data size and byte aligned slave memory: WRAP4, WRAP8, WRAP16 are 4,8 & 16 beats burst and from starting address the burst will have incrementing addresses but in contrast to incrementing	3.5.3	TR			The address boundary can be calculated as: Boundary Size = HBURST * HSIZE

		burst, after reaching the end of memory the address wraps around to the start address.					Such as for HBURST= b100 (WRAP8) and HSIZE=b 011 (64 bit or 8 byte data) then the boundary size will be 64 bytes. In this case address will be wrapped after 64 byte memory slave.

Explanation of Different Fields

No.	The serial number of the test.
Feature	The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user.
Test Description	A detailed description of the test case being performed. You can be as verbose as you want.
Ref.	Reference to the section in the related standard document. The section number as well as page numbers should be described here.
Type	Type of the test. Whether the test is an assertion (A) or a transaction (T) type.
Result	Pass (P) or Fail (F).
Expected Result	Expected outcome based on the AHB Lite protocol and Slave Memory Specifications.
Comments	Any other comments about the test or its results that you want to mention.