Introduction to 8086

Module 5

Introduction

Intel 8086 is 16 bit high performance N-channel HMOS microprocessor with following features-

- CPU has direct addressing capacity of 1MB memory.
- Bit, byte, word & block operations are available.
- 8-bit & 16-bit signed, unsighed arithmatic in binary & decimal operations are performed.
- It is available in dual In-Line package
- It has architectures designed for assembly language as well as high level language.

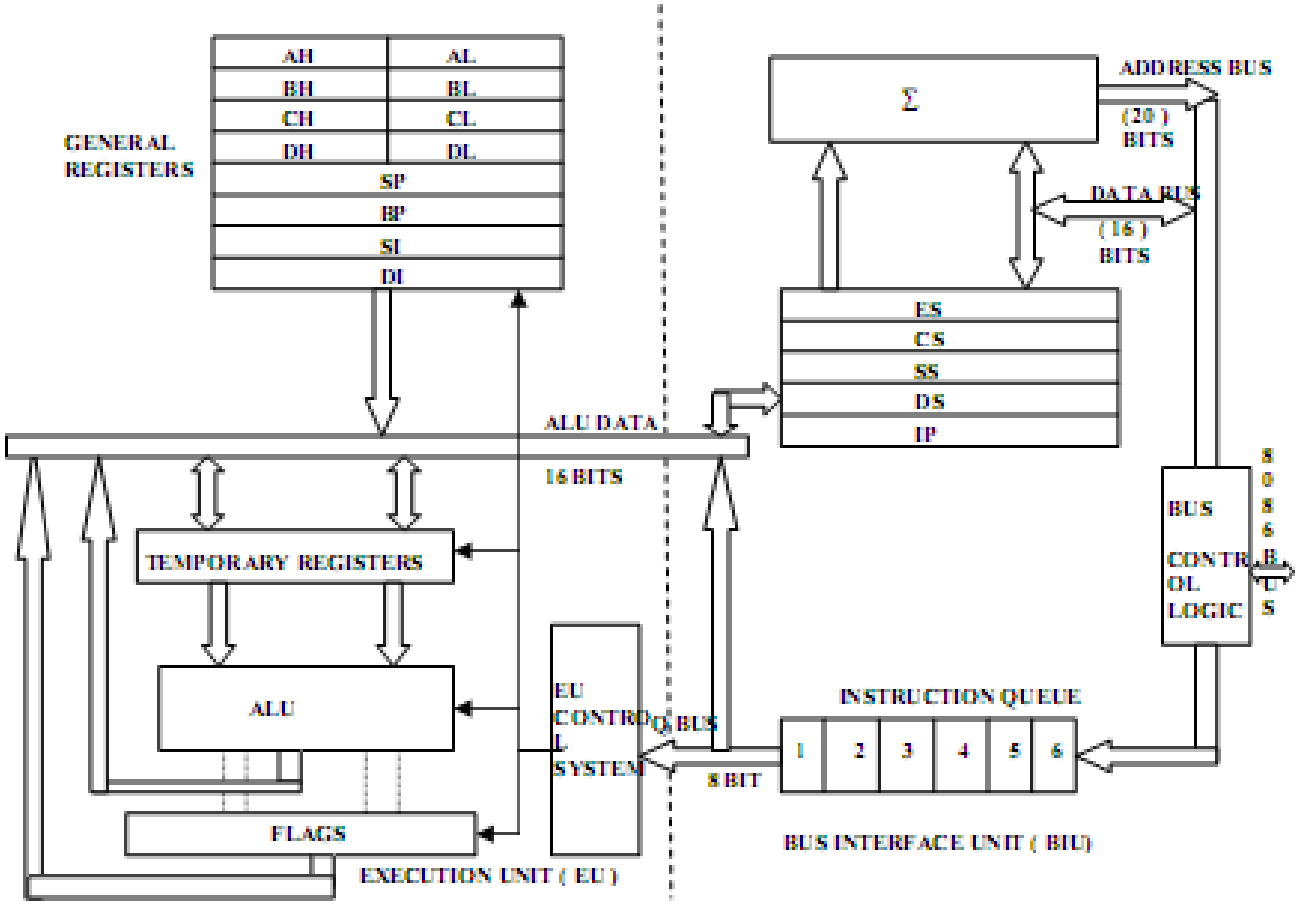
Introduction

- 8086 contains an electronic circuitry of 29000 transistors.
- It has 20 address lines & 16 data lines.
- 16-bit address lined are time multiplexed to select the lines of lower order byte & higher order byte separately.

Comparison between 8085 & 8086

8085	8086
8-bit processor with 8-bit data	16-bit processor with 16-bit data
Manufactured using NMOS technology & IC consists of 6200 transistors	Manufactured using HMOS technology & IC consists of approx 29000 transistors
16-bit address bus so 2^16=64KB memory locations are accessible	20-bit address bus so 2^20=1MB memory locations are accessible
No of flags are 5	No of flags are 9
Pipelining is not used	Pipelining is used
Instruction queue does not exists & it sequentially executes the instructions	It has 6-byte instruction queue in BIU(Bus interface unit)
No segment registers exits in 8085	There are 4 segment registers CS, DE, ES, SS in 8086
Only four types of addressing modes are used	Eight addressing modes are available
Less instructions than 8086. Direct multiplication, division, string byte block movement are not available	More instructions than 8085. Direct multiplication, division, string byte block movement are possible

Architecture of 8086

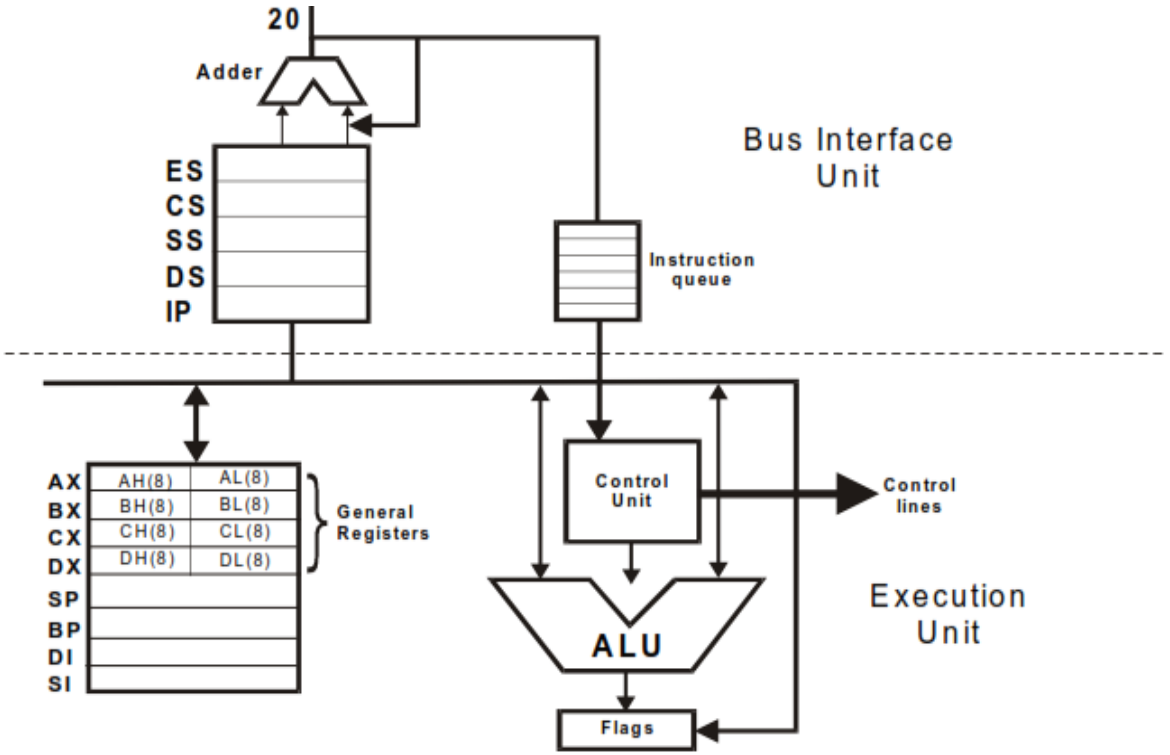


Block Diagram of 8086

Architecture of 8086

The 8086 architecture can be broadly divided into two groups:

- Execution Unit
- Bus Interface unit



Architecture of 8086

Bus Interface Unit (BIU):

The Bus Interface Unit (BIU) generates the 20-bit physical memory address and provides the interface with external memory (ROM/RAM). 8086 has a single memory interface. To speed up the execution, 6-bytes of instruction are fetched in advance and kept in a 6-byte Instruction Queue while other instructions are being executed in the Execution Unit (EU). Hence after the execution of an instruction, the next instruction is directly fetched from the instruction queue without having to wait for the external memory to send the instruction. This is called pipe-lining and is helpful for speeding up the overall execution process.

8086's BIU produces the 20-bit physical memory address by combining a 16-bit segment address with a 16-bit offset address. There are four 16-bit segment registers, viz., the code segment (CS), the stack segment (SS), the extra segment (ES), and the data segment (DS). These segment registers hold the corresponding 16-bit segment addresses. A segment address is the upper 16-bits of the starting address of that segment. The lower 4-bits of the starting address of a segment is always zero. The offset address is held by another 16-bit register. The physical 20-bit address is calculated by shifting the segment address 4-bit left and then adding that to the offset address.

Architecture of 8086

For Example:
Code segment Register CS holds the segment address which is 4569 H
Instruction pointer IP holds the offset address which is 10A0 H
The physical 20-bit address is calculated as follows.

Segment address : 45690 H
Offset address : + 10A0 H
Physical address : 46730 H

Architecture of 8086

Execution Unit

The EU decodes and executes instructions. A decoder in the EU control system translates instructions. The EU has a 16 bit ALU for performing arithmetic and logic operations. The EU has eight 16-bit general registers. These are AX,BX,CX,DX,SP,BP,SI and DI.

The flag registers in the EU holds the status flags after an ALU operation

The execution unit consists of

- General Registers
- Arithmetic Logic Unit
- Control unit
- Flag Registers

Architecture of 8086

General Registers

- The CPU has eight 16-bit general registers. They are divided into two files of
- four registers each. They are:

1. Data register file

AH	AL	AX
BH	BL	BX
CH	CL	CX
DH	DL	DX

2. Pointer & Index register file
   - SP- Stack Pointer
   - BP – Base pointer
   - SI – Source Index
   - DI – Destination Index

Architecture of 8086

The DX register is used to hold the high 16 bit result in 16X16 multiplication or the high 16 bit dividend before a 32%16 division and the 16 bit remainder after the division

The two pointer registers SP and BP are used to access data in the stack segment.

The two index registers SI and DI are used in indexed addressing mode. Note that instructions that process data strings use the SI and DI index registers together with the DS and ES respectively in order to distinguish between the source and destination addresses.

The 8086 has six one-bit flags: CF,OF,ZF,AF,PE,SF.

The 8086 has three control flags: DF,TF,IF

Architecture of 8086

Arithmetic Logic Unit (ALU)

ALU is 16-bits wide. It can do the following 16-bits arithmetic operations

(i) Addition
(ii) Subtraction
(iii) Multiplication
(iv) Division

Arithmetic operations may be performed on four types of numbers

- Unsigned binary numbers
- Signed binary numbers (Integers)
- Unsigned packed decimal numbers
- Unsigned unpacked decimal numbers

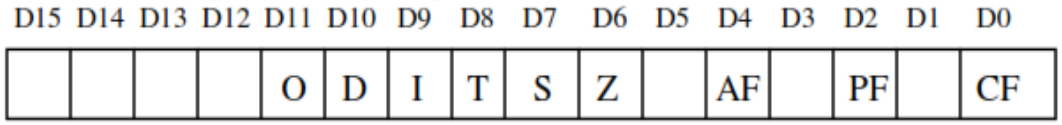
The ALU can also perform logical operations such as

(i) NOT
(ii) AND
(iii) OR
(iv) EXCLUSIVE OR
(v) TEST

Architecture of 8086

Flag Register

The Execution Unit has a 16-bit flag register which indicates some conditions affected by the execution of an instruction. Some bits of the flag register control certain operations of the EU. The flag register in the EU contains nine active flags shown in fig.1.6



Fig, 1.6 Flag Register

Six of the nine flags are used to indicate some condition produced by an instruction. These condition flags are also called status flags of 8086/8088 microprocessor. These are the Carry flag, Parity flag, Auxiliary carry flag, Zero flag, and Sign flag. The other three Control flags are Trap Flag, Direction Flag and Interrupt flag.

Architecture of 8086

Control Flags

Control flags are used to control certain operations of the processor. The application of these flags are different from that of six conditional flags. The conditional flags are set or reset by the EU on the basis of the result of some arithmetic or logic operations. The control flags are deliberately set or reset with specific instructions included in the program.

Trap flag (T)

This is used for single stepping through a program. It is used for debugging the programs. (Discusses with interrupts).

Interrupt Flag (I)

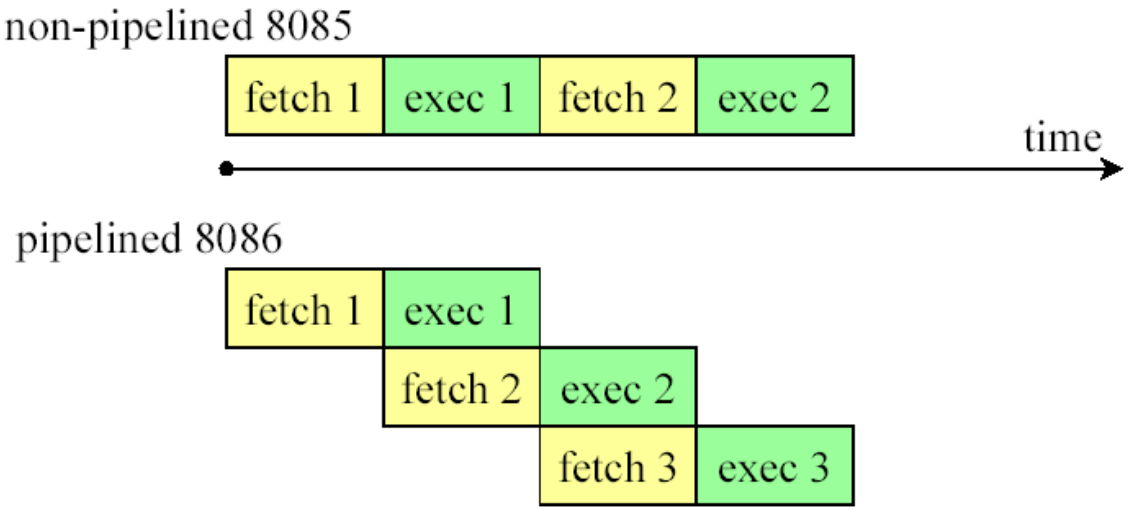
It is used to allow / prohibit the interruption of a program. When the flag set, it enables the interrupt from INTR. When the flag is reset (0), it disables the interrupt.

Direction Flag (D)

It is used for string instructiion (Discussed with the specific instructions later in the book). If the direction flag is set, the pointers are decremented else the pointers are incremented.

Inside The 8086…*pipelining*

- Pipelining
  - Two ways to make CPU process information faster:
    - Increase the working frequency – technology dependent
    - Change the internal architecture of the CPU
  - Pipelining is to allow CPU to fetch and execute at the same time



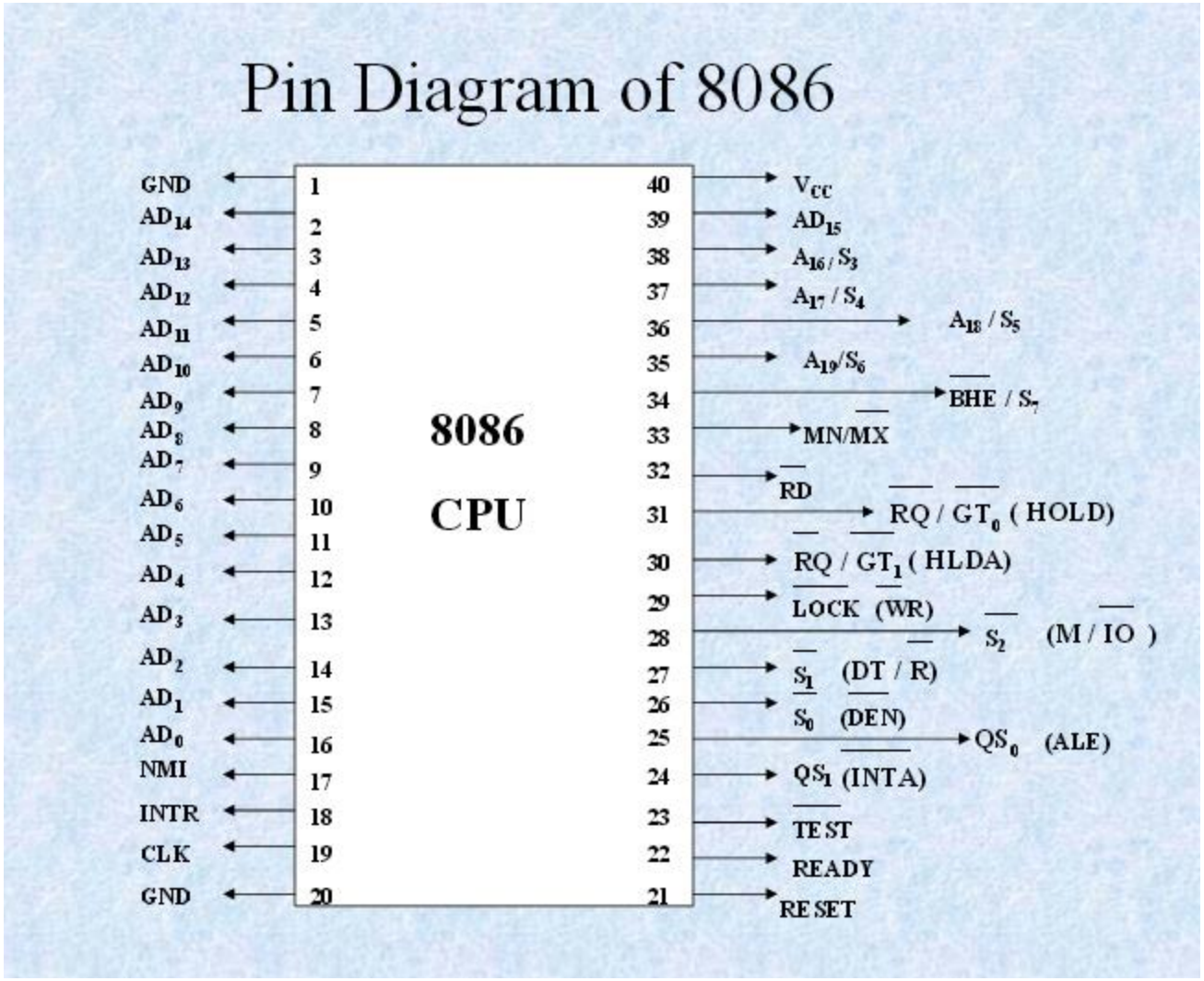
8086 Microprocessor

Minimum and Maximum Modes:

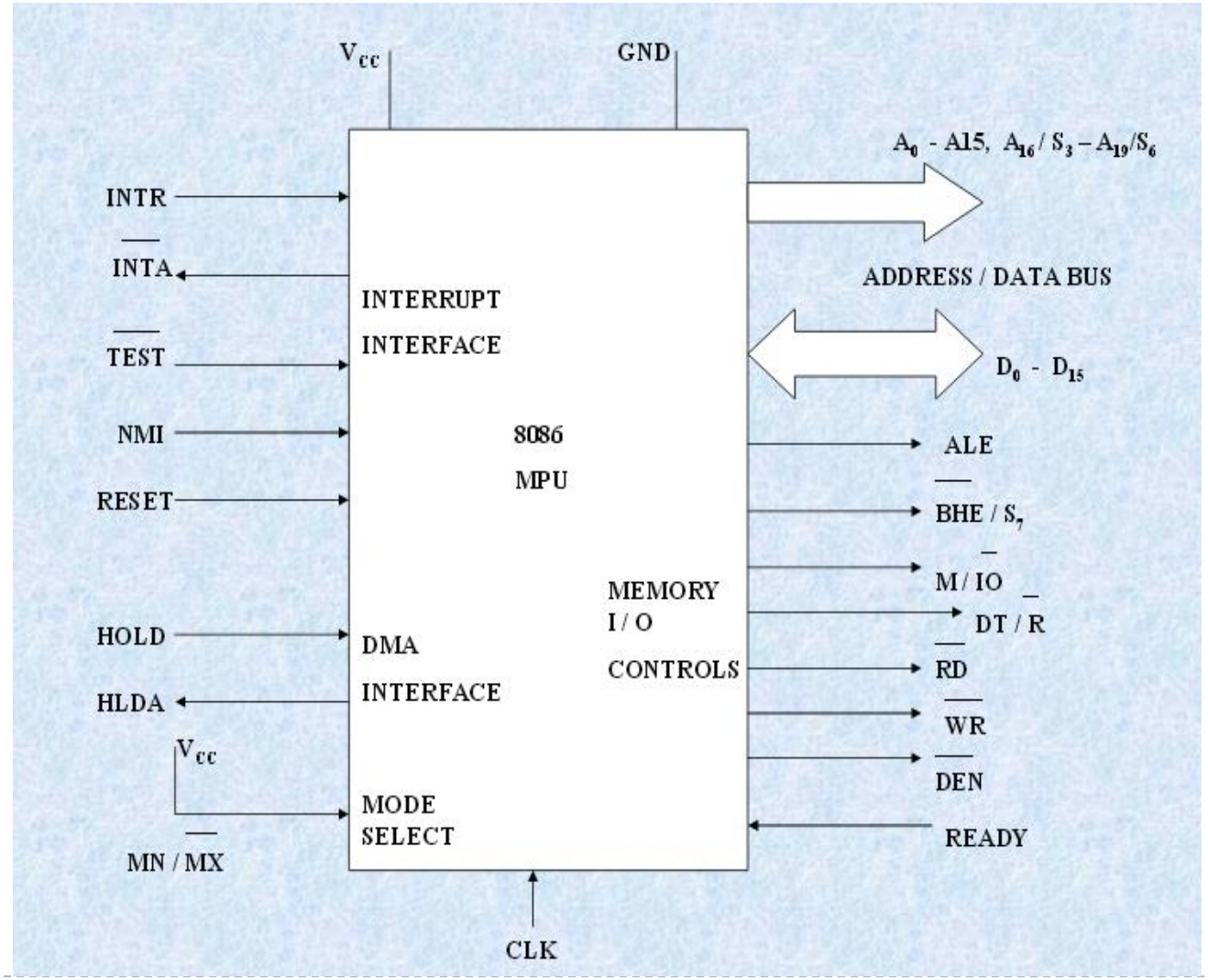
• The minimum mode is selected by applying logic 1 to the MN / MX# input pin. This is a single microprocessor configuration.

• The maximum mode is selected by applying logic 0 to the MN / MX# input pin. This is a multi micro processors configuration.

8086


Pin Diagram of 8086
8086
CPU
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
40 VCC
39 AD15
38 A16 / S3
37 A17 / S4
36 A18 / S5
35 A19/S6
34 BHE / S7
33 MN/MX
32 RD
31 RQ / GT0 (HOLD)
30 RQ / GT1 (HLDA)
29 LOCK (WR)
28 S2 (M / IO)
27 S1 (DT / R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET

8086


Vcc
GND
A0 - A15, A16 / S3 – A19/S6
INTR
INTA
ADDRESS / DATA BUS
INTERRUPT
INTERFACE
TEST
D0 - D15
NMI
8086
MPU
ALE
RESET
BHE / S7
M / IO
MEMORY
I / O
DT / R
HOLD
DMA
CONTROLS
RD
HLDA
INTERFACE
WR
Vcc
DEN
MODE
SELECT
READY
MN / MX
CLK

8086

COMMON SIGNALS		
Name	Function	Type
AD_{15} – AD_0	Address/ Data Bus	Bidirectional 3- state
A_{19}/S_6 – A_{16}/S_3	Address / Status	Output 3 - State
$\overline{BHE}$ /S 7	Bus High Enable / Status	Output 3- State
MN / MX	Minimum / Maximum Mode Control	Input
$\overline{RD}$	Read Control	Output 3- State
TEST	Wait On Test Control	Input
READY	Wait State Controls	Input
RESET	System Reset	Input
NMI	Non - Maskable Interrupt Request	Input
INTR	Interrupt Request	Input
CLK	System Clock	Input
Vcc	+ 5 V	Input
GND	Ground	

8086

Minimum Mode Signals ($\overline{MN}/MX$ = Vcc)		
Name	Function	Type
HOLD	Hold Request	Input
HLDA	Hold Acknowledge	Output
$\overline{WR}$	Write Control	Output 3- state
M/$\overline{IO}$	Memory or IO Control	Output 3-State
DT/$\overline{R}$	Data Transmit / Receiver	Output 3-State
$\overline{DEN}$	Date Enable	Output 3-State
ALE	Address Latch Enable	Output
$\overline{INTA}$	Interrupt Acknowledge	Output

8086

Minimum Mode Interface

- When the Minimum mode operation is selected, the 8086 provides all control signals needed to implement the memory and I/O interface.
- The minimum mode signal can be divided into the following basic groups : address/data bus, status, control, interrupt and DMA.

Address/Data Bus: these lines serve two functions. As an address bus is 20 bits long and consists of signal lines A0 through A19. A19represents the MSB and A0 LSB. A 20bit address gives the 8086 a 1Mbyte memory address space. More over it has an independent I/O address space which is 64K bytes in length.