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Module 05 : Diode Applications.

Rectifier circuits, Analytical Treatment, Filters (Ripple Voltage),
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for voltage & current, Diode voltage clamping Circuits.

Module 06 : Bipolar Junction Transistor.

Transistor structure, V-I characteristics of transistor : CB, CE & CC configurations & comparison, Leakage current & breakdown voltage, Limit of operation, DC Analysis (Load line) of transistor circuits, Transistor as switch, Methods of biasing, stability factors Transistor as amplifier.

NUMBER SYSTEMS.

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Most well-known number systems are :-

1) Decimal Number System : Base/Radix = 10

Digits = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

2) Binary Number System : Base/Radix = 2.

Digits = 0, 1, . . .

: Base/Radix = 8

Digits = 0, 1, 2, 3, 4, 5, 6, 7.

: Base = 16

Digits : 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

A, B, C, D, E, F.

Decimal No.	Binary No.	Octal No.	Hex. No.
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F
16		20	

* Conversion from Decimal to Binary.

① $[41.6875]$

Divide 41 by 2

$.6875 \times 2$

2	41	
2	20	1
2	10	0
2	5	0
2	2	1
2	1	0
0	1	

$[41]_{10} = [101001]_2$

bottom to top.

$$\begin{array}{l} 0.6875 \times 2 = 1.3750 \quad \text{carry on } 1 \\ 0.3750 \times 2 = 0.7500 \quad " \quad " \quad 0 \\ 0.7500 \times 2 = 1.500 \quad " \quad " \quad 1 \\ 0.5000 \times 2 = 1.000 \quad " \quad " \quad 1 \end{array}$$

$[0.6875]_{10} = [.1011]_2$

$\therefore [41.6875]_{10} = [101001.1011]_2$

* Conversion from decimal to octal.

① $[153.513]_{10} = [?]_8$

For integer part, divide by 8.

For decimal part, multiply by 8.

8	153	
8	19	1
8	2	3
0	2	

$[153]_{10} = [231]_8$

$0.513 \times 8 = 4.104$

$0.104 \times 8 = 0.832$

$0.832 \times 8 = 6.656$

$0.656 \times 8 = 5.248$

$[0.513]_{10} = [0.4065]_8$

$$[153.513]_{10} = [231.4065]_8$$

* Conversion from decimal to Hex.

① $[145.541]_{10} = [?]_{16 \text{ (Hex)}}$

For integer part divide by 16

For decimal part multiply by 16

$$\begin{array}{r} 16 \mid 145 \\ 16 \quad 9 \quad 1 \\ \downarrow \quad \uparrow \\ 0 \quad 9 \end{array} \quad [145]_{10} = [91]_{16}$$

$$0.541 \times 16 = 8.656$$

$$8.656 \times 16 = 10.496 \quad [.541] = [.8A7E]_{16}$$

$$0.496 \times 16 = 7.936$$

$$0.936 \times 16 = 14.976$$

$$[145.541]_{10} = [91.8A7E]_{16}$$

* Conversion from decimal to $[?]_2, [?]_3, [?]_4, [?]_6, \dots$

① $[60.120]_{10} = [?]_2, [?]_3, [?]_4$.

(a) $[60.120]_{10} = [?]_2$.

$$\begin{array}{r} 2 \mid 60 \\ 2 \quad 30 \quad 0 \\ 2 \quad 15 \quad 0 \\ 2 \quad 7 \quad 1 \\ 2 \quad 3 \quad 1 \\ 2 \quad 1 \quad 1 \\ 0 \quad 1 \end{array} \quad [60] = [111100]_2$$

$$0.120 \times 2 = 0.24$$

$$0.24 \times 2 = 0.48$$

$$0.48 \times 2 = 0.96$$

$$0.96 \times 2 = 1.920$$

$$[.120] = [.0001]_2$$

$$[60.120]_{10} = [111100.0001]_2$$

$$\textcircled{1} \quad [60.120] = [?]_3$$

3	60	
3	20	0
3	6	2
3	2	0
0	2	

$$[60]_{10} = [2020]_3$$

$$0.120 \times 3 = 0.36$$

$$0.36 \times 3 = 1.08 \quad [0.120]_{10} = [0100]_3$$

$$0.08 \times 3 = 0.24$$

$$0.24 \times 3 = 0.72$$

$$[60.120]_{10} = [2020.0100]_3$$

$$\textcircled{2} \quad [60.120] = [?]_4$$

4	60	
4	15	0
4	3	3
0	3	

$$[60]_{10} = [330]$$

$$0.120 \times 4 = 0.48$$

$$0.48 \times 4 = 1.92$$

$$0.92 \times 4 = 3.68$$

$$0.68 \times 4 = 2.72$$

$$[0.120]_{10} = [0132]_4$$

$$[60.120]_{10} = [330.0132]_4$$

$$\textcircled{3} \quad [60.120] = [?]_5$$

5	60	
5	12	0
5	2	2
0	2	

$$[220]$$

$$\Rightarrow [220.03]$$

$$0.120 \times 5 = 0.60$$

$$[03]$$

$$0.60 \times 5 = 3.00$$

$$3.00 \times 5 = 15.00$$

$$⑤ [60.120] = [?]_6$$

6	60	
6	10	0
6	1	4

[140].

$$0.12 \times 6 = 0.72 \quad [0.41].$$

$$.72 \times 6 = 4.32$$

$$.32 \times 6 = 1.92$$

$$\therefore [60.120] = [140.041].$$

$$⑥ [60.120] = [?]_7$$

7	60	
7	8	4
7	1	1
0		1

[114].

$$0.12 \times 7 = 0.84.$$

$$.84 \times 7 = 5.78 \quad [0.55]$$

$$.78 \times 7 = 5.46$$

$$[114.055].$$

* Conversion from Binary to Decimal.

$$① [1101.11] = [?]_{10}$$

$$1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^{-1} + 1 \times 2^{-2}$$

$$8 + 4 + 0 + 4 + 1 = 17$$

$$[17]$$

$$② \underline{[1101.11]}_2 = [11011.0110]_1$$

$$1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}$$

$$16 + 8 + 2 + 1 + 0.5 + 0.25 + 0.125.$$

$$27.375$$

$\frac{1}{2} = 0.1$

$\frac{0.1}{2} = 0.05$
 $\frac{0.05}{2} = 0.025$
 $\frac{0.025}{2} = 0.0125$

* Conversion from Octal to Decimal.

① $[427.35]_8 = [?]_{10}$.

$$4 \times 8^2 + 2 \times 8^1 + 7 \times 8^0 + 3 \times 8^{-1} + 5 \times 8^{-2}$$

$$256 + 16 + 7 \cdot \frac{3}{8} + \frac{5}{64}$$

$$= 279.4531$$

② $[428.35]_8 = [?]_{10}$. X.

* Conversion from Hex to decimal.

① $[6ABC.2A]_{16}$

$$\begin{array}{r} 6 \times 16^3 + 10 \times 16^2 + 11 \times 16^1 + 12 \times 16^0 + 2 \times 16^{-1} + 10 \times 16^{-2} \\ = 24576 + 2560 + 176 + 12 \cdot \frac{1}{16} + \frac{5}{16 \times 8} = \frac{8}{16 \times 8} + \frac{13}{16 \times 8} \\ = 27324.1640 \end{array}$$

* Octal & Hexadecimal Number System.

The conversion from & to binary, octal, hexadecimal placed an important part in digital computers. Since $2^3 = 8$ & $2^4 = 16$ each octal digit corresponds to 3 binary digits & each hexadecimal digit corresponds to 4 binary digits.

The conversion from binary to octal is easily accomplished by partitioning in binary nos. into groups of 3 digits each starting from binary point & proceeding left & to the right. The corresponding octal no. is then assigned to each group.

Binary to Octal.

$$[111011100011.1010101]_2 = [?]_8$$

111 011 100 011 . 101 010 100

7 3 4 3 . 5 2 4

$$[7343.524]_8$$

④ Conversion from Binary to Hexadecimal.

It is similar except that a binary no. is divided into groups of 4 digits.

$$[10011100011.1010101]$$

$$\begin{array}{r} 0110 \quad 1110 \quad 0011 \cdot 1010 \quad 1010 \\ 6 \quad 14 \quad 3 \quad \cdot \quad 10 \quad 10 \\ 6 \quad F \quad 3 \quad \cdot \quad A \quad A \end{array}$$

$$[6F3.AA].$$

④ Octal to Binary.

This conversion [Octal / hexadecimal] \rightarrow [Binary]

is done by a procedure reverse to the above. Each octal digit is converted to its three-digit binary equivalent. Similarly, each hexadecimal digit is converted to 4-digit binary equivalent.

① $[673.124]_8 = [?]_2$.

$$\begin{array}{r} 6 \quad 7 \quad 3 \quad . \quad 1 \quad 2 \quad 4 \\ 110 \quad 111 \quad 011 \quad . \quad 001 \quad 010 \quad 100 \end{array}$$

$$[110111011.001010100].$$

④ Hex to Binary.

$$[31D.CE]_{16} = [?]_2.$$

$$\begin{array}{r} 3 \quad 1 \quad D \quad . \quad C \quad E \\ 3 \quad 1 \quad 13 \quad . \quad 12 \quad 14 \\ 0011 \quad 0001 \quad 1101 \quad . \quad 1100 \quad 1110 \\ 001100011101.11001110 \end{array}$$

$$[001100011101.11001110].$$

Convert octal to hexadecimal.

$$[7324.456]_8 = [?]_{16}$$

7 3 2 4 . 4 5 6
0110 0011 010 100 100 101 110

$$[111011010100.100101110]$$

1110 1101 0100 1000 0111 0000 0,
14 13 4 . 9 7 0,
E D 4 . 9 7 0,

$$[ED4.970]$$

Convert hexal to octal

$$[EAFB.007]_{16} = [?]_8$$

E A F B . 0 0 7
14 10 15 11 . 0 0 7
1110 1010 1111 1011 . 0000 0000 0111

$$[111010101111011.0000000000111]$$

001 110 101 011 111 011 . 000 000 000 000 111
01 6 5 3 7 3 . 0 0 0 0 7

$$[165373.0007]$$

* Binary Coded Decimal Codes.

Decimal	8421 code BCD Code	(Decimal + 3) Excess-3 Code	8 4 - 2 - 1 Code
0	0000	0011	0000
1	0001	0100	0111
2	0010	0101	0110
3	0011	0110	0101
4	0100	0111	0100
5	0101	1000	1011
6	0110	1001	1010
7	0111	1010	1001
8	1000	1011	1000
9	1001	.	1111
10	0001 0000		1110
11	0001 0001		

* Weighted Code : BCD Code, (8,4,-2,-1) Code, (2,4,2,1) Code are weighted codes.

* Non-weighted Codes : Excess-3 Code, Grey/Reflected Code are the non-weighted codes.

(a) BCD Code \Rightarrow (8 4 2 1) Code i.e. BCD code. It represents each digit of decimal number by its 4-bit binary equivalent. The 6-code combinations that aren't used in BCD are 10, 11, 12, 13, 14, 15.

(b) Grey Code / Reflective Code \Rightarrow A binary code that progresses such that only one bit changes between two successive codes.

→ Conversion from binary to grey.

① $[0111]_2 = [?]_{\text{gray}}$.

Keep MSB as it is. Go xor-ing horizontally.

$$\begin{array}{cccc}
 0 & \oplus & 1 & \oplus \\
 & \downarrow & & \\
 \boxed{0} & 1 & 0 & 0 \\
 & & & \text{Grey.}
 \end{array}$$

② $[1111]_2 = [?]_{\text{gray}}$

$$\begin{array}{ccccc}
 & & 0 & 1 & 0 \\
 & & \downarrow & & \\
 1 & 1 & 1 & 1 & 0 \\
 \hline
 1 & 1 & 0 & 0 & 0
 \end{array}$$

③ $[1011001]_2 =$

$$\begin{array}{cccccc}
 1 & 0 & 1 & 1 & 0 & 0 & 1 \\
 \hline
 1 & 1 & 1 & 0 & 1 & 0 & 1
 \end{array}$$

→ Conversion from grey to binary.

keep MSB as its.

① $[1110101]_{\text{gray}} = [?]_2$.

x-or-ing diagonally.

$$\begin{array}{ccccccccc}
 1 & 1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\
 \diagup & \diagdown & \diagup & \diagdown & \diagup & \diagdown & \diagup & \diagdown & \diagup \\
 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1
 \end{array}$$

$[1011001]$

② $[1100111010]_{\text{gray}} = ?_2$

$$\begin{array}{ccccccccccccc}
 1 & 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\
 \diagup & \diagdown & \diagup \\
 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0
 \end{array}$$

$[1000101100]$

* Compliments:-

- ① r's compliment. $(r = \text{base})$,
- ② $(r-1)$'s compliment

(a) Decimal System.

$$r = 10$$

r's compliment = 10's compliment.

$(r-1)$'s " = 9's compliment.

- To get 9's compliment, subtract each digit from 9.
- To get 10's " , add '1' to 9's compliment.

e.g. $[52520]_{10}$

9's compliment = 47479.

10's compliment = ~~5858~~ 47480 [47479 + 1]

(b) Binary System.

$$r = 2$$

r's compliment = 2's compliment.

$(r-1)$'s " = 1's compliment.

- To get 1's compliment, change 1 to 0 & 0 to 1
- To get 2's compliment, add 1 to 1's compliment.

e.g. $[10010.1]$

1's compliment = 0111010.

2's compliment = 0111011. (0111010 + 1).

* Addition of Binary Numbers. / Subtraction of Binary Numbers

(A) Addition :-

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

↑ carry.

(B) Subtraction :-

$$0 - 0 = 0$$

$$0 - 1 = 1$$

Borrow

$$1 - 0 = 1$$

$$1 - 1 = 0$$

e.g.
$$\begin{array}{r} 10101 \cdot 10101 \\ + 01010 \cdot 10100 \\ \hline 11111 \cdot 01001 \end{array}$$

→ carry.

$\begin{array}{r} + 1 \\ + 1 \\ \hline 00 \end{array}$

$$\begin{array}{r} 10101 \cdot 10101 \\ - 01010 \cdot 10100 \\ \hline 11 \end{array}$$

→ Borrow.

$\begin{array}{r} - 1 \\ - 1 \\ \hline 11 \end{array}$

* Octal Numbers

e.g.
$$\begin{array}{r} 527 \cdot 54 \\ + 665 \cdot 37 \\ \hline 1415 \cdot 13 \end{array}$$

$8 \mid 11 \quad (11)_{10} = (13)_8$

$\begin{array}{r} 3 \mid 3 \\ 0 \mid 3 \end{array}$

$$\begin{array}{r} 527 \cdot 54 \\ + 665 \cdot 37 \\ \hline 135 \cdot 63 \end{array}$$

$8 \mid 665 \quad 665$

$\begin{array}{r} 328 \\ 3 \mid 28 \\ 8 \mid 8 \end{array}$

* Hex.

$$\begin{array}{r} 20(A0)7 C.11310 D \\ + 8 D 9 E 8 B \\ \hline 3.356(8)198 \end{array}$$

$(24)_{10} = (18)_{16}$

$16 \mid 24 \quad 16 \mid 17$

$\begin{array}{r} 16 \mid 18 \\ 16 \mid 18 \\ 0 \mid 17 \end{array}$

$0 = 0 - 0$

$1 = 1 - 0$

$1 = 0 + 1$

$0 = 1 - 1$

$0 = 1 + 1$

* Subtraction by r's compliment.

The subtraction of 2 +ve nos. ($M-N$), both of base "r", may be done as follows.

- 1) Add Minuend (M) to the r 's compliment of Subtrahend N .
- 2) Inspect the result obtained in 1) for an end carry.
 - (a) If an end carry occurs, discard it.
 - (b) If an end carry does not occur, then take the r 's compliment of the no. obtained in step 1) & place a negative sign in front.

e.g. ① Using 10's complement, subtract $72532 - 3250$.

Here $M = 72532$.

$N = 03250$.

9's compli. of N : 96749.

10's " " " : 96750.

$$\begin{array}{r} \text{Now } M + 10\text{'s comp. of } N = \\ 72532 \\ + 96750 \\ \hline 169282 \end{array}$$

end carry \leftarrow

\therefore Ans. 69282.

② subtract $3250 - 72532$.

Here, $M = 03250$

$N = 72532$.

9's compli. of N : 27467.

10's " " " : 27468.

$$\begin{array}{r} \text{Now, } M + N\text{'s comp. of } N = \\ 03250 \\ + 27467 \\ \hline 30717 \end{array}$$

no end carry. \leftarrow

Now, 9's comp. of X = 69282.

10's " " " = 69282.

\therefore Ans : -69282.

③ Using 2's compliment, to perform M-N with the given binary nos. $M = 1010100$

$$N = 1000100.$$

$$1\text{'s compli. of } N = 0111011.$$

$$2\text{'s } " \text{ " " } = 0111100$$

$$\text{Now, } 1010100$$

$$+ 0111100$$

$$\text{end carry } \underline{10010000}$$

$$\therefore \underline{\text{Ans}} \ 0010000. = 10000.$$

④ $M = 1000100$

$$N = 1010100.$$

$$1\text{'s compli. of } N = 0101011.$$

$$2\text{'s } " \text{ " " } = 0101100$$

$$\text{Now, } 1000100$$

$$+ 0101100$$

$$\underline{1110000}$$

$$1\$ \quad 000111$$

$$2\text{'s} \quad 0010000$$

$$\therefore \underline{\text{Ans}} -10000.$$

* Subtraction by (r-1)'s compliment

i) Add the Minuend M to the (r-1)'s compliment of subtrahend N.

2) Inspect the result obtained in step *<1>* for an end carry

- *(a)* If end carry occurs add 1 to the least significant digit (end around carry).

(b) If end carry doesn't occur, take the (r-1)'s compliment of the number obtained in step *<1>* & place negative sign in front.

e.g. ① Using 9's compliment, subtract $72532 - 3250$.

$$M = 72532$$

$$N = 03250$$

$$\text{9's compli. of } N = 96749.$$

$$\therefore M + \text{9's compli} = 72532.$$

$$\begin{array}{r}
 & \text{t} & 9 & 6 & 7 & 4 & 9 \\
 & \swarrow & & & & & \searrow \\
 \text{end carry.} & \xleftarrow{=} & 1 & 6 & 9 & 2 & 8 & 1
 \end{array}$$

$$\therefore 9\text{'s compli: } 18880918,$$

$$\begin{array}{r}
 1 & 6 & 9 & 2 & 8 & 1 \\
 \swarrow & & & & & \searrow \\
 \text{end around carry.}
 \end{array}$$

$$\therefore 69282$$

$\therefore \underline{69282}$: Ans.

② $M = 03250$

$$N = 72532$$

$$\text{9's compli. of } N = 27467$$

$$M + \text{9's compli} = 27467$$

$$\begin{array}{r}
 & & & & 0 & 3 & 2 & 5 & 0 \\
 & & & & \swarrow & & & & \searrow \\
 \text{no end carry.} & & & & 3 & 0 & 7 & 1 & 7
 \end{array}$$

$$\therefore \text{9's compli} \Rightarrow 69282.$$

$\therefore \underline{\underline{Ans}} : -69282.$

③ $M = 1010100$

$$N = 1000100$$

$$\text{9's compli: } 0111011.$$

$$\therefore 1010100$$

$$\begin{array}{r}
 & 0 & 1 & 1 & 1 & 0 & 1 & 1 \\
 & \swarrow & & & & & & \searrow
 \end{array}$$

$$\begin{array}{r}
 \text{end carry.} \xleftarrow{=} 10001111 \\
 \text{end around carry.} \xrightarrow{=}
 \end{array}$$

$$0001111$$

$$111,1$$

$$\underline{0010000}$$

Ans : 10000.

$$④ M = 1000100.$$

$$N = 1010100.$$

1's compli. of N : 0101011.

$$\therefore 1000100$$

$$0101011$$

$$\hline 1101111 \rightarrow \text{no end carry.}$$

∴ 1's compli : 0010000

$$\therefore \text{Ans. } \underline{\underline{10000}}.$$

1) Given that $(16)_{10} = (100)_b$, find the value of b.

$$\rightarrow \therefore 16 = 1 \times b^2 + 0 \times b^1 + 0 \times b^0$$

$$\therefore 16 = b^2$$

$$\therefore \boxed{b = 4}$$

2) Given that $(292)_{10} = (1204)$ in some no. system, Find the base of that system.

\rightarrow Let the base be 'b'.

$$\therefore 292 = 1 \times b^3 + 2 \times b^2 + 0 \times b^1 + 4 \times b^0.$$

$$\therefore 292 = b^3 + 2b^2 + 4.$$

$$\therefore b^3 + 2b^2 = 288.$$

\because 4 is the largest digit in given no. system,

$$\therefore b^2(b+2) = 288.$$

$b^2(b+2) > 288$

$$\therefore \boxed{b=6} \quad \text{-- (by trial & error)} \quad b > 5.$$

3) In the following series, the same integer is expressed in different no. systems. Determine the missing no. of the series
10,000, 121, 100, ?, 24, 22, 20.

$$1 \times b^3 + 2 \times b^2 + 1 \times b^1 + 1 \times b^0 = 16 \times$$

\rightarrow Taking first no. in binary : $(16)_{10}$.

The next no. is (121) which is equal to $(16)_{10}$ in base 3.
Similarly (100) is equal to $(16)_{10}$ in base 4.

Then, (24) is equal to $(16)_{10}$ in base 6.

Thus, base of missing no. is 5.

$$\therefore 16 = (?)_5$$

5	16	
	3	1
	0	3

missing no. is $(31)_5$.

- 4) Each of the following arithmetic operations is correct in at least one no. system. Determine the possible bases in each operation.

(a) $1234 + 5432 = 6666$.

→ It is valid in any no. system with base greater than or equal to 7.

$\therefore \boxed{b \geq 7}$... (\because the largest digit used is 6).

(b) $\frac{41}{3} = 13$

→ Let the base be 'b'

Express both sides in decimal.

$$\frac{4b+1}{3} = b+3$$

$$\therefore 4b+1 = 8b+9.$$

$$\therefore \boxed{b = 8}$$

Hence, above expression is valid in system with base 8.

(c) $\frac{33}{3} = 11$.

Let base be 'b'.

$$\therefore \frac{3b+3}{3} = b+1.$$

\therefore It is valid for any value of G

\therefore The largest digit in the no. is 3.

$$\therefore \boxed{b \geq 4}.$$

(d) $23 + 44 + 14 + 32 = 223$.

Let the base be 'b'.

Converting to decimal.

$$2b^3 + 4b^2 + b + 4 + b^4 + 3b^3 + 2 = 2b^2 + 2b + 3.$$

$$10b + 10 = 2b^2 + 2b.$$

$$5b + 10 = b^2 + b.$$

$$\therefore 4b + 5 = b^2.$$

$$\therefore b^2 - 4b - 5 = 0.$$

$$\therefore b^2 - 5b + b - 5 = 0.$$

$$\therefore b(b-5) + 1(b-5) = 0.$$

$$\therefore \boxed{b=5}$$

Thus, the relation is valid in base 5 system.

(e) $\frac{802}{20} = 12.1.$

Let base be 'b'.

Converting to decimal.

$$\therefore \frac{8b^2 + 2}{2b} = b + 2 + \frac{1}{b}.$$

$$\therefore \frac{8b^2 + 2}{2b} = \frac{b^2 + 2b + 1}{b}$$

$$\therefore 8b^2 + 2 = 2b^2 + 4b + 2.$$

$$\therefore b^2 = 4b.$$

$$\therefore \boxed{b=4}$$

(f) $\sqrt{41} = 5.$

Let base be 'b'.

Converting to decimal.

$$\sqrt{4b+1} = 5.$$

$$\therefore 4b + 1 = 25.$$

$$\therefore 4b = 24.$$

$$\therefore \boxed{b=6}.$$

BCD Arithmetic.

In BCD code, each decimal digit, 0 to 9, is coded by a four-bit binary no. It is a weighted code & is also sequential. There are 6 illegal combinations 10, 11, 12, 13, 14, 15 that are not used i.e. 1010, 1011, 1100, 1101, 1110, 1111 in this code. They are not part of the 8-4-2-1 BCD Code System.

→ **BCD Addition:** The BCD addition is performed by individually adding the corresponding digits of the decimal nos. expressed in 4-bit binary groups starting from the LSD.

- If there is a carry-out of one group to the next group, or if the result is an illegal code, then $(6)_{10}$ (0110) is added to the sum term of that group & the resulting carry is added to next group. This is done to skip the six illegal steps.

e.g. i) Perform following decimal addn in 8-4-2-1 code.

→ i) $25 + 13$.

$$\begin{array}{r}
 25 : 0010 \quad 0101 \quad [25 \text{ in BCD}] \\
 + 13 : 0001 \quad 0011 \\
 \hline
 0011 \quad 1000 \quad [\text{No carry}] \quad [\text{No illegal code}]
 \end{array}$$

Thus, this is the correct sum.

ii) $679.6 + 536.8$.

$$\begin{array}{r}
 679.6 : 0110 \quad 0111 \quad 1001 \cdot 0110 \\
 + 536.8 : 0101 \quad 0011 \quad 0100 \cdot 1000 \\
 \hline
 1216.4 \quad 1011 \quad 1010 \quad 1111 \cdot 1110 \quad (\text{All illegal}) \\
 + 0110 \quad 0110 \quad 0110 \cdot 0110 \\
 \hline
 1111 \quad 1111 \quad 1111 \quad 11 \\
 \hline
 10010 \quad 0001 \quad 0110 \cdot 0100 \\
 \hline
 1 \quad 2 \quad 1 \quad 6 \quad . \quad 4
 \end{array}$$

- BCD subtraction: In BCD subtraction, subtract the digits of each 4-bit group of the subtrahend from the corresponding 4-bit group of the minuend in binary starting from the LSD.
- If there is a borrow from the next group then $(6)_{10}$ (0110) is subtracted from the difference term of this group. This is done to skip the six illegal states.
- In practice, subtraction is performed by the complement method. Since, we are subtracting decimal digits, we must form the 9's or 10's complement of decimal subtrahend & encode that no. in the BCD code. The resulting BCD nos. are then added.

e.g. (i) Perform following decimal subtraction in 8421 BCD code.

$$38 - 15.$$

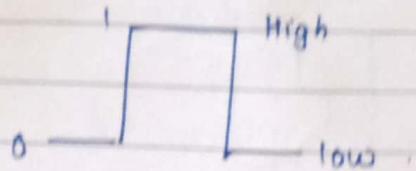
$$\begin{array}{r}
 \text{(i)} \quad \begin{array}{rr} 88 & 0011 \\ - 15 & 0001 \\ \hline 23 & 111 \end{array} \\
 \underline{0010 \quad 0011} \quad (\text{No borrow}) \quad
 \end{array}$$

$$\text{(ii)} \quad 206.7 - 147.8 .$$

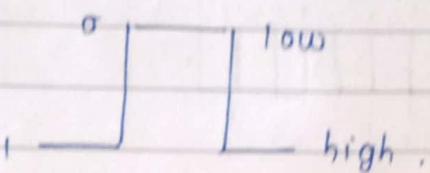
$$\begin{array}{r}
 \begin{array}{ccccccccc}
 206.7 & 0010 & 0000 & 0110 & 1 & 0111 \\
 147.8 & 0001 & 0100 & 0111 & 1 & 1000 \\
 \hline
 058.9 & 1111 & 1111 & 111 & &
 \end{array} \\
 \begin{array}{r}
 \hline
 0000 & 1011 & 1110 & \hline
 - 0110 & - 0110 & - 0110 & \\
 \hline
 0000 & 0101 & 1000 & \hline
 \end{array}
 \end{array}$$

* Positive & Negative Logic

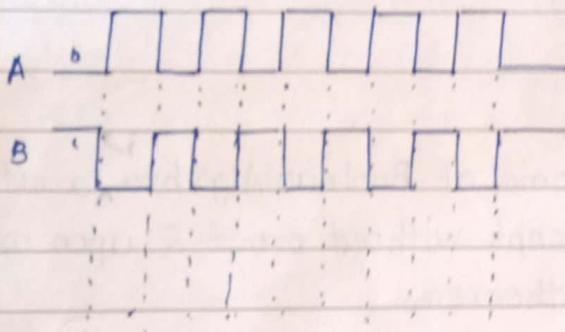
1. Positive logic :



2. Negative logic.



* Pulsed Operation of Logic Gates



a) AND

↓ ↓ ↓ ↓

b) OR

↓ ↓ ↓ ↓

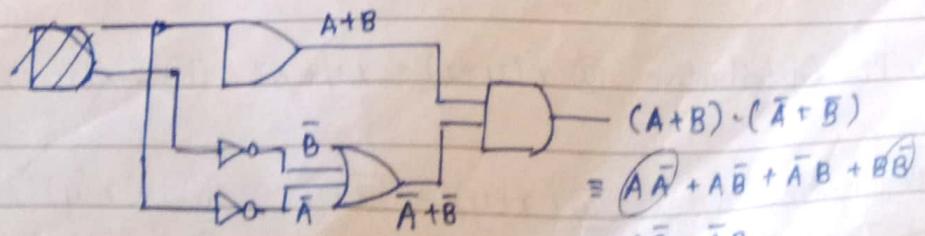
c) NAND

↓ ↓ ↓ ↓

d) NOR

q. Determine the o/p waveform in ckt shown in fig, when the i/p A & B & when i/p shown in fig A & B are applied to it.

Fig A)



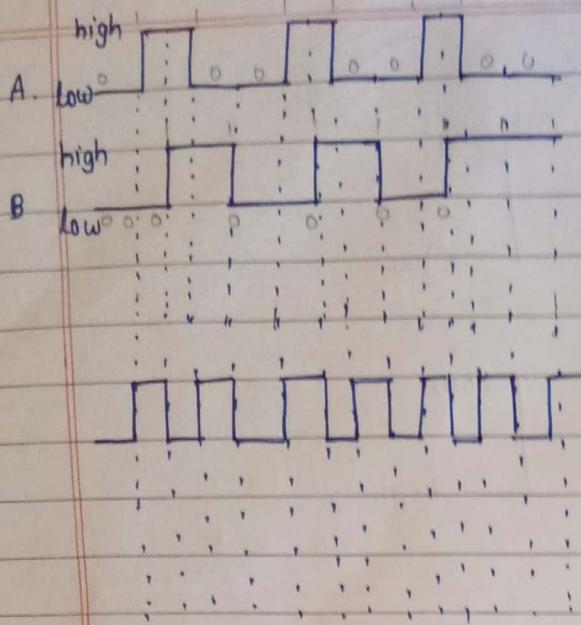
$$(A+B) \cdot (\bar{A} + \bar{B}) \\ = A\bar{A} + A\bar{B} + \bar{A}\bar{B} + B\bar{B}$$

$$= A\bar{B} + \bar{A}B$$

$$= A \oplus B \leftarrow$$

A	B	O/P
0	0	0
0	1	1
1	0	1
1	1	0

Both i/p same, o/p low.



X-or & X-NOR
complements of each other

* Boolean Algebra :-

Axioms & Laws :-

All postulates or axioms of Boolean Algebra, a set of logical expressions that we accept without proof & upon which we can build a set of useful theorems.

- 1) Postulate (a) $x + 0 = x$ (b) $x \cdot 1 = x$.
- 2) " (a) $x + x' = 1$ (b) $x \cdot x' = 0$
- 3) Theorem (a) $x + x = x$ (b) $x \cdot x = x$
- 4) Theorem (a) $x + 1 = 1$ (c) $x \cdot 0 = 0$
- 5) Th. Involution $(x')' = x$
- 6) Pos. Commutative (a) $x + y = y + x$ (b) $x \cdot y = y \cdot x$
- 7) Th. Associative (a) $x + (y + z) = (x + y) + z$ (b) $x \cdot (y \cdot z) = (x \cdot y) \cdot z$
- 8) Pos. Distributive (a) $x(y + z) = xy + xz$ (b) $x + (y \cdot z) = (x + y) \cdot (x + z)$
- 9) Th. De Moivre's (a) $(x + y)' = \bar{x} \cdot \bar{y}$ (b) $(x \cdot y)' = x' + y'$
- 10) Th. Absorption (a) $x + xy = x$ (b) $x \cdot (x + y) = x$

→ Commutative Law (theorem)

$$AB + \bar{A}C + BC = AB + \bar{A}C.$$

$$\text{LHS} = AB + \bar{A}C + BC.$$

$$= AB + \bar{A}C + BC(A + \bar{A})$$

$$= AB + \bar{A}C + ABC + \bar{A}BC.$$

$$= AB(1 + C) + \bar{A}C(1 + B),$$

$$= AB + \bar{A}C,$$

$$= \text{RHS}.$$

This theorem can be extended to any no. of variables.

$$\text{For e.g. } AB + \bar{A}C + BC\bar{B} = AB + \bar{A}C.$$

→ Transposition Theorem.

$$AB + \bar{A}C = (A + C)(\bar{A} + B)$$

$$\text{RHS} = A\bar{A} + AB + \bar{A}C + BC.$$

$$= AB + \bar{A}C + BC.$$

$$= AB + \bar{A}C + BC(\bar{A} + \bar{B})$$

$$= AB + \bar{A}C + ABC + \bar{A}BC.$$

$$= ABC(1 + C) + \bar{A}C(1 + B)$$

$$= AB + \bar{A}C.$$

Q. Reduce expression $[A + \bar{B}\bar{C}] \cdot [A\bar{B} + ABC]$.

$$\rightarrow [A + \bar{B}\bar{C}] \cdot [A\bar{B} + ABC]$$

$$= \bar{A} \cdot BC \cdot [A\bar{B} + ABC].$$

$$= \bar{A}BC[A\bar{B} + ABC].$$

$$= A\bar{A}B\bar{B} \cdot C + A\bar{A}(BC)(BC)$$

$$= 0 + 0.$$

$$= 0$$

Q. Show that $\bar{A}\bar{B}\bar{C} + B + B\bar{D} + A\bar{B}\bar{D} + \bar{A}C = B + C$.

$$\rightarrow \text{LHS} = \bar{A}\bar{B}\bar{C} + B + B\bar{D} + A\bar{B}\bar{D} + \bar{A}C.$$

$$= B + B\bar{D}(1 + A) + \bar{A}\bar{B}\bar{C} + \bar{A}C.$$

$$= B + B\bar{D} + A\bar{B}\bar{C} + \bar{A}C.$$

$$= B(1 + B) + A\bar{B}\bar{C} + \bar{A}C.$$

$$= B + C(A\bar{B} + \bar{A}C)$$

$$= B + C[(\bar{A} + A)(\bar{B} + \bar{A})]$$

$$\begin{aligned} & B + C(\bar{A}\bar{B} + \bar{A}C) \\ & B + C(\bar{A}\bar{B} + \bar{A}) \\ & B + C(\bar{A}\bar{B} + \bar{A}) \\ & B + C((\bar{A} + B) + \bar{A}) \\ & B + C[(\bar{A} + B)\bar{A}] \end{aligned}$$

$$\begin{aligned} & B + C\bar{A}\bar{B} + \bar{A}C(B + B) \\ & B + C(\bar{A}\bar{B} + \bar{A}\bar{B}C + \bar{A}\bar{B}C) \\ & B + C(\bar{A}\bar{B} + \bar{A}\bar{B}C + \bar{A}\bar{B}C) \end{aligned}$$

$$= B + \bar{B}\bar{C}(A + \bar{A}) + \bar{A}BC.$$

$$= B + C[1 \cdot (\bar{B} + \bar{A})]$$

$$= B + C [\bar{B} + \bar{A}]$$

$$= B + \bar{B}C + \bar{A}C$$

$$\cancel{B} + \bar{A}C (\text{A} \neq \bar{B})$$

\cancel{B}

$$(B + \bar{B})(B + C) + AC$$

$$B + C + AC$$

$$B + C$$

$$= C\bar{A} + (C\bar{B} + B\bar{B}) \quad \dots \text{TRANS.}$$

$$= C\bar{A} + [C\bar{B} + C] (\bar{B} + \bar{B})$$

expression

Q. Reduce the operation: $\bar{A}\bar{B} + \bar{A} + AB$

$$= AB / A / A\bar{B} \rightarrow \bar{A} + 1$$

$$= \bar{A} \cdot \bar{B} \cdot A \rightarrow 1$$

$$= \bar{A} \cdot \bar{B} \rightarrow 0$$

Q. Prove De Morgan's theorem for 3 variables.

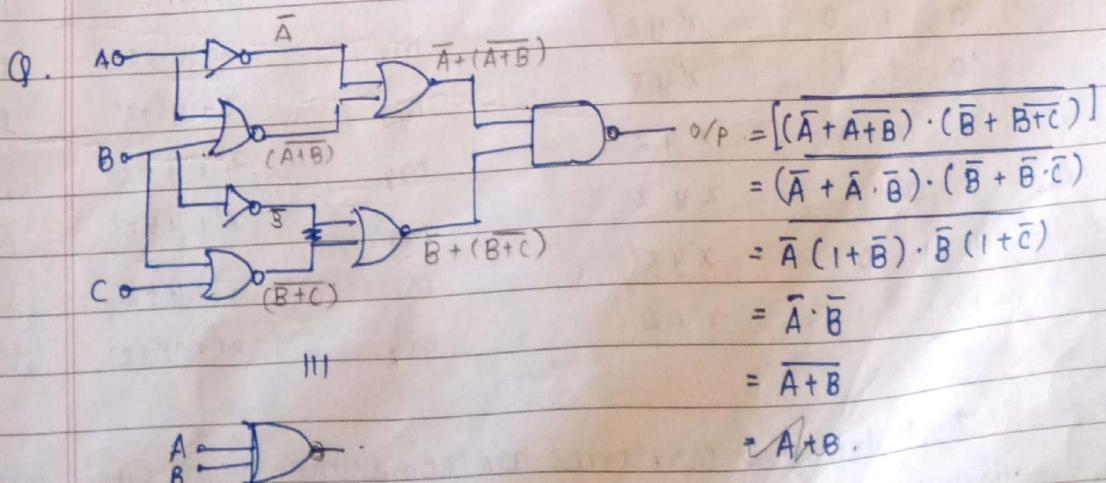
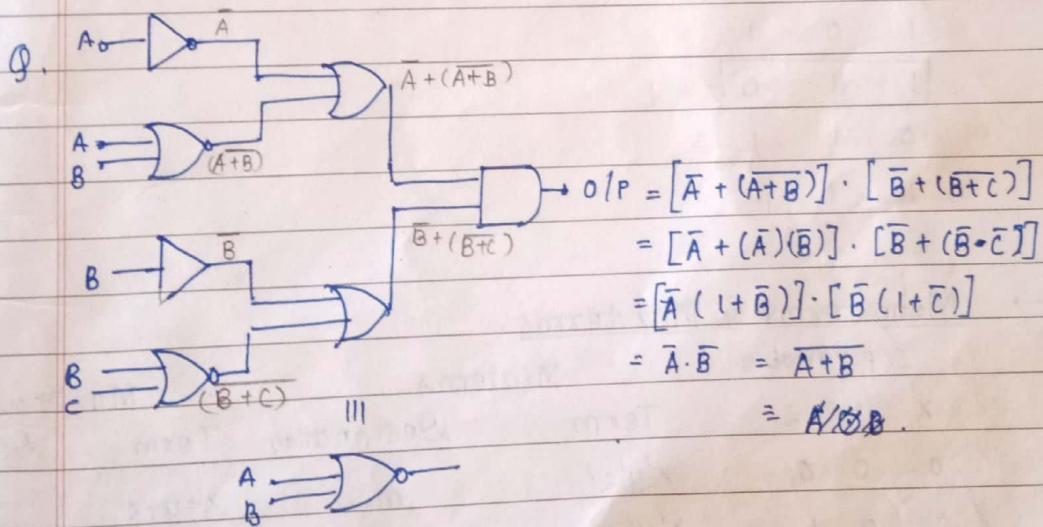
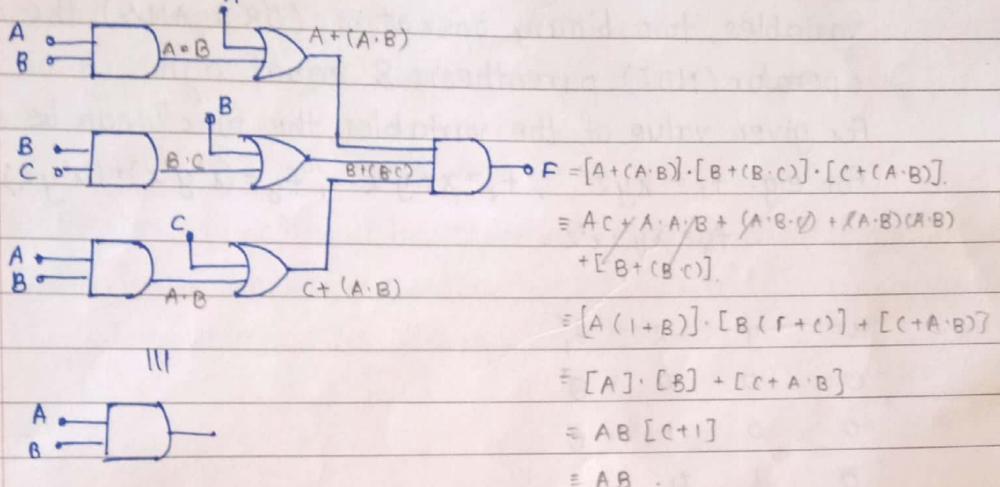
$$\textcircled{1} (A + B + C)' = A' \cdot B' \cdot C'$$

A	B	C	\bar{A}	B'	C'	
0	0	0	1	1	1	$f = A[B + \bar{C}(\bar{A}B + A\bar{C}')]$
0	0	1	1	1	0	$= A\bar{C} + \bar{C}(\bar{A}B + A\bar{C}')$
0	1	0	1	0	1	$= A(B + \bar{C}(\bar{A}(B + \bar{C})))$
1	0	0	0	1	1	$= A(B + \bar{C}(\bar{A} + \bar{B} + \bar{C}))$
1	1	0	0	0	1	$= A(B + \bar{C}(\bar{A} + \bar{B} + \bar{C})) \bar{B} \cdot 0$
0	1	1	1	0	0	$= A(B + \bar{A} \cdot \bar{C} + 0) =$
1	0	1	0	1	0	$= AB$
1	1	1	0	0	0	

$$\textcircled{2} A + B[A'C + (B + C)D] = A + BD$$

$$\textcircled{3} (B + BC)(B + \bar{B}C)(B + D) = B$$

Q. Write Boolean expression for logic diagram & simplify as much as possible & draw logic diagram that implements the simplifying expression.



* Boolean Function:-

A binary variable can take the value of 0 or 1.

A Boolean function is an expression formed with binary variables, two binary operators (OR & AND), the unary operator (NOT), parenthesis & equal sign.

For given value of the variables, the funcⁿ can be either 0 or 1.
For e.g. $f_1 = xyz'$, $f_2 = x + y'z$, $f_3 = (x'y'z) + (x'yz) + (xy)$
 $f_4 = xy' + x'z$.

x	y	z	f_i
0	0	0	0
0	0	1	0
0	1	0	
1	0	0	
1	0	1	
1	1	0	1
0	1	1	
1	1	1	

→ Mean terms & Max terms.

I/P variables.

x	y	z	Term	Minterms	Term	Maxterms
0	0	0	$x'y'z'$	m_0	$x+y+z$	M_0
0	0	1	$x'y'z$	m_1	$x+y+z'$	M_1
0	1	0	$x'yz'$	m_2	$x+y'+z$	M_2
0	1	1	$x'yz$	m_3	$x+y'+z'$	M_3
1	0	0	$xy'z'$	m_4	$x'+y+z$	M_4
1	0	1	$xy'z$	m_5	$x'+y+z'$	M_5
1	1	0	xyz'	m_6	$x'+y'+z$	M_6
1	1	1	xyz	m_7	$x'+y'+z'$	M_7

→ Minterms & Maxterms are complements of each other.

- Each minterm is obtained from an "AND" term of the n variables with each variable being 'primed' if the corresponding bit of

binary number is zero.(0) & unprimed if the corresponding bit of binary no. is (1).

- In similar way, M variables forming an 'OR' term with each variable being primed, if the corresponding bit of the binary no. is '1' & unprimed if the corresponding bit of binary no. is 0.
- A Boolean funcⁿ may be expressed algebraically by forming a ^{min} ~~mean~~ term for each combination of variables which produces '1' & then taking the OR-ing of all those min terms.

x	y	z	F_1	F_2
0	0	0	0	0
0	0	1	①	0
0	1	0	0	0
0	1	1	0	①
1	0	0	①	0
1	0	1	0	①
1	1	0	0	①
1	1	1	①	①

$$F_1 = x'y'z + xy'z' + xyz$$

$$F_2 = x'yz + x'y'z + xyz' + xyz.$$

These examples demonstrate an imp. property of Boolean algebra.

In sum of product [SOP] in sum of minterms form.

(contd.)

Now consider the complement of a Boolean funcⁿ. It may be read from the truth table by forming a min term for each combination that produces & then OR-ing those terms.

The compliment of F_1 is written as
The compliment of F_1 is read as

$$F_1' = x'y'z' + x'yz' + x'yz + xy'z + xyz'$$

on substituting F' we get

If we take the complement of F_i' we get F_i .

$$\begin{aligned} \therefore (F_1')' &= F_1 = \overbrace{\cancel{x'y'z} + \cancel{x'yz'} + \cancel{x'yz} + \cancel{xy'z} + \cancel{xyz'}}^{\cancel{x'y'z} + \cancel{x'yz'} + \cancel{x'yz} + \cancel{xy'z} + \cancel{xyz'}} \\ &= \cancel{x'y'z} + \cancel{x'yz'} + \cancel{x'yz} + \cancel{xy'z} + \cancel{xyz'} \end{aligned}$$

$$\begin{array}{c}
 \overline{x'y'z'} \cdot \overline{x'y'z'} \cdot \overline{x'y'z} \cdot \overline{xy'z} \cdot \overline{xyz'} \\
 x+y+z \cdot x+y'+z \cdot x+y'+z' \cdot x+y+z \\
 M_1 \quad M_2 \quad M_3 \quad M_4 \quad M_5 \\
 (\text{pos form})
 \end{array}$$

$$F_1 = (x'y'z) + (xy'z') + (xyz)$$

$$= M_1 + M_4 + M_7$$

$$f_1 = \leq(1,4,7)$$

This example demonstrate second important property
 poles - any boolean function can be expressed as a
 product of sums or product of max terms

The procedure for obtaining the product of max terms directly from the truth table is as follows:

i) Form a max term for each combination of the variables which produces 0 in the funcⁿ & then ANDing of all those Max terms.

Conversion between two Canonical forms: (SOP & POS)

$$\text{e.g. } P(x; y, z) = \pi(0, 2, 4, 5) \text{ (min)}$$

$$P(x,y,z) = \sum (1, 3, 6, 7)$$

$$\Sigma + (A, B, C, D) = \Sigma^{(1, 7)}$$

$$= \pi (0, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, \\ 13, 14, 15)$$

Non-Standard Form :

$$\begin{aligned}
 & (AB + CP)(A'B' + C'D') \\
 &= ABA'B' + ABC'D' + A'B'CD + CAD'C'D' \\
 &= ABC'D' + A'B'CD
 \end{aligned}$$

Q. Express Boolean Funcⁿ $F = A + B'C$ in a sum of minterms form.

→ The funcⁿ has 3 variables A, B & C. The first term A is missing two variables.

$$A = A(B+B') = AB + AB'$$

This is still missing one variable.

$$\begin{aligned}
 \therefore A &= (AB + AB')(C+C') \\
 &= ABC + ABC' + AB'C + AB'C'
 \end{aligned}$$

The second $B'C$ missing A.

$$\therefore B'C = B'C(A+A') = AB'C + A'B'C.$$

Combining all terms.

$$F = A + B'C = ABC + ABC' + AB'C + AB'C' + AB'C + A'B'C.$$

But $AB'C$ appears twice & according to th^m.

$$x+x=x$$

It is possible to remove one.

$$\begin{aligned}
 F &= A'B'C + AB'C + AB'C + ABC' + ABC \\
 &= \Sigma(1, 4, 5, 6, 7) \\
 &= \pi(2, 3, 8)
 \end{aligned}$$

Q. $F = xy + x'z$.

→ The funcⁿ into OR terms using the distributive law.

$$\begin{aligned}
 & (xy+x')(xy+x) \\
 & (x'+x)(x+y) (x+z)(y+z) \\
 & (x+x')(x+y) (x+z)(y+z) \\
 & (x'+y)(x+z) (y+z)
 \end{aligned}$$

The funcⁿ has 3 variables x, y & z each OR term is missing one variable.

$$\begin{aligned}
 \therefore (x'+y) &= (x'+y)\cancel{(x+x')} = (\cancel{x+x'}+y+x')x'z \\
 &= (x'+y) + xz' = (x+y+z)(x'+y+z')
 \end{aligned}$$

Finally

$$(x+y+z)(x+y'z)+(x'y+z)(x'+y+z') .$$

→ Simplification of Boolean Functions by K-Map [Karnaugh Map]

The map method provides a simple straight-forward procedure for minimizing Boolean function. Map is a diagram made up of squares. Each square represents 1 minterm. Since, any Boolean funcⁿ can be expressed as sum of minterms, it follows that a Boolean funcⁿ is recognized graphically in map from an area enclosed by those squares whose minterms are included in the funcⁿ. In fact, the map presents a visual diagram of all possible ways. A function may be expressed in a standard form. By recognizing various patterns, the user can derive alternative algebraic expressions for the same function, from which he can select the simplest function. We shall assume that the simplest algebraic expression is any one in a sum of products or product of sums i.e. it has minimum no. of literals. This expression is not necessarily unique.

(a) Two variable Map.

i) For Minterms :

	0	1
0	$x'y'$	$x'y$
1	xy'	xy

(SOP)

ii) For Maxterms

	0	1
0	$x+y$	$x+y'$
1	$x'+y$	$x'+y'$

(POS)

(b)

	$B'C'$	$B'C$	BC	BC'
A'	ABC'	$AB'C$	ABC	ABC'
$A'0$	$A'B'C'$	$A'B'C$	$A'BC$	$A'BC'$

	$B'C'$	$B'C$	BC'	BC	$B'C$
A'	$A'+B+C$	$A'+B+c'$	$A'+B+c$	$A'+B+c'$	$A'+B'c$
$A'0$	$A+B+C$	$A+B+c'$	$A+B+c$	$A+B+c'$	$A+B'c$

Q. Simplify: $f = x'y'z + x'y'z' + xy'z' + xy'z$.

→ (a) First mark 1 at blocks of given terms.

	3	2	4	5
$x'y'z$	00	01	11	10
$x'y'z'$	00	01	11	10
$xy'z'$			1	1
$xy'z$			1	0

(Write ~~the same~~ variables).

OR the obtained terms.

$$\therefore f = x'y' + x'y. \quad (\text{X-OR Gate}).$$

Take $2, 4, 8, n, 2$.

Q. Simplify: $f = x'y'z + x'y'z' + xy'z' + xyz + xyz'$.

	3	2	4	5	6
$x'y'z$	00	01	11	10	
$x'y'z'$	00	01	11	10	
$xy'z'$			1	1	
xyz			1	1	
xyz'			1	0	

\downarrow

$$\therefore f = xz' + yz.$$

$$= x'z \cdot y'z'$$

$$= x$$

Q. $\Sigma m(0, 2, 3, 4, 5, 6)$ using mapping & implement in AOI logic as well as NANO logic.

	3	2	1	0
A	BC	$B'C'$	$B'C$	BC'
A'	00	01	11	10
A'	10	11	10	11
A	11	10	01	00

\downarrow

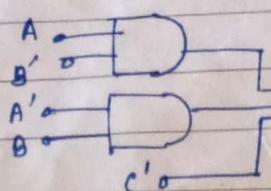
$$C' \quad AB'$$

$$f = C' + AB' + A'B. \quad (\text{using KMap}).$$

$$C' + \overline{A'B} \cdot AB' \\ \equiv \overline{C} \cdot A'B \cdot \overline{AB}$$

NANO LOGIC.

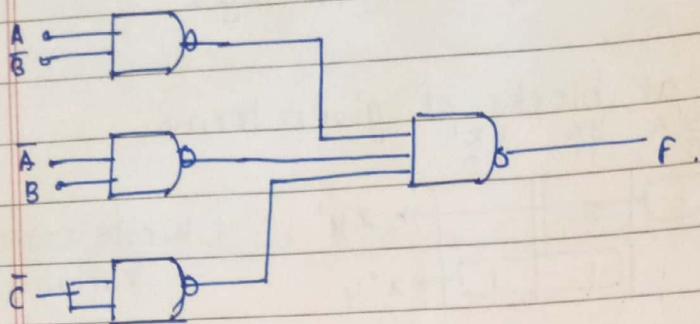
AOI Logic



$$f = C' + AB' + A'B$$

$$f' = \overline{C' + AB' + A'B}$$

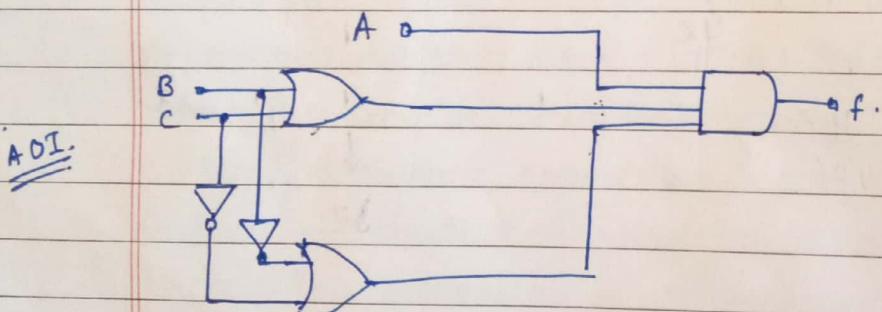
$$(f')' = \overline{\overline{C} \cdot \overline{AB} \cdot \overline{A'B}}$$



- Q. Reduce the expression $\prod M(0, 1, 2, 3, 4, 7)$ (POS) using mapping & implement it in AOI logic & NOR logic.

	$B'C$	$B'C'$	$B'C'$	$B'C'$
A	00	01	10	10
A'	0	1	1	0
$B + C$	0	1	1	0
$B' + C'$	1	0	0	1

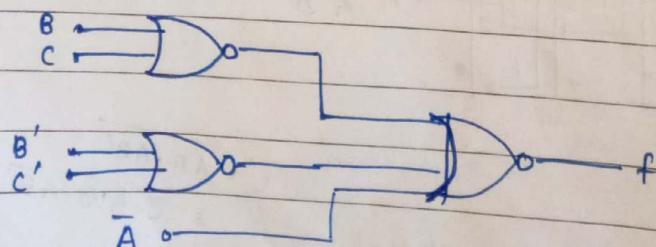
$$\therefore f = A \cdot (B+C) \cdot (B'+C') \quad (\text{POS})$$

NOR

$$f = A \cdot (B+C) \cdot (B'+C')$$

$$\therefore f' = \overline{A \cdot (B+C) \cdot (B'+C')} = \overline{A} + (\overline{B+C}) + (\overline{B'+C'})$$

$$(f')' = f = \overline{\overline{A} + (\overline{B+C}) + (\overline{B'+C'})}$$



(c) Four-variable maps.

\overline{AB}	\overline{CD}	$C'D'$	$C'D$	CD	CD'
\overline{AB}	\overline{CD}	00	01	11	10
$A'B' 00$	$A'B'C'D'_0$	$A'B'C'D_1$	$A'B'C'D'_3$	$A'B'C'D_2$	
$A'B' 01$	$A'B'C'D'_4$	$A'B'C'D'_5$	$A'B'C'D'_7$	$A'B'C'D'_6$	
$AB \quad 11$	$ABC'D'_2$	$ABC'D'_3$	$ABC'D'_5$	$ABC'D'_4$	
$AB' \quad 10$	$AB'C'D'_8$	$AB'C'D'_9$	$AB'C'D'_{11}$	$AB'C'D'_{10}$	

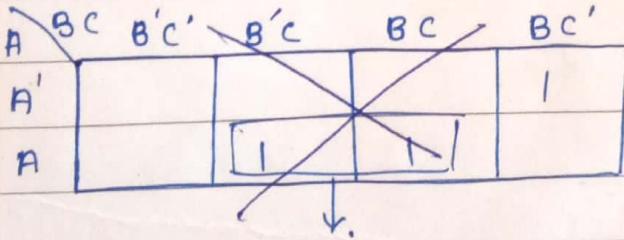
pos

\overline{AB}	\overline{CD}	AB	$\overline{A}\overline{B}$	$\overline{A}B$	$\overline{A}\overline{B}$
\overline{AB}	\overline{CD}	00	01	11	10
$A+B \quad 00$	$A+B+C+D_1$	$A+B+C+\overline{D}_2$	$A+B+\overline{C}+\overline{D}_4$	$A+B+\overline{C}+D_3$	
$\overline{A}\overline{B} \quad 01$	$\overline{A}+\overline{B}+C+D_5$	$\overline{A}+\overline{B}+C+\overline{D}_6$	$\overline{A}+\overline{B}+\overline{C}+\overline{D}_8$	$\overline{A}+\overline{B}+\overline{C}+D_7$	
$\overline{A}\overline{B} \quad 11$	$\overline{A}+\overline{B}+C+\overline{D}_{12}$	$\overline{A}+\overline{B}+C+\overline{D}_{13}$	$\overline{A}+\overline{B}+\overline{C}+\overline{D}_{15}$	$\overline{A}+\overline{B}+\overline{C}+D_{14}$	
$\overline{A}\overline{B} \quad 10$	$\overline{A}+\overline{B}+C+D_8$	$\overline{A}+\overline{B}+C+\overline{D}_9$	$\overline{A}+\overline{B}+\overline{C}+\overline{D}_{11}$	$\overline{A}+\overline{B}+\overline{C}+D_{10}$	

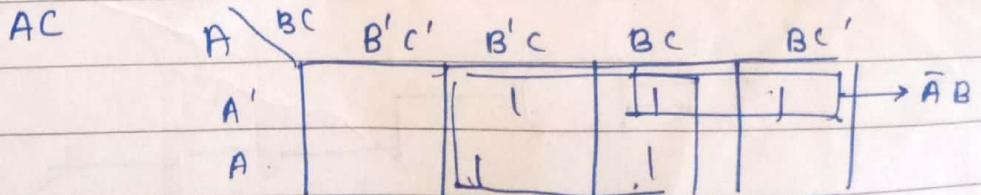
pos

Q. Simplify $f = \overline{A}C + \overline{A}B + A\overline{B}C + BC$.

$$\begin{aligned}
 &= \overline{A}C(B + \overline{B}) + \overline{A}B(C + \overline{C}) + A\overline{B}C + BC(A + \overline{A}) \\
 &= \overline{A}CB + \underline{A\overline{B}C} + \underline{\overline{A}BC} + \overline{A}\overline{B}\overline{C} + \underline{A\overline{B}C} + ABC + \underline{\overline{A}BC} \\
 &= A\overline{B}C + \underline{\overline{A}BC} + \overline{A}\overline{B}\overline{C} + ABC + \underline{\overline{A}BC} \\
 &= A\overline{B}C + \overline{A}\overline{B}\overline{C} + ABC.
 \end{aligned}$$



$$f = AC + BC'$$



Q) Reduce using mapping. the expression $\sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$
 & implement in universal logic. $\Rightarrow \Pi M(4, 6, 11, 14, 15)$

AB\CD	00	01	11	10
00	0	2	0	2
01	0	5	5	6
11	12	13	0	15
10	8	9	0	11

$$\sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13) \\ \Rightarrow \Pi M(4, 6, 11, 14, 15)$$

$$f = (\bar{A} + \bar{B} + b) \cdot (\bar{A} + \bar{B} + \bar{c}) \\ \cdot (\bar{A} + \bar{c} + \bar{b})$$

1	1	1	1
1	1	1	1
1	1	1	1
1	1	1	1

1	0	1	1	1	3	1	3
4		5		7		6	
12	1	13	15	11	14	10	
8	1	9	11	10			

$A\bar{C}$

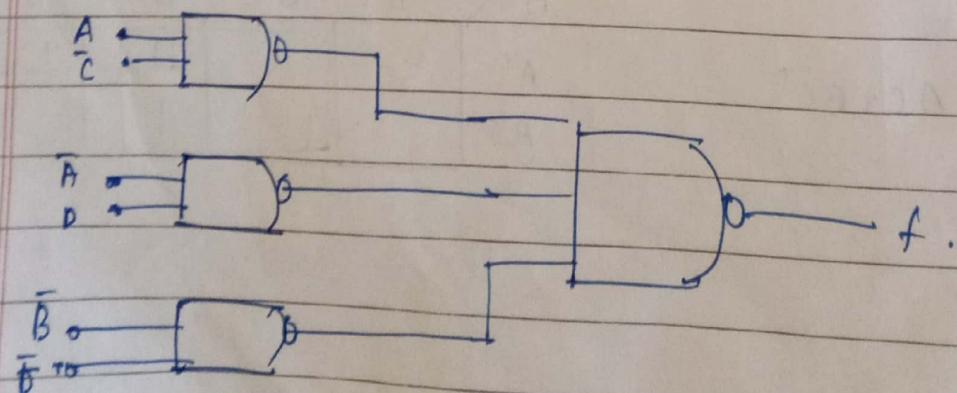
$\bar{B}\bar{D}$

$\bar{A}D$

$$f = A\bar{C} + \bar{A}D + \bar{B}\bar{D}$$

$$f' = \overline{A\bar{C} + \bar{A}D + \bar{B}\bar{D}}$$

$$(f')' = \overline{\overline{A\bar{C}} \cdot \overline{\bar{A}D} \cdot \overline{\bar{B}\bar{D}}}$$

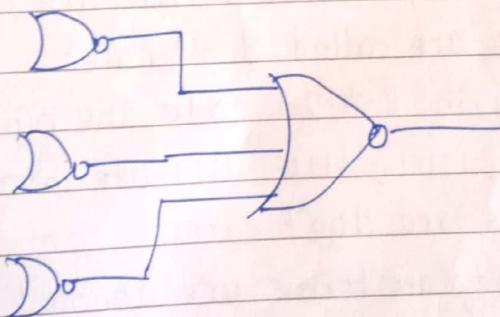
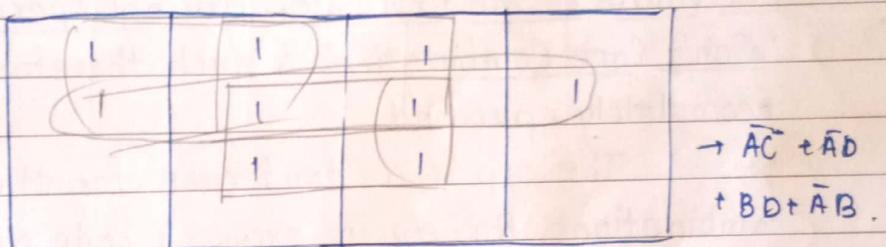


(0, 12, 13)

Q. Reduce using mapping $F = \pi M(2, 8, 9, 10, 11, 12, 14)$.

$AB \backslash CD$	00	01	10	11	
AB' 00	0	1	3	2	$C' + D + B$
AB' 01	4	5	7	6	$A' + D$
$A'B' 11$	0	12	13	15	
$A'B' 10$	0	8	9	11	$A' + B$

$$f = (B + D + C') \cdot (A' + D) \cdot (A' + B)$$



Q. $\Sigma M(0, 2, 3, 4,$
 $\pi M(1, 5, 6, 7)$

Don't Care Conditions / Combinations

The expressions specified / have been specified for every combinⁿ of input variables i.e. each minterm has been specified as a 1 each max term has been specified as a 0.

It often occurs that for certain i/p combinⁿ, the value of the o/p is unspecified either because the i/p combinations are invalid or because the precise value of the o/p is of no consequence. The combinations for which the values of the expression are not specified are called 'Don't Care Combination'. & such therefore stand incompletely specified.

The o/p is a don't care for these invalid combinations. For e.g. in excess-3 code system, the binary states 000, 0001, 0010, 1101, 1110, 1111 are unspecified & never occur. These are called don't cares.

Similarly, in 8-4-2-1 code, the binary states 1010, 1011, 1100, 1101, 1110, 1111 are invalid & the corresponding o/p's are don't cares.

The don't care terms are denoted by d, x or ϕ . During the process of design using a SOP map, each don't care is treated as a 1, if it is helpful in map reduction, otherwise it is treated as a 0 and left alone. During designing using a POS map, each don't care is treated as 0 if it is helpful in map reduction, otherwise it is treated as 1 & left alone.

An SOP expression with don't cares can be converted into a POS form by keeping the don't cares as they are & writing the missing ~~mean~~ minterms of SOP form as the maxterm of POS form. Similarly to convert a POS expression with don't cares into an SOP expression keep the dont care ~~as~~ as they are & write the missing ~~maxt~~ of POS as minterms of SOP.

1. Reduce: $\Sigma_m(1, 5, 6, 12, 13, 14) + \Sigma_d(2, 4)$

Implement in universal logic.

TLM (0, 2, 3, 4, 7, 8, 9, 10, 11, 15)

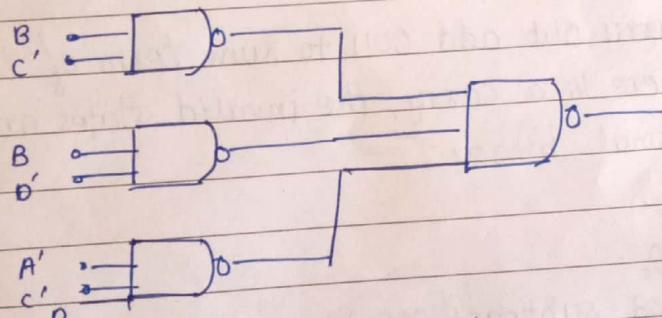
AB	CD	$C'D'$	$C'D$	CD	CD'
$A'B'$	00	0	1	1	2
$A'B$	01	X	1	5	6
AB	11	1	1	13	14
AB'	10	8	9	11	10

\downarrow
 BC'

$$f = BC' + BD' + A'C'D$$

$$f' = \overline{BC'} \cdot \overline{BD'} \cdot \overline{A'C'D}$$

$$f' = (f')' = \overline{\overline{BC'} \cdot \overline{BD'} \cdot \overline{A'C'D}}$$



AB	CD	$C+D$	$C'+D'$	$C'+D$	$C+D'$
$A+B$	00	0	0	1	2
$A+B'$	01	X	4	5	6
$A'+B'$	11	12	13	0	14
$A'+B$	10	0	8	9	10

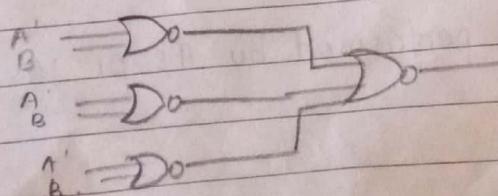
$B+D$

$C'+D'$

$A'+B$

$$f = (A'+B) \cdot (C'+D') + (A'+B)$$

$$f' = \overline{(A'+B)} + \overline{(C'+D')} + \overline{(A'+B)}$$



3 1 8 0 0
X 3 8 8 0 0

XS-3 Arithmetic :-

It is a non-weighted BCD code. It is a sequential code & therefore can be used for arithmetic operations. It is a self-complementing code. Hence, subtraction by the method of complement add" is more direct in XS-3 code than that in 8-4-2-1 code.

The XS-3 code has 6 invalid states 0000, 0001, 0010, 1001, 1110, 1111.

⇒ XS-3 Addition

To add in XS-3, add the XS-3 numbers by adding the 4-bit groups in each column starting from the LSD.

If there is no carry out from addition of any of the 4-bit groups, subtract 0011 from the sum term of those groups because when 2 decimal digits are add in XS-3 & there is no carry, the result is in XS-6.

If there is a carry out add 0011 to sum term of those groups because when there is a carry, the invalid states are skipped & result is in normal binary.

⇒ XS-3 Subtraction.

To subtract in XS-3, subtract XS-3 nos. by subtracting each 4-bit group of subtrahend from the corresponding 4-bit grp. of minuend starting from LSD.

If there is no borrow from next 4-bit grp, add 0011 to the difference term of such groups because when decimal digits are subtracted in XS-3 & there is no borrow, the result is in normal binary.

If there is a borrow subtract 0011 from the diff-term bcoz taking a borrow is equivalent to adding 6 invalid states, so, the result is in XS-6.

In practice, subtraction is performed by 9's or 10's complement method.

Q. Perform following operations in XS-3 codes.

(A) Addition

$$(247.6 + 359.4)$$

$$+ 333.3 \quad 335.5$$

$$\qquad\qquad\qquad \begin{matrix} & & 13 \\ & \downarrow & \rightarrow (3+3) \\ 0100 & 0110 \end{matrix}$$

$$\begin{array}{r}
 247.6 \qquad 0101 \quad 0111 \quad 1010 \cdot 1001 \\
 359.4 \qquad 0110 \quad 1000 \quad 1100 \cdot 0111 \\
 \hline
 607.0 \qquad 1111 \quad 1111 \quad 1 \quad 111 \\
 1100 \quad 0000 \quad 0111 \cdot 0000 \\
 - 0011 + 0011 + 0011 + 0011 \\
 \hline
 \cancel{11} \qquad \cancel{11} \\
 \cancel{1001} \quad 0011 \quad 1010 \cdot 0011 \\
 \hline
 \begin{matrix} 1001 \\ (9-3) \\ 6 \end{matrix} \quad \begin{matrix} (3-3) \\ 0 \end{matrix} \quad \begin{matrix} (16-3) \\ 7 \end{matrix} \cdot \begin{matrix} (3-3) \\ 0 \end{matrix}
 \end{array}$$

B) Subtraction

$$(57.6 - 27.8)$$

$$333 \quad 333$$

$$\begin{array}{r}
 57.6 \qquad 1000 \quad 1010 \cdot 1001 \\
 27.8 \qquad - 0101 \quad 1010 \cdot 1011 \\
 \hline
 29.8 \qquad 1111 \quad 1111 \quad 11 \\
 0010 \quad 1111 \cdot 1110 \\
 + 0011 \quad - 0011 \quad - 0011 \\
 \hline
 \begin{matrix} 1 \\ 0101 \end{matrix} \quad \begin{matrix} 11 \\ 1100 \end{matrix} \cdot \begin{matrix} 1011 \\ 1011 \end{matrix} \\
 \begin{matrix} (5-3) \\ 2 \end{matrix} \quad \begin{matrix} (12-3) \\ 9 \end{matrix} \cdot \begin{matrix} (11-3) \\ 8 \end{matrix}
 \end{array}$$

BCD subtraction by 9's & 10's complement.

Q. Perform decimal sub. in BCD by 9's complement.
 $(679.6 - 885.9)$

$$\begin{array}{r} 0110 \quad 0111 \quad 1001 \cdot 0110 \\ + 1000 \quad 1000 \quad 0101 \cdot 1001 \\ \hline \end{array}$$

g's comp. of $885.9 \Rightarrow 114.0$

$$\begin{array}{r} 0110 \quad 0111 \quad 1001 \cdot 0110 \quad (679.6) \\ + 0001 \quad 0001 \quad 0100 \cdot 0000 \quad (114.0) \\ \hline \end{array}$$

$$\begin{array}{r} 0111 \quad 1000 \quad 1101 \cdot 0110 \\ \hline \end{array}$$

$$\begin{array}{r} 0111 \quad 1000 \quad 0011 \cdot 0110 \\ \hline \end{array}$$

$$\begin{array}{r} 7 \quad 9 \quad 8 \cdot 6 \\ \hline \end{array}$$

(No carry).

∴ Result is -ve & is in its 9's complement form.

The 9's comple. $\rightarrow [2 \quad 0 \quad 6 \cdot 3] - 9's \text{ comp.}$

∴ Ans : -206.3

Q. Perform the following sub. in 8421 code using 10's comp.

$$\begin{array}{r} 0110 \quad 0111 \quad 1001 \cdot 0110 \\ + 0001 \quad 0001 \quad 0100 \cdot 0000 \\ \hline \end{array}$$

10's 115.0

$$\begin{array}{r} 0111 \quad 1000 \quad 1101 \cdot 0111 \\ \hline \end{array}$$

$7 - 8, \quad 0110$

$$\begin{array}{r} 0111 \quad 1001 \quad 0011 \cdot 0111 \\ \hline \end{array}$$

$7 \quad 9 \quad 3 \cdot 7$

$$\begin{array}{r} 2 \quad 0 \quad 6 \cdot 2 + 1 \\ \hline \end{array}$$

1

2 0 6.3

Clamper :

The ckt. that places +ve or -ve pic of signal at a desired DC level.

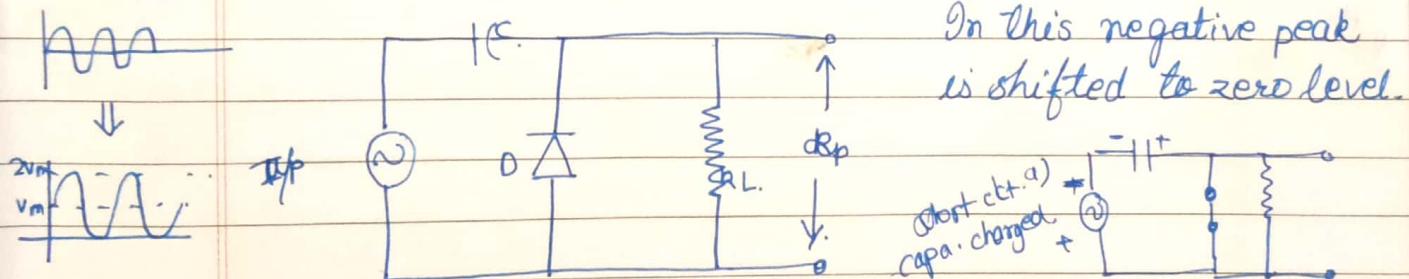
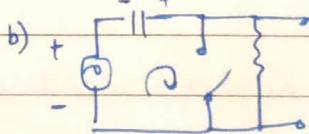
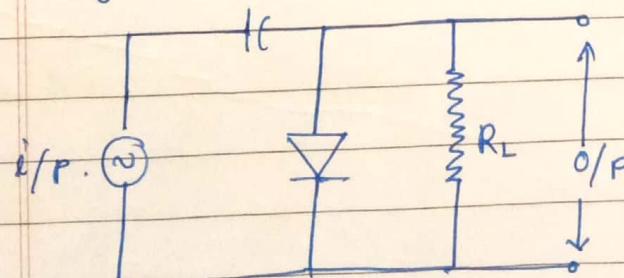
Types

- a) +ve
- b) -ve
- c) biased

+ve
-ve.

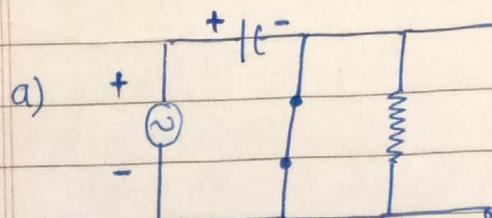
Note : Peak to peak voltage of waveform does not change
 : Shape of input waveform doesn't change.
 : Peak value as well as average value is changed.

Conditions : a) Charging time period of capacitor is very very small.
 b) Discharging time period of capacitor is very very large.

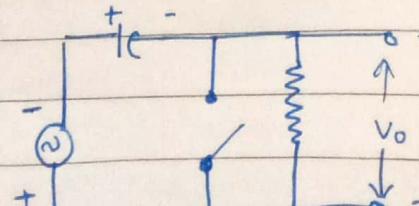
→ Positive Clamper :-→ Negative Clamper :-

$$\text{KVL: } V_m + V_m - V_o = 0 \Rightarrow V_o = 2V_m$$

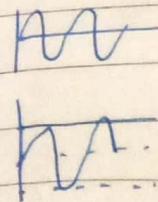
In negative clamper, this positive peak is shifted to zero level.



Diode as closed switch.
 Capacitor gets charged.

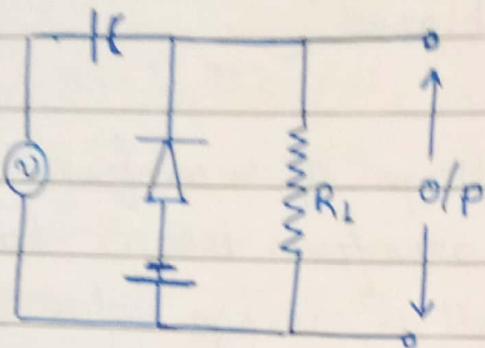


$$-V_m - V_m - V_o = 0 \Rightarrow V_o = -2V_m$$

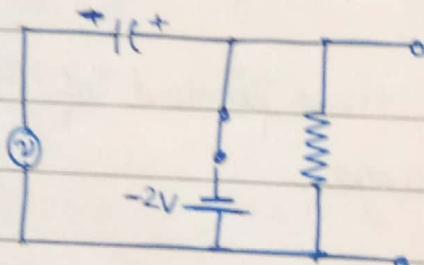


→ Biased Clamper: With the help of biased clamper +ve or -ve peak is shifted to desired DC level.

(a) +ve biased clamper



During -ve halfcycle $V_o = -2V$.



During +ve half cycle,

b) -ve biased clamper

- Knee voltage: min. forward voltage required to conduct the diode. For silicon, it 0.6 to 0.7 V. For germanium 0.3 V.
- Breakdown voltage: maximum reverse voltage above which current increases rapidly & diode damages permanently.
- PIV (Peak inverse voltage): It is max. reverse voltage that diode can withstand without damaging.
 $PIV < \text{Breakdown voltage}$.

Clipper

The ckt. by Wave-form is shaped, by removing some part of input signal is called "clipper".

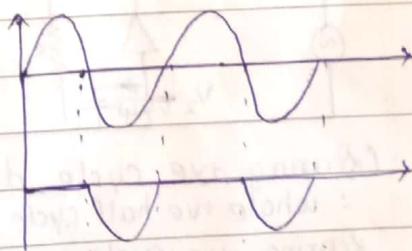
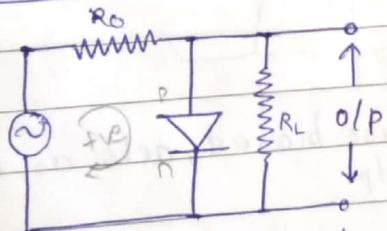
Types : i) Positive

ii) Negative

iii) Biased

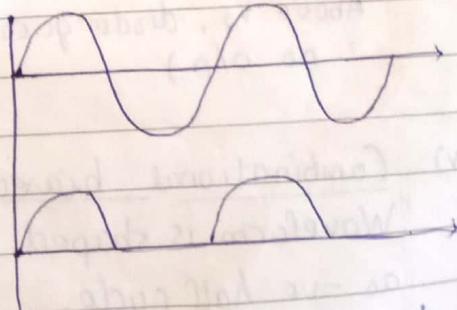
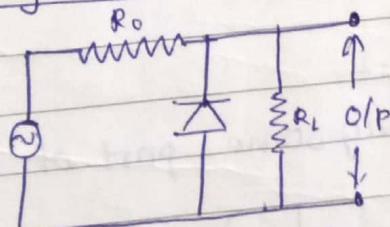
$\begin{array}{c} \xrightarrow{\text{+ve}} \\ \xrightarrow{\text{-ve}} \\ \text{combinational.} \end{array}$

i) Positive base Clipper:



Waveform is shaped by removing +ve half cycle.

ii) Negative Clipper:



Waveform is shaped by removing -ve half cycle.

During +ve half cycle, diode is reverse biased & acts as open switch.
∴ whole +ve appears at load R_L .

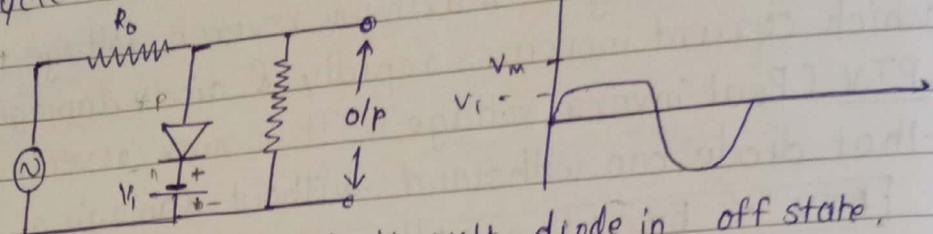
During -ve half cycle, diode is forward biased, acts as short ckt.
∴ no O/P at load).

sine \rightarrow square $\rightarrow V_m > V_1, V_2$

iii) Positive biased clipper

Waveform is shaped by removing some part of +ve half cycle.

$$V_o > V_1$$

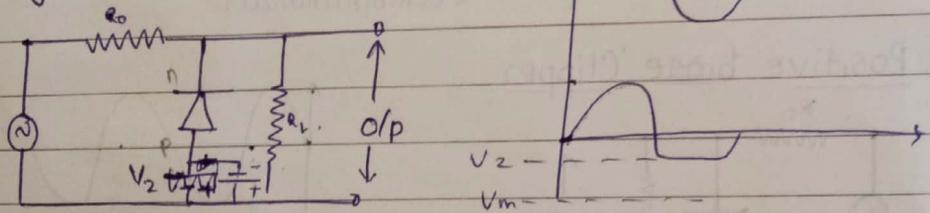


During +ve cycle, upto V_1 volt, diode is off state.
 \therefore upto V_1 volt, we get o/p.

Above V_1 , diode is forward biased, acts as short ckt.
 \therefore no o/p

During -ve cycle, diode is reverse biased, acts as open switch
 \therefore complete o/p).

iv) Negative biased clipper



During +ve cycle, diode is reverse biased, acts as open switch.
 \therefore whole +ve half cycle appears at o/p.

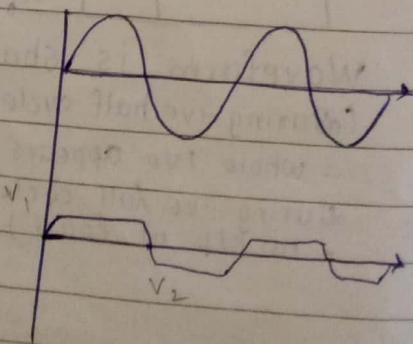
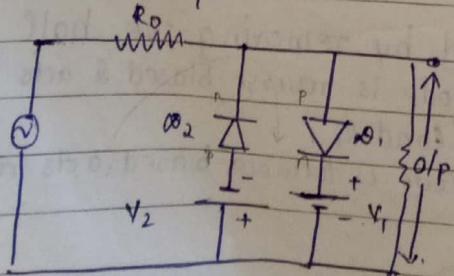
During -ve cycle,

upto V_2 , diode is OFF state.

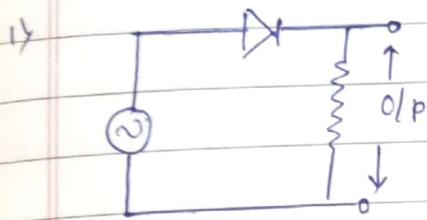
Above V_2 , diode goes in forward biased, acts as short ckt.
 \therefore no o/p)

v) Combinational biased clipper

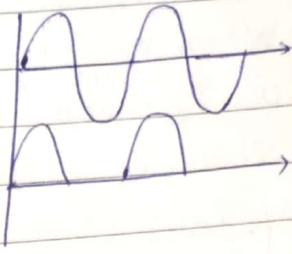
Waveform is shaped, by removing some part of +ve as well as -ve half cycle.



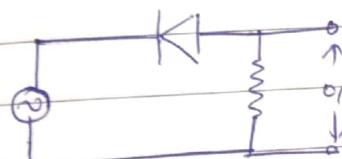
clippers



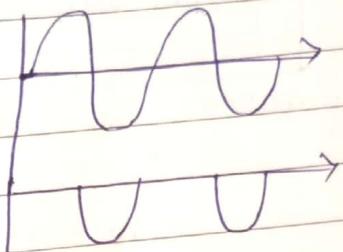
[Negative Clipper]



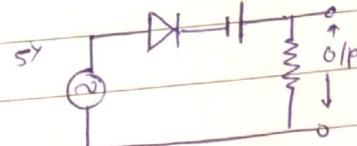
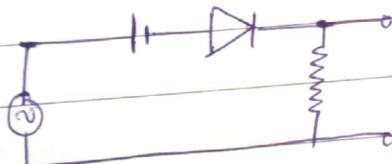
2)



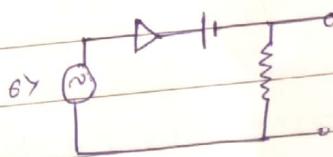
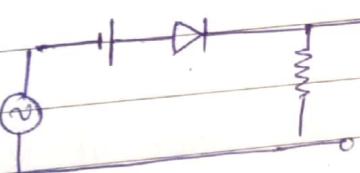
[Positive Clipper]



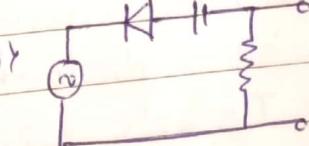
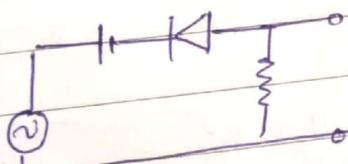
3)



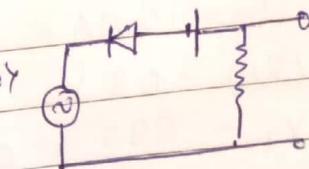
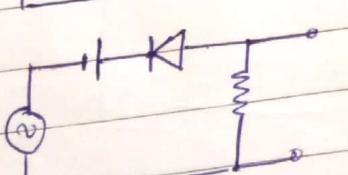
4)



7)

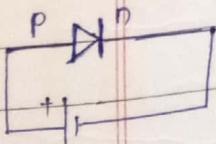


6)



Diode

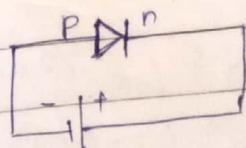
forward biased.



Knee voltage.

$$S_1 = 0.7 \text{ V}$$

$$G_e = 0.3 \text{ V}$$



Reverse biased.

Diodes

Date: _____

- When $V_D = 0$, current through diode, $I_D = 0$.
- When V_D is ~~more~~ ie Reverse Biased current through diode is, $I_D = \frac{I_{s0}}{n^n A}$ (leakage current) micro nano.
- When V_D is +ve. i.e. Forward Biased, current through diode is $I_D = i$ mA.

* Current Eqn. for diode.

$$I_D = I_s (e^{\frac{V_D}{nV_T}} - 1)$$

where, I_s = ~~forward~~ current through diode.

$I_s (I_{s0})$ = Reverse saturation current

V_D = applied ~~voltage~~ voltage across diode.

n = identity factor.

V_T = Thermal voltage.

$$V_T = \frac{kT}{q} \text{ where, } k = 1.38 \times 10^{-23} \text{ J/K.}$$

q = Magnitude of electric charge
 $= 1.6 \times 10^{-19}$.

$$V_T = \frac{T}{11600}$$

Q. Find current flowing through silicon diode at 22°C .

Reverse saturation current is $10 \mu\text{A}$. $V_D = 0.3 \text{ V}$, 0.4 V & 0.5 V

→ Given : silicon diode $\rightarrow n = 2$.

$$T = 22^\circ\text{C} = 22 + 273 = 295 \text{ K.}$$

$$I_s = 10 \mu\text{A} = 10^{-5} \text{ A.}$$

$$(V_D)_1 = 0.3 \text{ V.}$$

$$V_T = \frac{295}{11600} = 0.02543$$

$$\therefore I_D = I_s (e^{\frac{V_D}{nV_T}} - 1)$$

$$= 10^{-5} (e^{0.3/2 \times 0.02543} - 1)$$

$$= 10^{-5} (1.0038217 - 1)$$

$$= 0.0038217 \times 10^{-5} \text{ A.}$$

$$= 0.038 \mu\text{A.}$$

$$\text{Ans.} = 3.685 \text{ mA.}$$

Q. Voltage across silicon diode at room temperature 300K .

is 0.71 V , when 2.5 mA current flows through it. If voltage across diode increases to 0.8 V , calculate new I_D .

Given: $\eta = 2$, $T = 300 \text{ K}$, $(V_A) = 0.71$

$$(I_o)_1 = 2.5 \text{ mA}$$

$$V_T = \frac{300}{11600} = 0.02586.$$

$$\begin{aligned} I_s &= \frac{I_o}{e^{V_A/2V_T - 1}} \\ &= \frac{2.5 \times 10^{-3}}{e^{13.7277} - 1} \quad \text{Temperature} \\ &= \frac{2.5 \times 10^{-3}}{915933.37} \quad (I_s)_{T_2} = I_{s(T_1)} \cdot 2 \left(\frac{T_2 - T_1}{T_0} \right) \\ &= 2.7294 \times 10^{-9} \\ &= 2.7294 \text{ nA.} \end{aligned}$$

$$\begin{aligned} (I_o)_2 &= 2.7294 \times 10^{-9} \left(e^{0.8/2 \times 0.02586} - 1 \right) \\ &= (e^{15.4679} - 1) \\ &= (5219435.48 \\ &= 14245927.2 \times 10^{-9} \\ &= 14.245 \times 10^{-3} \\ &= 14.245 \text{ mA.} \end{aligned}$$

Note: For each 10°C increase in temperature, I_o (I_s) i.e. leakage current doubles.

$$(I_o)_{T_2} = I_{o(T_1)} \cdot 2 \left(\frac{T_2 - T_1}{T_0} \right)$$

- Q. If diode reverse saturation current is 2.5 mA at room temp. of $20^\circ\text{C} = 293 \text{ K}$, what will be reverse saturation current at $60^\circ\text{C} = 343 \text{ K}$. (4)
- $$\begin{aligned} (I_o)_{T_2} &= 2.5 \cdot 2 \\ &= 40.0 \text{ mA.} \end{aligned}$$

- Q. A silicon diode operates at fixed forward bias of 0.1 V . Calculate factor by which the current will get multiplied when its temperature is raised from 25°C to 150°C .

$$\frac{(I_0)_{T_2}}{(I_0)_{T_1}} = 2^{12.5} = 5792.6187 \Rightarrow (I_0)_1 = 1.7263.$$

$$(V_T)_1 = \frac{25+273}{11600} = 0.02569 \quad (I_0)_2 \\ (V_T)_2 = 0.03646.$$

$$\frac{(I_\theta)_1}{(I_\theta)_2} = \frac{(I_0)_1}{(I_0)_2} \times \frac{\left(e^{0.1/2 \times 0.02569} - 1\right)}{\left(e^{0.1/2 \times 0.03646} - 1\right)}$$

$$= 1.7263 \times \frac{e^{1.9463} - 1}{e^{1.8714} - 1}$$

$$= 1.7263 \times \frac{(7.00272 - 1)}{(3.94086 - 1)}$$

$$= \frac{1.7263 \times 6.0027}{2.94086}$$

$$= 3.52$$

Q. Germanium diode has $I_0 = 3 \text{ nA}$. Calculate the voltage at the rated current will flow through diode at room temperature 27°C . Diode is rated for 1A .

→ Given: $I_0 = 3 \times 10^{-6} \text{ A}$.

$$V_\theta = ?$$

$$T = 273 + 27 = 300 \text{ K}, n = 1.$$

$$I_\theta = 1 \text{ A}.$$

$$\therefore V_T = \frac{300}{11600} = 0.02586.$$

$$I_\theta = I_0 (e^{V_\theta/nV_T} - 1)$$

$$\therefore e^{V_\theta/nV_T} - 1 = \frac{I_\theta}{I_0} = \frac{1}{3 \times 10^{-6}}$$

$$= \frac{10^6}{3}$$

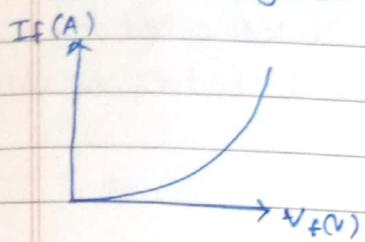
$$\therefore e^{V_\theta/0.02586} = \frac{10^6}{3} + 1.$$

$$\therefore e^{V_\theta/0.02586} = \frac{10^6 + 3}{3} = 333334.33,$$

$$\therefore \frac{V_\theta}{0.02586} = \log_e (333334.33)$$

$$\therefore V_\theta = 0.3288 \text{ V}$$

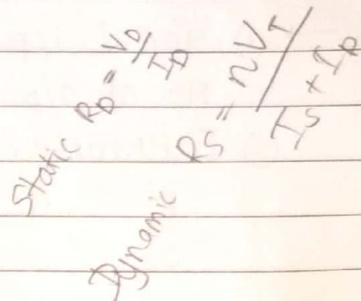
* Static & Dynamic resistance of Diode :-



a) Dynamic R_d

b) Static Resistance.

$$R_s = \frac{V_0}{I_0}$$



Numericals.

1. Obtain static & dynamic resistance of PN junction germanium diode if room temp. is 27°C, $I_0 = 2.5 \text{ nA}$. for applying forward bias voltage $V_f = 0.3 \text{ V}$.

$$\rightarrow R_s = \frac{V_0}{I_0} = \frac{0.3}{2.5 \times 10^{-9}} = 1.2 \times 10^8 \Omega ; V_T = 30$$

$$\begin{aligned} I_{\alpha} &= I_0 (e^{V_f/nV_T} - 1) \\ &= 2.5 \times 10^{-9} (e^{0.3/30} - 1) \\ &= 2.5 \times 10^{-9} \cdot 0.3 \times 10^{-6} \\ &\approx 2.72987 \cdot 10^{-6} \\ &= 0.273 \text{ A} . \end{aligned}$$

$$\therefore R_s = \frac{0.3}{0.273} = 1.0989 \Omega$$

$$\begin{aligned} R_{\alpha} &= \frac{1 \times 0.02586}{0.273 + 2.5 \times 10^{-6}} \\ &= \frac{0.02586}{(273000 + 2.5)} \times 10^6 \\ &= 9.4724 \times 10^{-8} \times 10^6 \\ &= 9.4724 \times 10^{-2} \\ &= 94.724 \times 10^{-3} \Omega \\ &\approx 94.724 \text{ m} \Omega . \end{aligned}$$

$$\begin{aligned} I_{\alpha} &= 2.5 \times 10^{-9} (e^{5.8004} - 1) \\ &= 2.5 \times 329.4317 \times 10^{-9} \\ &\approx 823.579 \times 10^{-9} \\ &= 0.8235 \text{ mA} . \end{aligned}$$

$$R_s = \frac{0.3 \times 10^3}{0.8235} = 364.298 \Omega$$

$$\begin{aligned} R_{\alpha} &= \frac{2 \times 0.02586}{0.8235 \times 10^{-3} + 2.5 \times 10^{-6}} \\ &= \frac{2 \times 0.02586 \times 10^6}{823.579 + 2.5} \\ &= 62.609 \Omega . \end{aligned}$$

Steps for Designing

- 1) Identify no. of I/p's & O/p's.
- 2) Prepare truth-table.
- 3) Obtain reduced Boolean funcn.
- 4) Implement using gates according to required logic (AND/NOT/NAND/NOR).

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Date: _____

Designing

- Q Construct hardware ckt using only NAND gates for
 $y = f(P, Q, R)$ where Y is true (high) if two or more
I/p's of P, Q, R are true (high).

$$\rightarrow \textcircled{1} \text{ No. of I/p's} = 3$$

$$\text{No. of O/p} = 1.$$

② Truthtable.

P	Q	R	Y	
0	0	0	0	Consider minterms
0	0	1	0	with value 1,
0	1	0	0	And then take their ORing.
$P'QR$ ✓	0	1	1	
$PQ'R'$	1	0	0	
$PQ'R$ ✓	1	0	1	
$PQ'R'$ ✓	1	1	0	
PPR ✓	1	1	1	

③ Boolean function.

$$P'QR + PQ'R' + PQR' + PQR. \quad P'QR + PQ'R + PQ(R+R')$$

	$P'QR$	$Q'R'$	$Q'R$	QR	QR'	$P'QR + PQ'R + PQ$
P'	00	01	11	10		
P	1	1	1	1	1	

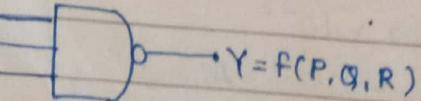
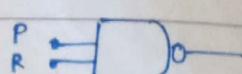
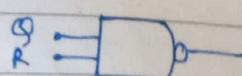
PR.

$$\therefore Y = P'QR + PQ + QR + PR.$$

$$Y' = \overline{PQ + QR + PR}$$

$$(Y')' = Y = \overline{PQ} \cdot \overline{QR} \cdot \overline{PR}$$

④ Implementation



Q. Construct hardware ckt. using AOI gates for $y = f(P, Q, R)$ where Y is true(high) if two/more i/p's of P, Q, R are false(low).

→ ① No. of i/p's = 3

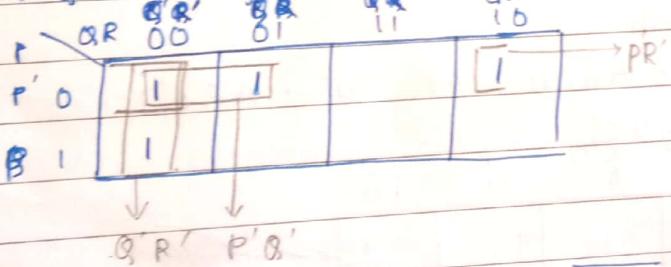
No. of o/p's = 1.

② Truth table.

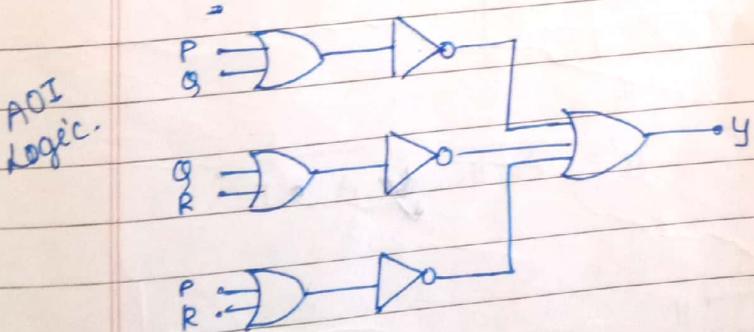
P	Q	R	y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

③ Boolean function.

$$P'Q'R' + P'Q'R + P'QR' + PQ'R'$$



$$y = P'R' + Q'R' + P'Q' = \overline{P+Q} + \overline{Q+R} + \overline{P+R}$$



nor
logic.

✓ 6 16

Q. Design logic ckt. whose o/p is high only when majority of i/p's are high. Consider three i/p logic.

Q. Design logic ckt. to detect a number greater than BCOD 5.

→ ① i/p's → 4 o/p's → 1.

② Truth table.

A	B	C	D	Y.
0	0	0	0	0
1	0	0	1	0
2	0	0	1	0
3	0	0	1	0
4	0	1	0	0
5	0	1	0	0
6	0	1	1	1
7	0	1	1	1
8	1	0	0	1
9	1	0	1	1

③ Boolean Function.

$$y = A'BCD' + A'BCD + AB'C'D' + AB'C'D$$

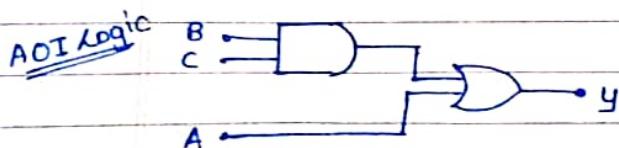
$$= A'BC + AB'C'$$

AB	CD	$\bar{C}D'$	$\bar{C}D$	$\bar{C}\bar{D}'$	$\bar{C}\bar{D}$
A'B' 00					
A'B 01				1	1
AB 10	X	X	X	X	
AB' 11	1	1	X	X	

A ↴

$$y = BC + AC$$

$$y' = \overline{A + BC} \Leftrightarrow \overline{A} \bullet \overline{BC}$$



→ ① i/p = 3, o/p \rightarrow 1.

② Truth table.

A	B	C	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Q. Design logic ckt whose o/p is false (low) only when majority of i/p are low consider there i/p logic.

Q. Design logic ckt whose o/p is false or low only when majority of i/p's are high. Consider A i/p logic

* Designing of Comparator :-

A) 1 bit Comparator.

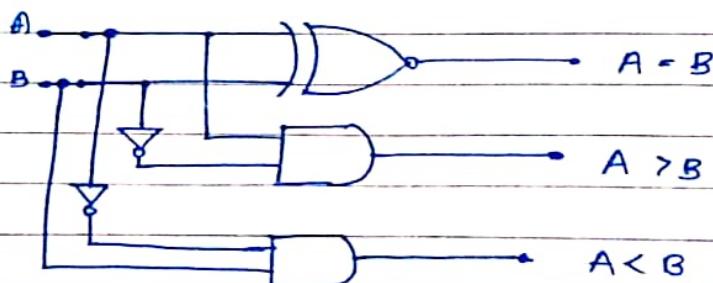
I/P O/P .

A	B	$A = B$	$A > B$	$A < B$
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

$$F(A = B) \equiv A'B' + AB$$

$$F(A > B) = AB'$$

$$F(A < B) = A'B$$



B) 2-Bit Comparator

I/P

	A_1	B_1	A_0	B_0	$A = B$	$A < B$	$A > B$
A_1, A_0	0	0	0	0	1	0	0
	0	0	0	1	0	1	0
B_1, B_0	0	0	1	0	0	0	1
	0	0	1	1	1	0	0
	0	0	0	0	0	1	0
	0	1	0	1	0	1	0
	0	1	1	0	0	1	0
	0	1	1	1	0	1	0
	1	0	0	0	0	0	1
	1	0	0	1	0	0	1
	1	0	1	0	0	0	1
	1	0	1	1	0	0	1
	1	1	0	0	1	0	0
	1	1	0	1	0	1	0
	1	1	1	0	0	0	1
	1	1	1	1	1	0	0

D

Q. Implement hardware for conversion from 4-bit binary code to gray code.

B_4	B_3	B_2	B_1	G_4	G_3	G_2	G_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

$F(G_4) : B_4 \overline{B_3} \overline{B_2}$

$\overline{B_4} B_3$	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$B_4 \overline{B_3}$	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
$B_4 B_3$	0	1	0	1	1	0	1	0	1	1	0	1	0	1	1	0
$\overline{B_4} \overline{B_3}$	1	1	0	0	1	1	0	0	1	1	1	0	1	0	0	1

$$\therefore F(G_4) = \underline{B_4}$$

$F(G_3) : B_3 \overline{B_4} \overline{B_2} \overline{B_1}$

$\overline{B_3} \overline{B_4} 00$	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$\overline{B_3} B_4 01$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$B_3 \overline{B_4} 11$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$B_3 B_4 10$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

$$\begin{aligned} \therefore F(G_3) &= \overline{B_3} B_4 + B_3 \overline{B_4} \\ &= B_3 \oplus B_4 \end{aligned}$$

$F(G_2)$	$B_2 B_1$	$B_1' B_2$	$B_1 B_2$	$B_1 B_2$	$B_1' B_2'$
	$B_4 B_3$	00	01	11	10
	$B_3 B_4$ 00	0	1	1	1
	$B_3 B_4$ 01	1	1	0	0
	$B_3 B_4$ 11	1	1	1	1
	$B_3 B_4$ 10	0	0	1	1

$$F(G_2) = B_2 \bar{B}_3 + \bar{B}_2 B_3 \\ = B_2 \oplus B_3$$

F
B

$F(G_1)$	$B_2 B_1$	00	01	11	10
	$B_4 B_3$	00	01	11	10
	00	1			1
	01	1	1		
	11		1	1	1
	10		1		

$$F(G_1) = B_2 \bar{B}_1 + \bar{B}_2 B_1 \\ = B_2 \oplus B_1$$

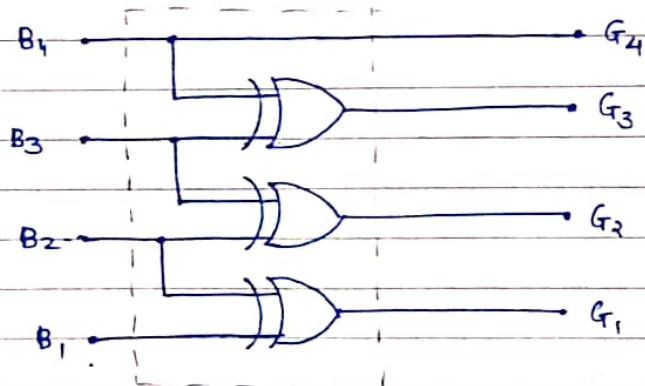
Thus, $F(G_4) = B_4$

$$F(G_3) = B_4 \oplus B_3$$

$$F(G_2) = B_3 \oplus B_2$$

$$F(G_1) = B_2 \oplus B_1$$

Logic Diagram :-



Q. Grey to Binary.

	<u>Grey</u>	<u>Binary</u>
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 1	0 0 1 0
3	0 0 1 0	0 0 1 1
4	0 1 1 0	0 0 0 0
5	0 1 1 1	0 1 0 1
6	0 1 0 1	0 1 1 0
7	0 1 0 0	0 1 1 1
8	1 1 0 0	1 0 0 0
9	1 1 0 1	1 0 0 1
10	1 1 1 1	1 0 1 0
11	1 0 1 1	1 0 1 1
12	1 0 1 0	1 0 0 0
13	1 0 0 1	1 0 0 1
14	1 0 0 0	1 0 1 0
15	1 1 1 0	1 0 1 1
16	1 1 0 0	1 1 0 0
17	1 0 1 0	1 1 0 1
18	1 0 0 1	1 1 1 0
19	1 0 0 0	1 1 1 1

	<u>Grey</u>	<u>Binary</u>						
	G_3	G_2	G_1	G_0	B_4	B_3	B_2	B_1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	0	1	1	0
6	0	1	1	0	0	1	1	1
7	0	1	1	1	0	1	1	0
8	1	0	0	0	0	1	1	1
9	1	0	0	1	0	1	1	0
10	1	0	1	0	0	1	0	0
11	1	0	1	1	1	1	0	1
12	1	1	0	0	0	1	0	0
13	1	1	0	1	0	1	0	0
14	1	1	1	0	0	1	0	1
15	1	1	1	1	1	1	1	0
16	1	0	0	0	1	1	1	1
17	1	0	0	1	1	1	1	0
18	1	0	1	0	1	1	0	0
19	1	0	1	1	1	1	0	1
20	1	1	0	0	1	0	0	0
21	1	1	0	1	1	0	0	1
22	1	1	1	0	1	0	1	1
23	1	1	1	1	0	1	0	0

$F(B_4)$	$G_4 G_3$	00	01	11	10	
00		0		3	2	
01		4	5	7	6	$\rightarrow G_4$
11	1	1	13	15	14	
10	1	1	14	1	10	

$$F(B_4) = G_4$$

$F(B_3)$	$G_2 G_1$	00	01	11	10	
00						
01	1	1	1	1	1	$\rightarrow \overline{G}_4 G_3$
11						
10	1	1	1	1	1	$\rightarrow G_4 \overline{G}_3$

$$\begin{aligned} F(B_3) &= \overline{G}_4 G_3 + G_4 \overline{G}_3 \\ &= G_4 \oplus G_3 \end{aligned}$$

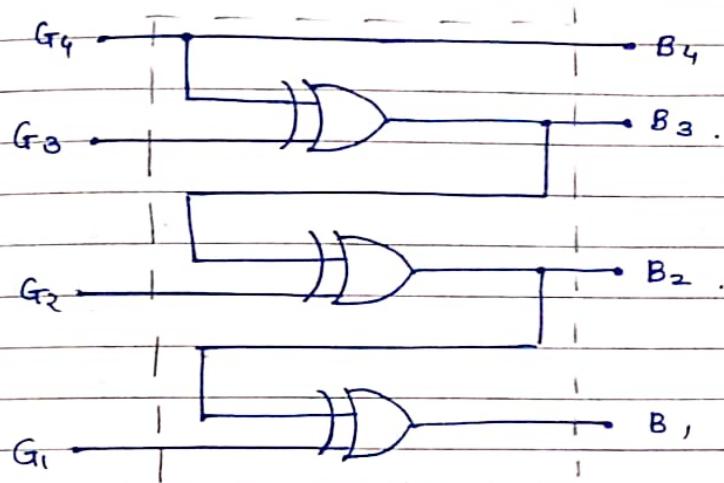
$F(B_2)$	$G_2 G_1$	00	01	11	10	
00				1	1	$\rightarrow G_2 \overline{G}_4 \overline{G}_3$
01	1	1				$\rightarrow \overline{G}_2 \overline{G}_4 G_3$
11				1	1	$\rightarrow G_2 G_4 G_3$
10	1	1				$\rightarrow \overline{G}_2 G_4 \overline{G}_3$

$$\begin{aligned} F(B_2) &= \overline{G}_2 (\overline{G}_4 G_3 + G_4 \overline{G}_3) \\ &\quad + G_2 (G_4 G_3 + \overline{G}_4 \overline{G}_3) \\ &= \overline{G}_2 (G_4 \oplus G_3) \\ &\quad + G_2 (\overline{G}_4 \oplus \overline{G}_3) \\ &= G_2 \oplus G_3 \oplus G_4 \\ &= G_2 \oplus B_3 \end{aligned}$$

$F(B_1)$	$G_2 G_1$	00	01	11	10	
00			1			
01	1			1		
11		1			1	
10	1			1		

$$\begin{aligned} F(B_1) &= \overline{G}_2 G_1 \overline{G}_4 \overline{G}_3 + G_2 \overline{G}_1 \overline{G}_4 G_3 + \overline{G}_2 \overline{G}_1 \overline{G}_4 G_3 + G_2 G_1 \overline{G}_4 G_3 \\ &\quad + \overline{G}_2 G_1 G_4 G_3 + G_2 \overline{G}_1 G_4 G_3 + \overline{G}_2 \overline{G}_1 G_4 \overline{G}_3 + G_2 G_1 \overline{G}_4 \overline{G}_3 \\ &= \overline{G}_4 \overline{G}_3 (\overline{G}_2 G_1 + G_2 \overline{G}_1) + G_4 G_3 (\overline{G}_2 G_1 + G_2 \overline{G}_1) \\ &\quad + \overline{G}_4 G_3 (\overline{G}_2 \overline{G}_1 + G_2 G_1) + G_4 \overline{G}_3 (\overline{G}_2 \overline{G}_1 + G_2 G_1) \\ &= \overline{G}_4 \overline{G}_3 (G_2 \oplus G_1) + G_4 G_3 (G_2 \oplus G_1) \\ &\quad + \overline{G}_4 G_3 (G_2 \oplus G_1) + G_4 \overline{G}_3 (\overline{G}_2 \oplus G_1) \\ &= (G_2 \oplus G_1) \cdot (\overline{G}_4 \oplus G_3) + (G_2 \oplus G_1) (G_4 \oplus G_3) \\ &= G_1 \oplus \underline{G_2 \oplus G_3 \oplus G_4} \\ &= B_2 \oplus G_1 \end{aligned}$$

Logic Diagram :



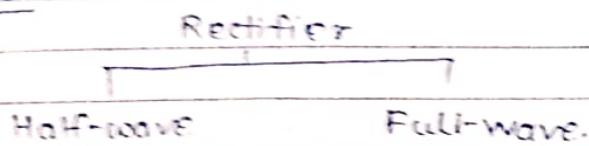
Q. Implement hardware for BCD to XS-3 code.

BCD				XS-3.			
P	Q	R	S	A	B	C	D
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

F(A)		QBRS			
		GG	01	11	10
0	0	0	.	.	.
0	1	1	1	1	1
1	1	X	X	X	X
1	0	1	1	X	X

$$\begin{aligned}
 f(A) &= P + QR + QS \\
 &= P + Q(R+S)
 \end{aligned}$$

Rectifier



Q. An AC supply of 250V apply through a transformer of turns ratio 10:1. Assuming the diode resistance of 10Ω and the load as 500Ω . Calculate.

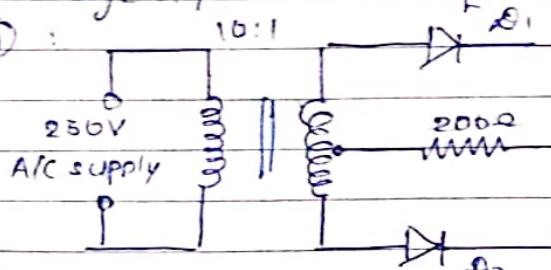
- 1) I_{m}, I_{dc}, I_{rms} 5) D.C. o/p voltage.
- 2) a.c. power o/p. 6) PIV
- 3) AC power i/p. 7) Frequency of D.C. o/p voltage
- 4) Efficiency of rectification.

Q. C.T. rectifier uses 2 diodes each of 20Ω .

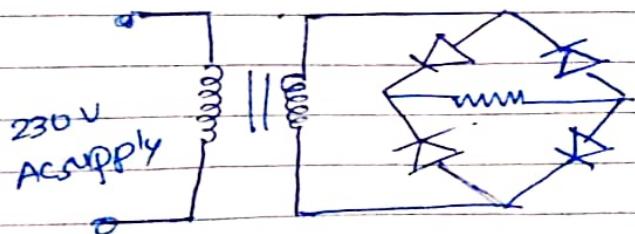
The transformer 2^o voltage from centre to each end of secondary is 100V. Assume load resistance as 500Ω . Find i) I_{dc} ii) I_{rms}

Q. Fig A & B shows C.T & Bridge R.C.s having same load & transformer turns ratio. The primary of each is connected to 230 V, 50 Hz supply. Find in each case
1) D.C. voltage o/p. 2) Frequency of DC o/p.

Fig(A) :



Fig(B) :



→ D.C. o/p voltage is double in bridge ckt than in C.T ckt.

→ O/P freq. of D.C. voltage will be double than that of the A.C. voltage

Rectifiers

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Rectifier

Conversion of AC to DC is called "Rectification".

When diode is in forward biased condition, it acts as short circuit and current flows from anode to cathode. When diode is in reverse biased condition, it acts as an open circuit & there will be no current through diode. These properties of diodes are used in rectification.

Classification

Rectifiers

Halfwave Rectifier

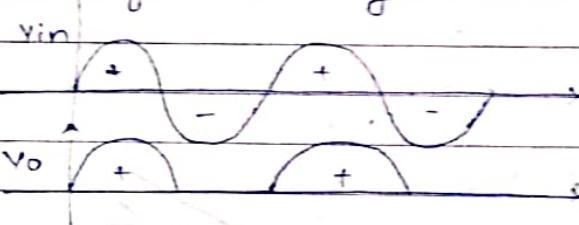
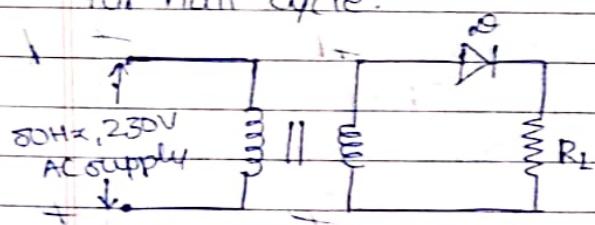
Fullwave rectifier

Centre Tap
rectifier

Bridge wave
rectifier

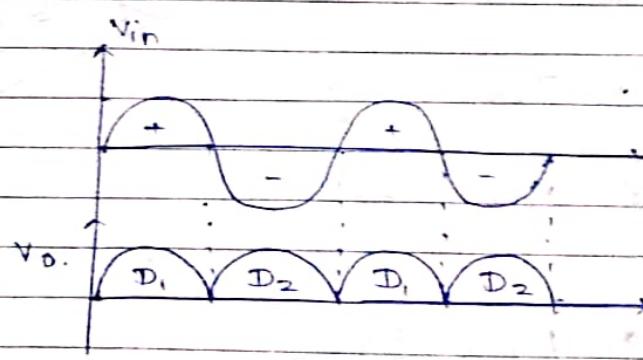
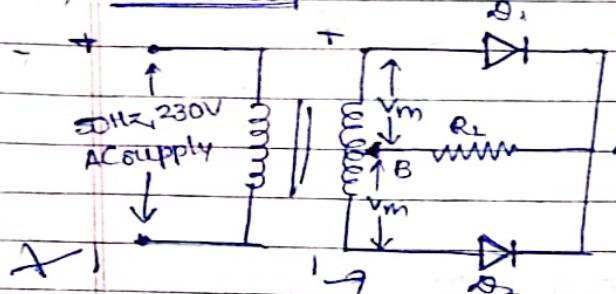
A) HALF-WAVE RECTIFIER :-

In half-wave rectifier, the current flows through the diode only for half cycle.

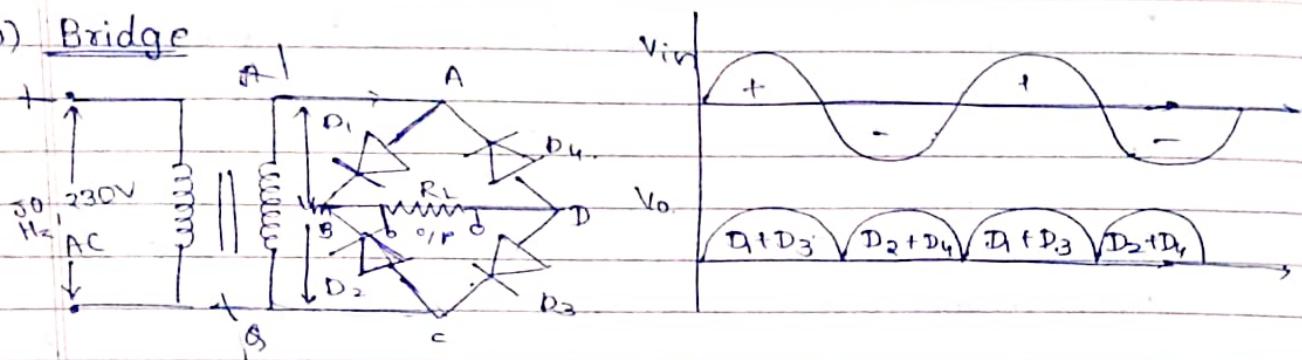


B) FULL-WAVE RECTIFIER :-

a) Centre-tap :-



b) Bridge



- * Ripple : AC component in DC o/p of the rectifier is called 'ripple'.
- * Ripple factor : Ratio of RMS value of AC component to the DC component in rectifier o/p.

$$R.F. = \frac{\text{RMS value of AC component}}{\text{DC component}} = \frac{I_{AC}}{I_{DC}}$$
- * Rectification efficiency : ratio of DC o/p power to AC i/p power

$$\eta = \frac{\text{DC O/P power}}{\text{AC I/P power}} = \frac{P_{DC}}{P_{AC}}$$

→ From knowledge of electrical engineering.

[HWR]

$$\textcircled{1} \quad V_{rms} = \frac{V_m}{2}$$

$$\textcircled{2} \quad V_{DC} = \frac{V_m}{\pi}$$

$$\textcircled{3} \quad I_{rms} = \frac{I_m}{2}$$

$$\textcircled{4} \quad I_{AV} = I_{DC} = \frac{I_m}{\pi}$$

[FWR]

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$V_{DC} = \frac{2V_m}{\pi}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$I_{AV} = I_{DC} = \frac{2I_m}{\pi}$$

→ Ripple Factor :-

$$R.F. = \frac{\text{rms value of AC component}}{\text{DC component}}$$

$$\therefore R.F. = \frac{I_{AC}}{I_{DC}} \quad \textcircled{1}$$

By defn.

rms value of total current is given by

$$I_{rms}^2 = I_{DC}^2 + I_{AC}^2$$

$$\therefore I_{AC} = \sqrt{I_{rms}^2 - I_{DC}^2} \quad \text{--- (2)}$$

From (1) & (2),

$$R.F. = \sqrt{I_{rms}^2 - I_{DC}^2}$$

$$= \frac{I_{DC}}{\sqrt{I_{rms}^2 - I_{DC}^2}}$$

$$R.F. = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} \quad \text{--- (3)}$$

- For Half-wave rectifier,

$$I_{rms} = \frac{I_m}{2}, \quad I_{DC} = \frac{I_m}{\pi}$$

$$\therefore R.F. = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

$$\therefore R.F. = 1.21$$

For Half wave rectifier, the ripple factor is 1.21. This indicates that value of AC component is greater than DC component in HWR. \therefore It is a poor rectifier.

- For full-wave rectifier,

$$I_{rms} = \frac{I_m}{\sqrt{2}}, \quad I_{DC} = \frac{2I_m}{\pi}$$

$$\therefore R.F. = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$\therefore R.F. = \sqrt{\frac{\pi^2}{8} - 1}$$

$$\therefore R.F. = 0.48$$

For Fullwave rectifier, the ripple factor is 0.48. This indicates that value of AC component is less than DC component in FWR. \therefore It is a good rectifier.

→ Rectification Efficiency

$$\eta = \frac{P_{DC}}{P_{AC}}$$

$$= \frac{I_{DC}^2 \times R_L}{I_{rms}^2 \times (r_f + R_L)}$$

$$= \frac{I_{DC}^2 \times R_L}{I_{rms}^2 \times (r_f + R_L)}$$

$$P_{DC} = I_{DC}^2 \times R_L$$

$$P_{AC} = I_{rms}^2 \times (R_L + r_f)$$

r_f = forward resist.

R_L = load resist.

- For HWR,

$$\eta = \left(\frac{4}{\pi^2} \right) \frac{R_L}{r_f + R_L}$$

$$= 0.406 \times \frac{R_L}{r_f + R_L}$$

$$I_{DC} = \frac{I_m}{\pi}$$

$$I_{rms} = \frac{I_m}{2}$$

We can neglect r_f in comparison to R_L .

$$\therefore \eta = 40.6\%$$

- For FWR,

$$\eta = \left(\frac{8}{\pi^2} \right) \frac{R_L}{r_f + R_L} = \left(\frac{8}{\pi^2} \right) \frac{R_L}{r_f + R_L}$$

$$\therefore \eta = 81.2\%$$

→ Comparison betw all rectifiers.

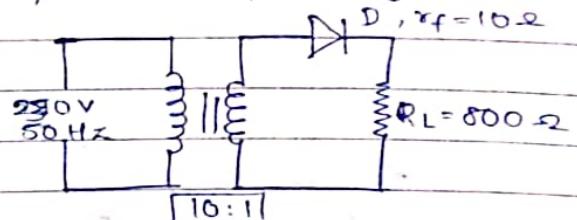
Parameter	Half-wave Red	Centre-tapped full wave	Bridge FWR
① No. of diodes	1	2	4
② Centre-tap	No	Yes	No
③ Rectification Efficiency	$\eta = 40.6\%$	$\eta = 81.2\%$	$\eta = 81.2\%$
④ Ripple factor	$R.F. = 1.21$	0.4834	0.4834
⑤ O/p frequency	f_m	$2f_m$	$2f_m$
⑥ PIV	v_m	$2v_m$	$4v_m$
⑦ Nature of o/p	$h.n$	$h.m$	$h.m$
⑧ Rectification	Only one cycle is rectified	Both cycles are rectified	Both cycles are rectified

Numericals

- 1) An AC supply of 230 V is applied to a half wave rectifier, to a transformer of ratio 10:1. Assuming diode resistance as 1Ω & the load as $800\ \Omega$. Calculate (a) I_m , I_{av} , I_{rms} (b) DC power o/p (c) AC power i/p. (d) Rectification efficiency (e) DC o/p voltage (f) PIV (g) Freq. of DC o/p voltage.

→ (a) RMS value of 2^o voltage,

$$V_2 = \frac{N_2}{N_1} \times V_1 = \frac{1}{10} \times 230 = 23\text{ V.}$$



$$V_m = \sqrt{2} V_2 = \sqrt{2} \times 23 = 32.52\text{ V.}$$

$$I_m = \frac{V_m}{r_f + R_L} = \frac{32.52}{10 + 800} = 0.04016\text{ A} = \underline{\underline{40.16\text{ mA}}}$$

$$I_{av} = I_{av} = \frac{I_m}{\pi} = \frac{40.16}{\pi} = \underline{\underline{12.78\text{ mA}}}$$

$$I_{rms} = \frac{I_m}{2} = \underline{\underline{20.08\text{ mA}}}$$

(b) DC power o/p

$$P_{DC} = I_{DC}^2 \times R_L = (12.78)^2 \times 10^{-6} \times 800 = \underline{\underline{130\text{ mW}}}$$

(c) AC power i/p.

$$P_{AC} = I^2 R_{rms} (R_L + r_f) = (20.08)^2 \times 10^{-6} \times 810 = \underline{\underline{326.59\text{ mW}}}$$

(d) Rectification efficiency.

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{130 \times 10^{-3}}{326.59 \times 10^{-3}} = 39.87\%$$

(e) DC o/p voltage, $V_{DC} = I_{DC} \times R_L = 12.78 \times 10^{-3} \times 800 = \underline{\underline{10.224\text{ V}}}$

(f) PIV = $V_m = \underline{\underline{32.52\text{ V}}}$

(g) Freq. of DC o/p voltage = 50 Hz

∴ In HWR, there is only one o/p for each complete cycle of the i/p AC voltage. Therefore, frequency of DC o/p is same as AC i/p ie. 50 Hz

- 2) A centre tap rectifier uses 2 diodes each of resistance 2Ω . The transformer 2^o voltage from centre to each end of secondary is 100V. Assume load resistance as $800\ \Omega$. Find I_{DC} & I_{rms} .

→ $r_f = 2\Omega$, $R_L = 800\ \Omega$, $V = 100\text{ V}$.

$$\therefore V_m = \sqrt{2} V = 141.42\text{ V}$$

$$I_m = \frac{V_m}{R_L + R_s} = \frac{141.42}{820} = 172.4 \text{ mA}$$

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2 \times 172.4}{\pi} = 109.75 \text{ mA}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = 121.30 \text{ mA}$$

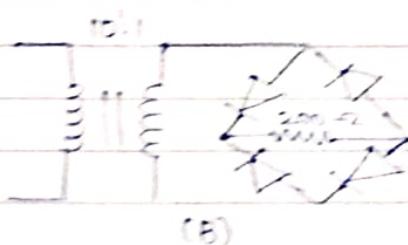
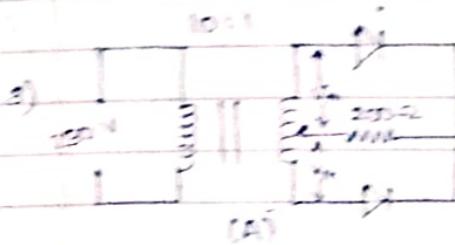
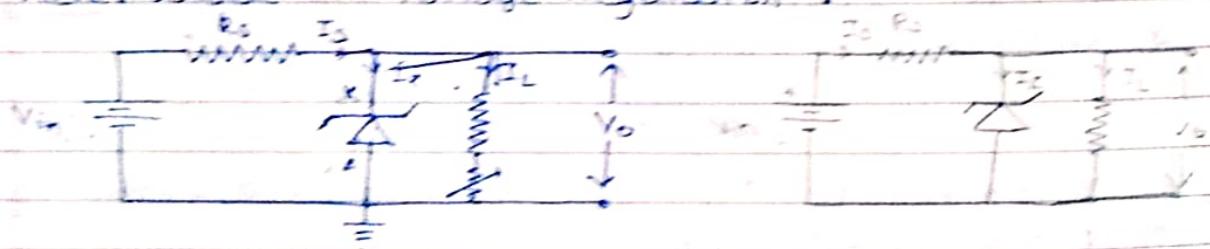


Fig (A) & (B) show centre tap & bridge rectifier having same load and transformer or turn ratio. The 1st coil of each is connected to 230 V. AC supply find in each case.

(a) DC voltage o/p. (b) freq. of DC voltage o/p.

(a) Ideal Diode (b) Practical Diode - 10.2

* Zener Diode \rightarrow Voltage Regulation :-



(A) Line Regulation

~~upto breakdown~~ Load constant, vary i/p supply
voltage, voltage By KVL, $I_o = I_Z + I_L$ [Zener must be in breakdown region]

~~upto breakdown~~ $V_o = I_o R_L + V_Z$

After breakdown $V_o = V_{in} - I_o R_s$

constant voltage. $V_{in} \uparrow$, $I_o \downarrow \Rightarrow I_o R_s \uparrow \Rightarrow V_o \text{ constant}$

$V_{in} \downarrow$, $I_o \downarrow \Rightarrow I_o R_s \downarrow \Rightarrow V_o \text{ constant}$
(upto breakdown)

Comparison → Avalanche Breakdown
Zener Breakdown.

$$V_{IN} = V_o + V_z$$

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b) Load Regulation.

Constant I/p voltage, load current vary.

$$V_{IN} \geq V_z$$

$$I_O = I_Z + I_L$$

$$V_o = \frac{V_{IN} - I_O R_S}{I_O \text{ constant}}$$

$$V_o = V_{IN} - (I_Z + I_L) R_S$$

$$I_L \uparrow \Rightarrow I_Z \downarrow$$

$$I_L \downarrow \Rightarrow I_Z \uparrow$$

$$\frac{V_o}{I_O}, \frac{V_o}{I_L}$$

$$V_{IN} = I_O R_S + V_o$$

$$I_O R_S = V_{IN} - V_o$$

$$R_S = \frac{V_{IN} - V_o}{I_O}$$

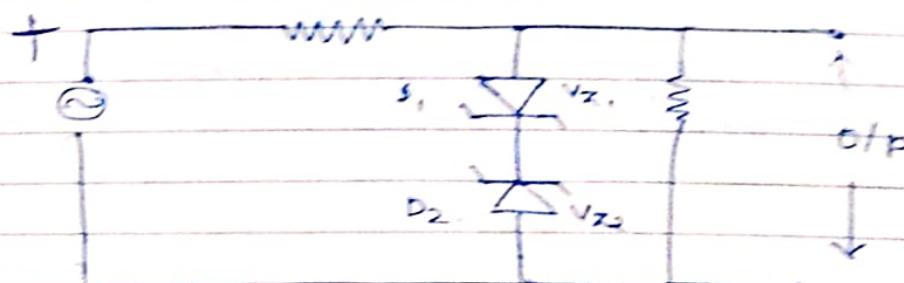
$$R_S = \frac{V_{IN} - V_o}{I_Z + I_L}$$

→ min load current.

$$\% \text{ Regulation} = \frac{V_{IN, \text{load}} - V_{IN, \text{no load}}}{V_{IN, \text{no load}}} \rightarrow \text{no load current.}$$

Numericals :-

→ Zener Diode as Clipper



+ve halfcycle, D_2 in breakdown \rightarrow o/p $\rightarrow V_{Z2}$

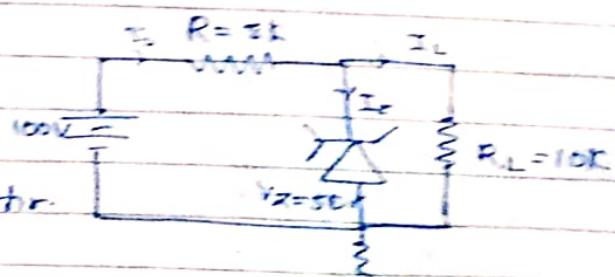
-ve halfcycle, D_1 in reverse i.e. breakdown \rightarrow o/p $\rightarrow V_{Z1}$

Numericals :

i) Fig shows a zener diode in

ckt. calculate i) o/p voltage

ii) Drop against R iii) Current thr. $V_z = 50V$



$V_o = 50V$ $\because V_{IN} > V_o \rightarrow$ constant o/p i.e. zener voltage

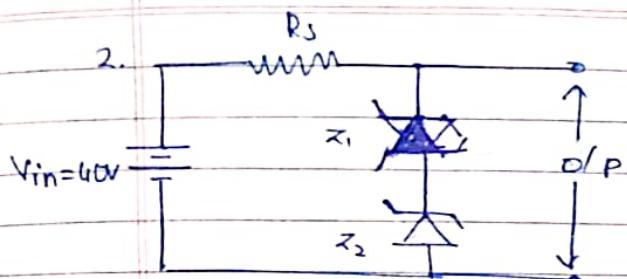
$$I_O R_S = V_{IN} - V_o \Rightarrow I_O R_S = 50$$

$$\therefore I_S = \frac{50}{10000} = 0.01A = 10 \times 10^{-3}$$

$$I_L = \frac{50}{10000} = 5 \times 10^{-3}$$

$$\therefore I_Z = I_S - I_L = (10 - 5) \times 10^{-3} = \underline{\underline{5mA}}$$

$$\frac{V_{in}}{R_s} = \frac{V_{z_1} + V_{z_2}}{V_{in}}$$



What value of R_s is req. when
12 ~~V~~ 12V - 1000 mA Zeners
are connected in series to obtain
a 24 V Regulated DC power supply
from a 40 V unregulated DC source

→ We shall consider 1st case, at no load when zener's will carry max. current.

Suppose resistance R will be required to be connected in series with arrangement.

Data: $V_{in} = 40V$ $V_{z_1} = 12V$ $V_{z_2} = 12V$

$V_o = 24V$ $I_z = 1A$

$$I_s R_s = V_{in} - V_o = 40 - 24 = 16V$$

$$\therefore I_s = I_z = 1A \quad (\text{No load cond'n})$$

$$\therefore R_s = \frac{16}{I_s} = 16\Omega$$

Q. Encode decimal by means of weighted codes 3321, 4221, 731-2, 631-1,
5311, 74-2-1 & 7421.

→ 74-2-1

0 0 0 0 0

1 0 1 1 1

2 0 1 1 0

3 0 1 0 1

4 0 1 0 0

5 1 0 1 0

6 1 0 0 1

7 1 0 0 0

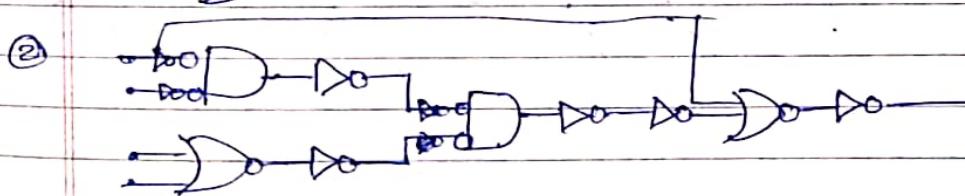
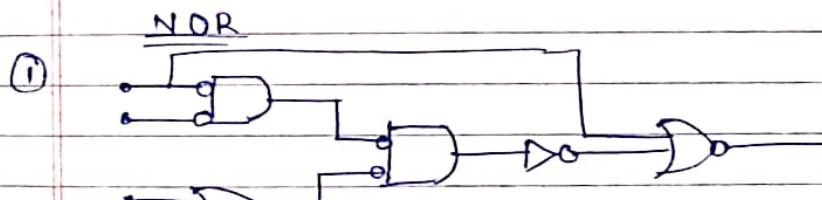
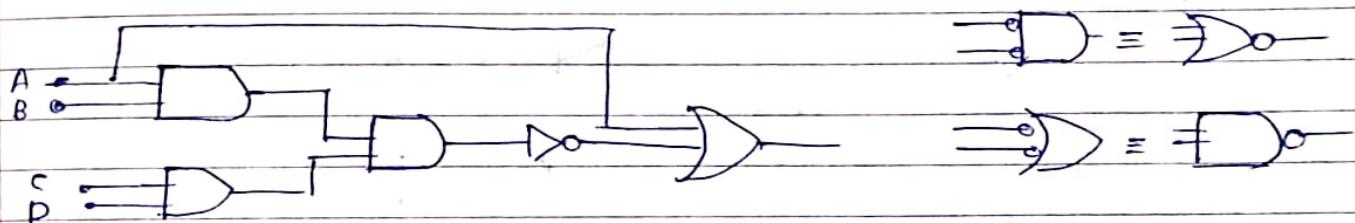
8 1 1 1 1

9 1 1 1 0

* Signed Binary Number -

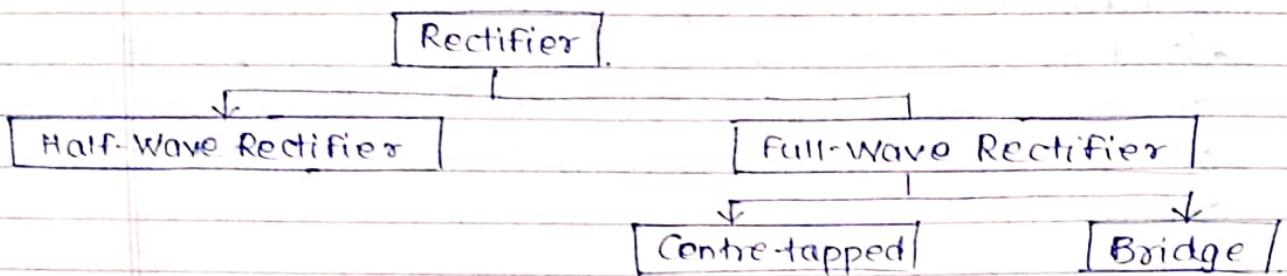
- * Converting AOI logic into NAND & NOR.
- ① Draw ckt. in AOI logic. If NAND hardware is chosen, add a circle at the o/p of each 'and' gate & at the i/p/s to all the OR gates. (•) If NOR hardware is chosen add a circle at o/p of each OR gate & at i/p/s of each AND gates.
- (•) Add or subtract an inverter for each line that is received a circle in steps two or three so that the polarity of signals on those lines remains unchanged from that of the original diagram.

① Convert following AOI Logic to a)NAND b) NOR

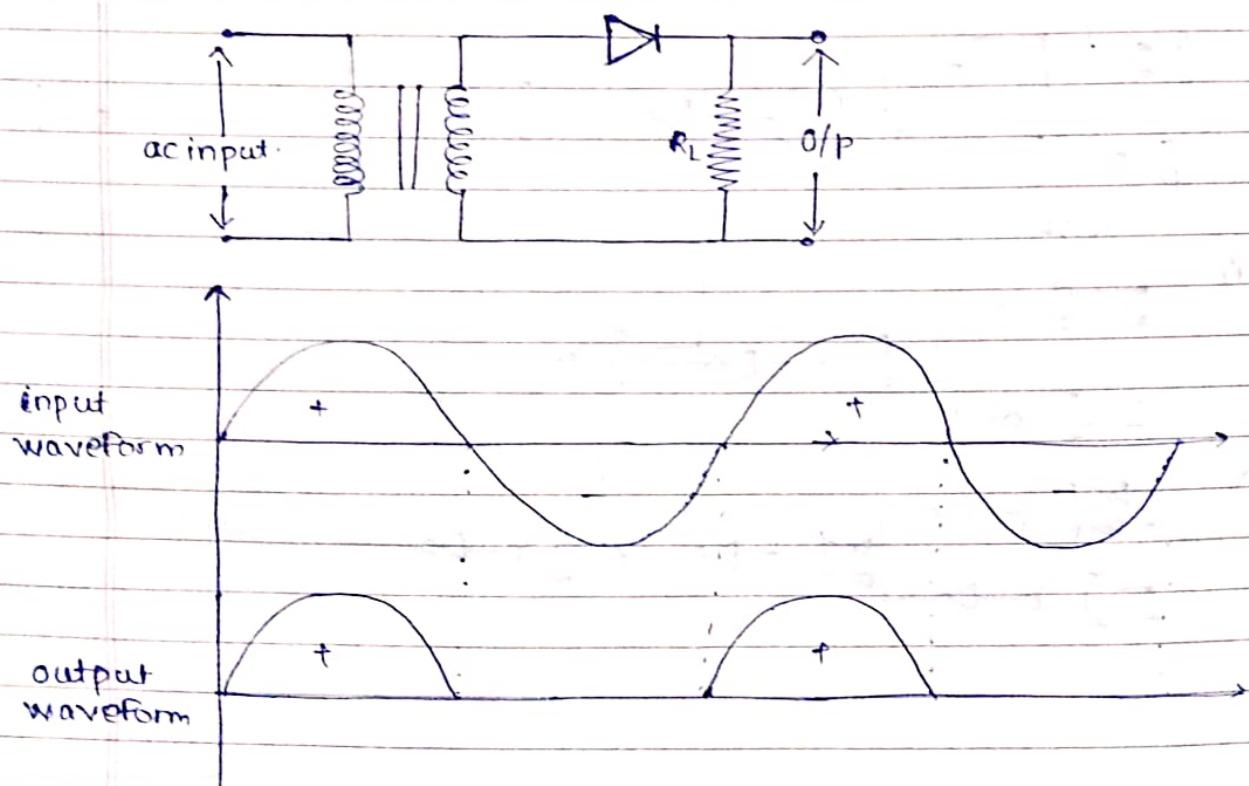


A) Rectifier Circuits :-

Because of their ability to conduct current in one direction & block current in other direction, diodes are used in circuits called "rectifiers" that convert ac voltage into dc voltage.



① Half-Wave Rectifier :-



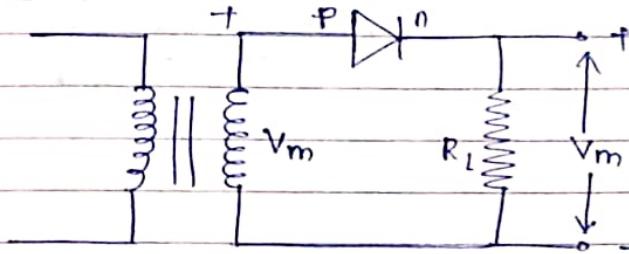
Circuit : The circuit of HWR comprises of a single diode connect in series with secondary of transformer & a load resistor R_L .

Working : a) During positive half cycle

The diode is forward biased & acts as a closed switch.

It conducts current through the load resistor R_L . As a result,

we get output voltage same as the input voltage.



b) During negative half cycle.

The diode is reverse biased & acts as an open switch. As a result, no current flows through resistor R_L and hence, output voltage is zero.

Thus, the diode conducts only during positive half cycle & it rectifies the negative half cycle. Hence, HWR.

Important Parameters :-

i) Average Load Voltage & Load Current

$$V_{DC} = \frac{V_m}{\pi}$$

$$I_{DC} = \frac{I_m}{\pi}$$

ii) RMS Value

$$V_{RMS} = \frac{V_m}{2}$$

$$I_{RMS} = \frac{I_m}{2}$$

iii) Ripple factor

R.F. = RMS value of AC components in output
AC/Avg value of output.

$$= \sqrt{(V_{RMS}^2 - V_{DC}^2) / 2}$$

$$= \sqrt{\frac{V_{RMS}^2 - 1}{V_{DC}^2}} = \sqrt{\frac{\pi^2 - 1}{4}} = 1.21$$

$$\therefore RF = 1.21$$

$$v) \frac{V_{DC}}{V_{AC}} = \frac{I_{DC}^2}{I_{RMS}^2} + \frac{C}{L}$$

$$P_{DC} = \left(\frac{I_m}{\pi}\right)^2 R_L$$

iv) DC O/P Power

$$P_{DC} = I_{DC}^2 \times R_L$$

$$= \left(\frac{I_m}{\pi}\right)^2 R_L$$

v) Rectification Efficiency

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 \times R_L}{I_{RMS}^2 \times (R_F + R_L)}$$

$$= \frac{4}{\pi^2} \times \frac{R_L}{R_F + R_L}$$

$\because R_F \ll R_L$, we neglect it.

$$\therefore \eta = \frac{4}{\pi^2} \times 0.6 \times 10^{-2}$$

$$\therefore \boxed{\eta = 40.6\%}$$

vi) Peak Inverse Voltage (PIV)

\hookrightarrow maximum negative voltage which appears across nonconducting reverse biased diode.

$$\boxed{PIV = V_m}$$

② Full-Wave Rectifier

$$i) \boxed{V_{DC} = \frac{V_m}{\pi}}$$

$$I_{DC} = \frac{2I_m}{\pi L}$$

$$ii) \boxed{V_{RMS} = \frac{V_m}{\sqrt{2}}}$$

$$I_{RMS} = \frac{I_m}{\sqrt{2}}$$

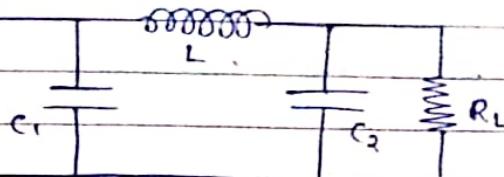
$$iii) \boxed{P_{DC} = I_{DC}^2 R_L}$$

$$v) \boxed{\eta = 81.2\%}$$

$$iv) \boxed{P_{AC} = I_{RMS}^2 R_L}$$

$$v) \boxed{PIV = 2V_m}$$

1) Capacitor-input Filter = π (Pi) Filter :-



Construction : A typical π filter consists of → Filter or reservoir capacitor C_1 connected across rectifier output
→ An inductor L in series
→ Another filter or smoothing capacitor C_2 across load R_L

Operation : The filter functions in 3 steps :

- ① The capacitor C_1 offers low reactance to AC component of the rectifier output while it offers infinite resistance to DC component. As a result, the capacitor shunts an appreciable amount of the AC component while the DC component continues its journey to the inductor L .
- ② The inductor L offers a high reactance to the AC component but it offers almost zero resistance to DC component. As a result, the DC component flows through the inductor while the AC component is blocked.
- ③ The capacitor C_2 shunts the AC component which the inductor had failed to block. As a result, only DC component appears across the load R_L .

Advantages : More output voltage
Ripple-free output.

Disadvantages : Large size

Heavy

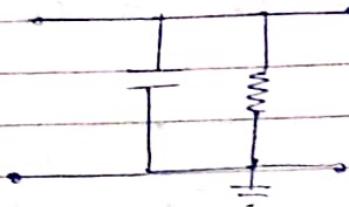
High cost.

* The ripple factor 'r' is an indication of the effectiveness of filter.

$$r = \frac{V_{r(PP)}}{V_{DC}} \rightarrow V_{r(PP)} \text{ ... peak-to-peak ripple voltage.}$$

2) Capacitor Filter

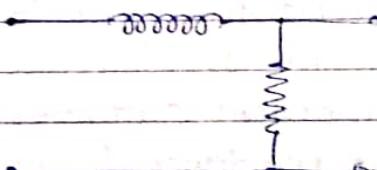
$$\frac{1}{j\omega C}$$



$$\text{Capacitive reactance } X_C = \frac{1}{2\pi f C}$$

- C acts as open ckt. for DC component
- provides low impedance path for AC components of the current.
- DC passes only through load & produces DC o/p voltage.
- AC bypasses to ground.

3) Inductor filter



$$\text{Inductive reactance } X_L = 2\pi f L$$

- consist of choke coil in series.
- offers high impedance to AC components.
- & small resistance to DC components.

VOLTAGE REGULATION

Zener Diode As Voltage Regulator :-

Voltage Doubler

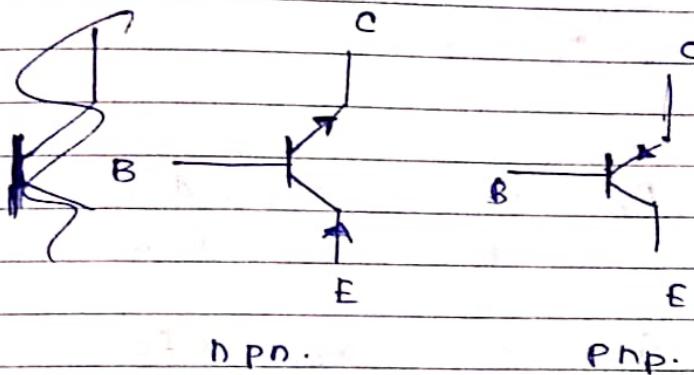
Transistor

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The bipolar junction ~~double~~ transistor is a three terminal 2 junction device.

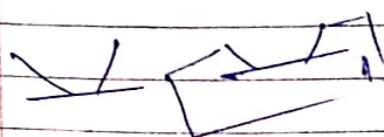
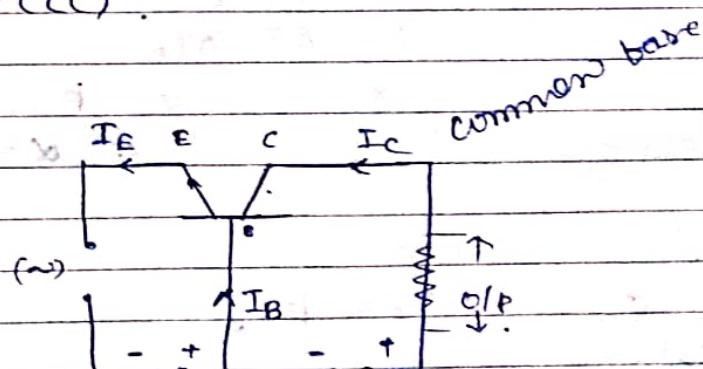
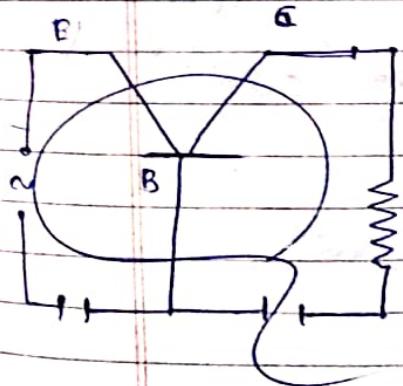
Emitter	Thickness	Doping
Base	Med	Heavy.
Collector	Thin	Light
	Large	Moderate .



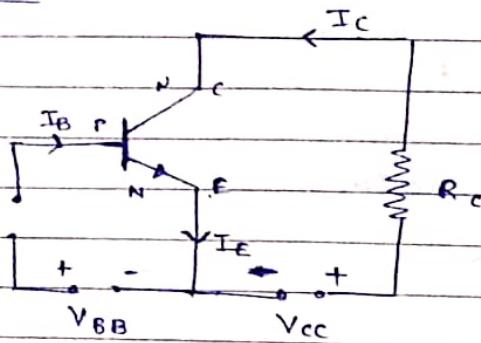
$$I_E = I_C + I_B$$

Three configurations.

- ① Common Base (CB)
- ② Common Emitter (CE)
- ③ Common Collector (CC).



Common Emitter



$$\Phi_{DC} = \frac{I_C}{I_B}$$

$$\beta_{DC} = \frac{I_C}{I_B}$$

$$\beta_{AC} = \frac{\Delta I_C}{\Delta I_B}$$

$$\alpha_{DC} = \frac{I_C}{I_E}$$

$$\alpha_{AC} = \frac{\Delta I_C}{\Delta I_E}$$

$$\beta = \frac{I_C}{I_E}$$

$$\Delta I_B$$

$$= \frac{\Delta I_C}{\Delta I_E - \Delta I_C}$$

$$= \frac{\Delta I_C}{\Delta I_E}$$

$$1 - \frac{\Delta I_C}{\Delta I_E}$$

$$\beta =$$

$$\frac{\alpha}{1-\alpha}$$

$$\Rightarrow \beta(1-\alpha) = \alpha$$

$$\therefore \alpha = \beta$$

$$1 + \beta$$

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = I_B + I_C$$

$$I_B R_B + V_{BE} + I_E R_E = V_{CC}$$

$$I_B R_B = \frac{V_{CC} - I_E R_E + I_B}{I_B + I_C}$$

$$V_{CC} = I_B R_B + I_C R_C$$

$$I_C = \beta I_B + I_{CEO}$$

$$I_B = \frac{V_{CC}}{R_B + \beta R_C}$$

$$= \frac{V_{CC}}{R_B + \frac{I_C R_C}{I_B}}$$

$$I_B = \frac{V_{CC}}{R_B I_B + I_C R_C}$$

Half Adder.

Page No. _____

Date: ___ / ___ / ___

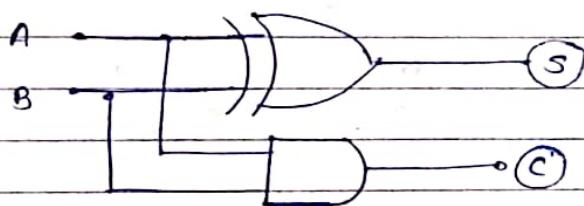
I/P		O/P	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

For S,

A	B	B'	B''
A'	0	1	
A	1	0	
			AB'

$$\rightarrow A'B \rightarrow S = A'B + AB' \\ = X - OR \\ S = A \oplus B$$

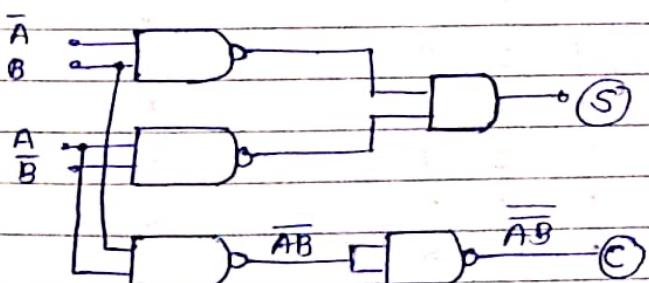
$$C = AB$$



NAND Logic.

$$S = A'B + AB' \Rightarrow S' = \overline{A}\overline{B} \cdot \overline{A}\overline{B} \Rightarrow S = (S')' = \overline{\overline{A}\overline{B} \cdot \overline{A}\overline{B}}$$

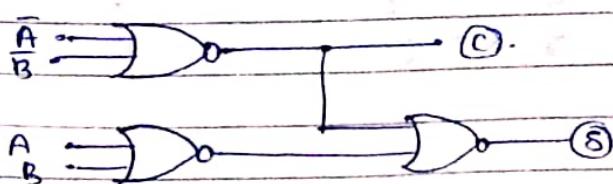
$$C = \overline{AB}$$



$$\text{NOR}$$

$$S = (A'+B') \cdot (A+B) \\ = \overline{A'+B'} + \overline{A+B}$$

$$C = \overline{A} + \overline{B}$$



FULL ADDER

① IIP OIP

A	B	G	S	C ₁
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

For S,

A	BC	BC'	B'C	BC'	BC'
A'0	00	1	1	1	1
A'1	11	1	1	1	1

$$\begin{aligned}
 S &= AB'C' + ABC + A'B'C + A'BC' \\
 &= C'(AB' + A'B) + C(AB + A'B') \\
 &= C'(X-OR) + C(\overline{X}-OR) \\
 &= C \oplus A \oplus B
 \end{aligned}$$

For C,

BCD → Grey

B ₄	B ₃	B ₂	B ₁
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Grey:

G ₄	G ₃	G ₂	G ₁
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	0
0	1	0	1
0	1	1	1
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	1	0	1
1	1	1	0

$$a) \quad B_4 = G_4.$$

b) $G_3 = ?$

		B ₂	B ₁	B ₀					
		01	11	10					
B ₄ B ₃		00	0	1	3	2			
01		1	9	1	=	1	1	9	$\rightarrow B'_4 B_3$
11			12	13	15	14			
10		1	8	1	9	1	10	$\rightarrow B_4 B'_3$	

$$\therefore G_3 = B'_4 B_3 + B_3' B_4 \\ = B_3 \oplus B_4$$

c) $G_2 = ?$

$$G_2 = B_2 B_3' + B_3' B_2 \\ = B_2 \oplus B_3$$

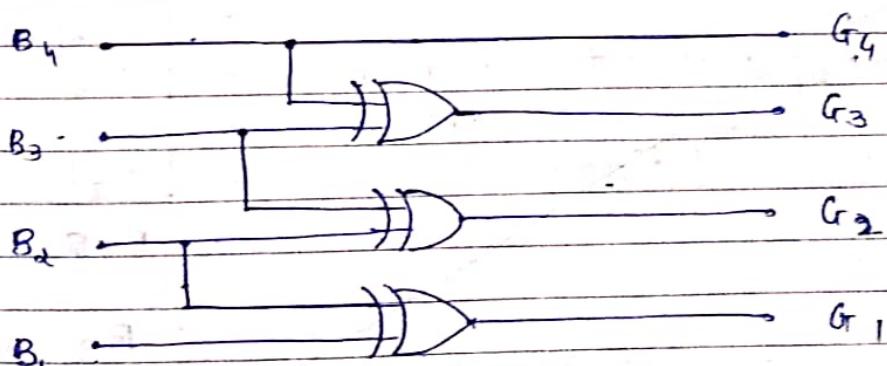
$B_4 B_3$	00	01	11	10	$B'_2 B'_3$	
$B_4 B_3$	00	0	1	1 ₃	1 ₂₁	$B'_2 B'_3$
$B_4 B_3$	01	1 ₄	1 ₅	7	6	$B'_2 B'_3$
$B_4 B_3$	11	1 ₁₂	1 ₁₃	1 ₁₅	1 ₁₄	$B'_2 B'_3$
$B_4 B_3$	10	5	9	1 ₁₁	1 ₁₆	$B'_2 B'_3$

$$d) \quad G_1 = ?$$

$$G_1 = B_1 B_2' + B_1' B_2$$

$$= B_1 \oplus B_2$$

	$B_2 B_1$	00	01	10	11	10
$B_4 B_3$	00	0	4	12	15	5
	01	1	1	1	1	1
	10	5	9	11	15	10
	11	1	3	1	1	1
	10	2	7	14	13	6
	01	1	5	1	1	1
	00	0	4	12	15	5



Grey to BCD

<u>Grey</u>	<u>BCD</u>			
$G_4\ G_3\ G_2\ G_1$	$B_4\ B_3\ B_2\ B_1$			
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1
0 0 1 0	0 0 1 1	0 0 1 1	0 0 1 1	0 0 1 1
0 0 1 1	0 0 1 0	0 0 1 0	0 0 1 0	0 0 1 0
0 1 0 0	0 1 1 1	0 1 1 1	0 1 1 1	0 1 1 1
0 1 0 1	0 1 1 0	0 1 1 0	0 1 1 0	0 1 1 0
0 1 1 0	0 1 0 0	0 1 0 0	0 1 0 0	0 1 0 0
0 1 1 1	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1
1 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1
1 0 0 1	1 1 1 0	1 1 1 0	1 1 1 0	1 1 1 0
1 0 1 0	1 1 0 0	1 1 0 0	1 1 0 0	1 1 0 0
1 0 1 1	1 1 0 1	1 1 0 1	1 1 0 1	1 1 0 1
1 1 0 0	1 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0
1 1 0 1	1 0 0 1	1 0 0 1	1 0 0 1	1 0 0 1
1 1 1 0	1 0 1 1	1 0 1 1	1 0 1 1	1 0 1 1
1 1 1 1	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0

a) $B_4 = G_4$

b) $B_3 = ?$

$G_4\ G_3$	00	01	11	10		$G_4\ G_3$	00	01	11	10	
00	0	1	3	2			0	1	3	2	
01	4	5	7	6			1	4	1	6	
11	12	13	15	14			12	13	15	14	
10	18	19	11	16			18	19	11	16	

$\rightarrow G_2 G_4' G_3$

$\rightarrow G_1 G_4' G_3$

$\rightarrow G_4 G_3'$

$\rightarrow G_4 G_1' G_2$

$\therefore B_3 = G_4 \oplus G_3$

$(B_4 B_3 + B_3 B_4')$

$B_3 = G_1' G_2' G_4 + G_1 G_3 G_4' + G_2 G_3 G_4' + G_4 G_3'$

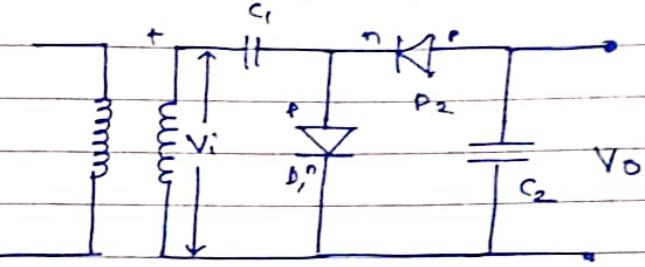
Khaadi Pidde Flat → 8329968591
Khaadi flat Ganjganey → 07020089169

Design of SOP Ckt. to detect decimal nos. 0, 2, 4, 6, 8 in a 4-bit BCD code

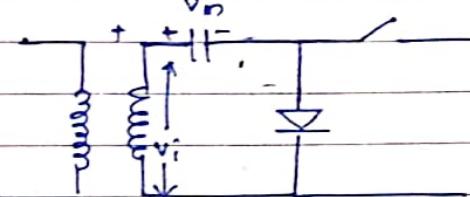
BCD

decimal	5 2 1 1
0	0 0 0 0
1	0 0 0 1
2	0 0 1 1
3	0 1 0 1
4	0 1 1 1
5	1 0 0 0
6	1 0 1 0
7	1 1 0 0
8	1 1 1 0
9	1 1 1 1

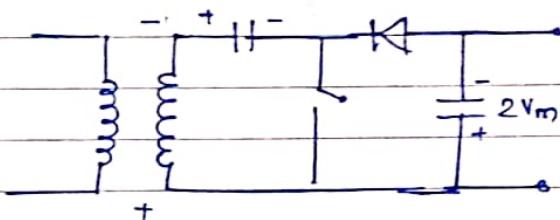
* Half-Wave Voltage Doubler :-



+ve half cycle :-



-ve half cycle :-



$$V_i - V_{C_2} + V_m = 0.$$

$$V_{C_2} = V_m + V_m$$

$$V_{C_2} = 2V_m$$

If load connected, during +ve cycle voltage of C_2 drops & it again is charged to $2V_m$ in -ve halfcycle.

Khosadi flat Gejganj → 7020089169

Khosadi → } Anshul → 90966409 ~~9~~
 Anjimkyā → 9404886290

Khosadi flat → Nagerh → 8484012524
 Mohindukar → 9740479062

Mundada Khosadi → 8575202202

Flat Vivek Khosadi → 9698359191
 Khosadi flat Peenom → 7796293668

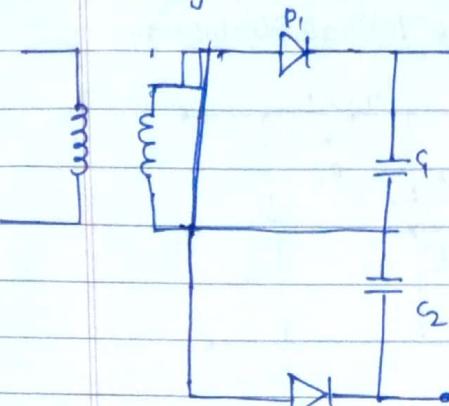
A B

$A \rightarrow A_1, A_2$

$B \rightarrow B_1, B_2$

Date: _____ / _____ / _____
 $A = B$

* Full wave Voltage Doubler.

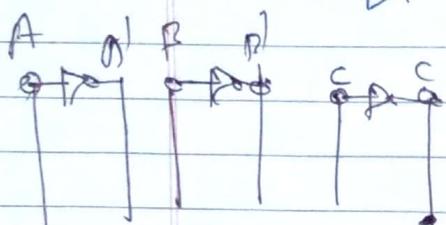


$A - B$

$A \neq B$

$\oplus : \ominus$

①



0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

0, 2, 5, 7, 8, 9, 10, 12, 13, 15

$T' = 0 \oplus 1 \oplus 0 \oplus 1$

A. B.

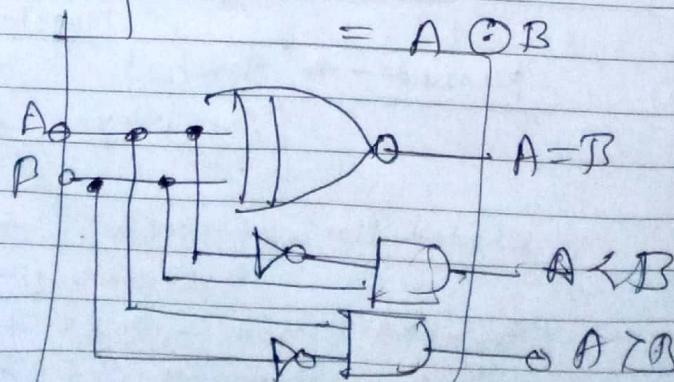
A	B	$A = B$	$A < B$	$A > B$
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

$F(A = B) = A \oplus B$

$= A \odot B$

$$A < B = A \oplus B$$

$$A > B = A \odot B$$



XS-3 addition

No carry - subtract 0011

If carry - add 0011

XS-3 sub.

No borrow - add 0011

If borrow - subtract 0011

BCD addition -

If carry / illegal code - add 0110

BCD Subtraction

If borrow → subtract 0110

Never
forget
to mention

Things
experiences
lives make the D

$$(A + \bar{A})(\bar{A} + \bar{B})$$
$$A\bar{A} + A\bar{B} + \underline{\bar{A}} + \underline{\bar{A}\bar{B}}$$
$$\cancel{A\bar{A} + A\bar{B}}$$

Zener Diode

- special purpose semiconductor diode designed to work under reverse biased condⁿ in the breakdown voltage region.
 - it is heavily doped in both p- & n-sides, thus the depletion layer formed is very thin & the electric field of the junction is very high, even for a small reverse bias.
 - After the breakdown voltage, the Zener voltage remains constant even when the current through it varies over a wide range
- This property is very useful.
- Application : Voltage Regulator, Clipper.

Zener

LED

✓ 1) LED

✓ 2) Photo

✓ 3) Shottkey

✓ 4) Tunnel

5) P-N Juⁿ as photovoltaic cell

6) infrared LED.

1. Voltage Regulation

B+C

$$A\bar{B}C + \underline{B + BD} + AB\bar{B} + \bar{A}C$$

$$= A\bar{B}C + \underline{B + AB\bar{D}} + \bar{A}C.$$

$$= B + A\bar{B}C + \bar{A}C$$

$$= B + C [A\bar{B} + \bar{A}]$$

$$= B + C [\bar{A} + AB]$$

$$= B + C [(A + \bar{A})(\bar{A} + \bar{B})]$$

$$= B + C \bar{A} + C\bar{B}$$

$$= B + C\bar{B} + C\bar{A}$$

256

4-bit binary
grey code

$$A + B [AC + (B + \bar{C})D]$$

$$= (\bar{B} + \bar{B}) + BC +$$

$$A + (ABC + BBD + B\bar{C}D)$$

$$= (B + \bar{B})(B + C) + C\bar{A}$$

$$A + ABC + BD.$$

$$= B + C + C\bar{A}$$

257

Revere

$$A + BD$$

$$= B + C (1 + \bar{A})$$

$$= B + C.$$