* Memory Interfacing with 8085 →

Step 1: Address lines required for Interfacing

8085 handles 64 kB memory i.e. $A_0 - A_{15}$ = 64 kB

for, 32 K = $A_0 - A_{14}$ 2 K = $A_0 - A_{10}$

16 K = $A_0 - A_{13}$ 1 K = $A_0 - A_9$

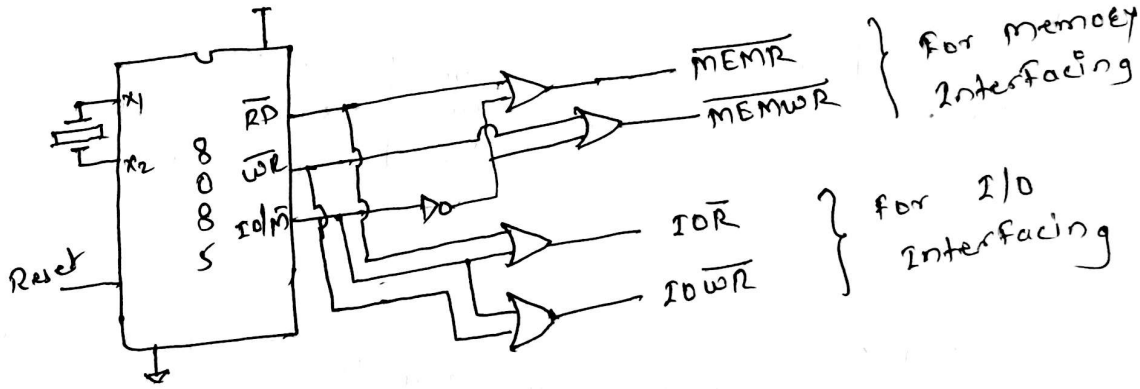
8 K = $A_0 - A_{12}$ 512 K = $A_0 - A_8$

4 K = $A_0 - A_{11}$

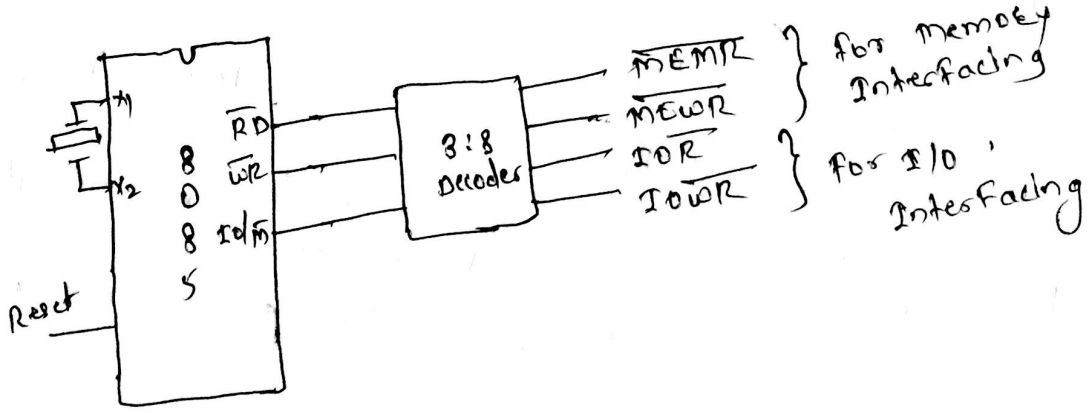
Step 2: There are two ways of generation of control signals. Req'd by using,

(1) Gates (2) 3:8 Decoder

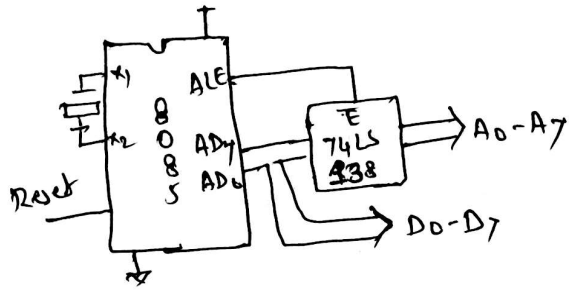
(1) Using Gates →



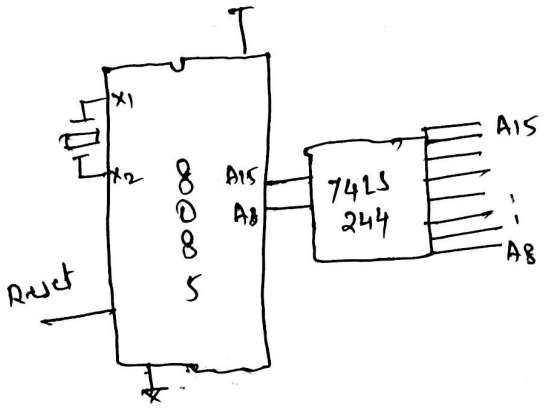
(2) Using 3:8 Decoder →



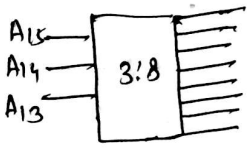
Step 3 → Demux Lower order Address bus & Data bus



Step 4 → separate out higher order Address bus & chip select Logic



For chip select you can use 2:4, 3:8 & 4:16 decoders as per requirement of selecting How many memory chip. you can also use any address lines of A0 - A15.



* Interfacing →

8085 provides $\overline{RD}$, $\overline{WR}$ signals to start read or write operation, Bcoz of the signals writing to memory or reading from memory is possible.

The combination of $\overline{RD}$, $\overline{WR}$ & IO/$\overline{M}$ signals is used to generate the control signals like, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$ & $\overline{IOWR}$ signals.

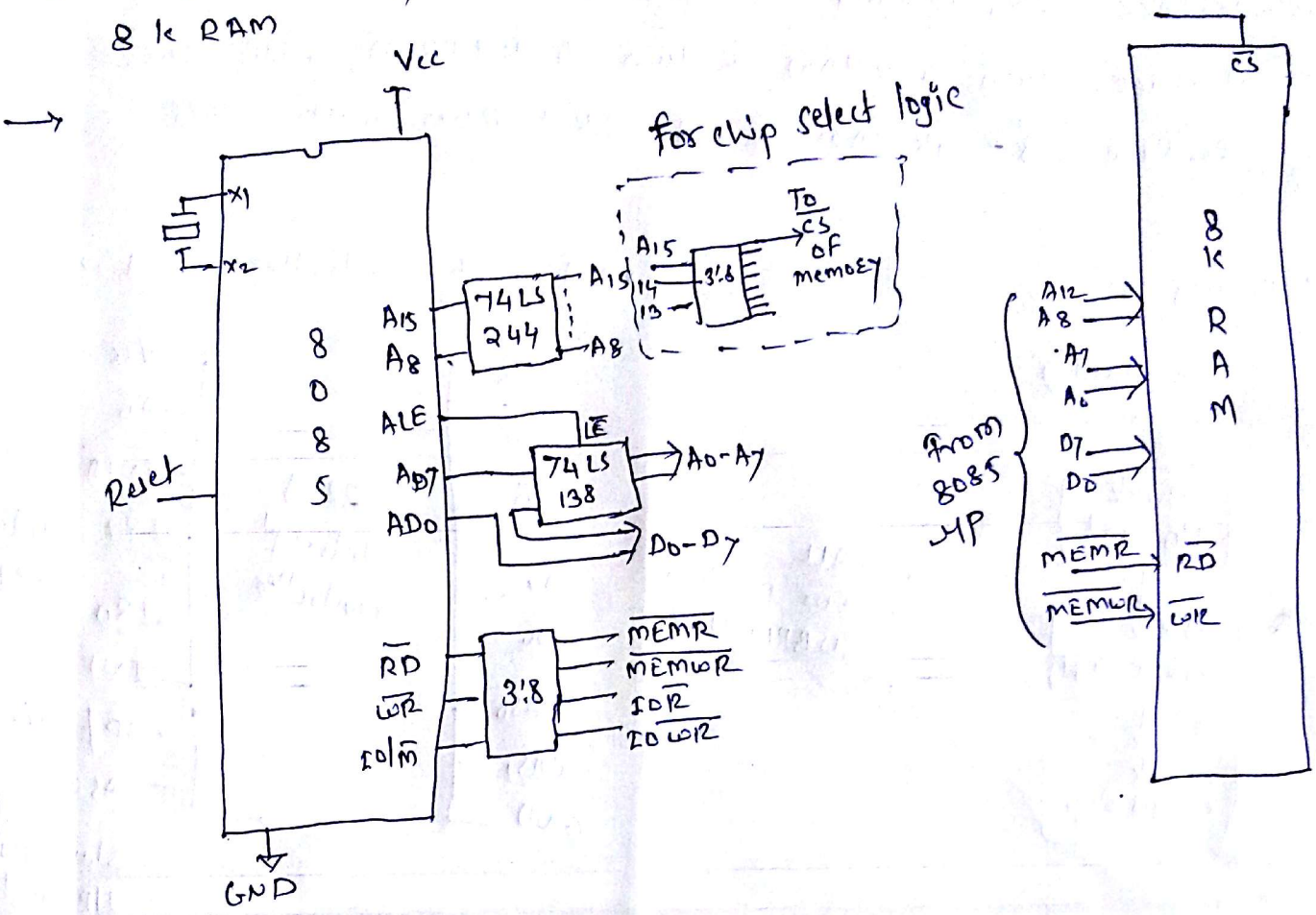
Sometimes using 74LS138 (3:8 decoder) control signals are generated.

74LS244 or 74LS245 is used to separate the add & data bus of lower add Demux.

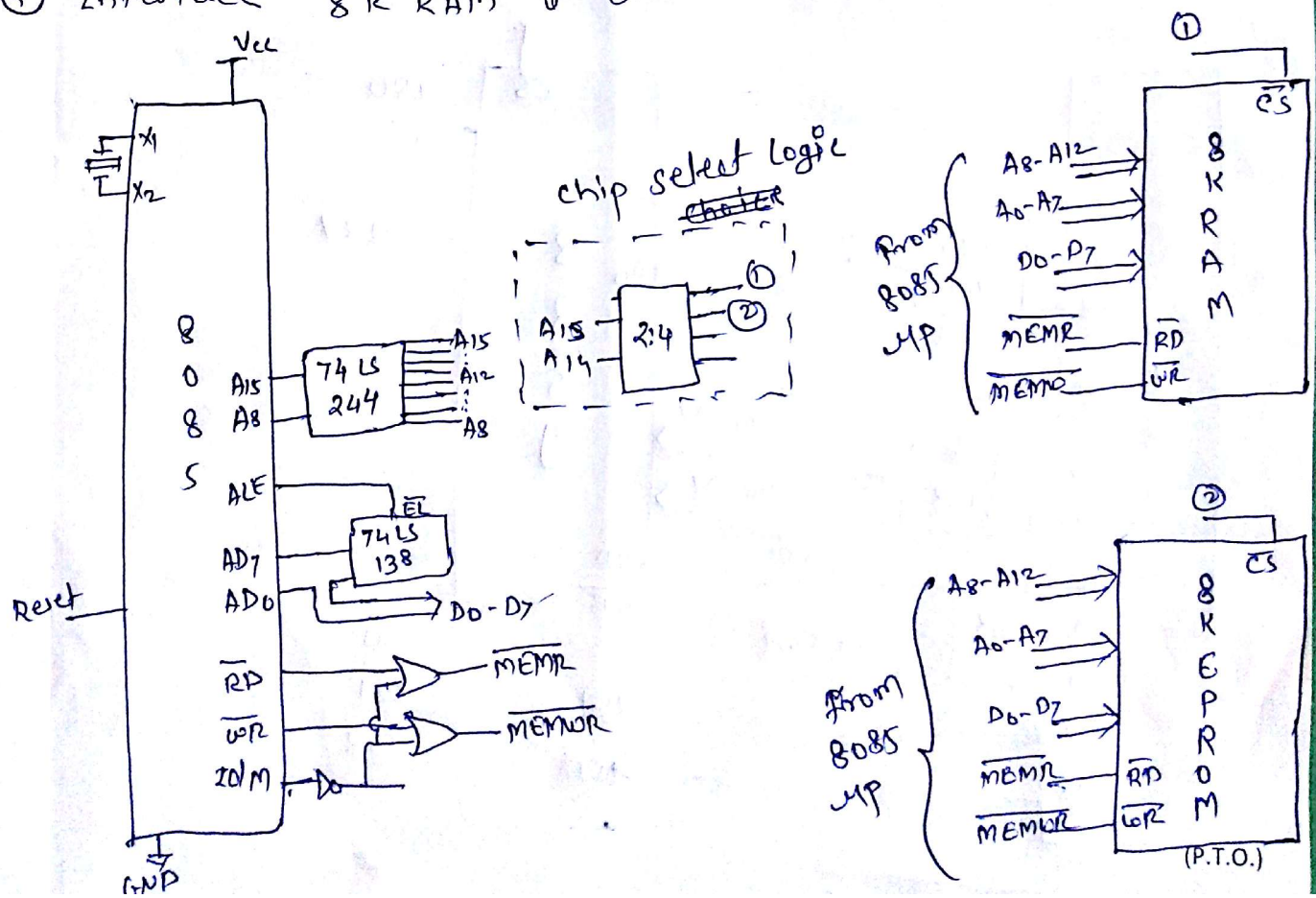
74LS373 is used as a latch for generation of lower order add. bus.

① Design memory system such that it should contain ③
8 k RAM

→



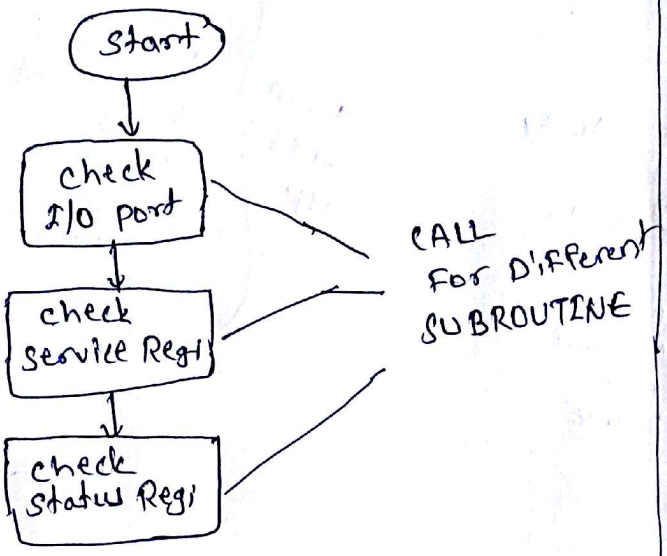
② Interface 8 k RAM & 8k EPROM



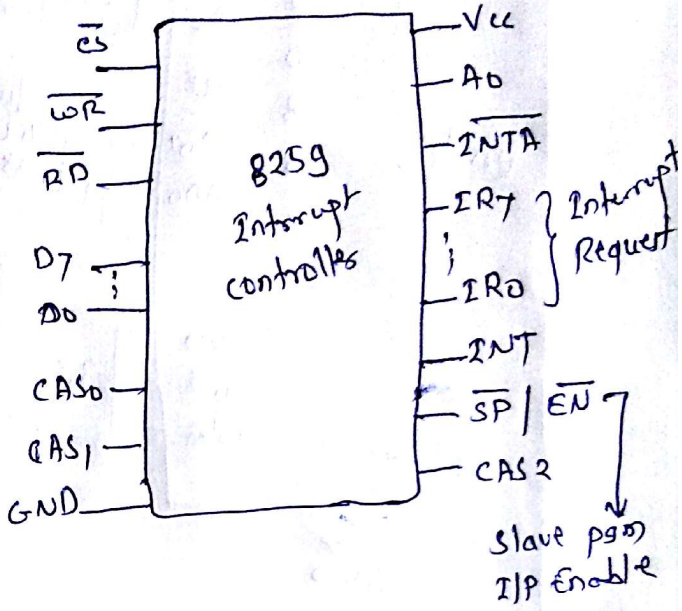
Problem Statements →

1. Interface 2K, 4K, and 8K RAM with 8085
2. Interface two 4-K RAM & two 4-K EPROM with 8085
3. Interface 3 - 4K RAM & 3 - 8K EPROM with 8085

* Poling →



*Interrupt controller 8259 →



* Interface between 8085 with 8259 controller →