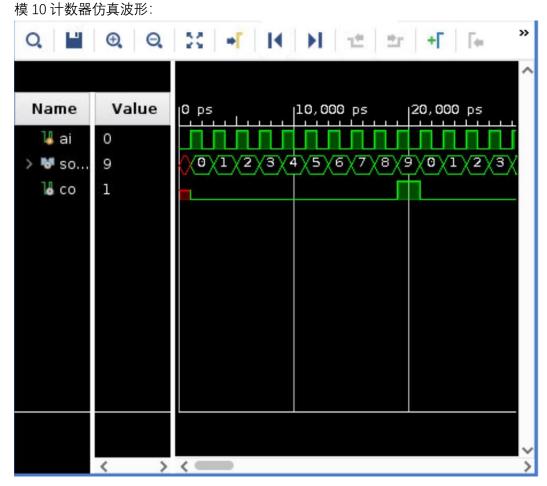
1. 修改模 10 计数器,使进位信号产生在最大那个数字的周期。



# 源码截图:

```
`timescale lns / lps
 2
 4 !
         input ai;
 5 !
         output[3:0] so;
 6
         reg [3:0] so;
 7
         output co;
 8
         reg co;
 9
10 🖯
         always@(posedge ai)
11 🖯
         begin
12 ₪
            if(so < 4'blood)
13 ⊕
                begin
14 :
                    so <= so+1'b1;
15
                    co = 0;
160
                end
17 🖯
            else if(so == 8)
18 ⊖
                begin
19 ;
                    so <= so+l'bl;
20 :
                    co = 1;
21 (
                end
```

```
11 (D)
12 (D)
         begin
              if(so < 4'b1000)
13 ∯
                  begin
14:
                      so <= so+1'b1;
15 :
                      co = 0;
                  end
16
17 🖨
              else if(so == 8)
18 🖯
                  begin
19
                      so <= so+l'bl;
20
                      co = 1;
21 🖨
                  end
22 :
             else
23 ⊖
                  begin
24
                      so = 4'b00000;
25
                      co = 0;
26 🖨
                  end
27 🖨
         end
28 !
29 @ endmodule
30
```

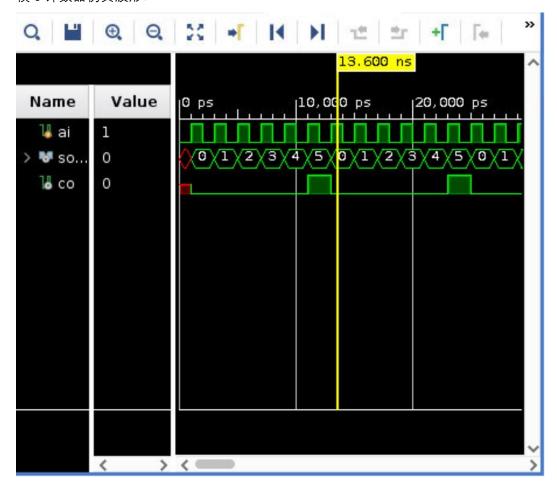
# 测试文件:

```
1    timescale lns / lps
3 ─ module test_10;
 4 ; reg ai;
5 | wire[3:0] so;
 6 | wire co;
 7 :
8 🖨 always
9  begin
10 ; #l ai = ~ai;
11 end
12 :
13 □ initial
14⊖ begin
15
        ai = 1'b0;
16
17 end
18 ;
19 countl0 ul(
20 1
        .ai(ai),
21 !
         sn(sn)
```

```
wire co;
 6 :
 7
8 ⊝ always
9 ─ begin
10 ;
      #l ai = ~ai;
11 ⊝ end
12 :
13 ⊖ initial
14 ⊕ begin
15 :
         ai = 1'b0;
16 :
17 	☐ end
18 :
19 count10 ul(
20 :
        .ai(ai),
21
         .so(so),
22
         .co(co)
23 !
         );
24 !
25 @ endmodule
```

### 2. 模 6 计数器。

模 6 计数器仿真波形:



### 源码截图:

```
`timescale lns / lps
 4 :
         input ai;
         output[3:0] so;
 6 1
         reg [3:0] so;
 7 :
         output co;
8
         reg co;
9
10 🗇
         always@(posedge ai)
11 🖯
         begin
             if(so < 4'b0100)
12 🖯
13 ⊖
                begin
14
                    so <= so+1'b1;
15
                     co = 0;
16 (a)
17 (b)
                 end
             else if(so == 4)
18 ⊖
                begin
19 ;
                    so <= so+1'b1;
20 :
                     co = 1;
21 🛆
                 end
```

```
11 🖨
          begin
12 🗇
              if(so < 4'b0100)
13 ⊖
                  begin
14 :
                       so <= so+1'b1;
15 ;
                       co = 0;
16 🖨
                   end
17日
              else if(so == 4)
18 🖨
                  begin
19 :
                       so <= so+1'b1;
20 :
                       co = 1;
21 🖨
                  end
22 :
              else
23 □
                  begin
24
25
                       so = 4'b00000;
                       co = 0;
26 🖨
                  end
27 🖨
          end
28 !
29 endmodule
30 1
```

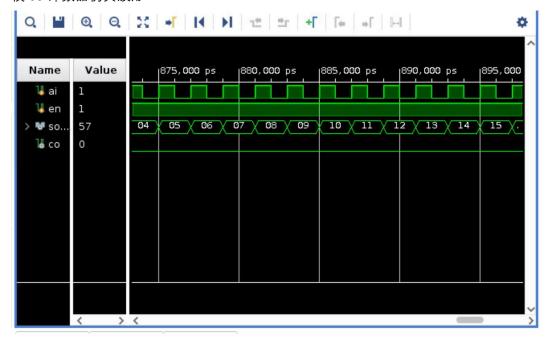
## 测试文件:

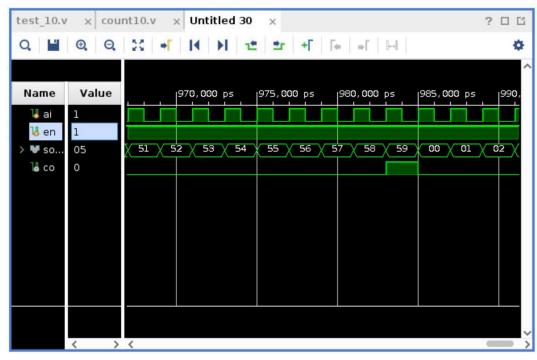
```
1 | `timescale lns / lps
 4   reg ai;
5   wire[3:0] so;
 6 | wire co;
 7 :
8⊜ always
9⊝ begin
10  #l ai = ~ai;
11 a end
12 ;
13 ─ initial
14 ⊖ begin
15 ai = 1'b0;
16
17 🖨 end
18 :
19 : count6 ul(
20 : .ai(ai),
20 .
         sn(sn)
```

```
6 wire co;
8 ⊝ always
9 ⊝ begin
10 ; #l ai = ~ai;
11 @ end
12
13  initial
14  begin
15 | ai = 1'b0;
16 ;
17 ⊝ end
18 :
19 | count6 ul(
20 | .ai(ai),
        .so(so),
.co(co)
21 :
22 ;
23 :
         );
24 !
25 @ endmodule
```

3. 级联模 10 计数器和模 6 计数器, 生成模 60 计数器。

模 60 计数器仿真波形:





#### 源码截图:

```
/mnt/cgshare/project_1/project_1.srcs/sources_1/new/count10.v

→ X ■ ■ X // ■ ♀
                                                             ٠
 1
     `timescale lns / lps
 2 module count60(ai,so,co,en);
 3
         input ai, en;
 4
         output[7:0] so;
 5
         output co;
 6
         wire col0, co6, en 6;
 7
         wire[3:0] sol0, so6;
 8
 9
         countl0 ul(
10
         .ai(ai),
11
         .so(sol0),
         .co(co10),
12
13
         .en(en)
14
         );
15
         and u2(en 6,en,col0);
16
         count6 u3(
17
         .ai(ai),
         .so(so6),
18
19
          .co(co6),
20
          .en(en 6)
21
         1.
```

```
20
          .en(en 6)
21
          );
22
          and u4(co,en 6,co6); //simultaneous carry
23
          assign so = {so6,sol0}; //connect
24
25 @ endmodule
26
27 🖯 module count6(ai, so, co, en);
28
          input ai, en;
29
          output[3:0] so;
30
          reg [3:0] so;
31
          output co;
32
          reg co;
33
          always@(posedge ai)
34 🖯
35 🖯
          begin
36 ⊝
              if(en)
37 □
                  begin
                      if(so < 4'b0100)
38 □
39 ⊝
                           begin
40 !
                               sn <= sn+1'h1.
```

```
40
                              so <= so+l'bl;
41
                              co = 0;
42 🖨
                          end
                      else if(so == 4)
43 □
44 ⊖
                          begin
45 :
                              so <= so+1'b1;
46
                              co = 1:
47 🖨
                          end
                      else
48
49 Ö
                          begin
50 !
                              so = 4'b00000;
51 :
                              co = 0;
52 🖨
                          end
53 🖨
                   end
54
             else
55 🖨
                  50 = 50;
56 🖨
         end
57 !
58 @ endmodule
59 :
60 module countl@(ai so co en).
```

```
60 module countl0(ai, so, co,en);
61 :
         input ai,en;
62 :
         output[3:0] so;
63 ;
         reg [3:0] so;
64 :
         output co;
65 :
         reg co;
66
67 🖯
         always@(posedge ai)
68 🖨
         begin
              if(en)
69 □
70 □
                  begin
                      if(so < 4'b1000)
71 ⊖
72 🖯
                          begin
73 :
                               so <= so+l'bl;
74
                              co = 0;
75 🖨
                          end
                      else if(so == 8)
76 ⊖
77 O
                          begin
78 :
                              so <= so+l'b1;
79 !
                              co = 1.
```

```
73
                              so <= so+1'b1;
74
                              co = 0;
75 🖨
                          end
76 ⊖
                      else if(so == 8)
77 ⊖
                          begin
78 :
                              so <= so+l'b1;
79 :
                              co = 1;
80 🖨
                          end
81 :
                      else
82 🖯
                          begin
83 ;
                              so = 4'b00000;
84 :
                              co = 0;
85 🖨
                          end
86 🖨
                   end
              else
87
88
                  50 = 50;
89 🖨
         end
90 !
91 @ endmodule
92 :
```

# 测试文件:

```
1 'timescale lns / lps
 2:
 3 → module test 60;
 4 | reg ai,en;
5 | wire[7:0] so; //8bit
 6 | wire co;
 7
8 always
 9  begin
10 : #l ai = ~ai;
11 🗀 end
12 :
13 ─ initial
14 ⊖ begin
15 ai = l'b0;
16 en = l'b0;
17 #4 en = l'bl;
18 @ end
19 ;
20 | count60 ul(
21 :
         ai(ai)
```

```
8⊜ always
9⊝ begin
10 #l ai = ~ai;
11 🖨 end
12 ;
13 □ initial
14⊖ begin
15¦ ai
         ai = 1'b0;
16
        en = 1'b0;
17
        #4 en = 1'b1;
18 🗀 end
19 ;
20 count60 ul(
21
22
        .ai(ai),
        .so(so),
23
        .co(co),
24
         .en(en)
25 ;
         );
26 ;
27 ⊝ endmodule
```