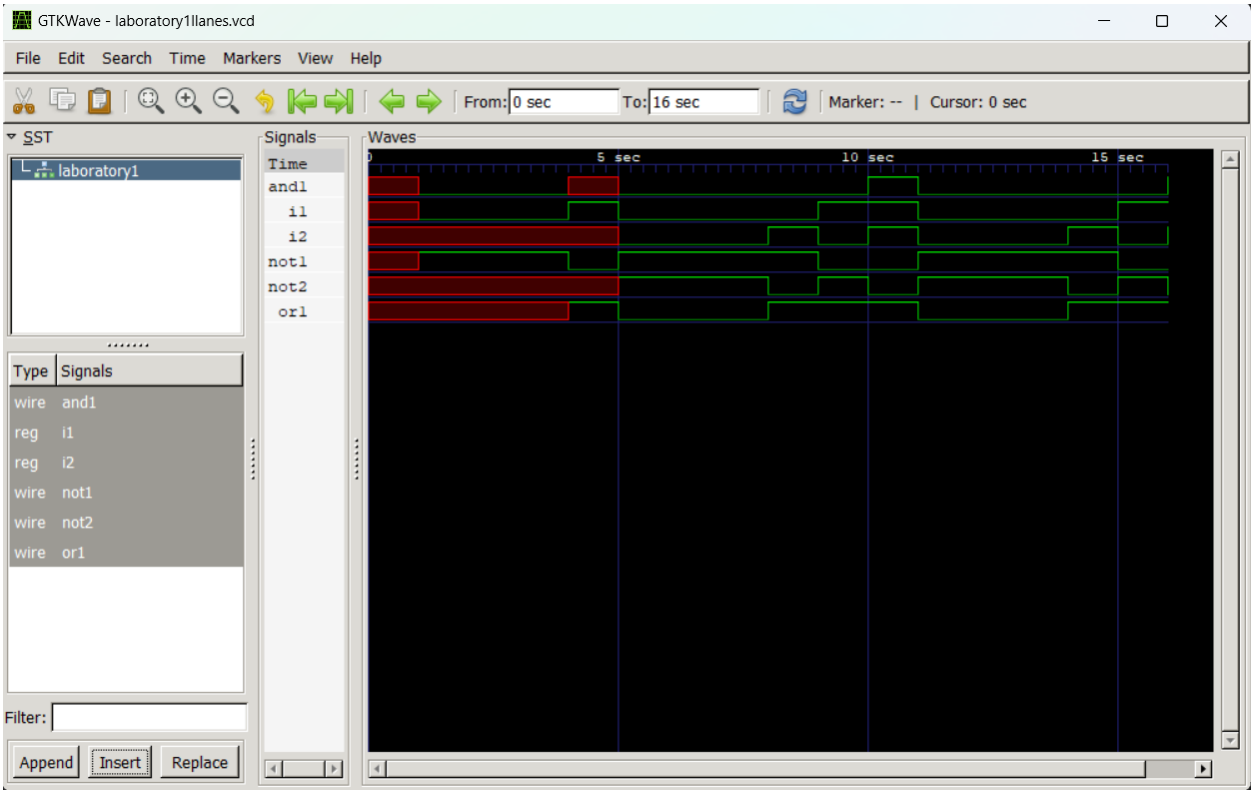
Laboratory 1

laboratory1llanes.v

```
module laboratory1;
    reg i1,i2;
    wire not1,not2,and1,or1;

    not(not1,i1);
    not(not2,i2);
    and(and1,i1,i2);
    or(or1,i1,i2);

    initial
        begin
            $dumpfile("laboratory1llanes.vcd");
            $dumpvars(-1, i1,i2,not1,not2,and1,or1);
            $monitor("%b", i1,i2,not1,not2,and1,or1);
        end
    initial begin
```

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL JUPYTER

```
PS C:\Users\jesie\OneDrive\Documents\verilogg> vvp laboratory1llanes
VCD info: dumpfile laboratory1llanes.vcd opened for output.
xxxxxx
0x1x0x
NOT Gate
x=0,n=1
x=1,n=0
x=0,n=1
AND Gate
x=0,y=0,n=0
x=0,y=1,n=0
x=1,y=0,n=0
x=1,y=1,n=1
x=0,y=0,n=0
OR Gate
x=0,y=0,n=0
x=0,y=1,n=1
x=1,y=0,n=1
x=1,y=1,n=1
PS C:\Users\jesie\OneDrive\Documents\verilogg> gtkwave laboratory1llanes.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
```


GTKWave - laboratory1llanes.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 16 sec
Marker: -- | Cursor: 0 sec
SST
laboratory1
Type Signals
wire and1
reg i1
reg i2
wire not1
wire not2
wire or1
Filter:
Append Insert Replace
Signals
Time
and1
i1
i2
not1
not2
or1
Waves
5 sec
10 sec
15 sec