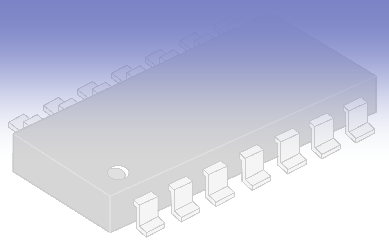
Xilinx ISE

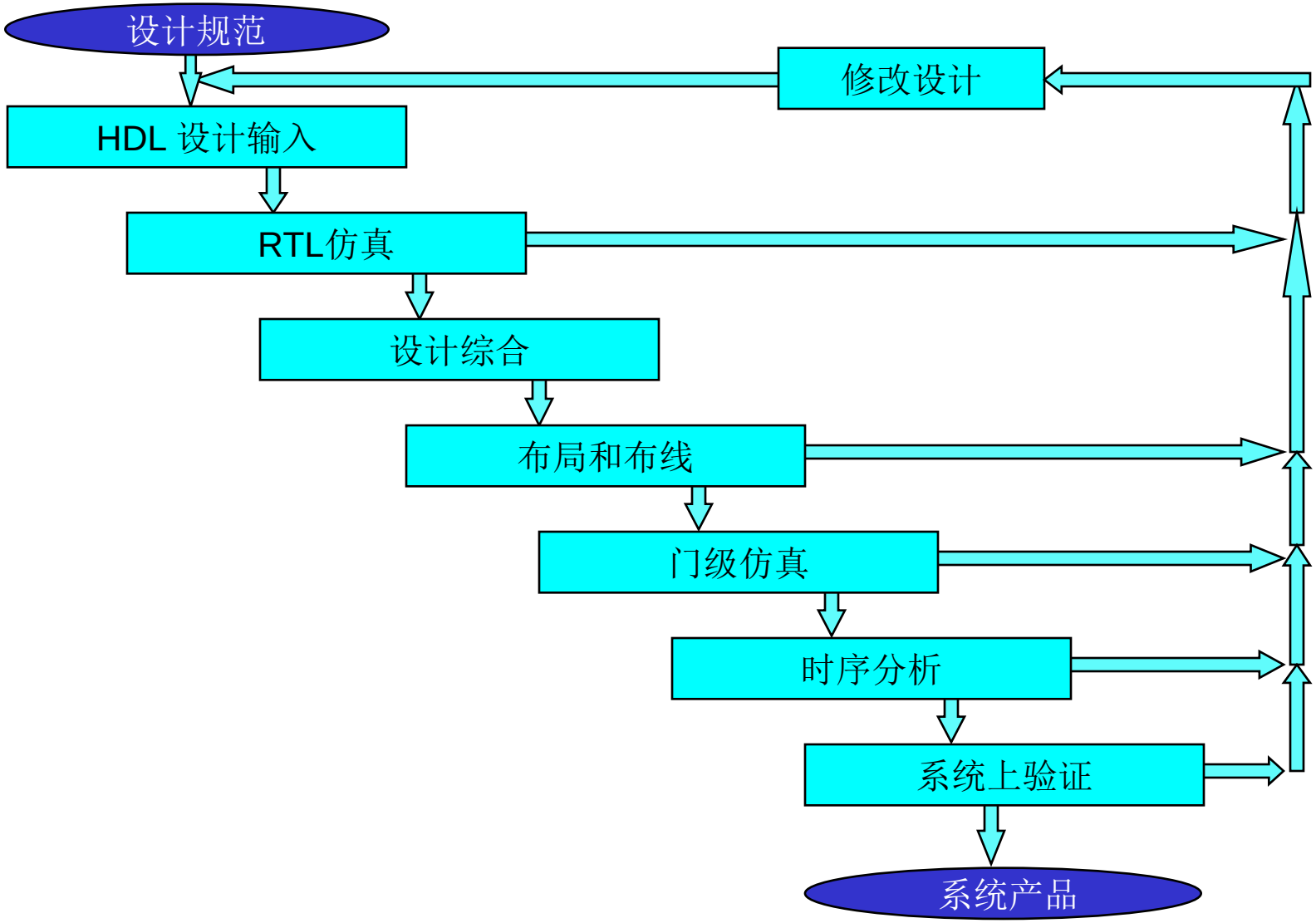
FPGA 设计系统

FPGA 设计系统

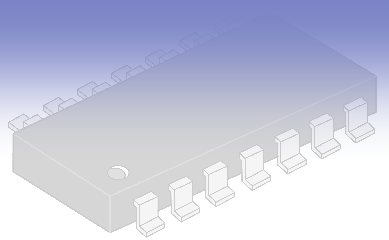


- 面向FPGA设计的EDA系统的典型构成
  - 设计输入——编辑
    - 接受设计描述、语法/语言检查
  - 设计数据库——工程管理
    - 保存系统提供的库单元、用户的设计描述和中间结果
  - 仿真——仿真工具
    - 仿真用户的设计描述
  - 分析和验证工具
    - 模拟验证、设计规则检查等
  - 综合——相对于电路编译器
    - 从高层次描述向低层次描述进行转换
  - 布局、布线——电路模块在FPGA的安排、连接实现
    - 由逻辑设计到物理实现的映射

基于FPGA/CPLD的数字电路设计流程

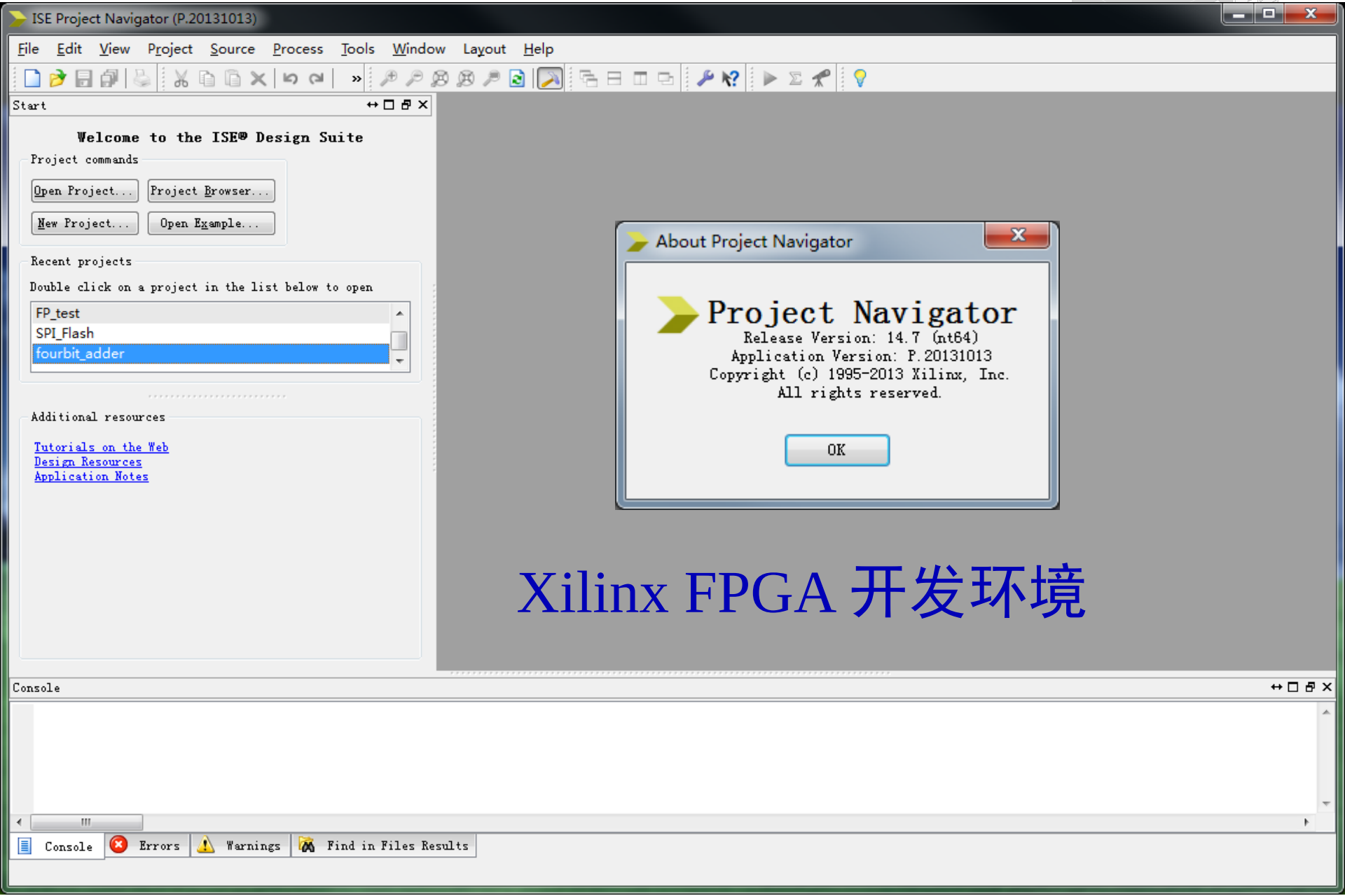


Xilinx FPGA设计步骤

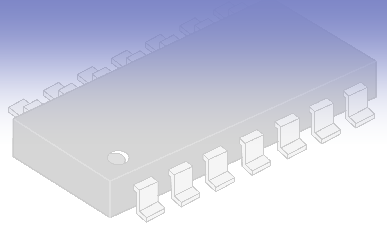


- 设计输入
  - 设计规划——规划系统的构架及器件的选型
  - 设计输入
    - HDL
    - 原理图
  - 使用综合工具生产EDIF网表文件
    - XST、Synplify
  - 对设计进行仿真
- FPGA实现
  - 转换——将多个设计文件合并为一个网表
  - 映射——将网表表示的逻辑电路映射到物理元件中
    - 物理元件
      - CLB——Configurable logic block
      - IOB——Input/Output Block
  - 布局布线——将**编程实行的功能部件**放到FPGA/CPLD器件中，并将它们连接起来，同时提取时序数据
- 调试与仿真
  - 后仿真——根据实际的时序数据进行仿真
- 设计完成及下载
  - 生产CPLD/FPGA的编程文件
    - FPGA —— 位流文件（BIT）
  - 将BIT文件下载到FPGA中，实现物理电路

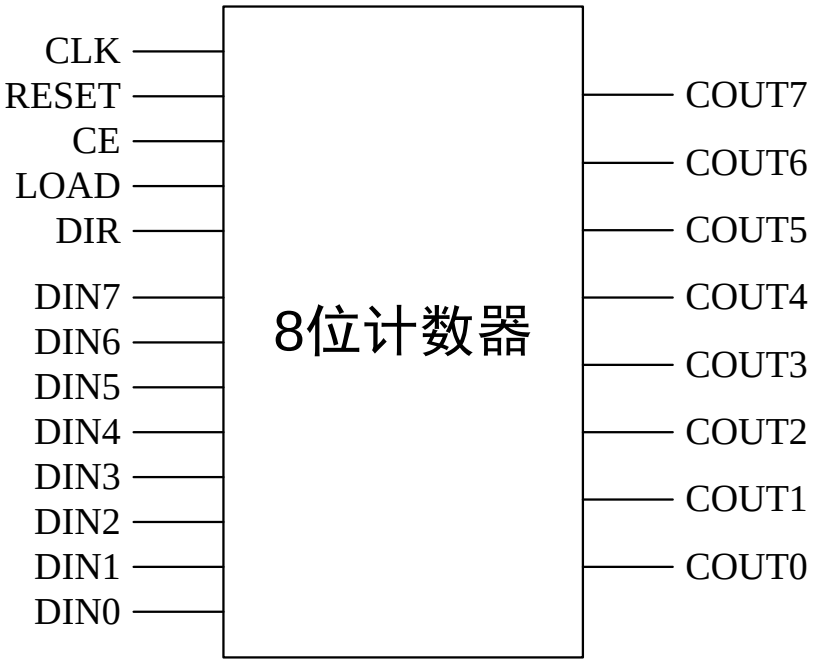
Xilinx ISE 14.7



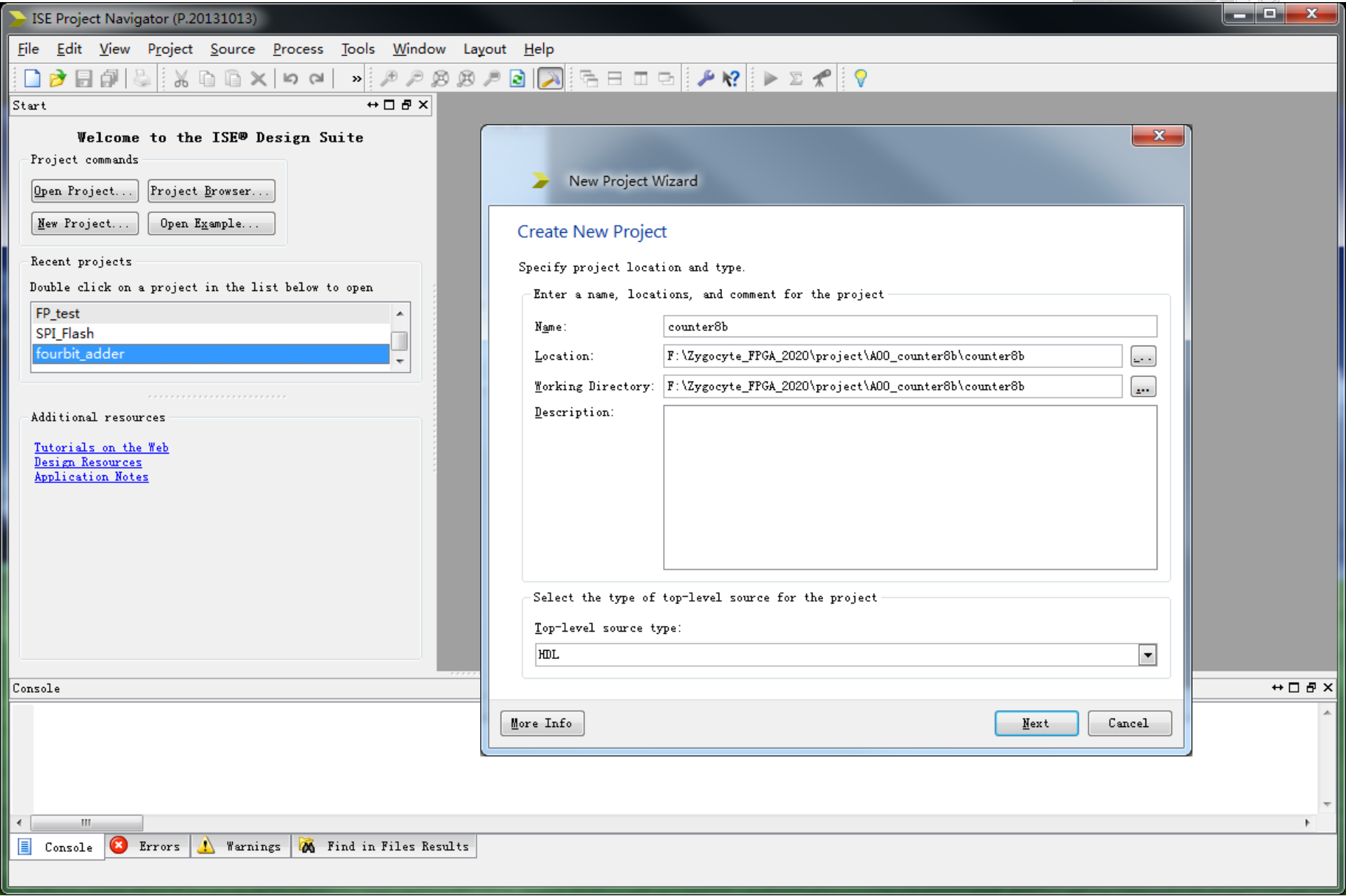
例、设计一个计数器



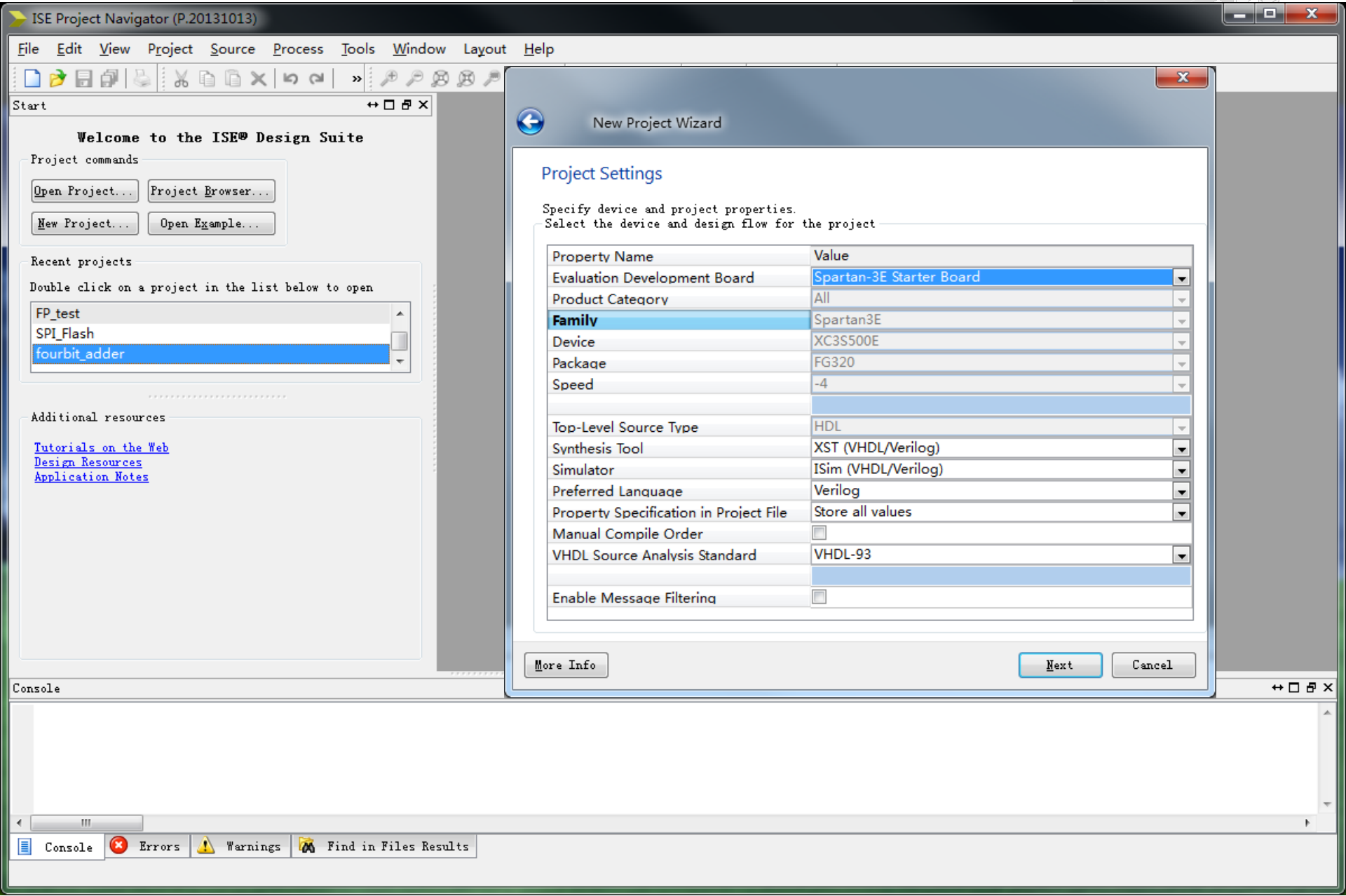
- 计数器功能
  - CLK——计数时钟信号
    - 计数器在该信号的驱动下开始工作；
  - RESET——复位信号
    - 在上升沿处，输入复位为全零；
  - CE——使能信号
    - 为1时计数正常进行，为0时停止计数；
  - LOAD——置数信号
    - 当在时钟上升沿到来时，
    - 如果该信号为 1 时，
    - DIN[7:0] 分别置给 COUT[7:0] 的各位
  - DIR——计数方向控制
    - 为1时递增计数，为0时递减计数。



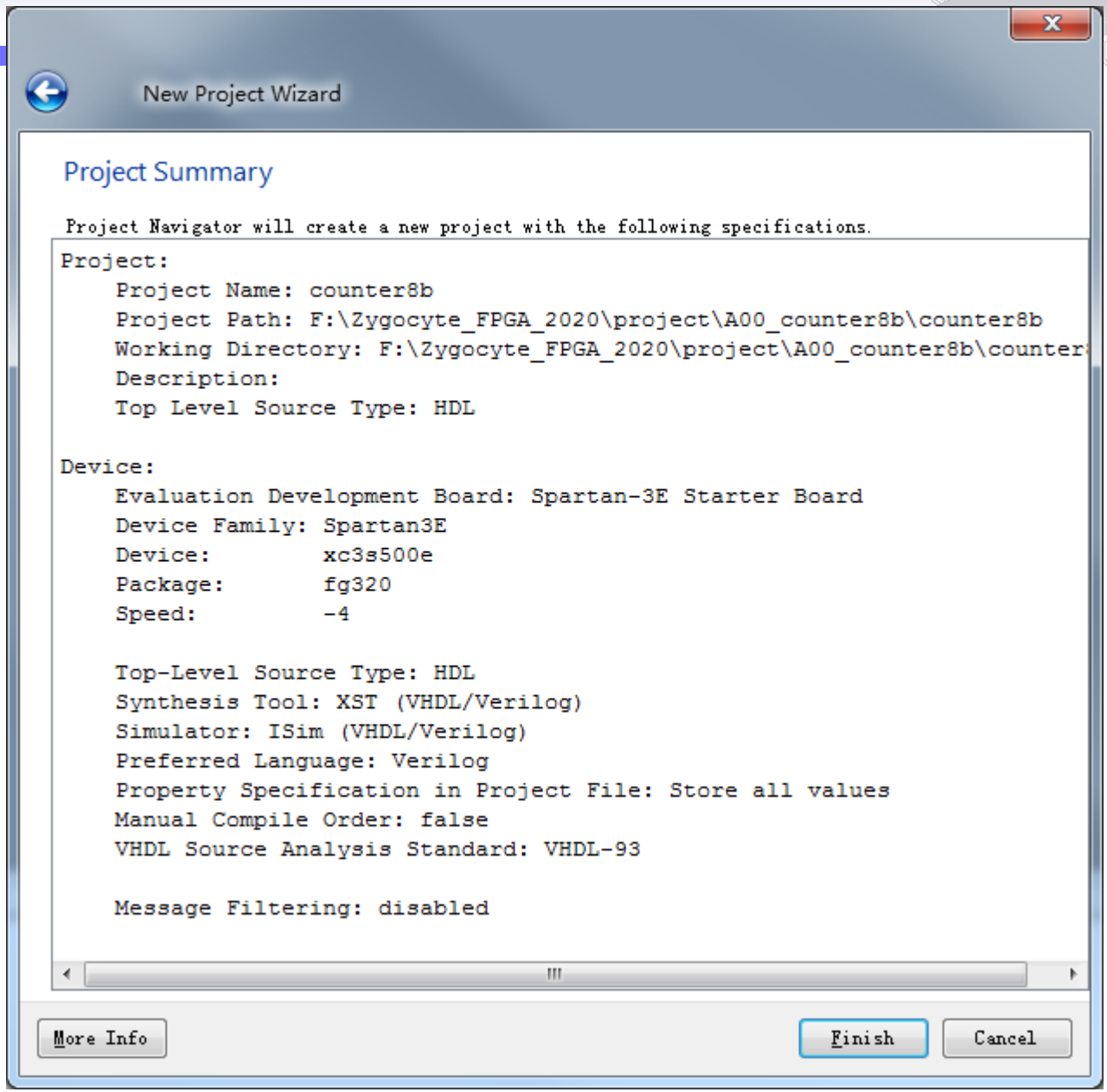
Project

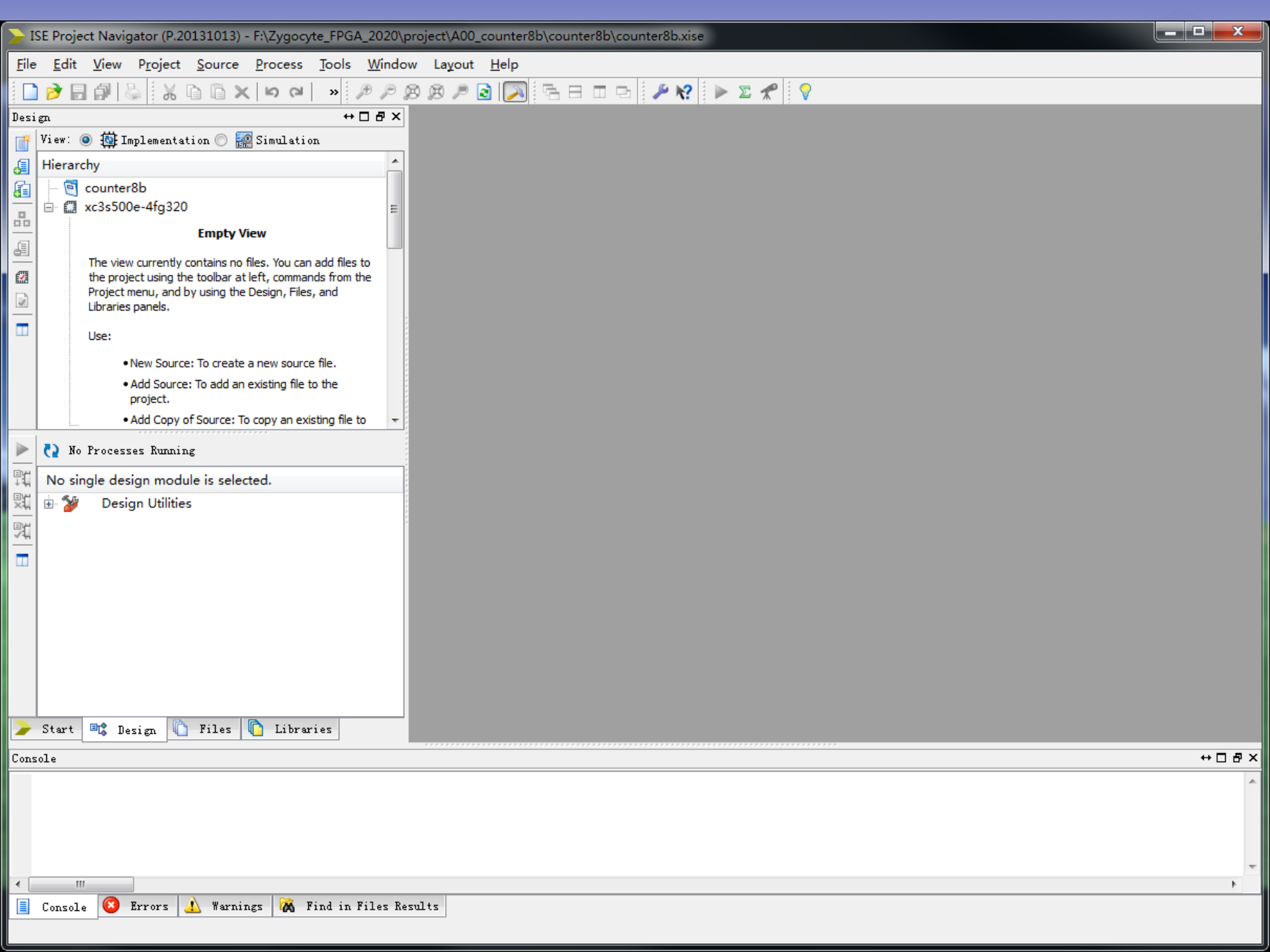

ISE Project Navigator (P.20131013)
File Edit View Project Source Process Tools Window Layout Help
Start
Welcome to the ISE® Design Suite
Project commands
Open Project...
Project Browser...
New Project...
Open Example...
Recent projects
Double click on a project in the list below to open
FP_test
SPI_Flash
fourbit_adder
Additional resources
Tutorials on the Web
Design Resources
Application Notes
New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Name: counter8b
Location: F:\Zygocyte_FPGA_2020\project\A00_counter8b\counter8b
Working Directory: F:\Zygocyte_FPGA_2020\project\A00_counter8b\counter8b
Description:
Select the type of top-level source for the project
Top-level source type:
HDL
More Info
Next
Cancel
Console
Console
Errors
Warnings
Find in Files Results

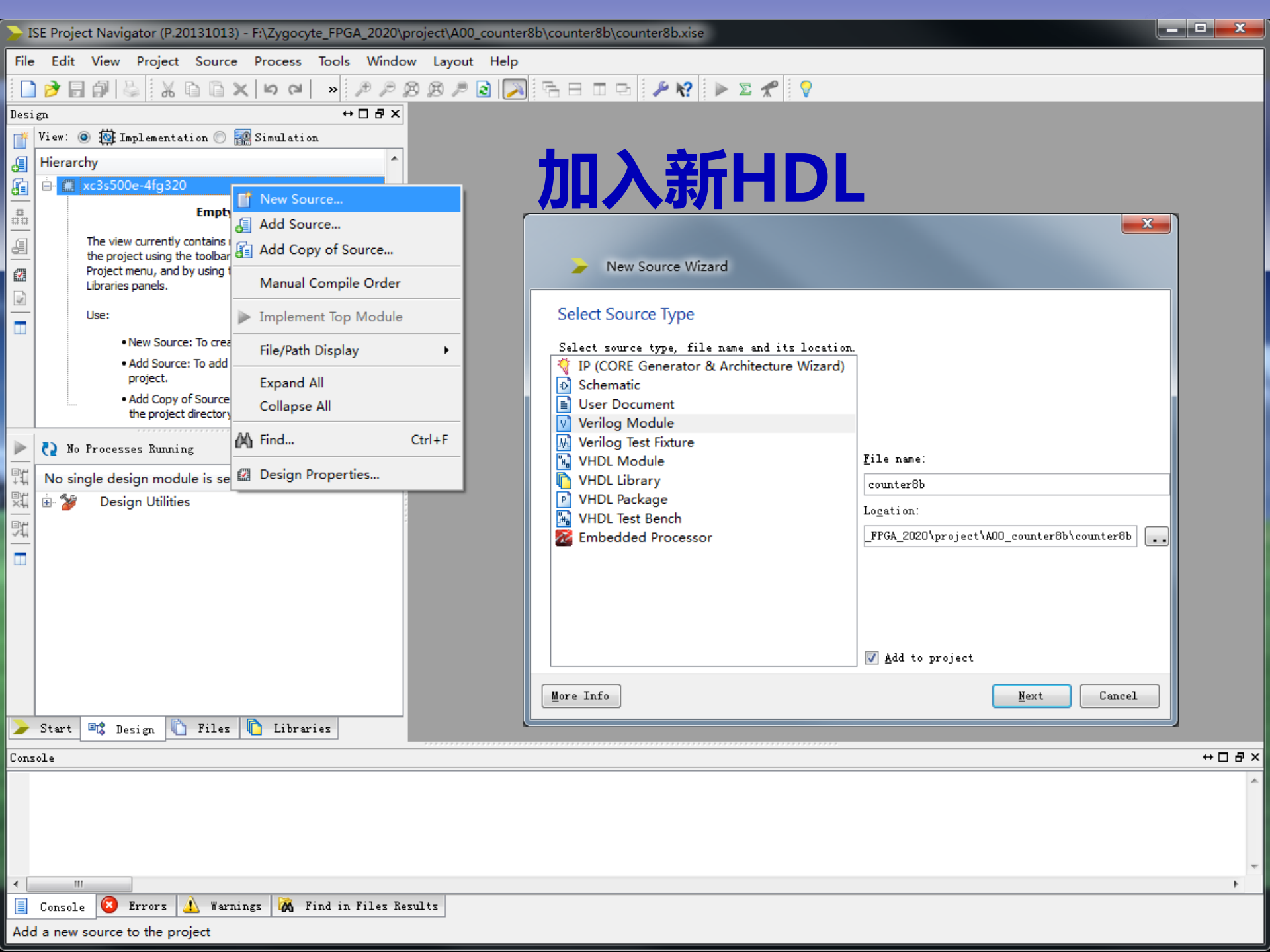
Evaluation Development Board

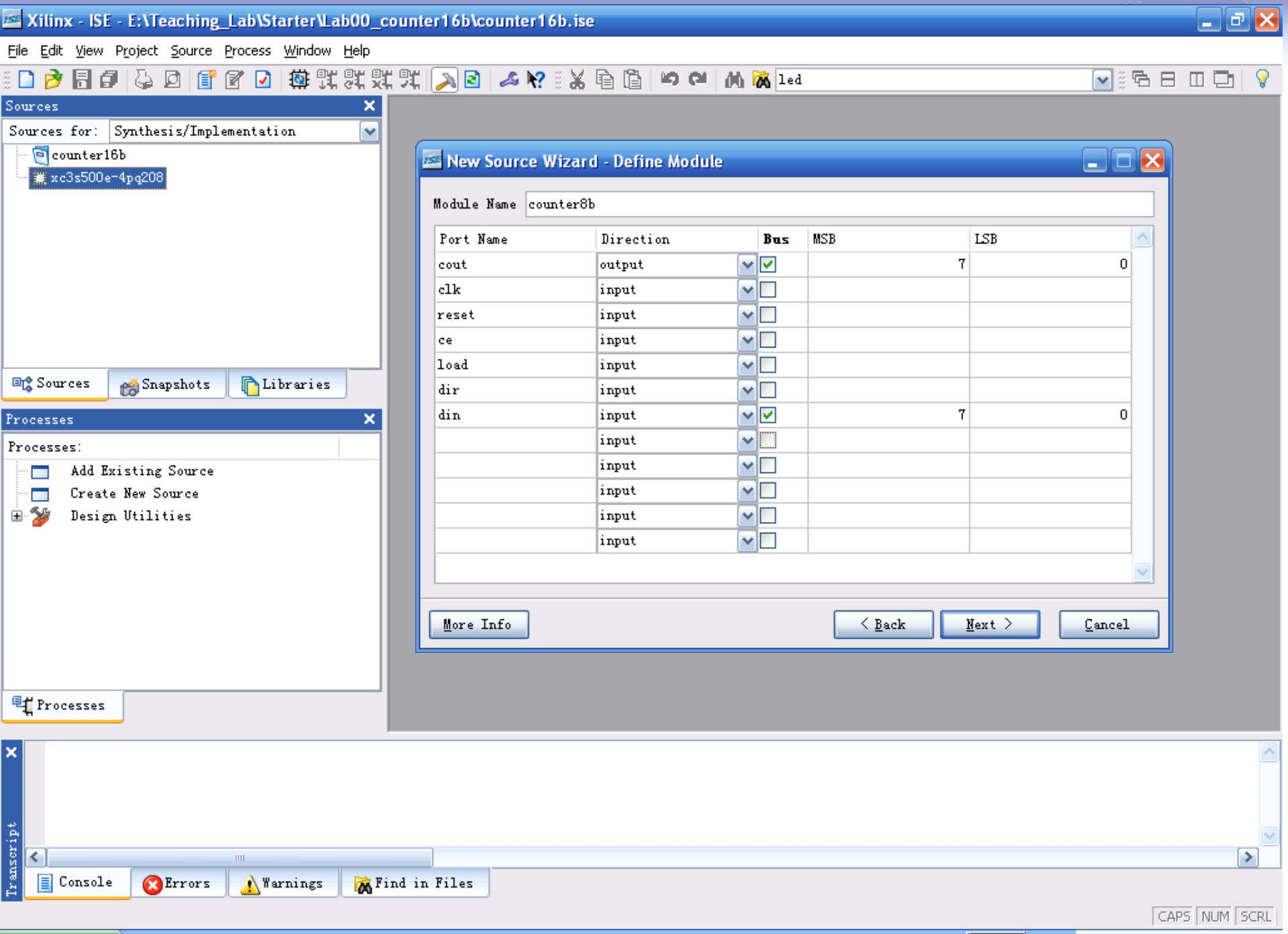


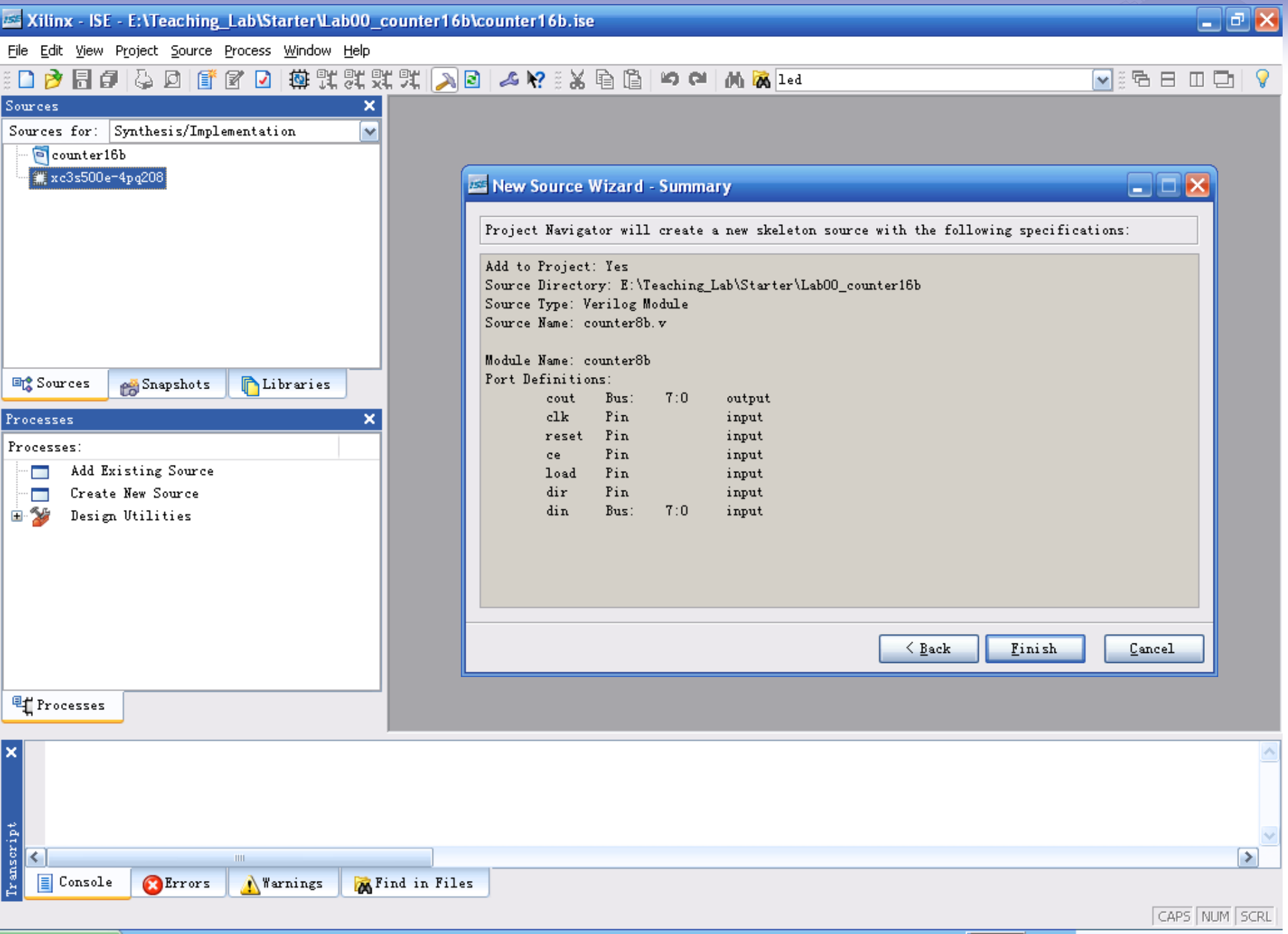
New Project

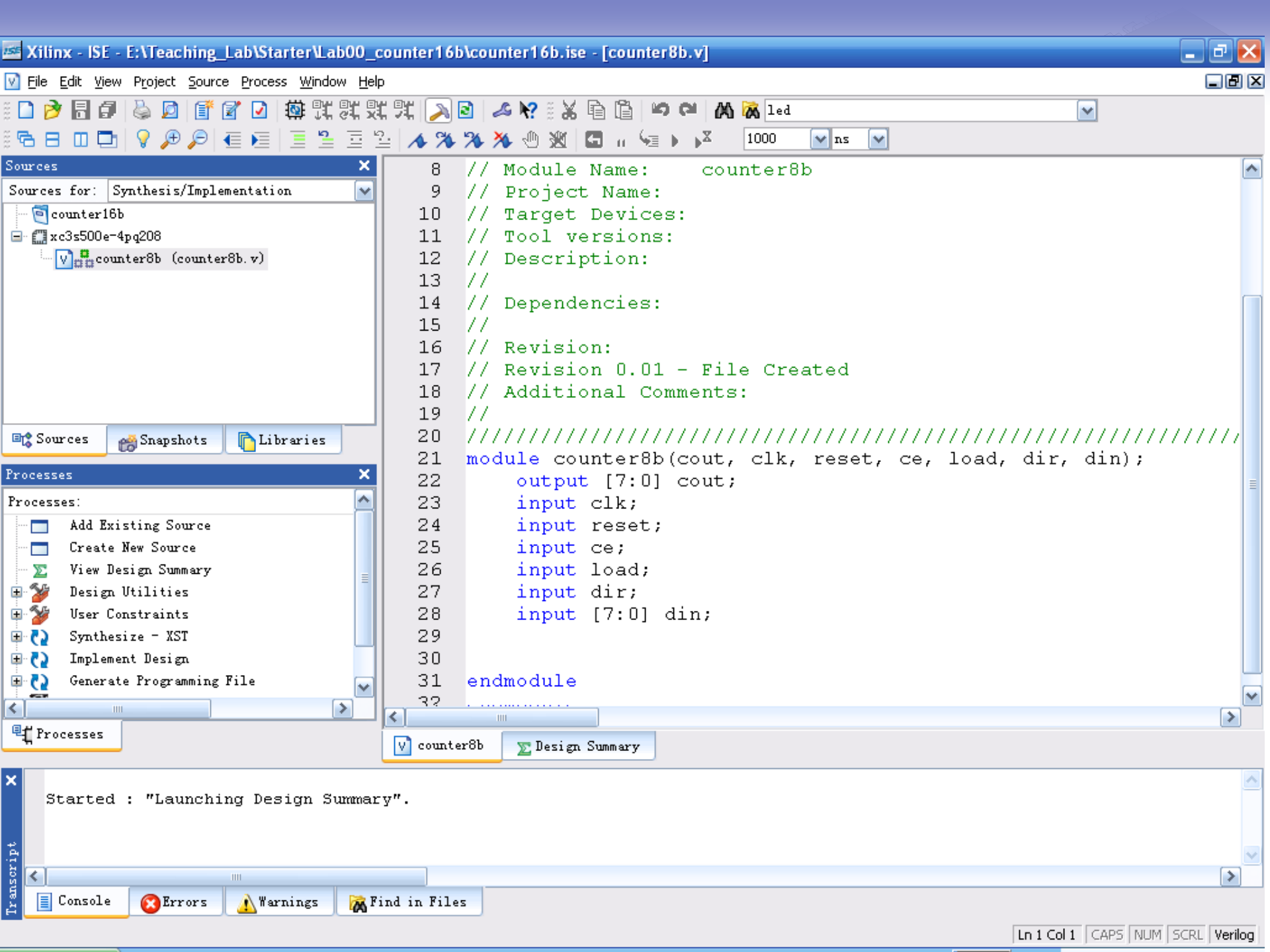

New Project Wizard
Project Summary
Project Navigator will create a new project with the following specifications.
Project:
Project Name: counter8b
Project Path: F:\Zygocyte_FPGA_2020\project\A00_counter8b\counter8b
Working Directory: F:\Zygocyte_FPGA_2020\project\A00_counter8b\counter
Description:
Top Level Source Type: HDL
Device:
Evaluation Development Board: Spartan-3E Starter Board
Device Family: Spartan3E
Device: xc3s500e
Package: fg320
Speed: -4
Top-Level Source Type: HDL
Synthesis Tool: XST (VHDL/Verilog)
Simulator: ISim (VHDL/Verilog)
Preferred Language: Verilog
Property Specification in Project File: Store all values
Manual Compile Order: false
VHDL Source Analysis Standard: VHDL-93
Message Filtering: disabled
More Info
Finish
Cancel

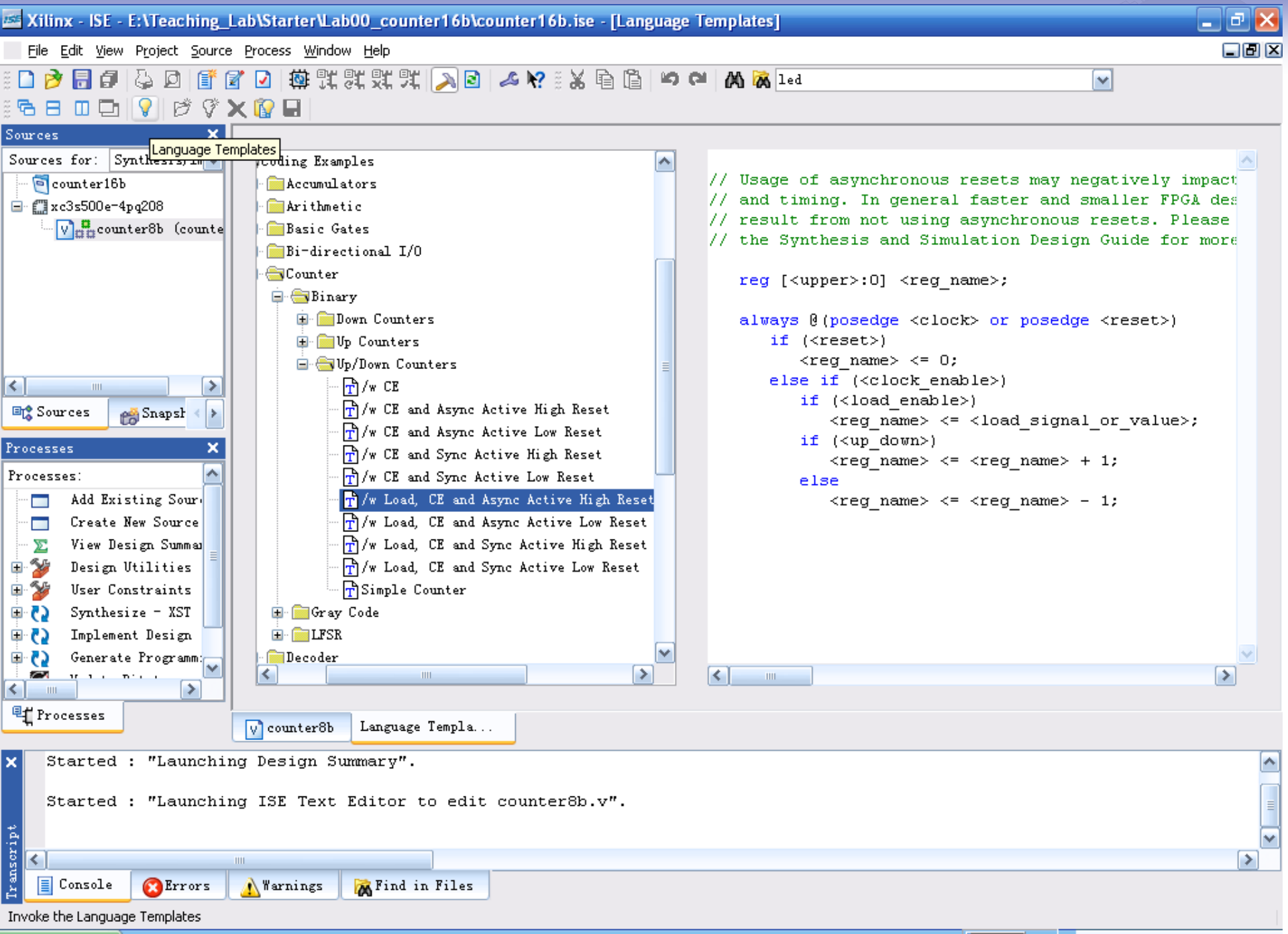

ISE Project Navigator (P.20131013) - F:\Zygocyte_FPGA_2020\project\A00_counter8b\counter8b\counter8b.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
counter8b
xc3s500e-4fg320
Empty View
The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.
Use:
• New Source: To create a new source file.
• Add Source: To add an existing file to the project.
• Add Copy of Source: To copy an existing file to
No Processes Running
No single design module is selected.
Design Utilities
Start Design Files Libraries
Console
Console Errors Warnings Find in Files Results


ISE Project Navigator (P.20131013) - F:\Zygocyte_FPGA_2020\project\A00_counter8b\counter8b\counter8b.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
xc3s500e-4fg320
New Source...
Add Source...
Add Copy of Source...
Manual Compile Order
Implement Top Module
File/Path Display
Expand All
Collapse All
Find... Ctrl+F
Design Properties...
No Processes Running
Design Utilities
Start Design Files Libraries
加入新HDL
New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wizard)
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
counter8b
Location:
_FPGA_2020\project\A00_counter8b\counter8b
Add to project
More Info
Next
Cancel
Console
Console Errors Warnings Find in Files Results
Add a new source to the project


Xilinx - ISE - E:\Teaching_Lab\Starter\Lab00_counter16b\counter16b.ise
File Edit View Project Source Process Window Help
led
Sources
Sources for: Synthesis/Implementation
counter16b
xc3s500e-4pq208
Sources Snapshots Libraries
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
New Source Wizard - Define Module
Module Name counter8b
Port Name Direction Bus MSB LSB
cout output 7 0
clk input
reset input
ce input
load input
dir input
din input 7 0
More Info
< Back
Next >
Cancel
Transcript
Console Errors Warnings Find in Files
CAPS NUM SCRL


Xilinx - ISE - E:\Teaching_Lab\Starter\Lab00_counter16b\counter16b.ise
File Edit View Project Source Process Window Help
led
Sources
Sources for: Synthesis/Implementation
counter16b
xc3s500e-4pq208
Sources Snapshots Libraries
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
New Source Wizard - Summary
Project Navigator will create a new skeleton source with the following specifications:
Add to Project: Yes
Source Directory: E:\Teaching_Lab\Starter\Lab00_counter16b
Source Type: Verilog Module
Source Name: counter8b.v
Module Name: counter8b
Port Definitions:
cout Bus: 7:0 output
clk Pin input
reset Pin input
ce Pin input
load Pin input
dir Pin input
din Bus: 7:0 input
< Back
Finish
Cancel
Transcript
Console
Errors
Warnings
Find in Files
CAPS
NUM
SCRL


Xilinx - ISE - E:\Teaching_Lab\Starter\Lab00_counter16b\counter16b.ise - [counter8b.v]
File Edit View Project Source Process Window Help
led
1000
ns
Sources
Sources for: Synthesis/Implementation
counter16b
xc3s500e-4pq208
counter8b (counter8b.v)
Sources
Snapshots
Libraries
Processes
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Processes
8 // Module Name: counter8b
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module counter8b(cout, clk, reset, ce, load, dir, din);
22 output [7:0] cout;
23 input clk;
24 input reset;
25 input ce;
26 input load;
27 input dir;
28 input [7:0] din;
29
30
31 endmodule
counter8b
Design Summary
Started : "Launching Design Summary".
Transcript
Console
Errors
Warnings
Find in Files
Ln 1 Col 1
CAPS
NUM
SCRL
Verilog


Xilinx - ISE - E:\Teaching_Lab\Starter\Lab00_counter16b\counter16b.ise - [Language Templates]
File Edit View Project Source Process Window Help
led
Sources
Language Templates
Sources for:
counter16b
xc3s500e-4pq208
counter8b (counte
Sources
Snapsh
Processes
Processes:
Add Existing Sour
Create New Source
View Design Summa
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programm
Processes
Coding Examples
Accumulators
Arithmetic
Basic Gates
Bi-directional I/O
Counter
Binary
Down Counters
Up Counters
Up/Down Counters
/w CE
/w CE and Async Active High Reset
/w CE and Async Active Low Reset
/w CE and Sync Active High Reset
/w CE and Sync Active Low Reset
/w Load, CE and Async Active High Reset
/w Load, CE and Async Active Low Reset
/w Load, CE and Sync Active High Reset
/w Load, CE and Sync Active Low Reset
Simple Counter
Gray Code
LFSR
Decoder
// Usage of asynchronous resets may negatively impact
// and timing. In general faster and smaller FPGA des
// result from not using asynchronous resets. Please
// the Synthesis and Simulation Design Guide for more
reg [<upper>:0] <reg_name>;
always @(posedge <clock> or posedge <reset>)
if (<reset>)
<reg_name> <= 0;
else if (<clock_enable>)
if (<load_enable>)
<reg_name> <= <load_signal_or_value>;
if (<up_down>)
<reg_name> <= <reg_name> + 1;
else
<reg_name> <= <reg_name> - 1;
counter8b
Language Templa...
Started : "Launching Design Summary".
Started : "Launching ISE Text Editor to edit counter8b.v".
Transcript
Console
Errors
Warnings
Find in Files
Invoke the Language Templates

counter8b.v

File Edit View Window

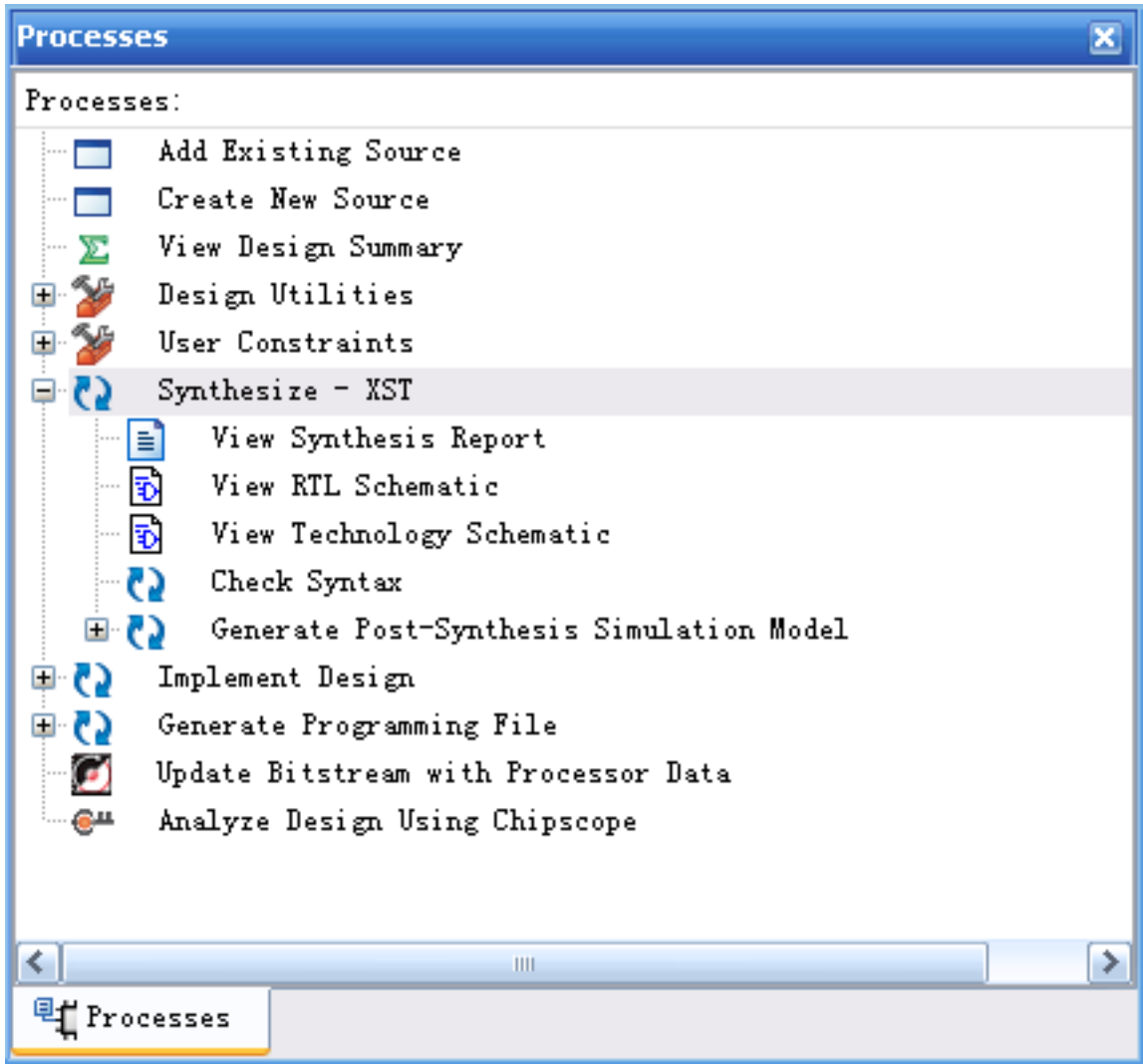
cnt

```
20  ////////////////////////////////////////////////////////////////////////////////
21  module counter8b( cout, clk, reset, ce, load, dir, din);
22      output [7:0] cout;
23      input clk;
24      input reset;
25      input ce;
26      input load;
27      input dir;
28      input [7:0] din;
29
30      reg [7:0] cnt;
31
32      always @(posedge clk or posedge reset)
33      begin
34          if ( reset )
35              cnt <= 0;
36          else if ( ce )
37              if ( load )
38                  cnt <= din;
39              else if ( dir ) // dir 计数方向控制, 为1时递增计数, 为0时递减计数。
40                  cnt <= cnt + 1'b1;
41              else
42                  cnt <= cnt - 1'b1;
43      end
44
45      assign cout = cnt;
46
47  endmodule
48
49
```

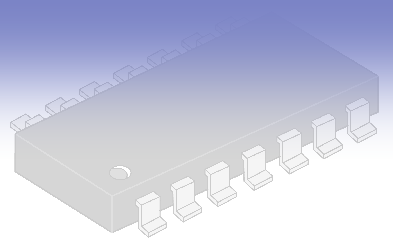
CAPS NUM SCRL LOC Verilog

对设计进行综合

- 在 Processes 窗口
  - 双击 Synthesize-XST



查看综合结果



- Design Overview
  - Summary
  - IOB Properties
  - Module Level Utilization
  - Timing Constraints
  - Pinout Report
  - Clock Report
  - Static Timing
- Errors and Warnings
  - Parser Messages
  - Synthesis Messages
  - Translation Messages
  - Map Messages
  - Place and Route Messages
  - Timing Messages
  - Bitgen Messages
  - All Implementation Messages
- Detailed Reports
  - Synthesis Report
  - Translation Report
  - Map Report
  - Place and Route Report
  - Post-PAR Static Timing Report
  - Power Report
  - Bitgen Report
- Secondary Reports

Design Properties
- Enable Message Filtering

Optional Design Summary Contents
- Show Clock Report
- Show Failing Constraints
- Show Warnings
- Show Errors

counter8b Project Status (05/08/2020 - 15:38:54)			
Project File:	counter8b.xise	**Parser Errors:**	No Errors
Module Name:	counter8b	**Implementation State:**	Synthesized
Target Device:	xc3s500e-4fg320	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	No Warnings
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	5	4656	0%
Number of Slice Flip Flops	8	9312	0%
Number of 4 input LUTs	10	9312	0%
Number of bonded IOBs	21	232	9%
Number of GCLKs	1	24	4%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	周五 五月 8 15:38:52 2020	0	0	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

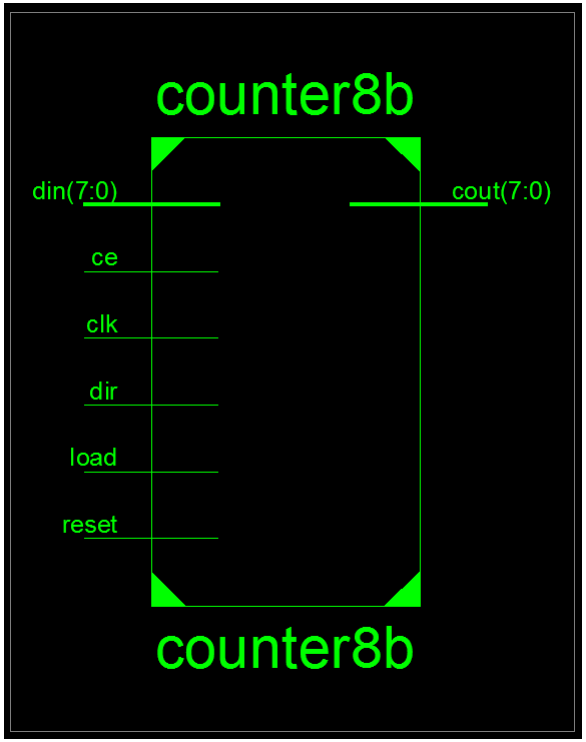
Secondary Reports [-]		
Report Name	**Status**	**Generated**

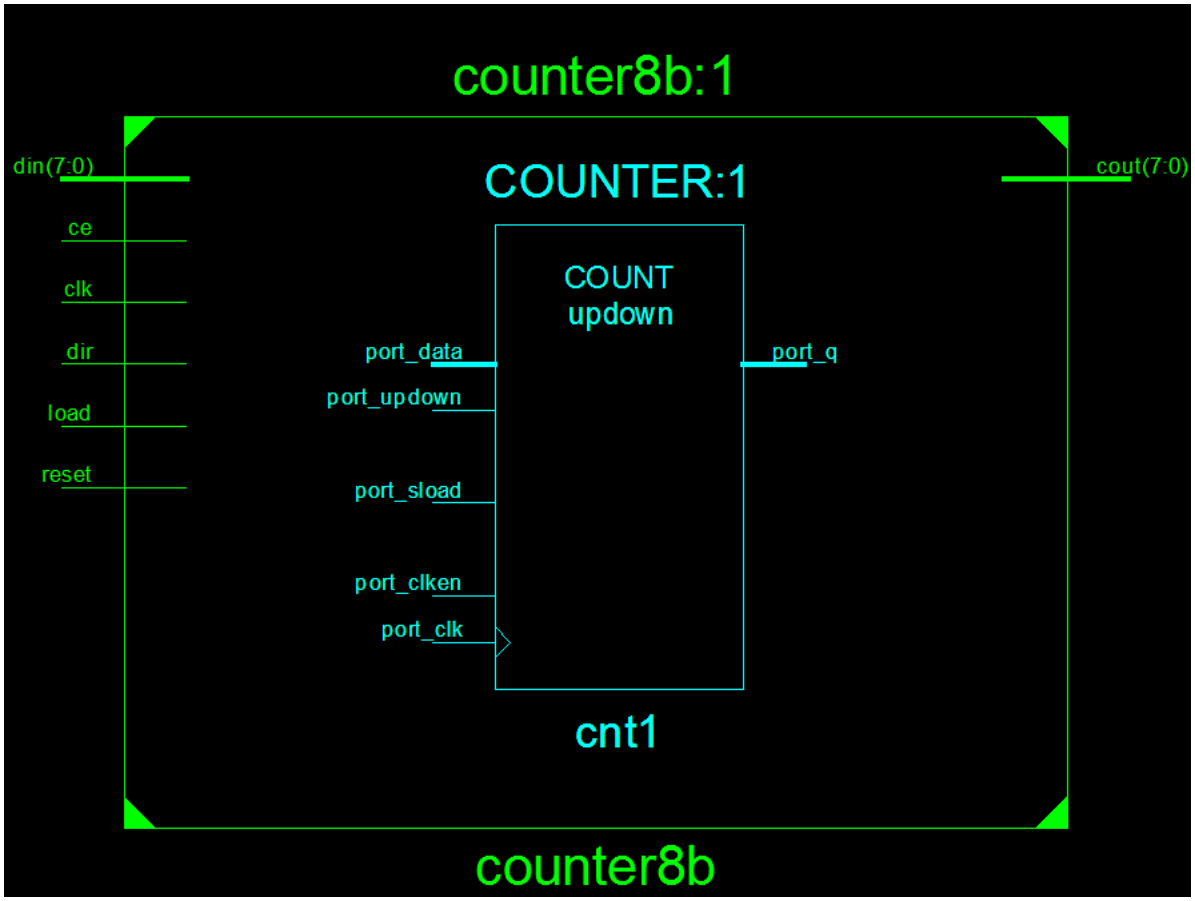
Date Generated: 05/08/2020 - 15:38:54

Design Summary (Synthesized) | counter8b.v

查看 RTL 原理图

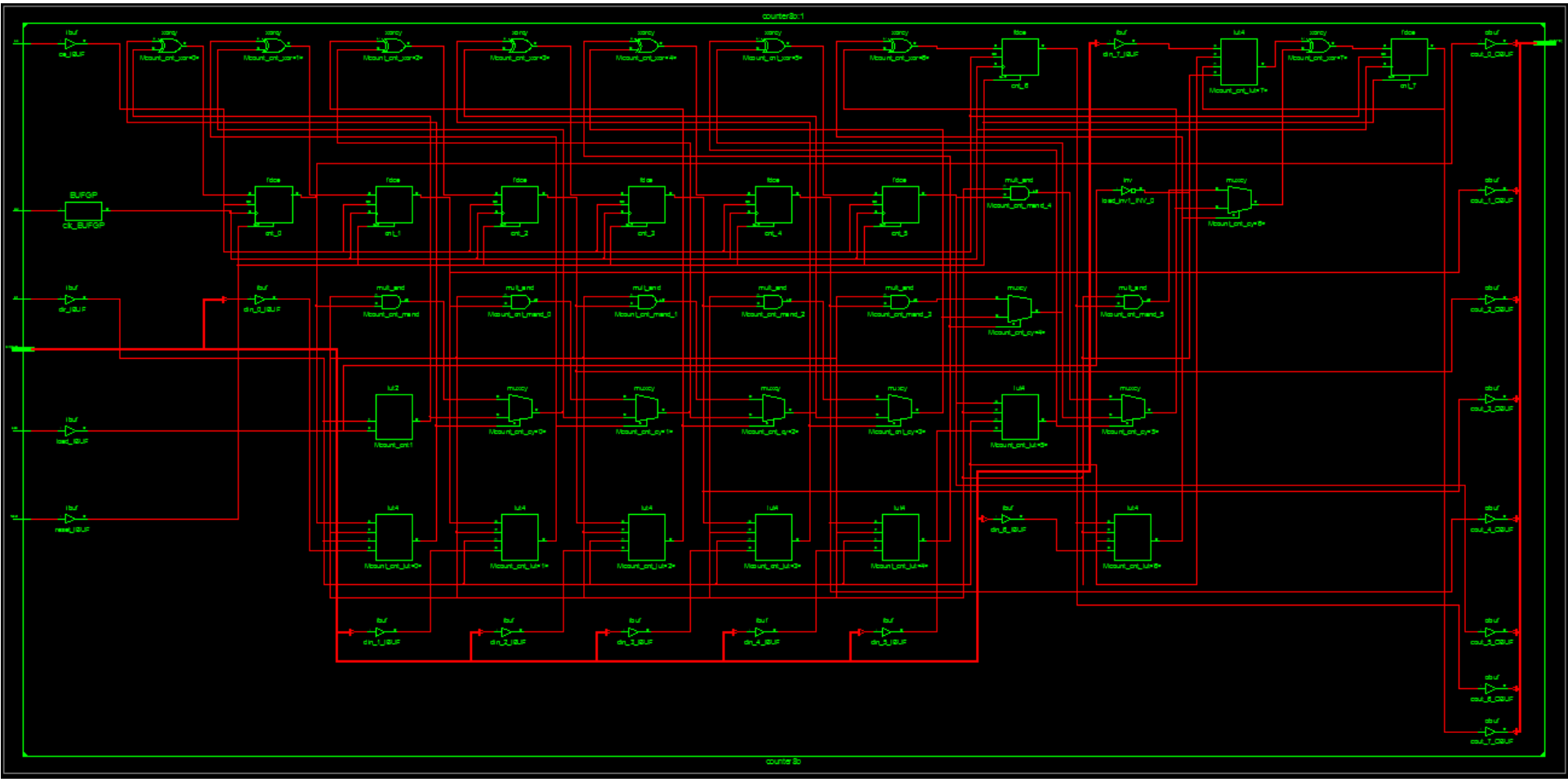
- 双击 View RTL Schematic





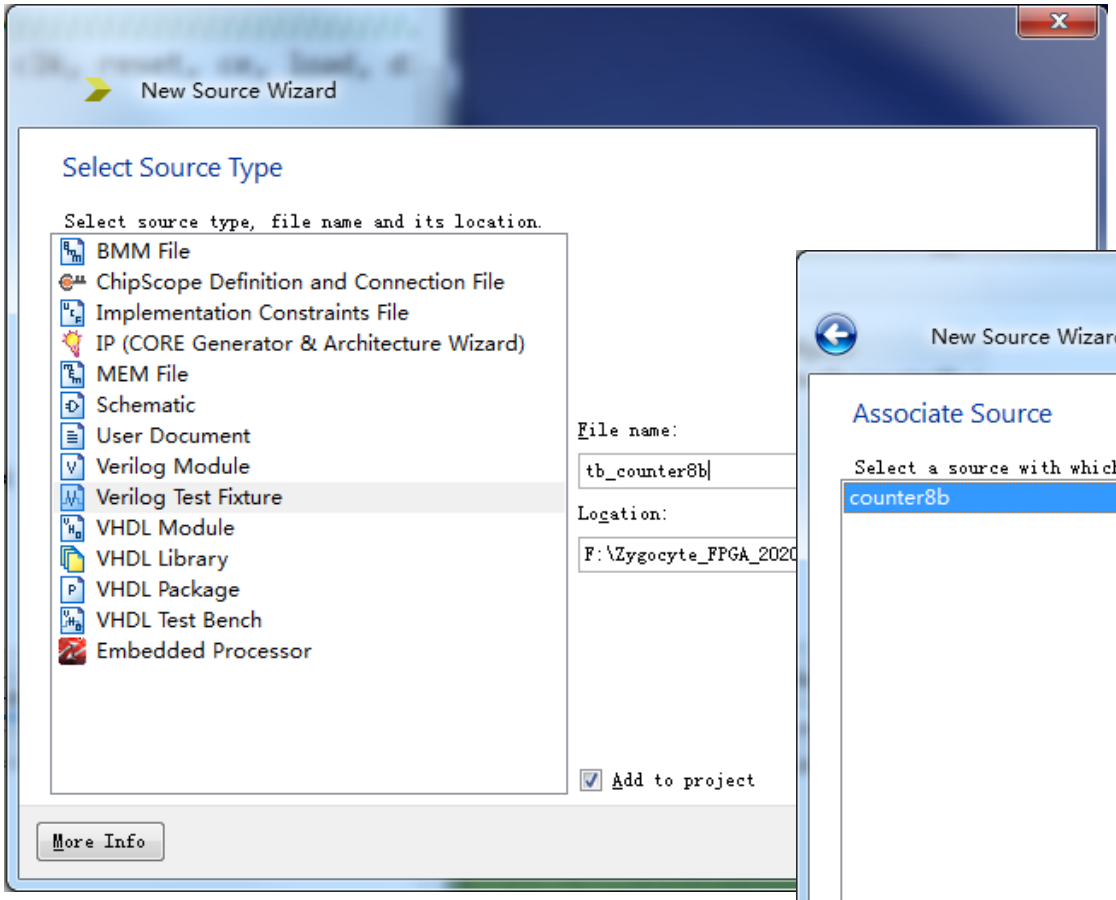
查看工艺原理图

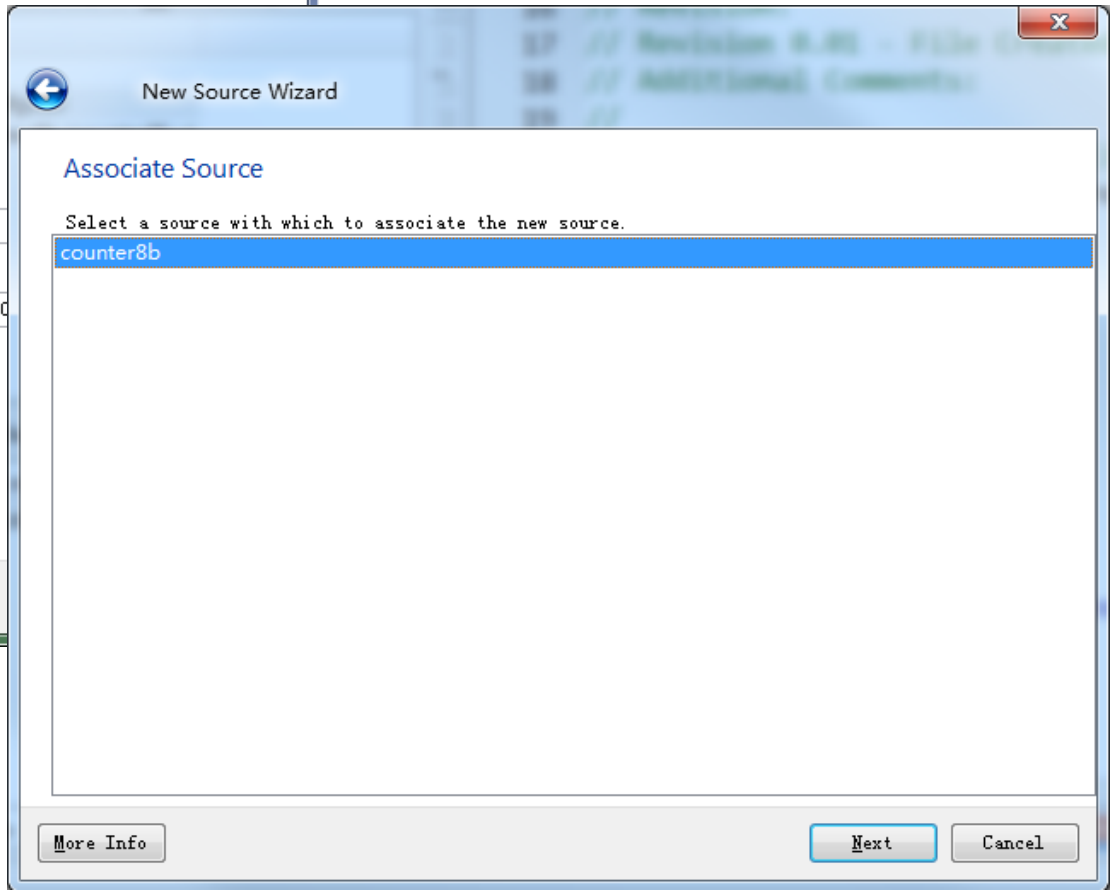
- 双击 View Technology Schematic



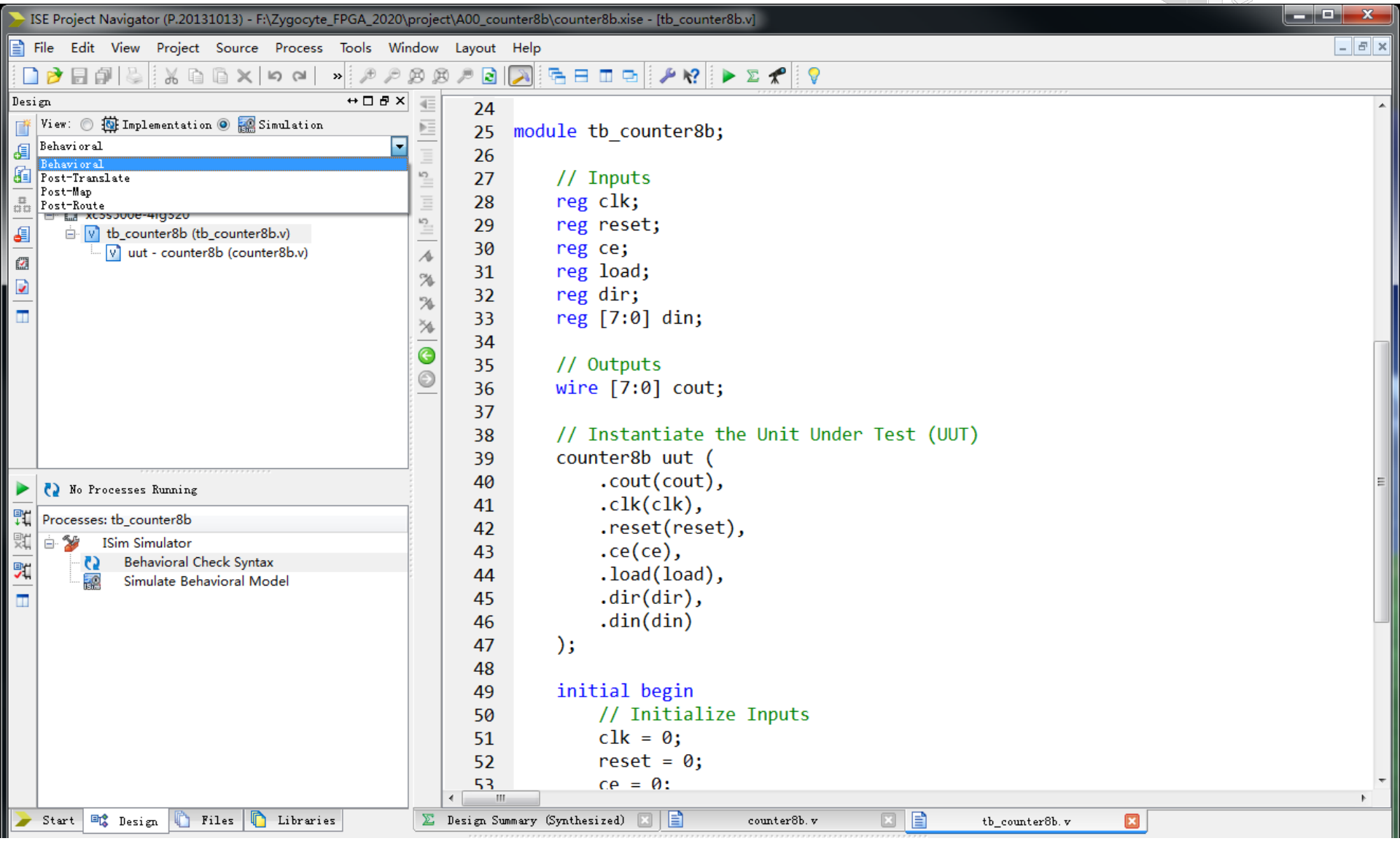
功能仿真

- 创建一个测试矢量波形源文件

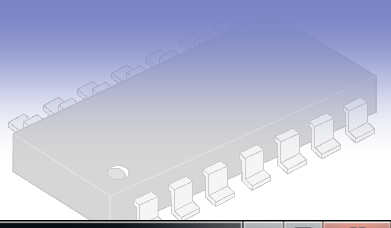




选择行为仿真


ISE Project Navigator (P.20131013) - F:\Zygocyte_FPGA_2020\project\A00_counter8b\counter8b.xise - [tb_counter8b.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Behavioral
Post-Translate
Post-Map
Post-Route
tb_counter8b (tb_counter8b.v)
uut - counter8b (counter8b.v)
No Processes Running
Processes: tb_counter8b
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Start Design Files Libraries
Design Summary (Synthesized)
counter8b.v
tb_counter8b.v
24
25 module tb_counter8b;
26
27 // Inputs
28 reg clk;
29 reg reset;
30 reg ce;
31 reg load;
32 reg dir;
33 reg [7:0] din;
34
35 // Outputs
36 wire [7:0] cout;
37
38 // Instantiate the Unit Under Test (UUT)
39 counter8b uut (
40 .cout(cout),
41 .clk(clk),
42 .reset(reset),
43 .ce(ce),
44 .load(load),
45 .dir(dir),
46 .din(din)
47);
48
49 initial begin
50 // Initialize Inputs
51 clk = 0;
52 reset = 0;
53 ce = 0;

选择行为仿真



ISE Project Navigator (P.20131013) - F:\Zygocyte_FPGA_2020\project\A00_counter8b\counter8b.xise - [tb_counter8b.v]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Behavioral

Hierarchy

- counter8b
- xc3s500e-4fg320
  - tb_counter8b (tb_counter8b.v)
    - uut - counter8b (counter8b.v)

No Processes Running

Processes: tb_counter8b

- ISim Simulator
  - Behavioral Check Syntax
  - Simulate Behavioral Model

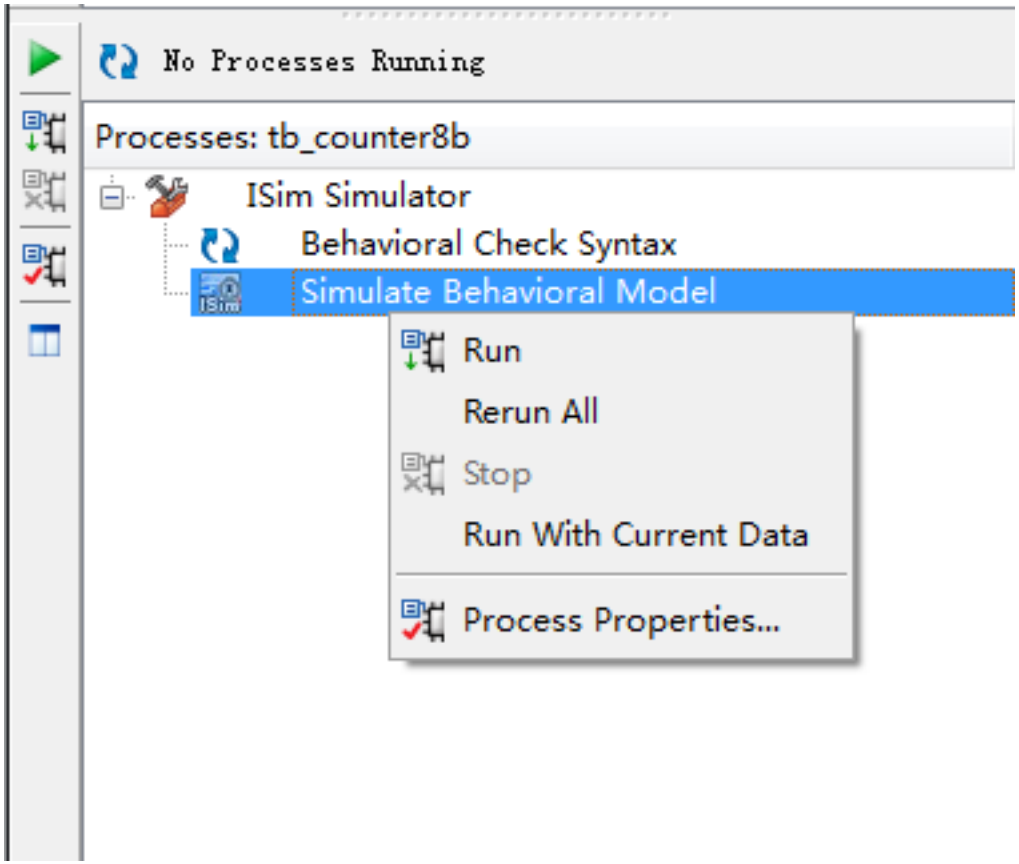
Start | Design | Files | Libraries

Design Summary (Synthesized) | counter8b.v | tb_counter8b.v

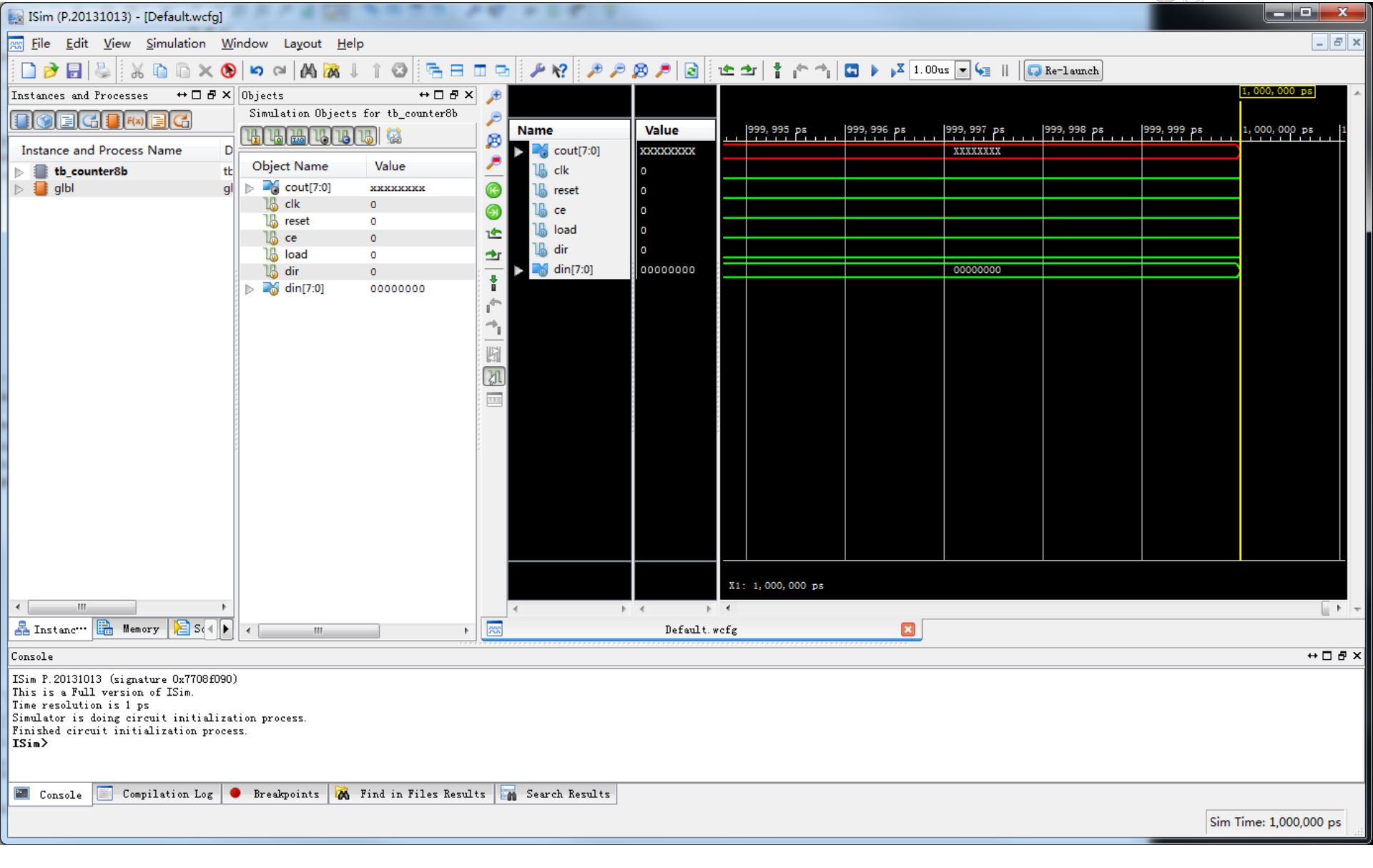
```
24
25  module tb_counter8b;
26
27      // Inputs
28      reg clk;
29      reg reset;
30      reg ce;
31      reg load;
32      reg dir;
33      reg [7:0] din;
34
35      // Outputs
36      wire [7:0] cout;
37
38      // Instantiate the Unit Under Test (UUT)
39      counter8b uut (
40          .cout(cout),
41          .clk(clk),
42          .reset(reset),
43          .ce(ce),
44          .load(load),
45          .dir(dir),
46          .din(din)
47      );
48
49      initial begin
50          // Initialize Inputs
51          clk = 0;
52          reset = 0;
53          ce = 0;
```

获得仿真结果

- 双击 Simulate Behavioral Model



行为仿真结果

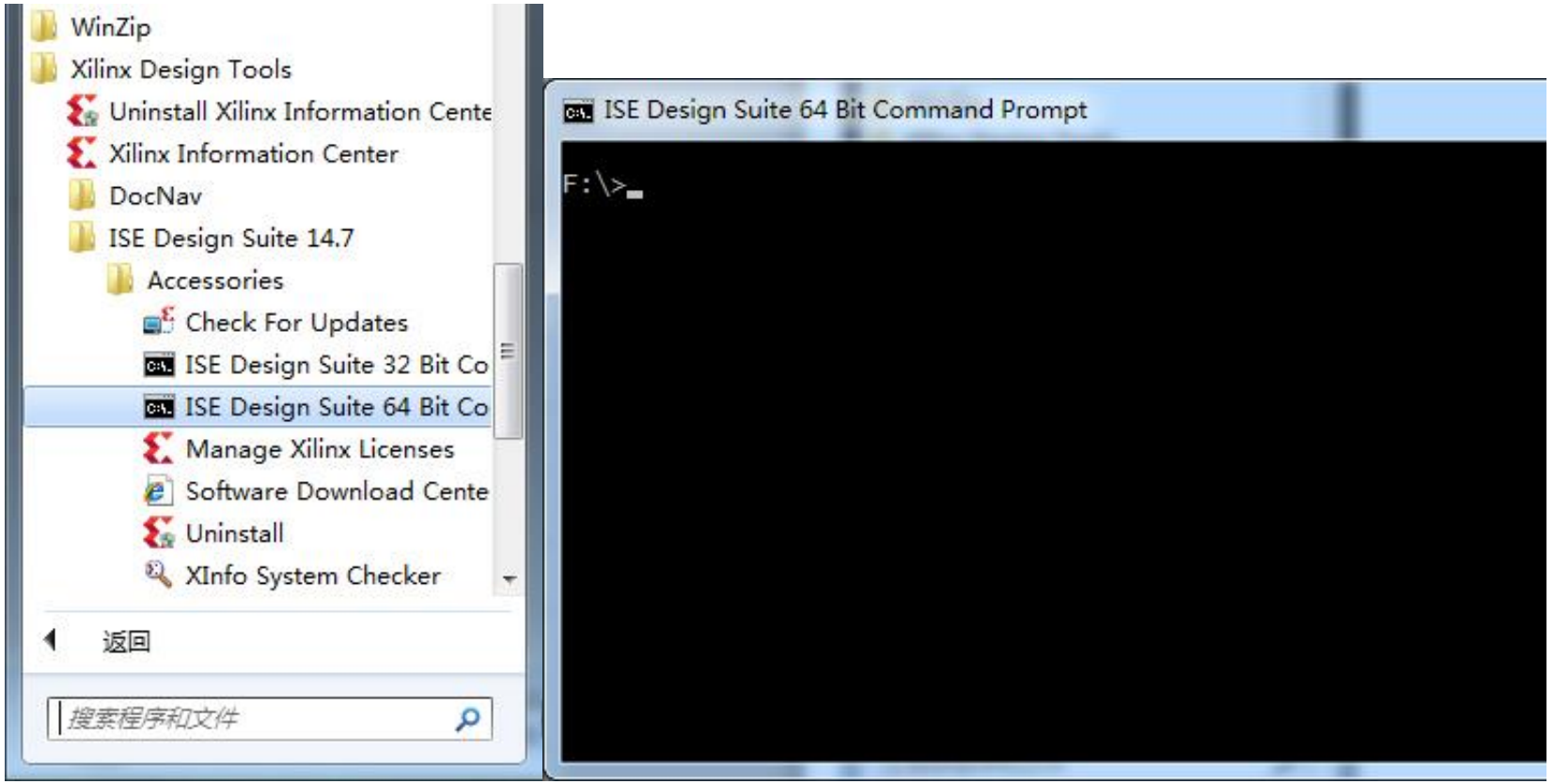

ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
tb_counter8b
glbl
Objects
Simulation Objects for tb_counter8b
Object Name Value
cout[7:0] xxxxxxxx
clk 0
reset 0
ce 0
load 0
dir 0
din[7:0] 00000000
Name
Value
999,995 ps
999,996 ps
999,997 ps
999,998 ps
999,999 ps
1,000,000 ps
X1: 1,000,000 ps
Default.wcfg
Console
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

Xilinx FPGA 综合结果进行仿真（0）

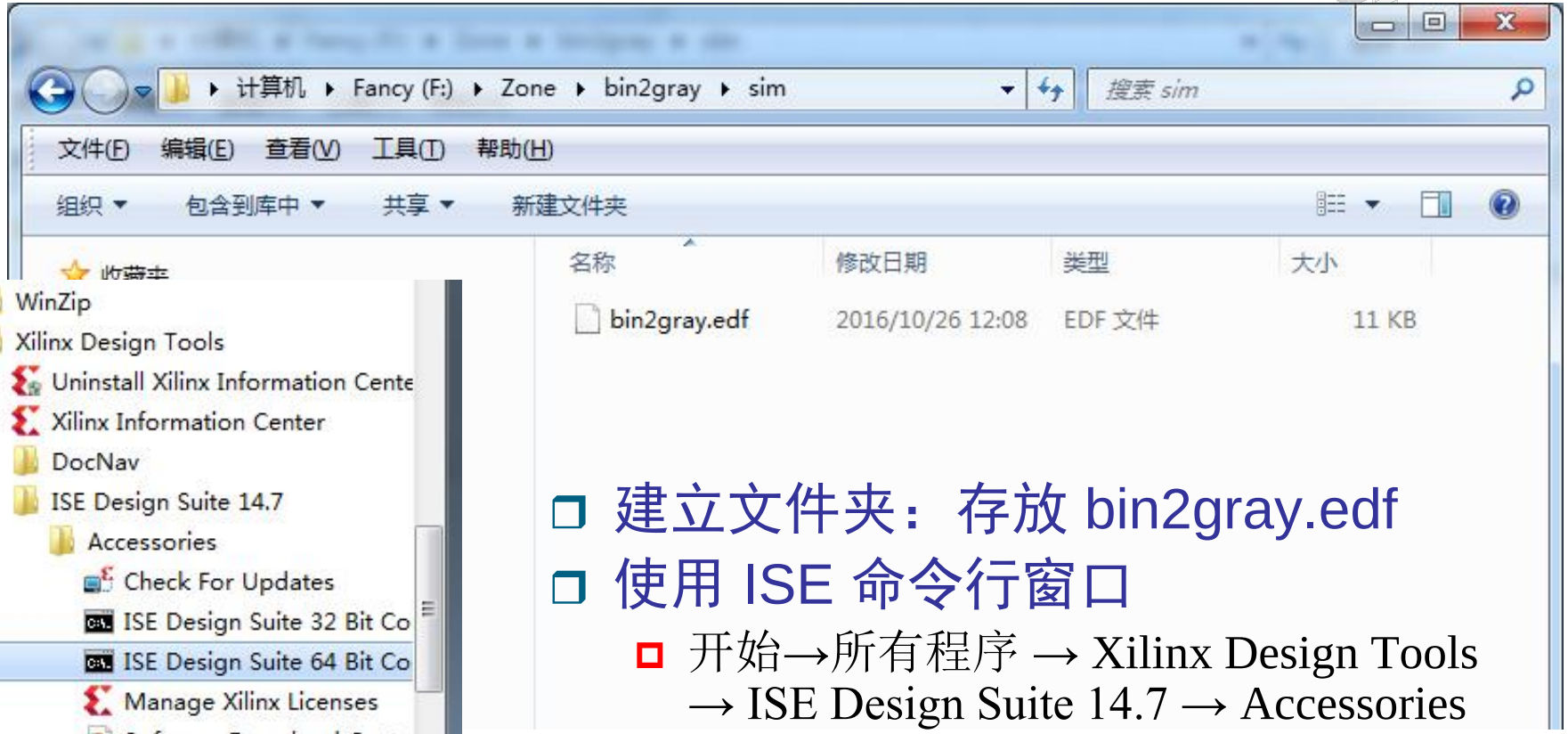
- 安装 Xilinx ISE 设计系统
- 安装与 Xilinx ISE 版本兼容（对应） 的 ModelSim SE
- 使用 ISE 命令行窗口，使用命令编译 Xilinx Simulation Libraries

compxlib -s mti_se -arch all -l all -dir X:\<ModelSim_folder>\xilinx -p X:\<ModelSim_folder>\win64 -w -64bit

————耐心等待约 1 小时



Xilinx FPGA 综合结果进行仿真（1）



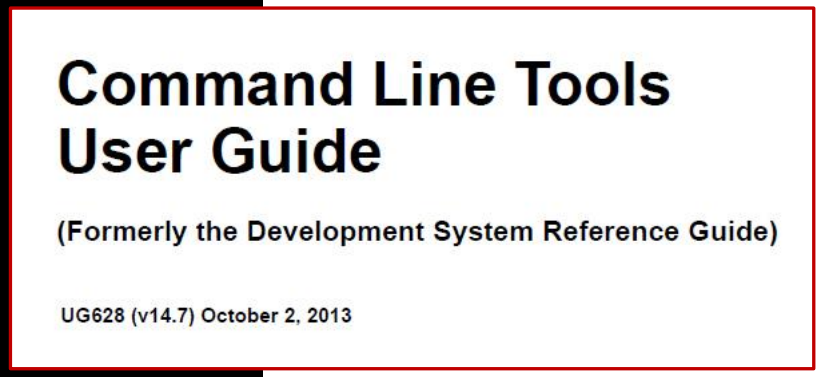
- 建立文件夹：存放 bin2gray.edf
- 使用 ISE 命令行窗口
  - 开始→所有程序 → Xilinx Design Tools → ISE Design Suite 14.7 → Accessories → ISE Design Suite 64 Bit Command Prompt
  - 进入 bin2gray.edf 所在的文件夹

Xilinx FPGA 综合结果进行仿真（2）

- edif 文件转换成 ngc：

```
ngcbuild bin2gray.edf bin2gray.ngc
```

```
ISE Design Suite 64 Bit Command Prompt

F:\>cd F:\Zone\bin2gray\sim

F:\Zone\bin2gray\sim>ngcbuild bin2gray.edf bin2gray.ngc
Release 14.7 - ngcbuild P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.

Command Line: D:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\ngcbuild.exe
bin2gray.edf bin2gray.ngc

Executing edif2ngd -noa "bin2gray.edf" "bin2gray.ngo"
Release 14.7 - edif2ngd P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
INFO:NgdBuild - Release 14.7 edif2ngd P.20131013 (nt64)
INFO:NgdBuild - Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
Writing module to "bin2gray.ngo"...
Reading NGO file "F:/Zone/bin2gray/sim/bin2gray.ngo" ...

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

NGCBUILD Design Results Summary:
  Number of errors:     0
  Number of warnings:   0

Writing NGC file "bin2gray.ngc" ...
Total REAL time to NGCBUILD completion:  7 sec
Total CPU time to NGCBUILD completion:   3 sec

Writing NGCBUILD log file "bin2gray.blc"...

NGCBUILD done.

F:\Zone\bin2gray\sim>
```



Xilinx FPGA 综合结果进行仿真（3）

- ngc文件转换成 Verilog： `netgen -ofmt verilog bin2gray.ngc`


```
ISE Design Suite 64 Bit Command Prompt

F:\Zone\bin2gray\sim>netgen -ofmt verilog bin2gray.ngc
Release 14.7 - netgen P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.

Command Line: netgen -ofmt verilog bin2gray.ngc

Reading design 'bin2gray.ngc' ...
Flattening design ...
Processing design ...
  Preping design's networks ...
  Preping design's macros ...
Writing Verilog netlist file 'bin2gray.v' ...
INFO:NetListWriters:633 - The generated Verilog netlist contains Xilinx UNISIM
   simulation primitives and has to be used with UNISIM simulation library for
   correct compilation and simulation.
Number of warnings: 0
Number of info messages: 1
Total memory usage is 144916 kilobytes

Created netgen log file 'bin2gray.nlf'.

F:\Zone\bin2gray\sim>
```

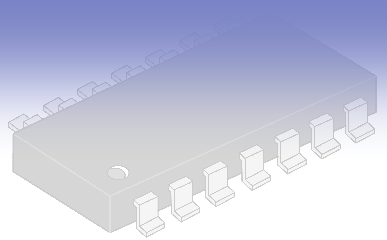
Xilinx FPGA 综合结果进行仿真（4）

- 综合结果网表的 Verilog 功能（行为）模型：bin2gray.v

```
//////////////////////////////////////////////////////////////////////////////
// Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
//////////////////////////////////////////////////////////////////////////////
//   ____  ____
//  /   /\/   /
// /___/  \  /    Vendor: Xilinx
// \   \   \/     Version: P.20131013
//  \   \         Application: netgen
//  /   /         Filename: bin2gray.v
// /___/   /\     Timestamp: Wed Oct 26 14:52:48 2016
// \   \  /  \
//  \___\/\___\
//
// Command  : -ofmt verilog bin2gray.ngc
// Device   : 3s500efg320-4
// Input file   : bin2gray.ngc
// Output file  : bin2gray.v
// # of Modules : 1
// Design Name  : bin2gray
// Xilinx        : D:\Xilinx\14.7\ISE_DS\ISE\
//
// Purpose:
//     This verilog netlist is a verification model and uses simulation
//     primitives which may not represent the true implementation of the
//     device, however the netlist is functionally correct and should not
//     be modified. This file cannot be synthesized and should only be used
//     with supported simulation tools.
//
// Reference:
//     Command Line Tools User Guide, Chapter 23 and Synthesis and Simulation Design Guide, Chapter 6
//
//////////////////////////////////////////////////////////////////////////////

`timescale 1 ns/1 ps

module bin2gray (
gray_val, bin_val
);
  output [7 : 0] gray_val;
  input [7 : 0] bin_val;
  wire [0 : 0] gray_val_2;
  wire [1 : 1] gray_val_3;
  wire [2 : 2] gray_val_4;
  wire [3 : 3] gray_val_5;
  wire [4 : 4] gray_val_6;
  wire [5 : 5] gray_val_7;
  wire [6 : 6] gray_val_8;
  wire [7 : 0] bin_val_c;
```

```
LUT2 #(
  .INIT ( 4'h6 ))
\gray_val_2[0]  (
  .I0(bin_val_c[0]),
  .I1(bin_val_c[1]),
  .O(gray_val_2[0])
);
LUT2 #(
  .INIT ( 4'h6 ))
\gray_val_3[1]  (
  .I0(bin_val_c[1]),
  .I1(bin_val_c[2]),
  .O(gray_val_3[1])
);
```

Xilinx FPGA 综合结果进行仿真（5）

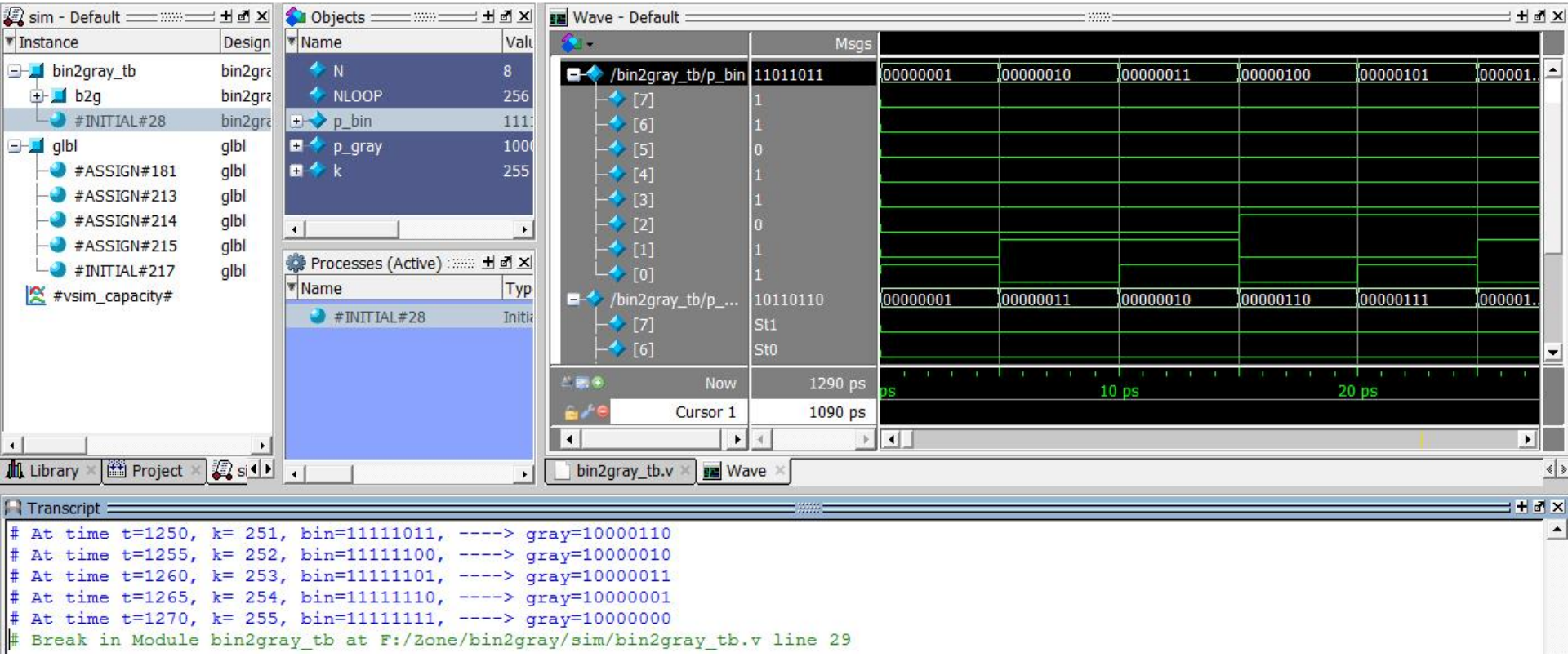


- 建立用于仿真的文件夹：X:\bin2gray\sim
  - 存放综合结果功能模型 Verilog 文件和测试台顶层文件：
    - bin2gray.v　　// 综合结果网表的 Verilog 功能（行为）模型
    - bin2gray_tb.v
- 启动ModelSim，在此文件夹中建立工程： bin2gray
  - 将上面的Verilog文件添加进工程
  - 编译 Verilog 文件
- 启动仿真：
  - 在 Transcrip 窗口执行命令：

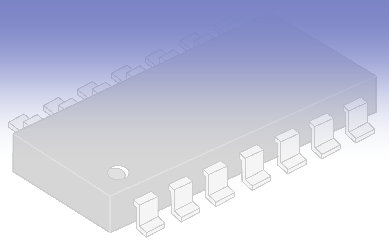
```
vsim -novopt -t ps -L unisims_ver -L xilinxcorelib_ver work.bin2gray_tb work.glbl
```

Xilinx FPGA 综合结果进行仿真（6）

- 综合结果的仿真结果



小结



- 数字系统设计的目标
  - 使用HDL，利用IP核
- 使用HDL
  - 将数字系统分层次进行设计
  - 两种方法相结合
    - 自顶向下
    - 自底向上