COSS HW-03 Solution Key

1. In direct mapped - main memory is 16 GB, cache with block size 4 KB and 10 bits in the tag. The tag directory size would be?

Answer:

Size of main memory = 16 GB = 2^{34} bytes

Number of bits in physical address = 34 bits

Number of bits in line number

= Number of bits in physical address – (Number of bits in tag + Number of bits in block offset)

= 12 bits

Total number of lines in cache = 2^{12} lines

Tag directory size = Number of tags x Tag size

= Number of lines in cache x Number of bits in tag

= 2^{12} x 10 bits

= 5120 bytes

2. Consider a direct mapped cache having 512 cache lines machine with a byte addressable main memory of 2^{32} bytes divided into blocks of size 32 bytes. The size of the tag field in bits would be?

Answer:

Size of main memory= 2^{32} bytes

Number of bits in physical address = 32 bits

Block size = 32 bytes = 2^{5} bytes

Number of bits in block offset = 5 bits

Total number of lines in cache = 512 lines = 2^{9} lines

Number of bits in line number = 9 bits

No of bits in tag = No of bits in physical address – (No of bits in line number + Nor of bits in block offset)

= 18 bits

3. In 8-way set associative mapped cache of size 512 KB with block size 1 KB & 7 bits in the tag. The size of main memory would be

Answer:

Block size = 1 KB = 2^{10} bytes

Number of bits in block offset = 10 bits

Total number of lines in cache = Cache size / Line size
= 512 KB / 1 KB = 512 lines

Total number of sets in cache = Total number of lines in cache / Set size
= 512 / 8 = 64 sets = 2^6 sets
Number of bits in set number = 6 bits

No of bits in physical address = No of bits in tag + No of bits in set number + No of bits in block offset
= 23 bits
Size of main memory = 2^{23} bytes **= 8 MB**

4. The size of main memory is 64 MB and 10 bits in the tag of a 4-way set associative mapped cache, the size of cache memory would be
Answer:
Size of main memory = 64 MB = 2^{26} bytes
Number of bits in physical address = 26 bits

Let Number of bits in set number field = x bits , Number of bits in block offset field = y bits

No of bits in physical address = No of bits in tag + No of bits in set number + No of bits in block offset
26 bits = 10 bits + x bits + y bits
x + y = 16
Sum of number of bits of set number field and block offset field = 16 bits

Cache memory size = Number of sets in cache x Number of lines in one set x Line size
= 2^x x 4 x 2^y bytes = 2^{2+x+y} bytes = 2^{2+16} bytes = 2^{18} bytes = **256 KB**

5. Cache access time is 100 ns & Memory access time is 500 ns. If the effective access time is 10% greater than the cache access time, hit ratio would be
Answer:
cache access time=100 ns memory access time=500 ns Effective Access Time=110
Effective Access Time =cache hit ratio*cache access time+ cache miss ratio *(cache access time +main memory access time)
110 = h*100ns +(1-h) (100+500)
110= 100h+600-600h
500h= 490
h= 490/500= .98 = **98%**

6) Consider a direct mapped cache of size 64 KB with block size 512 bytes. The size of main memory is 512 KB. Find Number of bits in tag.

Answer:

Number of Bits in Physical Address-

Size of main memory = 512 KB

= 2^19 bytes

Thus, Number of bits in physical address = 19 bits.

We have, Block size = 512 bytes

= 2^9 bytes

Thus, Number of bits in block offset = 9 bits.

Total number of lines in cache

= Cache size / Line size = 64 KB / 512 bytes

= 2^16 bytes / 2^9 bytes

= 2^7 lines

Thus, Number of bits in line number = 7 bits

Number of bits in tag

= Number of bits in physical address – (Number of bits in line number + Number of bits in block offset)

= 19 bits – (7 bits + 9 bits)

Thus, Number of bits in tag = 3 bits

= 17 bits – 14 bits

= 3 bits

Thus, Number of bits in tag = **3 bits**

7) Consider a direct mapped cache of size 256 KB with block size 512 Bytes. There are 7 bits in the tag. Find the size of main memory.

Answer:

Block size

= 512

= 2^9 bytes

Thus, Number of bits in block offset = 9 bits

Total number of lines in cache

= Cache size / Line size

= 256 KB / 512

= 2^9 lines

Thus, Number of bits in line number = 9 bits

Number of bits in physical address

= Number of bits in tag + Number of bits in line number + Number of bits in block offset

= 7 bits + 9 bits + 9 bits

= 25 bits

Thus, Number of bits in physical address = 25 bits

Thus, Size of main memory

= 2^{25} bytes

= 32 MB

8) Consider a fully associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.

Answer:

Size of main memory

= 128 KB

= 2^{17} bytes

Thus, Number of bits in physical address = 17 bits

Block size

= 256 bytes

= 2^8 bytes

Thus, Number of bits in block offset = 8 bits

Number of bits in tag

= Number of bits in physical address – Number of bits in block offset

= 17 bits – 8 bits

= 9 bits

Thus, Number of bits in tag = **9 bits**

9) Consider a fully associative mapped cache of size 4 MB with block size 4 KB. There are 17 bits in the tag. Find Size of main memory and tag size.

Answer:

Block size

= 4 KB

= 2^{12} bytes

Thus, Number of bits in block offset = 12 bits

Number of bits in physical address

= Number of bits in tag + Number of bits in block offset

= 17 bits + 12 bits

= 29 bits

Number of bits in physical address = 29 bits

Thus, Size of main memory

= 2^{29} bytes

= 512 MB

10) A cache has an access time of 0.2 microseconds with memory access time of 3 microsecond. If the cache miss ratio is 25%, what is the average access time for a memory reference?

Answer:

Avg access time = Hit ratio * cache access time + miss ratio * (Cache access time + MM access time)

= (0.6 * 4) + 0.4 * (4 + 30)

= 2.4 + 13.6

=16 usec.

11. The memory access time is 2 nanosecond for a read operation with a hit in cache, 7 nanoseconds for a read operation with a miss in cache, 4 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache.

Execution of a sequence of instructions involves 160 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9.

The average memory access time (in nanoseconds) in executing the sequence of instructions is __________.

Answer:
Time taken for 60 read operations = 160*((0.9*2)+(0.1*7))

= 400 ns

Time taken for 40 write operations = 40*((0.9*4)+(0.1*10))

= 184 ns

Total time taken for 200 operations is = 400 + 184 = 584 ns

Average time taken = time taken per operation = 584/200 ns

= 2.92 ns

12. The main memory is structured into modules each with its own address register called ______

Answer:
Key: ABR stands for Address Buffer Register.

13. The number successful accesses to memory stated as a fraction is called as _____

Answer:
Key: The hit rate is an important factor in performance measurement.

14. 16K Bytes of main memory, How many address bits are required?

Answer:

Key: 16K = 2^4 * 2^10 = 2^14 Therefore 14 address bits are required

15. Convert Hexa A201 to Binary

Answer:

Key: Hex A = Binary 1010, Hex A = Binary 0010, Hex   = Binary 0000, Hex 1 = Binary 0001

Hexa A201 = Binary 1010 0010 0000 0001