Computer Organization and Software Systems

Session 16

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Problems

Problem 1

Consider a cache performance on a machine with a 1024-byte direct-mapped data cache with 16-byte blocks .Determine the cache performance for the following code(Assume sizeof (int) = 4, also initially cache is empty)

```
struct cache1
{
  int x;
  int y;
};
```

```
struct cache1 co[4][4];
void main()
{
int total_x = 0, total_y = 0;
int i, j;
for (i = 0; i < 4; i++)
{
      for (j = 0; j < 4; j++) {
            total_x += co[j][i].x;
            total_y += co[j][i].y;
}}}
```

a. What is the total number of reads?

[Sol:4*4*2= 32 Reads]

b .What is the total number of reads that miss in the cache?

[Sol: 16 Misses]

c. What is the miss rate?

[Sol: 16/32=> 50% Miss Rate]

d. What would the miss rate be if the cache were twice as big?

[Increasing the cache size by any amount would not change the miss rate, since cold misses are unavoidable.]

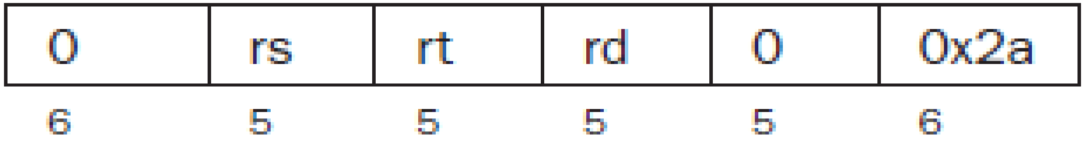
Problem 2

Regs

Write down the machine code (i,e Binary Code) for the following MIPS Instruction

slt $t3, $s3,$s7

represent your answer in hexadecimal



0	rs	rt	rd	0	0x2a
6	5	5	5	5	6

rs: $s3=> 19 ➔ 10011

rt: $s7=> 23 ➔ 10111

rd: $t3=> 11➔ 01011

000000 10011 10111 01011 00000 101010

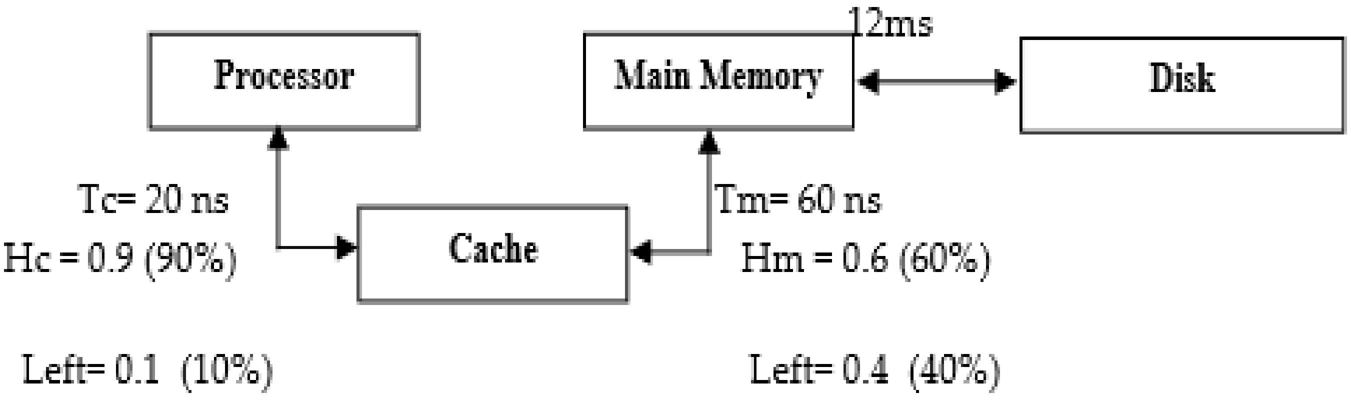
0000 0010 0111 0111 0101 1000 0010 1010

0 2 7 7 5 8 2 A

Problem 3

A computer has a cache, main memory, and a disk used for virtual memory. If a referenced word is in the cache, 20 ns are required to access it. If it is in main memory but not in the cache, 60 ns are needed to load it into the cache and then the reference is started again.

If the word is not in main memory, 12 ms are required to fetch the word from disk, followed by 60 ns to copy it to the cache, and then the reference is started again. The cache hit ratio is 0.9(90%) and the main memory hit ratio is 0.6 (60%). What is the average time in ns required to access a referenced word on this system?



Processor

Main Memory

12ms

Disk

Cache

Tc= 20 ns

Hc = 0.9 (90%)

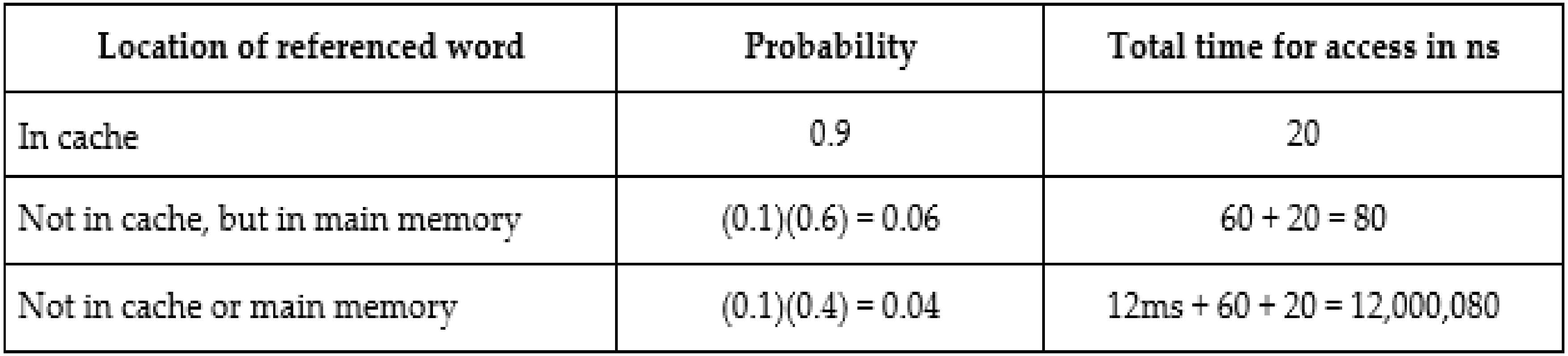
Tm= 60 ns

Hm = 0.6 (60%)

Left= 0.1 (10%)

Left= 0.4 (40%)

There are three cases to consider:

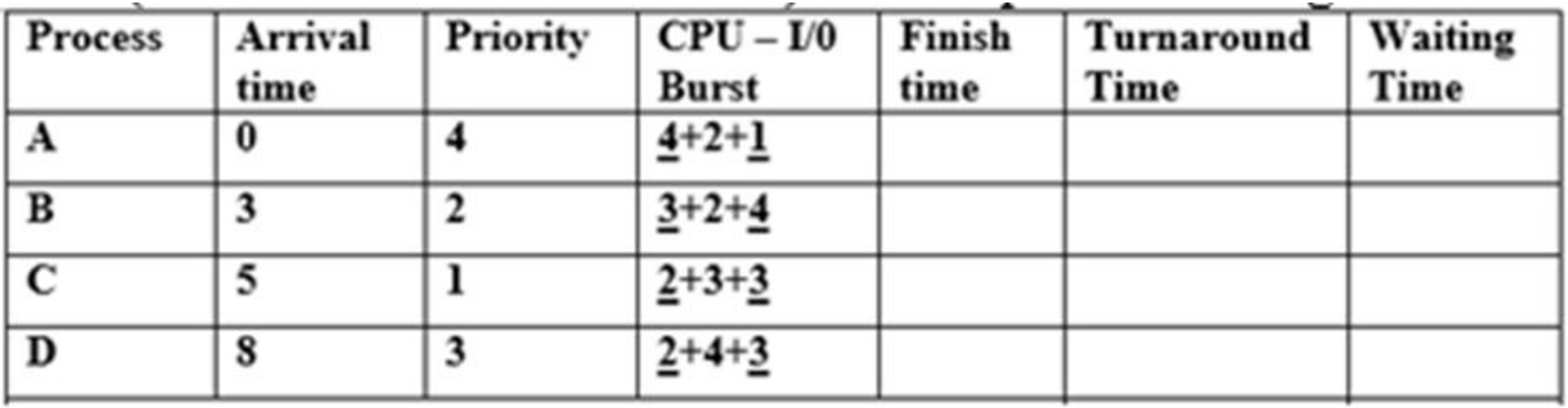


Location of referenced word	Probability	Total time for access in ns
In cache	0.9	20
Not in cache, but in main memory	(0.1)(0.6) = 0.06	60 + 20 = 80
Not in cache or main memory	(0.1)(0.4) = 0.04	12ms + 60 + 20 = 12,000,080

So, the average access time would be:

Avg = (0.9) (20) + (0.06) (80) + (0.04) (12000080) = 480026 ns = 480 usec

Problem 5 (Priority - pre-emptive)



Process	Arrival time	Priority	CPU – I/0 Burst	Finish time	Turnaround Time	Waiting Time
A	0	4	4+2+1			
B	3	2	3+2+4			
C	5	1	2+3+3			
D	8	3	2+4+3			

Problem 6

State whether the following statements are **True** or **False** with proper justification. Answers without proper justification will not be given any marks.

a) DMA to main memory is given higher priority than CPU access to main memory.

b) Temporal coherence suggests the use of LRU (Lease Recently Used) replacement policy for cache memory.

Problem 7

A byte addressable computer has on-chip data cache with eight lines (L0 to L7). Each cache line is capable of storing 4 bytes. The mapping function used is direct mapped. Following address sequence is generated by the CPU (hex notation) during the program execution :

212, 215, 236, 231, 2F5

a) Identify the main memory block number and line number to which each address corresponds to.

b) Show the contents of the cache memory when the pattern is repeated two times,

c) The access time of the cache is 5ns, and it has an 80 percent hit rate. The access time of the main memory is 100 ns. What is the average access time of the hierarchy?

Problem 7 Cont.

A byte addressable computer has on-chip data cache with eight lines (L0 to L7). Each cache line is capable of storing 4 bytes. The mapping function used is direct mapped. Following address sequence is generated by the CPU (hex notation) during the program execution :

212, 215, 236, 231, 2F5

a) Identify the main memory block number and line number to which each address corresponds to.

212H	**Block 132D line 4**
215H	**Block 133D line 5**
236H	**Block 141D line 5**
231H	**Block 140D line 4**
2f5H	**Block 189D line 5**

Problem 7 Cont.

A byte addressable computer has on-chip data cache with eight lines (L0 to L7). Each cache line is capable of storing 4 bytes. The mapping function used is direct mapped. Following address sequence is generated by the CPU (hex notation) during the program execution :

212, 215, 236, 231, 2F5

b) Show the contents of the cache memory when the pattern is repeated two times,

Line 0 -xxx

Line 1 – xxx

Line 2 -xxx

Line 3 - xxx

Line 4 -140D

Line 5 - 189D

Line 6 -xxx

Line 7 - xxx

Problem 7 Cont.

A byte addressable computer has on-chip data cache with eight lines (L0 to L7). Each cache line is capable of storing 4 bytes. The mapping function used is direct mapped. Following address sequence is generated by the CPU (hex notation) during the program execution :

212, 215, 236, 231, 2F5

c) The access time of the cache is 5ns, and it has an 80 percent hit rate. The access time of the main memory is 100 ns. What is the average access time of the hierarchy?

Average Access Time: 0.8x5ns + 0.2 [5 +100] = 25 ns

Problem 8

Consider a 6 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, and I3 in stages FI, DI, FO, DO, EI, WB is shown below

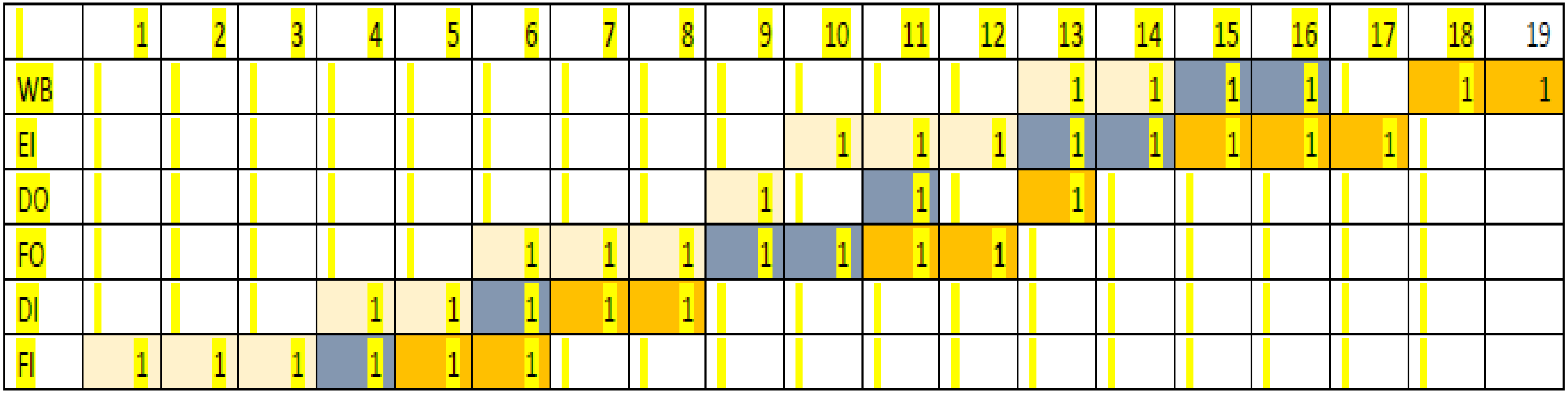
	FI	DI	FO	DO	EI	WB
I1	3	2	3	1	3	2
I2	1	1	2	1	2	3
I3	2	2	2	1	3	2

a) Draw the Time Space diagram for this pipeline with Time(Tx) on the X-axis and Instructions (Iy) on Y axis or vice versa.

b) If pipelined, How many Time cycles will be taken for executing these instructions

c) If non-pipelined, how many time cycles would be needed to execute the instructions?

Solution



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
WB													1	1	1	1		1	1
EI										1	1	1	1	1	1	1	1		
DO									1		1		1						
FO						1	1	1	1	1	1	1							
DI				1	1	1	1	1											
FI	1	1	1	1	1	1													

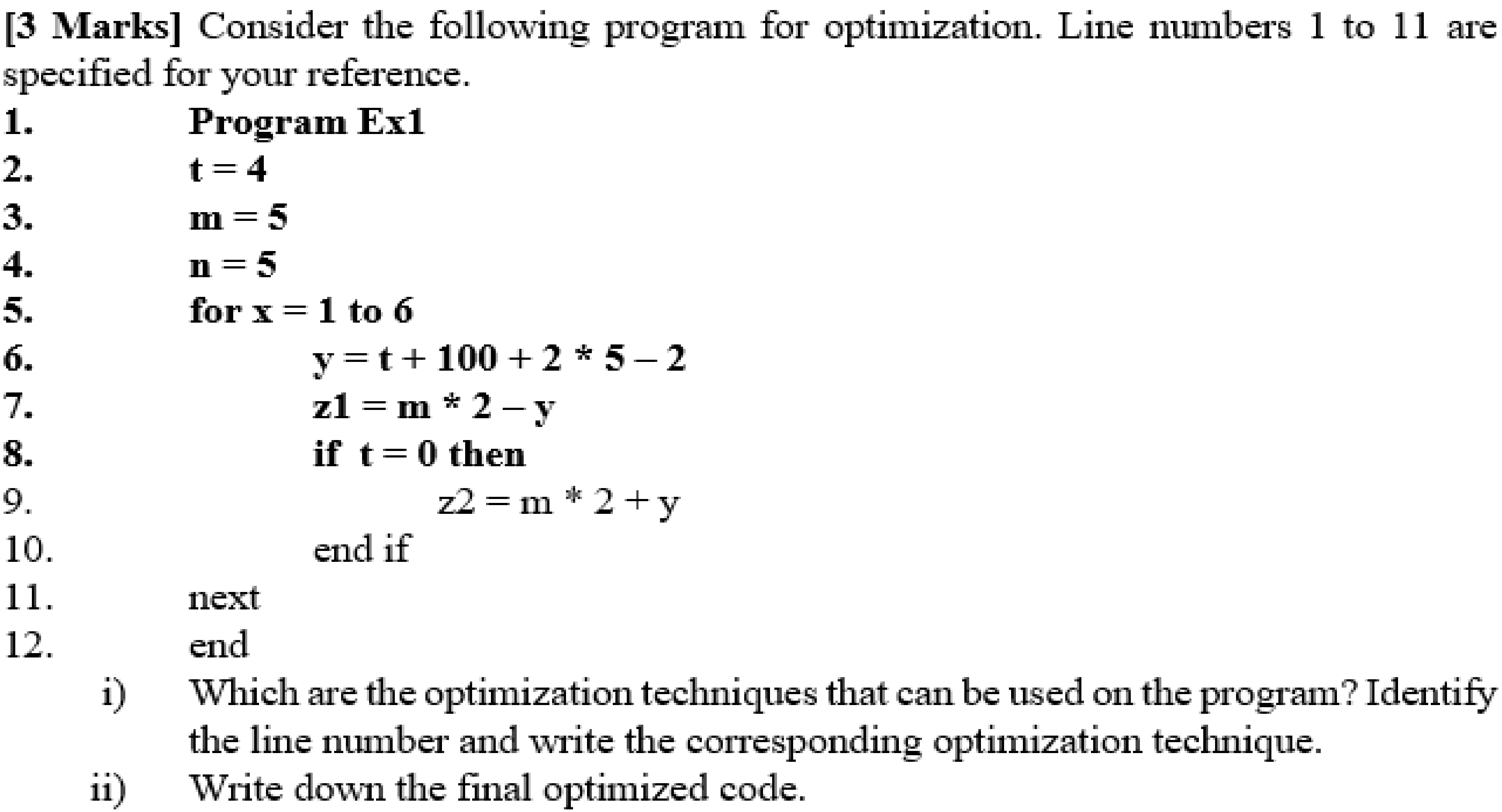
Ans

(a) time space diagram (next page) – it can be transposed as well; x and y axis can change their places

(b) pipelined – 19 cycles

(c) non pipelined - 36 cycles;

Problem 10



[3 Marks] Consider the following program for optimization. Line numbers 1 to 11 are specified for your reference.

```
1.      Program Ex1
2.      t = 4
3.      m = 5
4.      n = 5
5.      for x = 1 to 6
6.          y = t + 100 + 2 * 5 – 2
7.          z1 = m * 2 – y
8.          if  t = 0 then
9.              z2 = m * 2 + y
10.         end if
11.     next
12.     end
```

i) Which are the optimization techniques that can be used on the program? Identify the line number and write the corresponding optimization technique.

ii) Write down the final optimized code.

Solution

Line number 4 :Dead code Elimination n=5 where n is not used in the program
Line number 8 to 10 : Unreachable code because t is a global variable assigned with the value 4 so it cannot be 0
Line number 7: Strength Reduction replace m*2 by m + m
Line number 6: Compile time evaluation and the final optimized instruction is
y = t + 108

Final Contact Session 16 done!!!

Start Preparations for the Compre exam
ReadText/Reference books –refer ppts
BoL and ATB

&

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Use CHAT Window

Bye COSS2021-2 Sec2 Students

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General-Purpose Register Usage Conventionback

back

Register name	Number	Intended usage
Zero	0	Constant 0
at	1	Reserved for assembler
v0,v1	2,3	Values for function results and Exp evaluation
a0,a1,a2,a3	4-7	Arguments 1-4
t0-t7	8-15	Temporary (not preserved across call)
s0-s7	16-23	Saved temporary(preserved across call)
t8,t9	24,25	Temporary (not preserved across call)
k0,k1	26,27	Reserved for OS kernel
gp	28	Pointer to Global area
sp	29	Stack Pointer
fp	30	Frame pointer(if needed);Otherwise, a saved register $s8
ra	31	Return address(used by a procedure call)