Computer Organization and Software Systems

Session 7+

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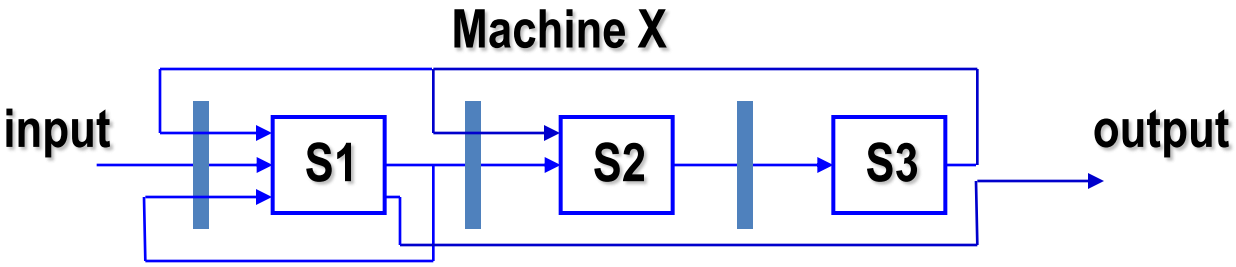
Static and Dynamic pipelining

- Based on the configuration i.e. the interconnection pattern between its stages
- A static pipeline assumes only one functional configuration at a time
- Useful when instructions of the same type can be streamed for execution

Reservation Table



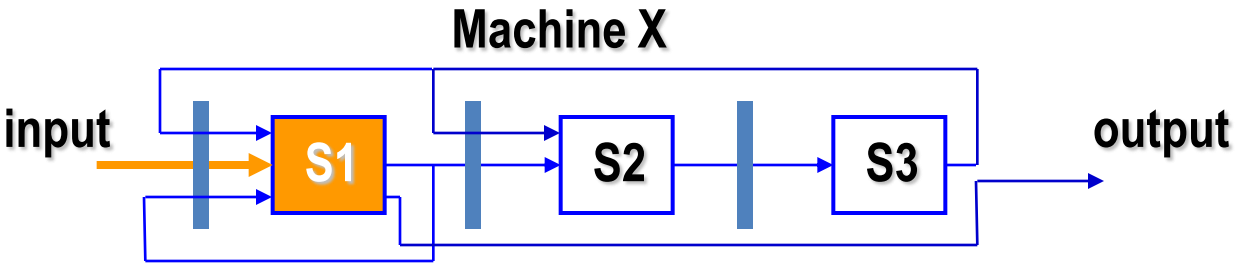
Reservation Table

Time →

Stage ↓

	0	1	2	3	4	5	6	7
S1	X	X					X	X
S2			X		X			
S3				X		X		

Reservation Table



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S3				X		X		

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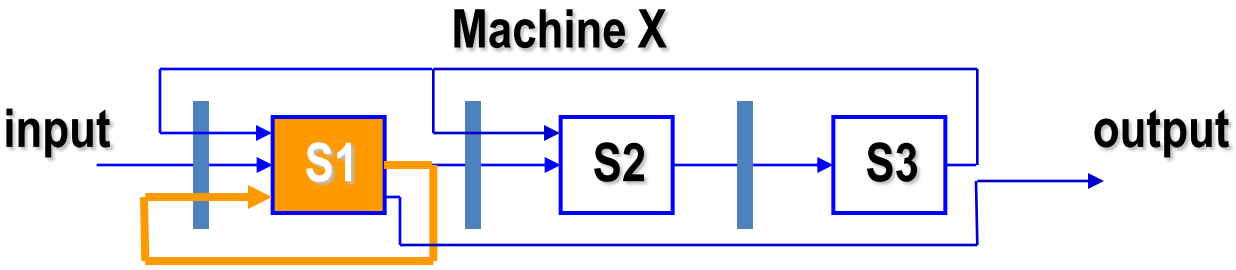

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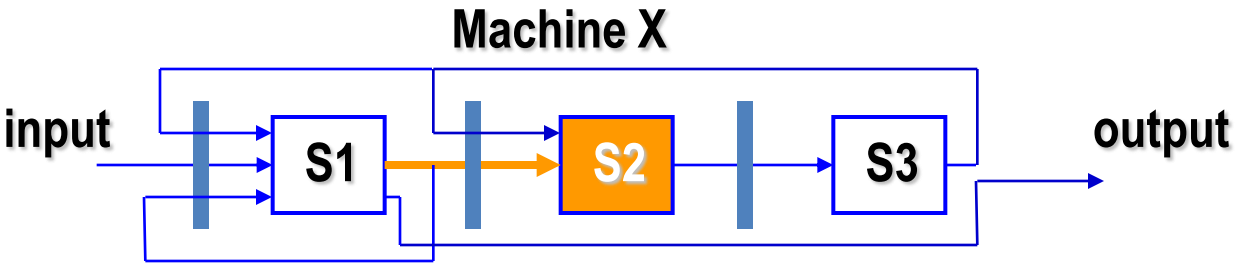

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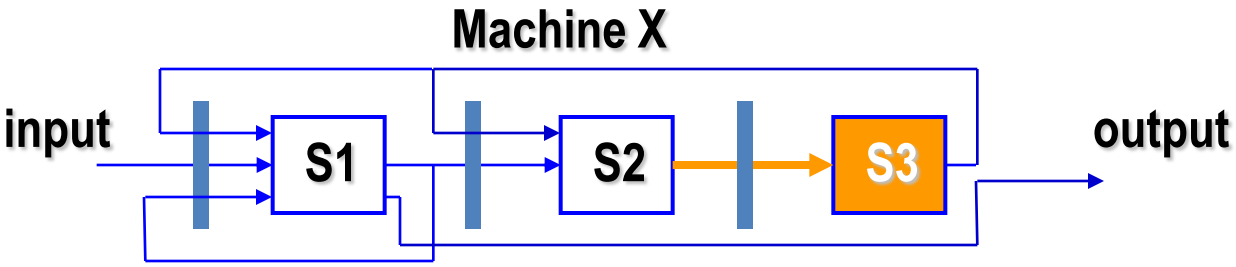

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Time →

Stage ↓

	0	1	2	3	4	5	6	7
S1	X	X					X	X
S2			X		X			
S3				X		X		

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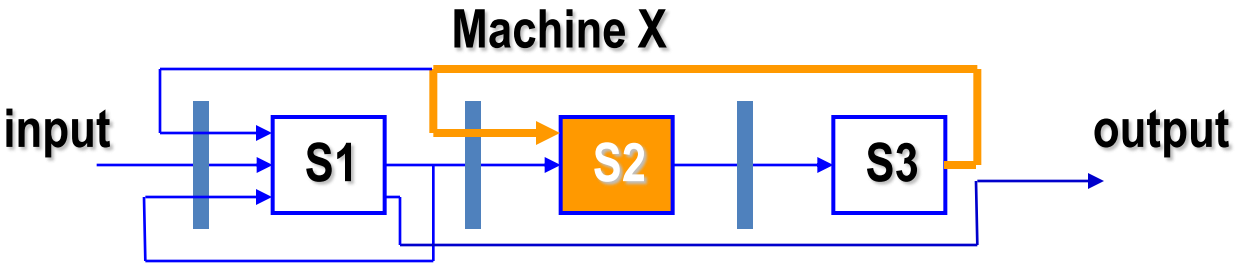

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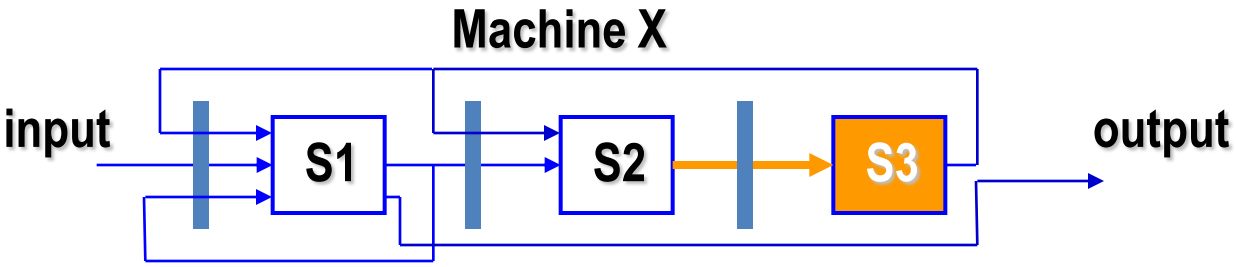
S1	X	X					X	X
S2			X		X			
S3				X		X		

Reservation Table



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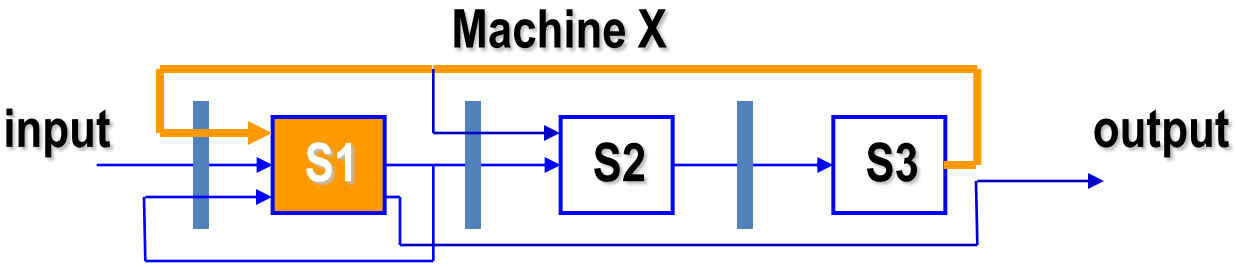

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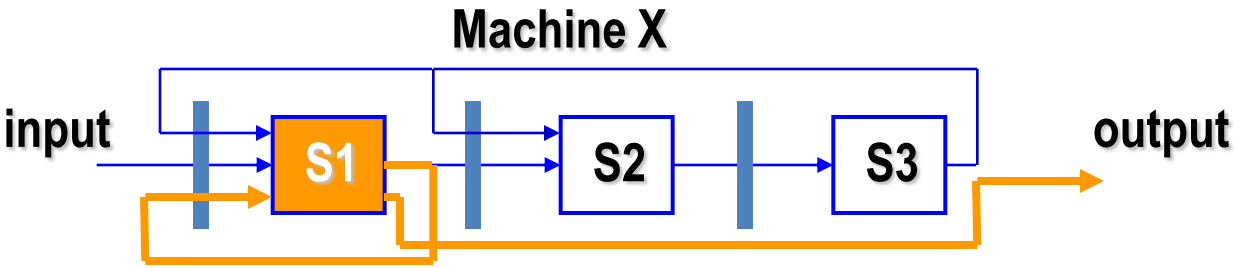

Reservation Table

Time →

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	0	1	2	3	4	5	6	7
S1	X	X					X	X
S2			X		X			
S3				X		X		

Static and Dynamic pipelining

- Dynamic pipeline allows more frequent changes in its configuration
- Require more elaborate sequencing and control mechanisms

Scalar and Vector pipelining

- Based on the operand types or instruction type
- Scalar pipeline processes scalar operands
- Vector pipeline operate on vector data and instructions.

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Important Terms

Clock period: τ

τ_i: time delay of S_i stage

τ_L: time delay of latch

$$\tau = \max\{\tau_i\} + \tau_L$$

Pipeline processor frequency $f = 1/\tau$

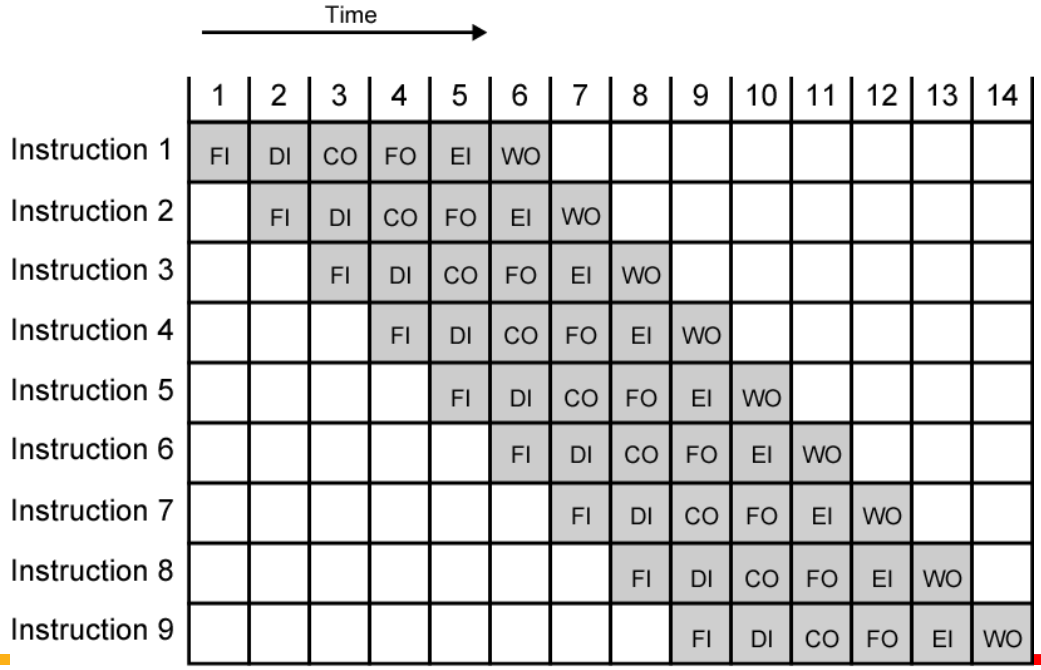
Important Terms

Time taken to complete n tasks by k stage pipeline is

$$T_k = [k + (n-1)]\tau$$

Time taken by the nonpipelined processor

?



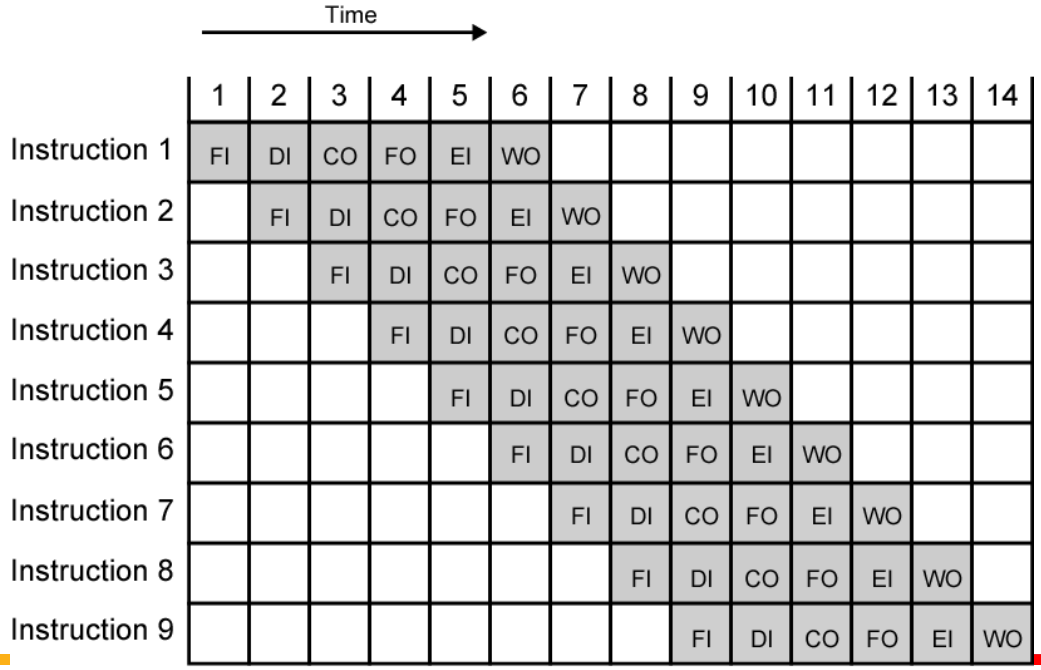
Important Terms

Time taken to complete n tasks by k stage pipeline is

$$T_k = [k + (n-1)]\tau$$

Time taken by the nonpipelined processor

$$T_1 = k^* n^* \tau$$



Important Terms

Speedup: speedup of a k-stage linear-pipeline over an equivalent non pipelined processor

$$S_k = \frac{T_1}{T_k}$$

$$= \frac{n*k*\tau}{[k+(n-1)]\tau}$$

$$= \frac{n*k}{[k+(n-1)]}$$

Important Terms……

The maximum speedup is $S_k \rightarrow k$ when n →INF

Maximum speedup is very difficult to achieve because of data dependencies between successive tasks, program branches, interrupts etc.

Important Terms

Efficiency: the ratio of actual speedup to ideal speedup k

$$\eta = \frac{n.k}{k.\left[k + (n-1)\right]}$$

$$= \frac{n}{\left[k + (n-1)\right]}$$

Contd…

- Maximum efficiency

$$\eta \rightarrow 1 \text{ as } n \rightarrow \infty$$

- Implies that the larger the number of tasks flowing through the pipeline, the better is its efficiency
- In steady state of a pipeline, we have n >> k, then efficiency should approach 1
- However, this ideal case may not hold all the time because of program branches and interrupts and data dependencies

Important Terms

Throughput : The number of tasks that can be completed by a pipeline per unit time

$$H_k = \frac{n}{[k+(n-1)]\tau} = \frac{nf}{[k+(n-1)]} = \eta f$$

Problem 1

Draw a space-time diagram for a six segment pipeline showing the time it takes to process eight tasks

Determine the number of clock cycles that it takes to process 200 tasks in a six segment pipeline

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Draw a space-time diagram for a six segment pipeline showing the time it takes to process eight tasks

Determine the number of clock cycles that it takes to process 200 tasks in a six segment pipeline

Problem 2

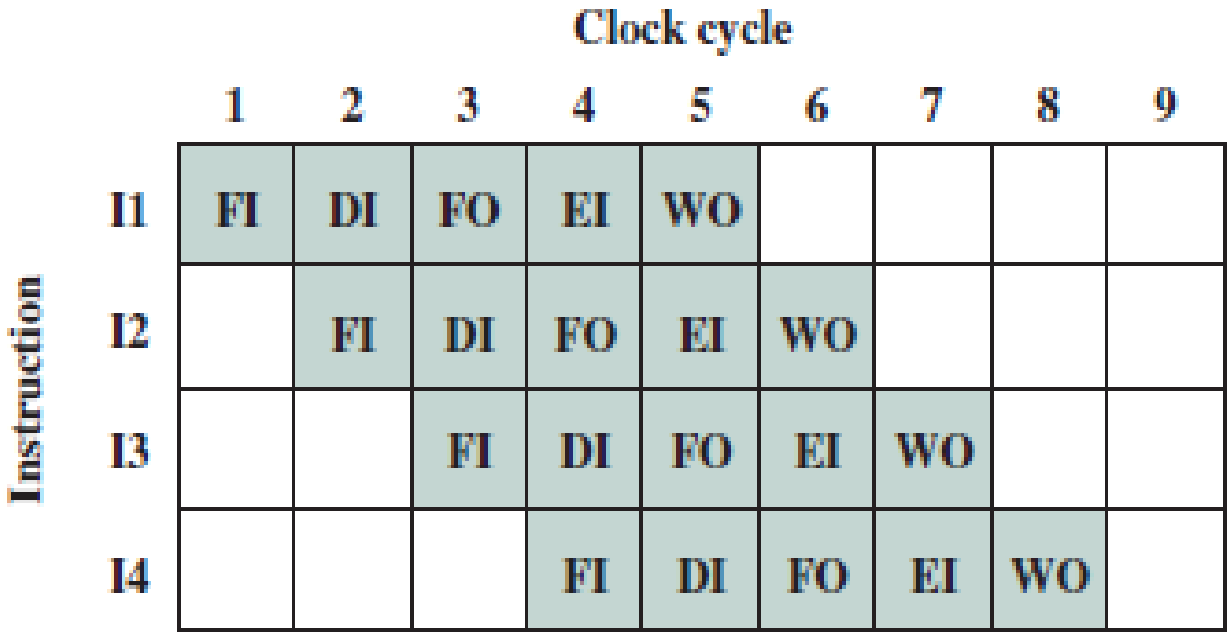
Assume each task is subdivided in to 6 subtasks and clock cycle is 10 microseconds.

- Determine the number of clock cycles that is taken to process 50 tasks in six stage pipeline
- Determine the number of clock cycles that is taken to process 50 tasks in non- pipeline processor
- Compute speed up, efficiency and throughput

Pipeline Hazards / Conflicts

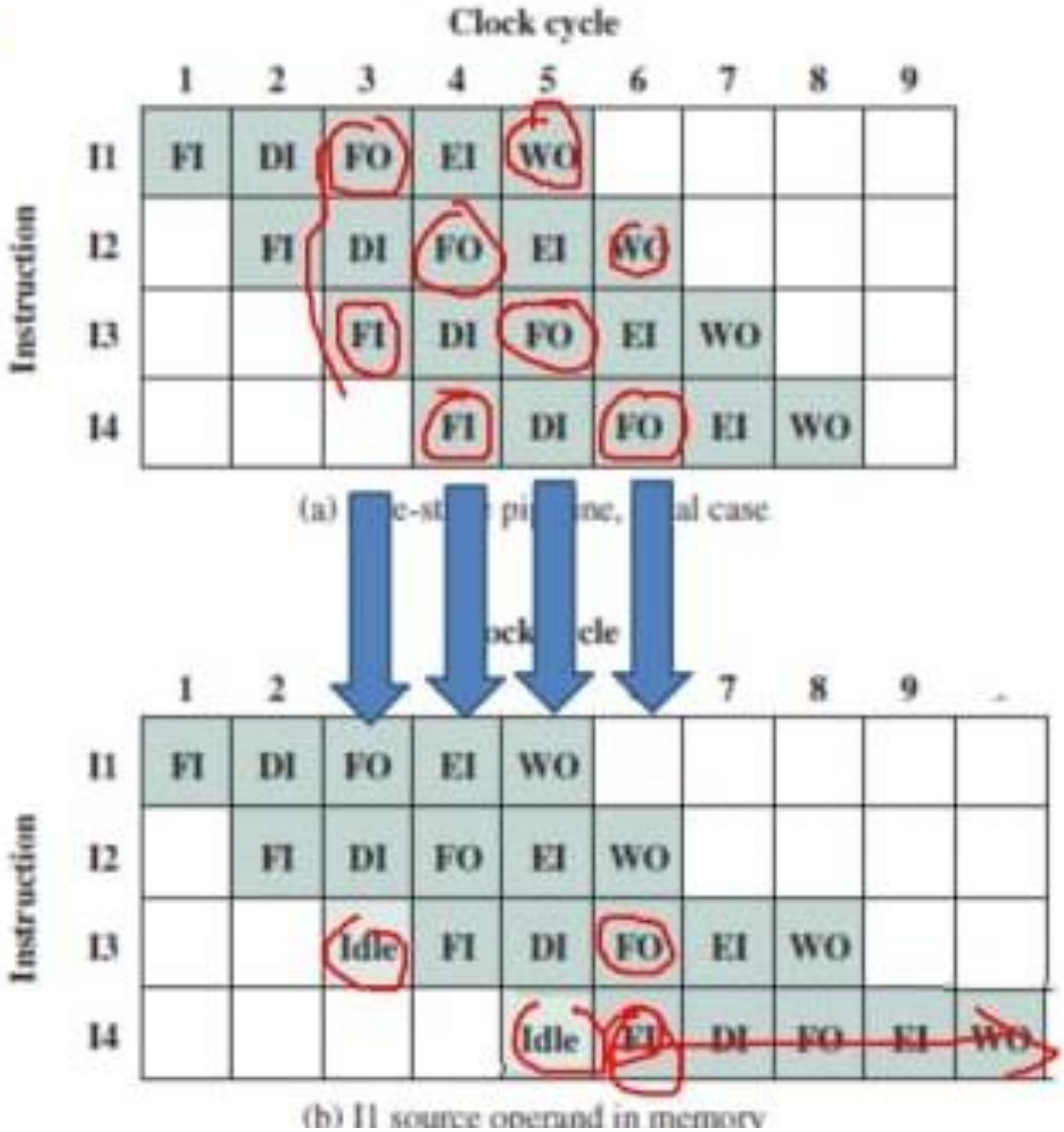
- Resource Hazard: access to same resource by two segments at the same time
- Data Hazard : an instruction depends on the result of a previous instruction, but this result is not yet available
- Control Hazard: arise from branch and other instructions that change the value of PC

Resource Hazard



(a) Five-stage pipeline, ideal case

Resource Hazard



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Problem

Consider the following code. Assume that initial contents of all the registers is zero.

```
START:    MOV R3, #1
          MOV R1, #2
          MOV R2, #3
          ADD R3, R1, R2
          SUB R4, R3, R2
          HLT
```

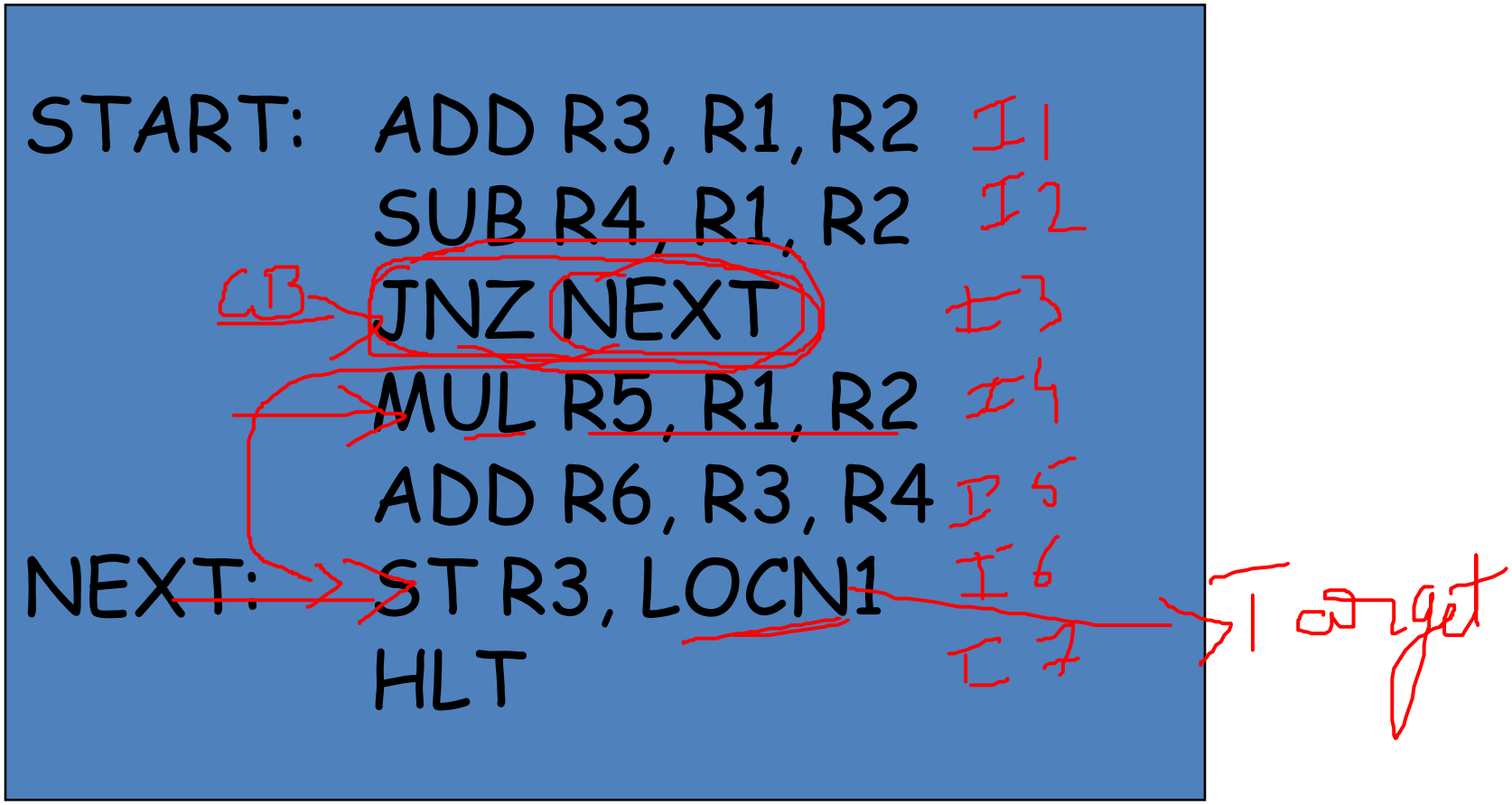
- Write timing of instruction pipeline with FIVE stages
- What is the content of various registers after the execution of program?

Data Dependency Conflict

```
MOV R3, #1
MOV R1, #2
MOV R2, #3
ADD R3, R1, R2
SUB R4, R3, R2
HLT
```

time	0	1	2	3	4	5	6	7	8	
I1	**FI**	**DI**	**FO**	**EI**	**WO**					
I2		**FI**	**DI**	**FO**	**EI**	**WO**				
I3			**FI**	**DI**	**FO**	**EI**	**WO**			
I4				**FI**	**DI**	**FO**	**EI**	**WO**		
I5					**FI**	**DI**	**FO**	**EI**	**WO**	
I 6						**FI**	**DI**	**FO**	**EI**	**WO**

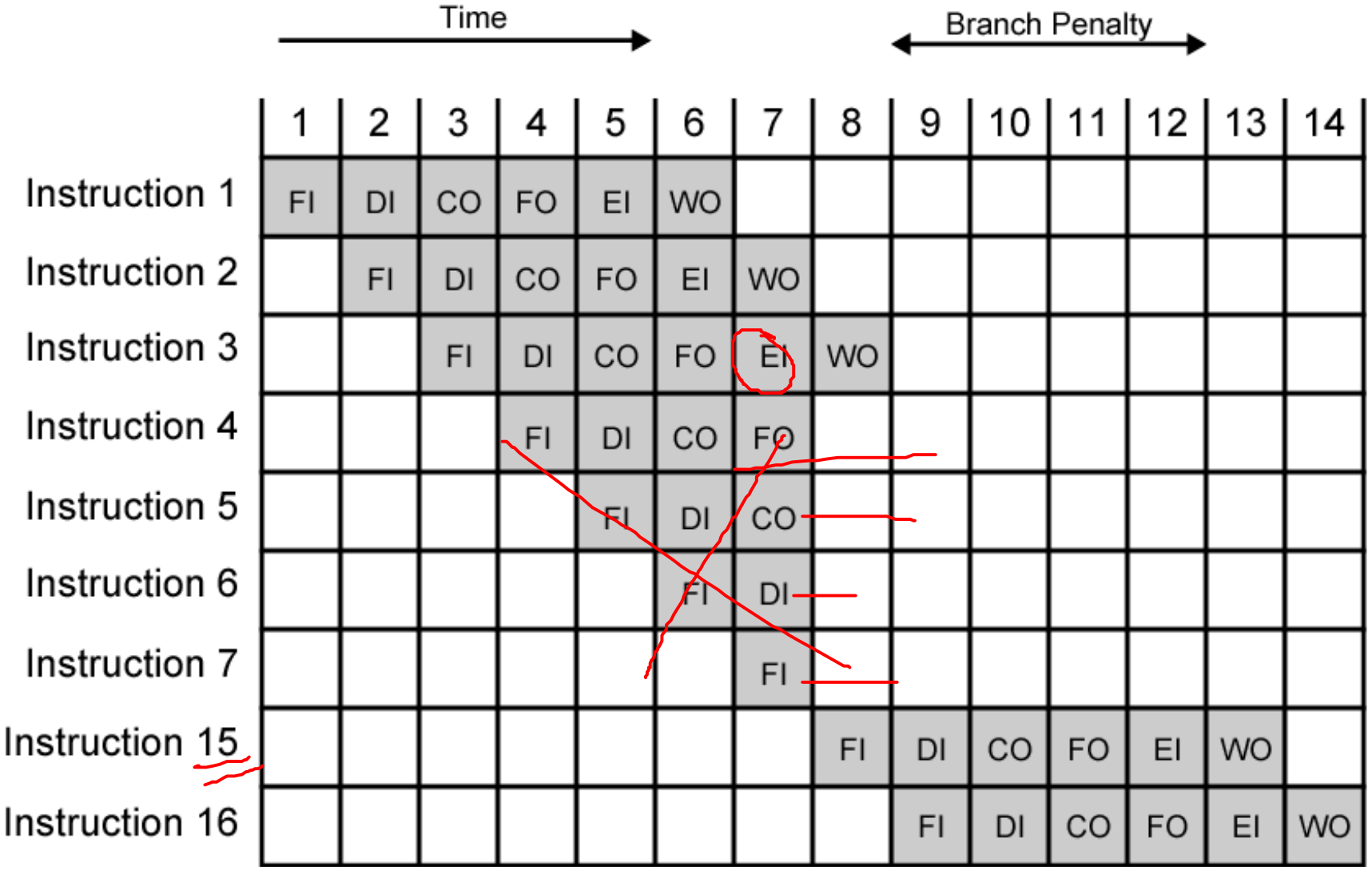
Example



Write timing of instruction pipeline

Time	0	1	2	3	4	5	6	7	8	9	10	11
I1	FI	DI	FO	EI	WO							
I2		FI	DI	FO	EI	WO						
I3			FI	DI	FO	EI	WO					
I4				FI	DI	FO						
I5					FI	DI						
I6							FI	DI	FO	EI	WO	
i7								FI	DI	FO	EI	WO

The Effect of a Conditional Branch on Instruction Pipeline Operation



Dealing with Branches

innovate achieve lead

- Multiple Streams
- Prefetch Branch Target
- Loop buffer
- Branch prediction
- Delayed branching

Multiple Streams

- Have two pipelines
- Pre-fetch each branch into a separate pipeline
- Use appropriate pipeline
- Used by IBM 370/168 and the IBM 3033
- Issues :
  - Leads to bus & register contention
  - Multiple branches lead to further pipelines being needed

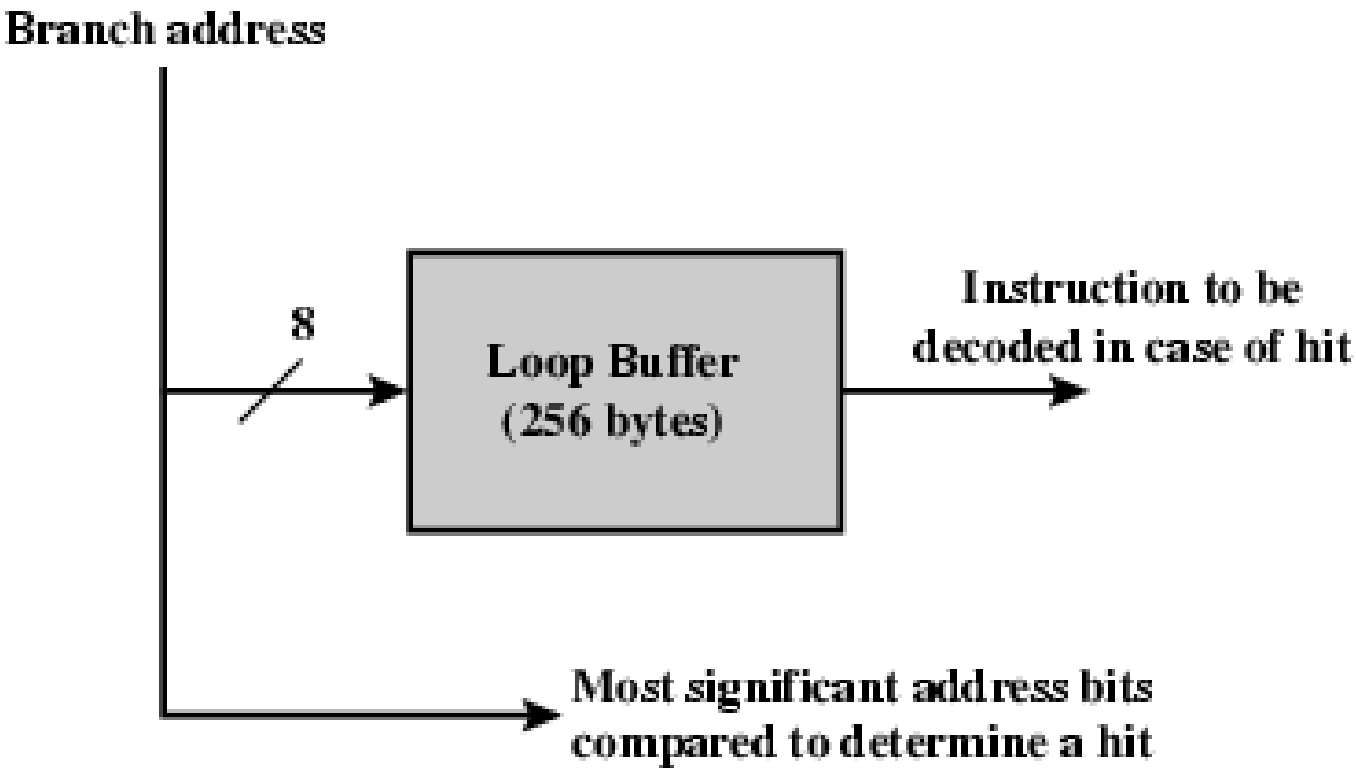
Prefetch Branch Target

- Target of branch is prefetched in addition to instructions following branch
- Keep target until branch is executed
- Used by IBM 360/91

Loop Buffer

- Very fast memory
- Maintained by fetch stage of pipeline
- Check buffer before fetching from memory
- Very good for small loops or jumps
- Working principle is similar to cache
- Used by CRAY-1

Loop Buffer Diagram



Branch Prediction (1)

- Predict never taken
- Predict always taken
- Predict by opcode
- Taken/not taken switch
- Branch history table

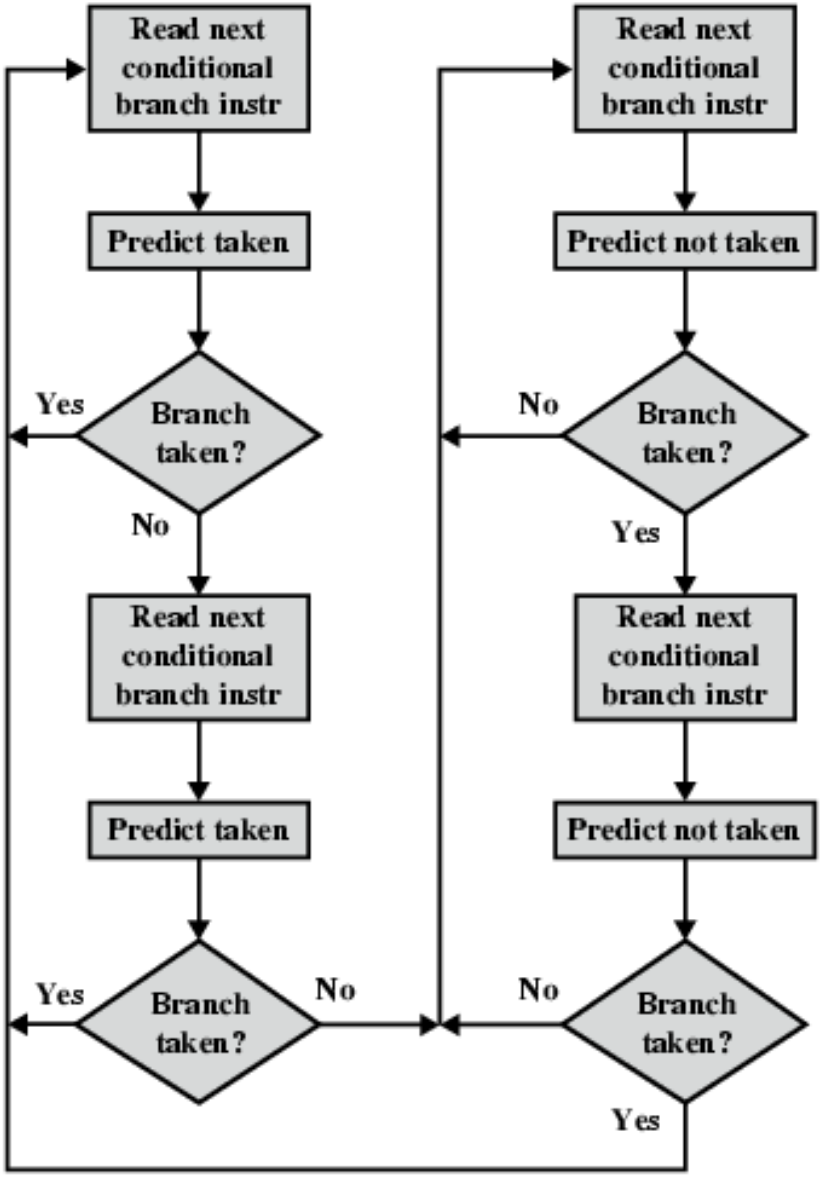
Branch Prediction (2)

- Predict never taken
  - Assume that jump will not happen
  - Always fetch next instruction
- Predict always taken
  - Assume that jump will happen
  - Always fetch target instruction
- Predict by Opcode
  - Some instructions are more likely to result in a jump than others
  - Can get up to 75% success

Branch Prediction (3)

- Taken/Not taken switch
  - Based on previous history
  - Good for loops

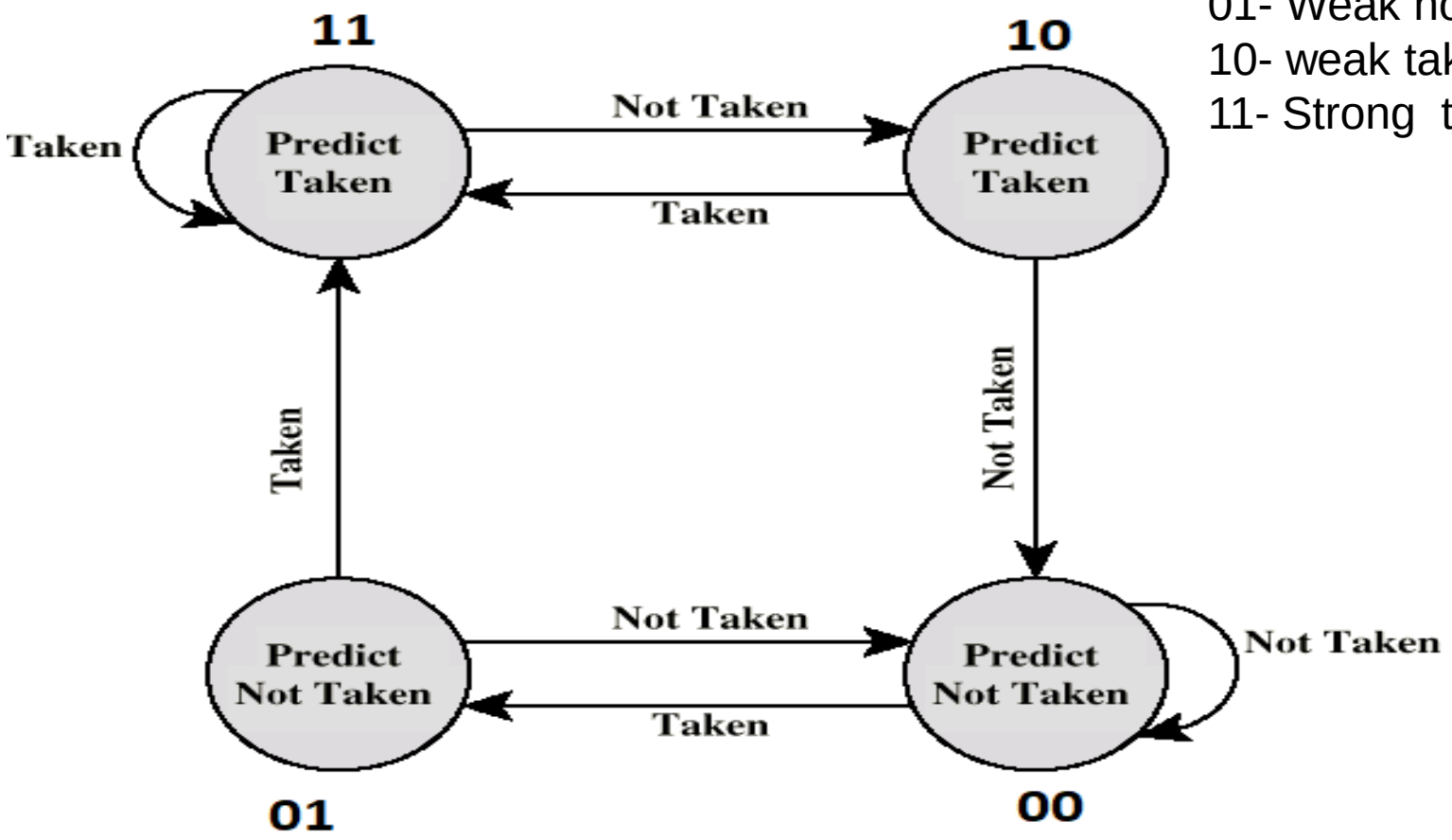
Branch Prediction Flowchart



Branch Prediction State Diagram

First bit is prediction bit and second bit is conviction bit

00 – strong not taken
01- Weak not taken
10- weak taken
11- Strong taken



Branch Prediction (4)

- Delayed Branch
  - Do not take jump until you have to
  - Rearrange instructions

Problem 3

Consider a computer system that requires four stages to execute an instruction. The details of the stages and their time requirements are listed below:

Instruction Fetch (IF) stage: 30 ns,

Instruction Decode (ID) stage: 9 ns

Execute (EX) stage: 20 ns

Store Results (WO stage): 10 ns.

Assume that inter-stage delay is 1 ns and every instruction in the program must proceed through the stages in sequence.

a) What is the frequency of the Processor?

b) What is the minimum time for 10 instructions to complete in non-pipelined manner?

c) What is the minimum time for 10 instructions to complete in pipelined manner?

Problem 4

A computer program is developed to run the DBSCAN algorithm on a processor with L1 cache and main memory organization with hit ratio of 67%. The processor supports 64-bit address bus, an 8-bit data bus and has a 256 KByte data cache memory with 4-way set associativity. The main memory is logically divided into a block size of 256 Bytes. Each cache line entry contains, in addition to address tag, 1 dirty bit.

i. What is the number of bits in the tag field of an address?

ii. If the associativity in the above problem, is changed to 8-way, do you see any performance gain and/ or drawback? Comment.

Cont.

i. What is the number of bits in the tag field of an address?

Number of lines in the cache = 256 KB / 256 B = 2^10 = 1 K lines

4 way = 4 lines per set

Therefore Number of sets = 1K/ 4 = 256 sets = 2^8
Number of bits needed to address sets = 8 bits
Number bits needed to address a word in the block : 256 = 2^8→ 8 bits

Tag bit = 64 – 8 -8 = 48 bits

Cont.

ii. If the associativity in the above problem, is changed to 8-way, do you see any performance gain and/ or drawback?

There is a performance gain in terms number of HITS
Tag comparison circuit becomes complex

Problem 5

Indian Meteorological Department's computer data scientists contemplating the preference of using LFU and FIFO replacement algorithms. The associative cache is having 4 lines and the address block generated by the CPU is 2,3,6,4,3,2,5,7,6,5. Help these Data scientists to choose the better of the two replacement algorithms. Justify your selection with the help of the following table.

Note: In LFU, in case of tie between cache lines for replacement, select the line which has been there for longer time in the cache

LFU

Time	0	1	2	3	4	5	6	7	8	9
Ref	2	3	6	4	3	2	5	7	6	5
L0	2_1	2_1	2_1	2_1	2_1	2_2	2_2	2_2	2_2	2_2
L1		3_1	3_1	3_1	3_2	3_2	3_2	3_2	3_2	3_2
L2			6_1	6_1	6_1	6_1	5_1	5_1	6_1	6_1
L3				4_1	4_1	4_1	4_1	7_1	7_1	5_1
M/H	M	M	M	M	H	H	M	M	M	M

$2/10$

FIFO

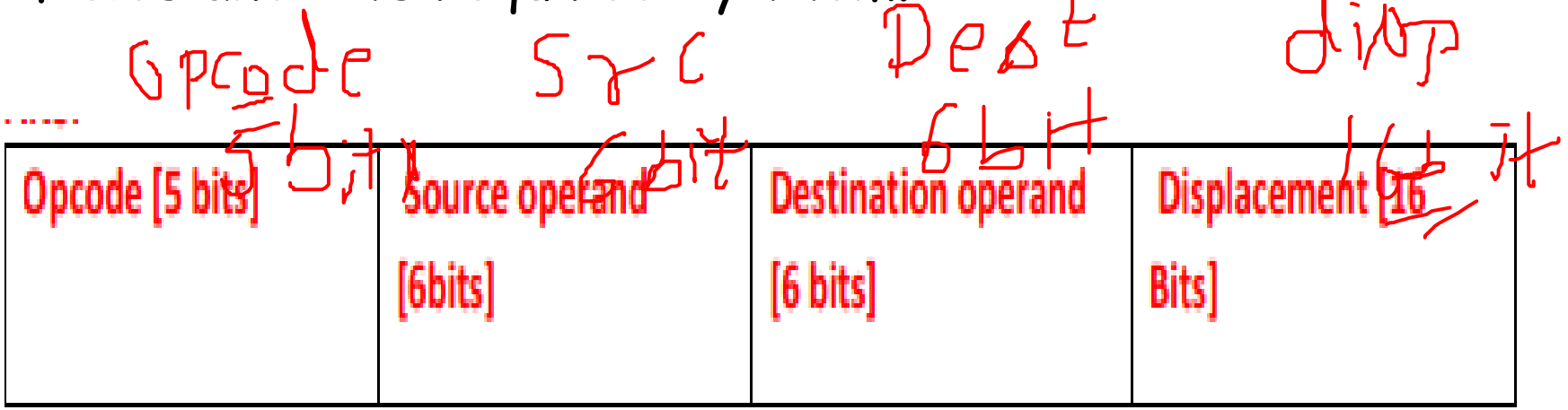
Time	0	1	2	3	4	5	6	7	8	9
Ref	2	3	6	4	3	2	5	7	6	5
L0	2	2	2	2	2	2	5	5	5	5
L1		3	3	3	3	3	3	7	7	7
L2			6	6	6	6	6	6	6	6
L3				4	4	4	4	4	4	4
M/H	M	M	M	M	H	H	M	M	H	12

4/10

FIFO is better as it results in hit rate of 4/10 compared to LFU whose hit rate is 2/10

Problem 6

A RISC based CPU is to be designed to have 32 opcodes, source and destination operands referring to 64 registers, and a displacement of value such as 2ABCH. Specify the instruction format mentioning the various fields and bits required by them.



Problem 7

The single cycle implementation of MIPS is as shown below. Answer the following questions with reference to "beq $S1, $S2, 8H" instruction. Assume that the contents of the registers S1 = 10 H, S2 = 10H, and PC = 16H, pointing to the instruction under consideration.

i. What is the addressing mode of the instruction?

ii. Which part of the instruction format, address of S1 and S2 are stored?

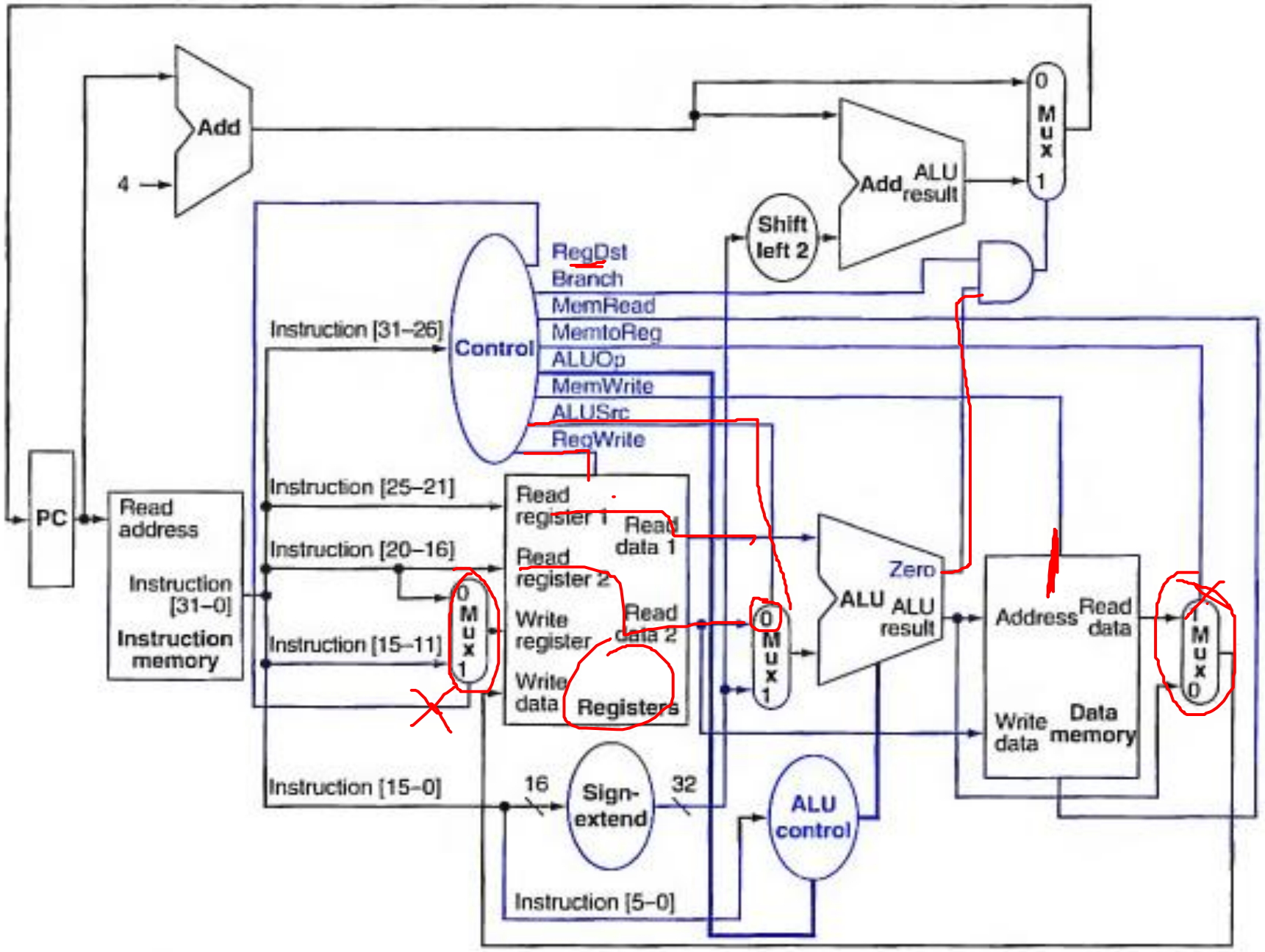
iii. What is the value of Zero Flag

iv. What is the value of PC, after the execution of the instruction?

Cont.

What is the status of different control signals to execute the instruction? Answer should be presented in the form of table given below. Indicate Don't care as X

Signal	Status
RegDst	X
Branch	1
MemRead	0
MemtoReg	X
ALUOp	01
ALUSrc	0
RegWrite	0



The simple datapath with the control unit.

Problem 8

A company named CacheFul is designing a machine with a byte addressable main memory. The size of the main memory is 218 Bytes and block size is 16 Bytes. The machine employs a direct mapping cache consisting of 32 lines. This machine is specifically configured to run a classification algorithm

i. When the algorithm is run it is noted that a memory access to main memory on a cache "miss" takes 30 ns and memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", how much time does it take to access memory on average?

Cont.

ii. Recommended average memory access time for the algorithm to perform optimally is not more than 5 ns, what option as a developer, do you have to keep it near to 5ns?

5ns=3h+(1-h)*33

5ns =3h+33-33h

5ns =-30h+33

30h=28

H=28/30=>93%