

**UNIVERSITY OF BATANGAS – LIPA CAMPUS
COLLEGE OF ENGINEERING AND ARCHITECTURE
COMPUTER ENGINEERING**

**Seven Segment Display
HDL**

NAME: Dimple G. Valencia

STUDENT NUMBER: 2021083

DATE OF SUBMISSION: 12/20/2022

ENGR. CHARLES RAY JUANILLAS

PROFESSOR



Result and Discussion:

```
C:\iverilog\exercises\logic>iverilog -o SevenSegment SevenSegment.v

C:\iverilog\exercises\logic>vvp SevenSegment
VCD info: dumpfile SevenSegmentDisplay.vcd opened for output.
Letter=Pin
A=1, B=1, C=1, D=1, E=1, F=1, G=0,
A=0, B=1, C=1, D=0, E=0, F=0, G=0,
A=1, B=1, C=0, D=1, E=1, F=0, G=1,
A=1, B=1, C=1, D=1, E=0, F=0, G=1,
A=0, B=1, C=1, D=0, E=0, F=1, G=1,
A=1, B=0, C=1, D=1, E=0, F=1, G=1,
A=1, B=0, C=1, D=1, E=1, F=1, G=1,
A=1, B=1, C=1, D=0, E=0, F=0, G=0,
A=1, B=1, C=1, D=1, E=1, F=1, G=1,
A=1, B=1, C=1, D=1, E=0, F=1, G=1,
SevenSegment.v:68: $finish called at 100 (1s)

C:\iverilog\exercises\logic>gtkwave SevenSegmentDisplay.vcd
```

