

**UNIVERSITY OF BATANGAS – LIPA CAMPUS
COLLEGE OF ENGINEERING AND ARCHITECTURE
COMPUTER ENGINEERING**

Laboratory #5

HDL

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PROFESSOR

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C:\iverilog\exercises\logic>iverilog -o experiment5 experiment5.v

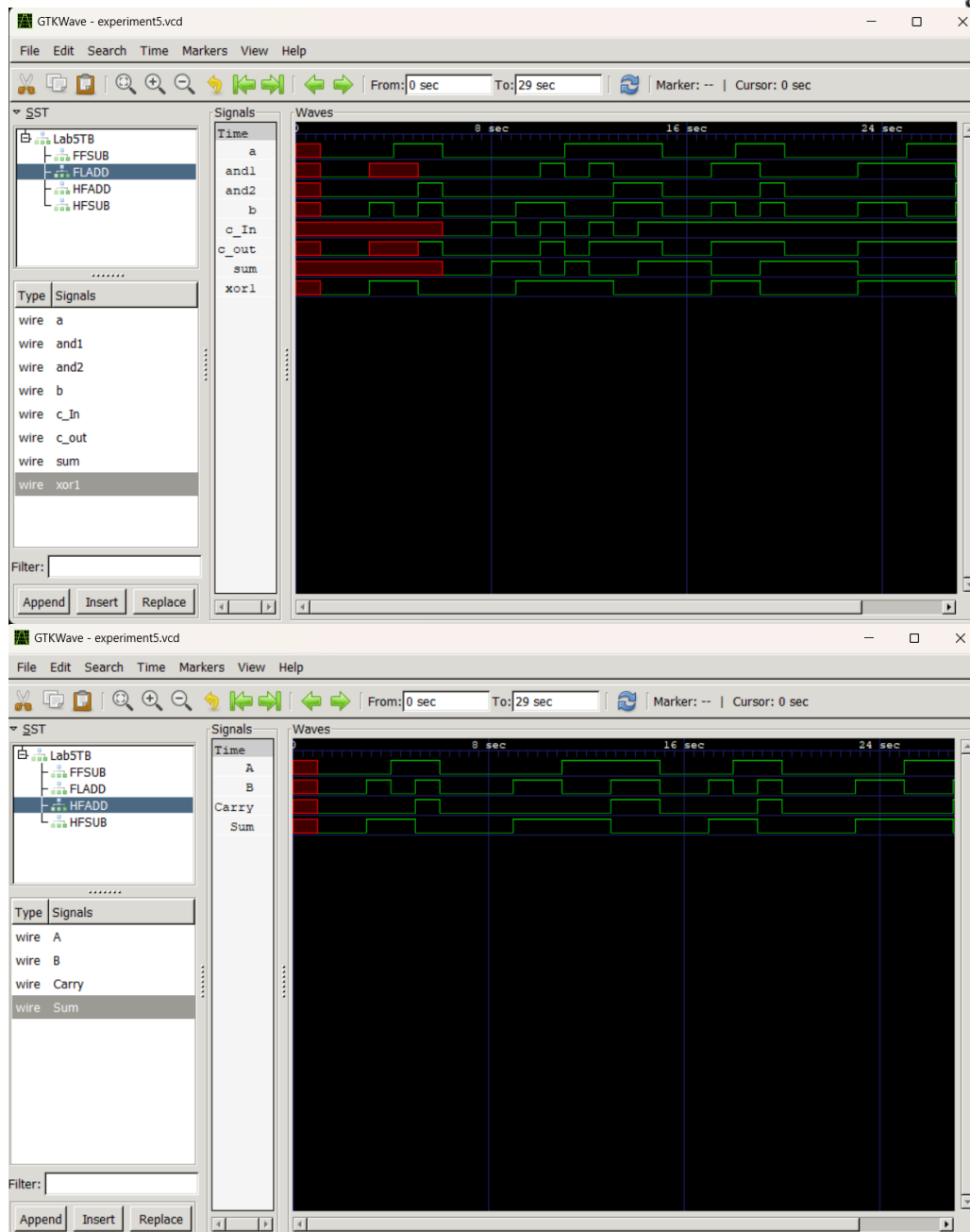
C:\iverilog\exercises\logic>vvp experiment5
VCD info: dumpfile experiment5.vcd opened for output.
xxxxxxx
00x000xx
Simulating Half Adder
A=0, B=0, sum=0, carry=0
A=0, B=1, sum=1, carry=0
A=1, B=0, sum=1, carry=0
A=1, B=1, sum=0, carry=1
A=0, B=0, sum=0, carry=0
Simulating Full Adder
A=0, B=0, c_in=0, sum=0, C_out=0
A=0, B=0, c_in=1, sum=1, C_out=0
A=0, B=1, c_in=0, sum=1, C_out=0
A=0, B=1, c_in=1, sum=0, C_out=1
A=1, B=0, c_in=0, sum=1, C_out=0
A=1, B=0, c_in=1, sum=0, C_out=1
A=1, B=1, c_in=0, sum=0, C_out=1
A=1, B=1, c_in=1, sum=1, C_out=1
A=0, B=0, c_in=1, sum=1, C_out=0
Simulating Half Subtract
A=0, B=0, D=0, bOut=0
A=0, B=1, D=1, bOut=1
A=1, B=0, D=1, bOut=0
A=1, B=1, D=0, bOut=0
A=0, B=0, D=0, bOut=0
Simulating Full Subtract
A=0, B=0, bIn=0, D=0, bOut=0
A=0, B=0, bIn=1, D=1, bOut=1
A=0, B=1, bIn=0, D=1, bOut=1
A=0, B=1, bIn=1, D=0, bOut=1
A=1, B=0, bIn=0, D=1, bOut=0
A=1, B=0, bIn=1, D=0, bOut=0
A=1, B=1, bIn=0, D=0, bOut=0
A=1, B=1, bIn=1, D=1, bOut=1
experiment5.v:107: $finish called at 29 (1s)

C:\iverilog\exercises\logic>
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