

**UNIVERSITY OF BATANGAS – LIPA CAMPUS
COLLEGE OF ENGINEERING AND ARCHITECTURE
COMPUTER ENGINEERING**

Laboratory #2

HDL

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Result and Discussion:

```
Command Prompt
C:\iverilog\exercises\logic>iverilog -o experiment2 experiment2.v
C:\iverilog\exercises\logic>vvp experiment2
VCD info: dumpfile experiment2.vcd opened for output.
xxxxxx
DeMorgan's Law
~((a)(b))
a=0, b=0, n=1
a=0, b=1, n=1
a=1, b=0, n=1
a=1, b=1, n=0
~a+~b
a=0, b=0, n=1
a=0, b=1, n=1
a=1, b=0, n=1
a=1, b=1, n=0
Therefore, ~((a)(b)) == (~a)+(~b)

~(a+b)
a=0, b=0, n=1
a=0, b=1, n=0
a=1, b=0, n=0
a=1, b=1, n=0
~a(~b)
a=0, b=0, n=1
a=0, b=1, n=0
a=1, b=0, n=0
a=1, b=1, n=0
Therefore, ~(a+b) == (~a)(~b)

part 1B
a=1, b=1, n=1
a=0, b=1, n=0
a=1, b=0, n=0
a=1, b=1, n=1

part 2A
a=1, b=1, n=1
a=1, b=0, n=0
a=0, b=1, n=0
a=0, b=0, n=0

part 2B
a=0, b=0, n=0
a=0, b=1, n=1
a=1, b=0, n=1
a=1, b=1, n=1
experiment2.v:129: $finish called at 36 (1s)

GTKWave - experiment2.vcd
File Edit Search Time Markers View Help
Signals
Time: 0.00 sec To: 36 sec Marker: -- | Cursor: 1 sec
SST
Experiment2
--a2
--b1
--b2
negativeAND1
negativeOR1
notA
notB
Type Signals
wire NAND1
wire NOR1
wire a
wire b
wire negativeAND1
wire negativeOR1
wire notA
wire notB
Append Insert Replace
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[36] end time.
(gtkwave.exe:18516): Gdk-CRITICAL **: inner_clipboard_window_procedure: assertion 'success' failed
```



