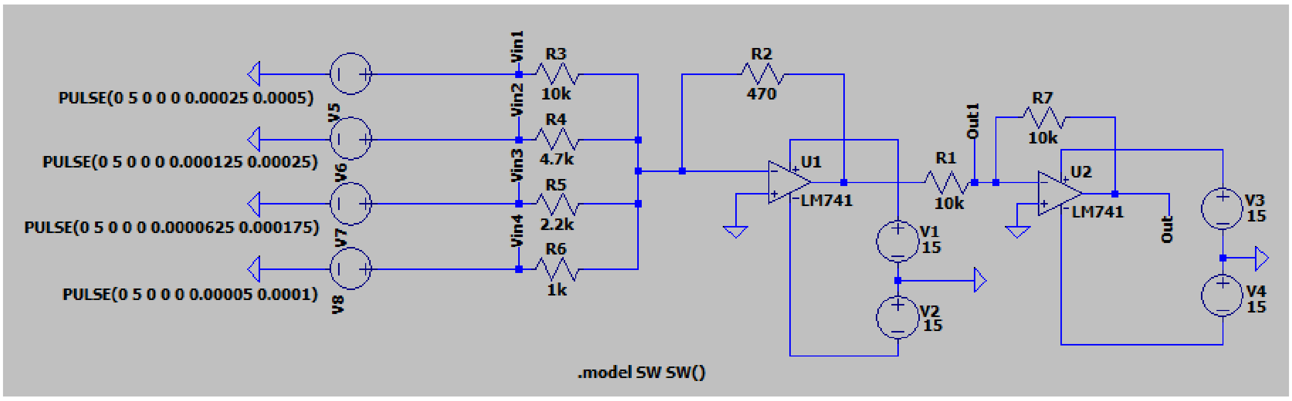
TITLE GOES HERE

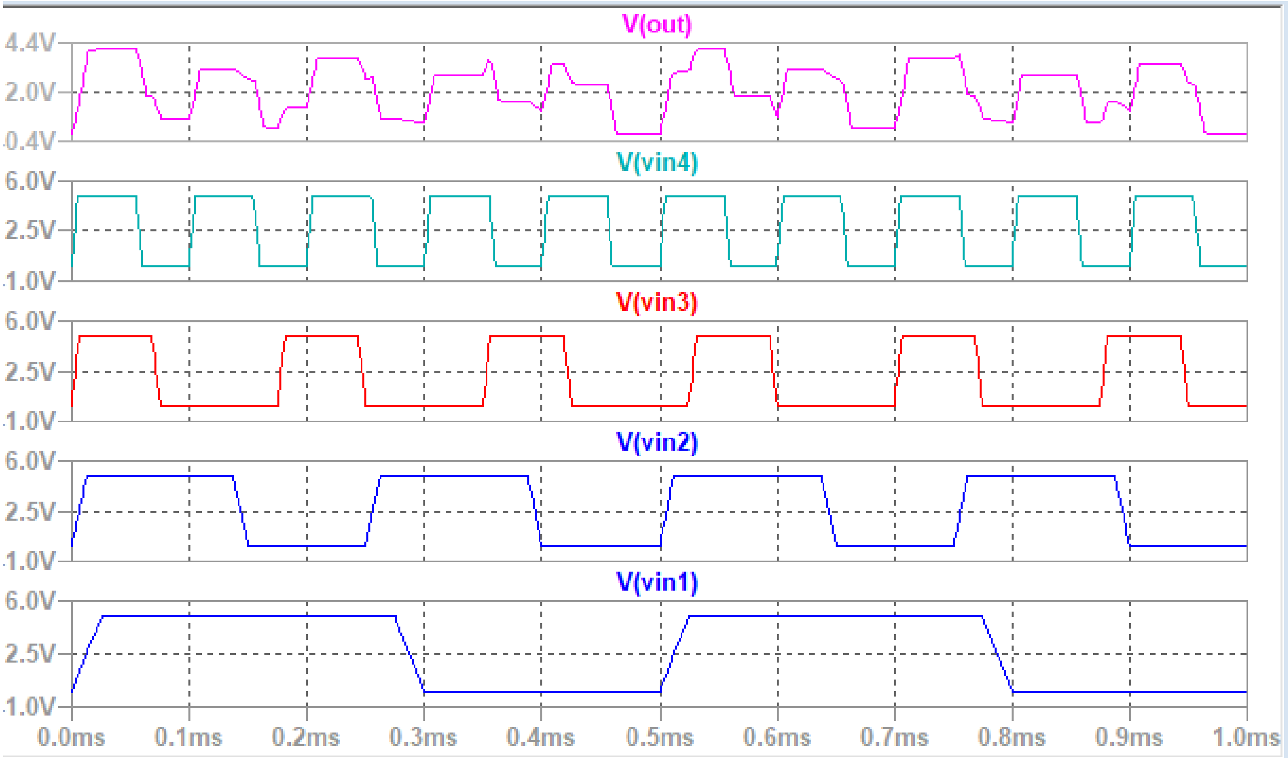
Necessary steps to get the simulations done: Download and install 74hct model to your LTspice.

TASK 1:

Circuit:



Transient analysis 1 ms



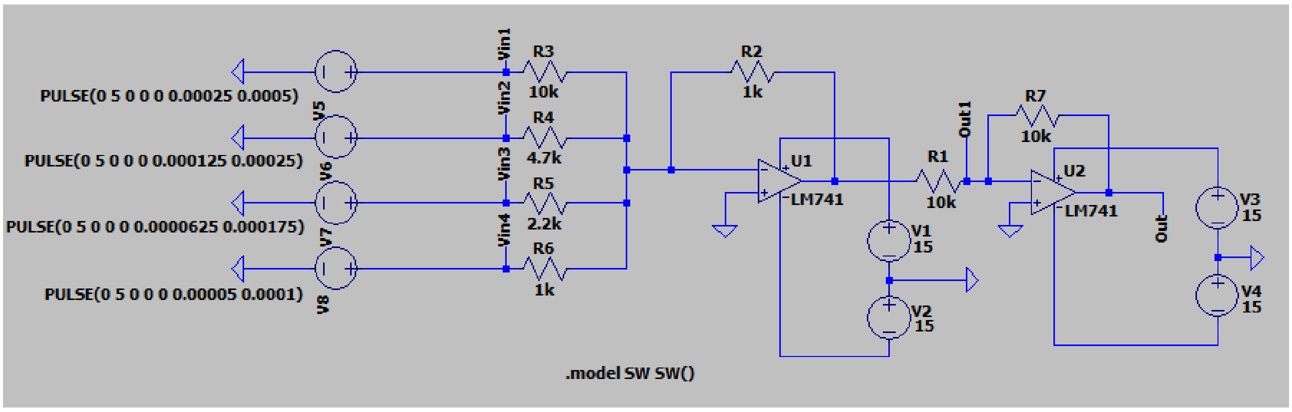
(Graph shows all 4 inputs and Vout.)

Question: What would you say the circuit above is?

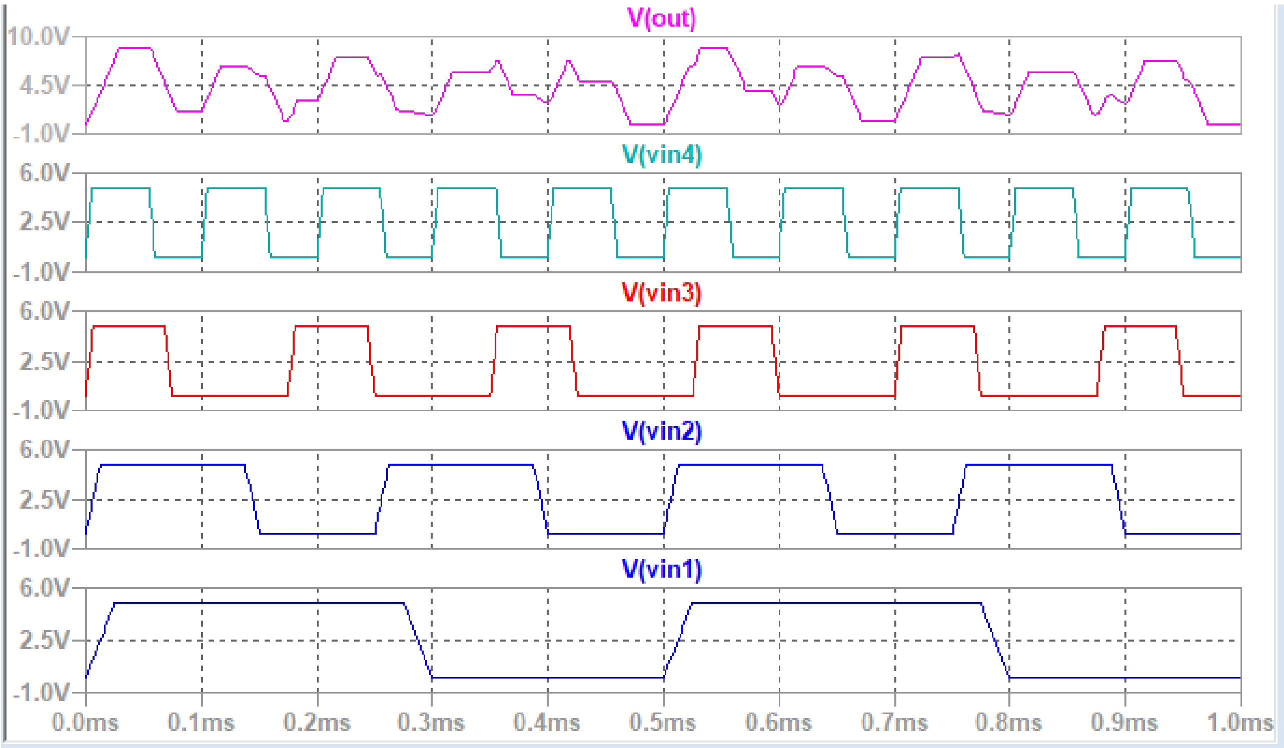
Answer: It's a summing operational amplifier circuit with 4 inputs.

TASK 2:

Circuit:



Transient analysis 1 ms

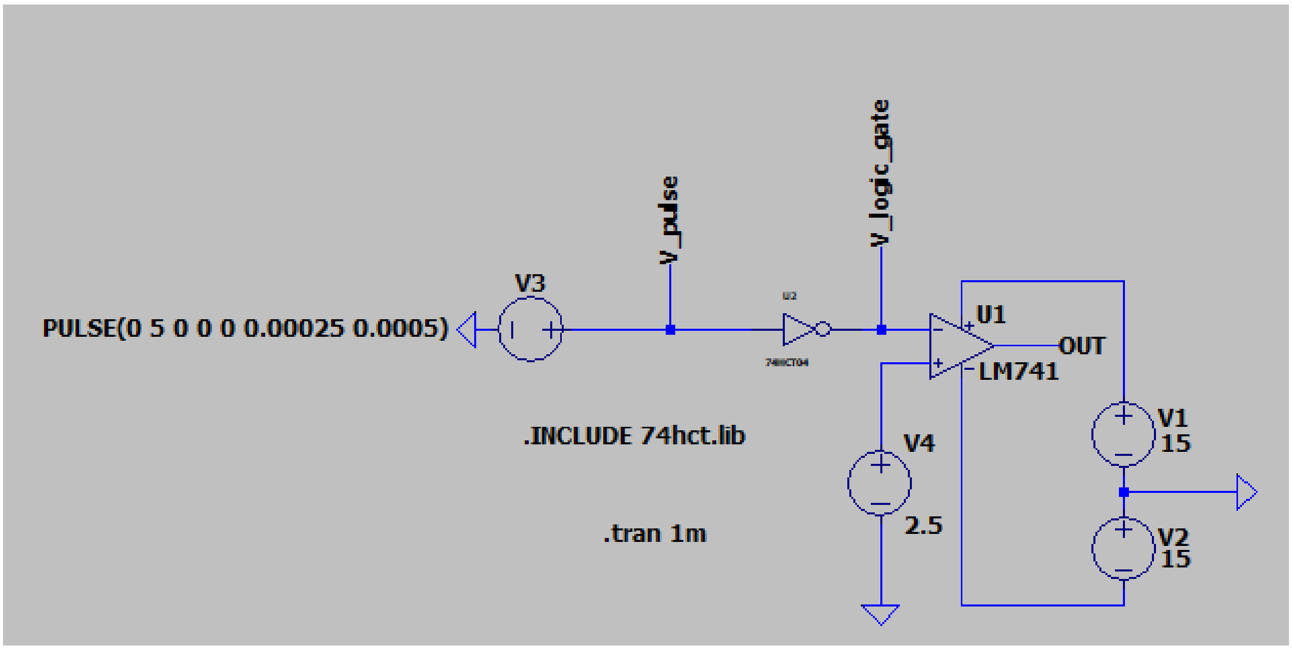


(The graph shows the signals replaced with R2 470 ohm => R2 1k ohm.)

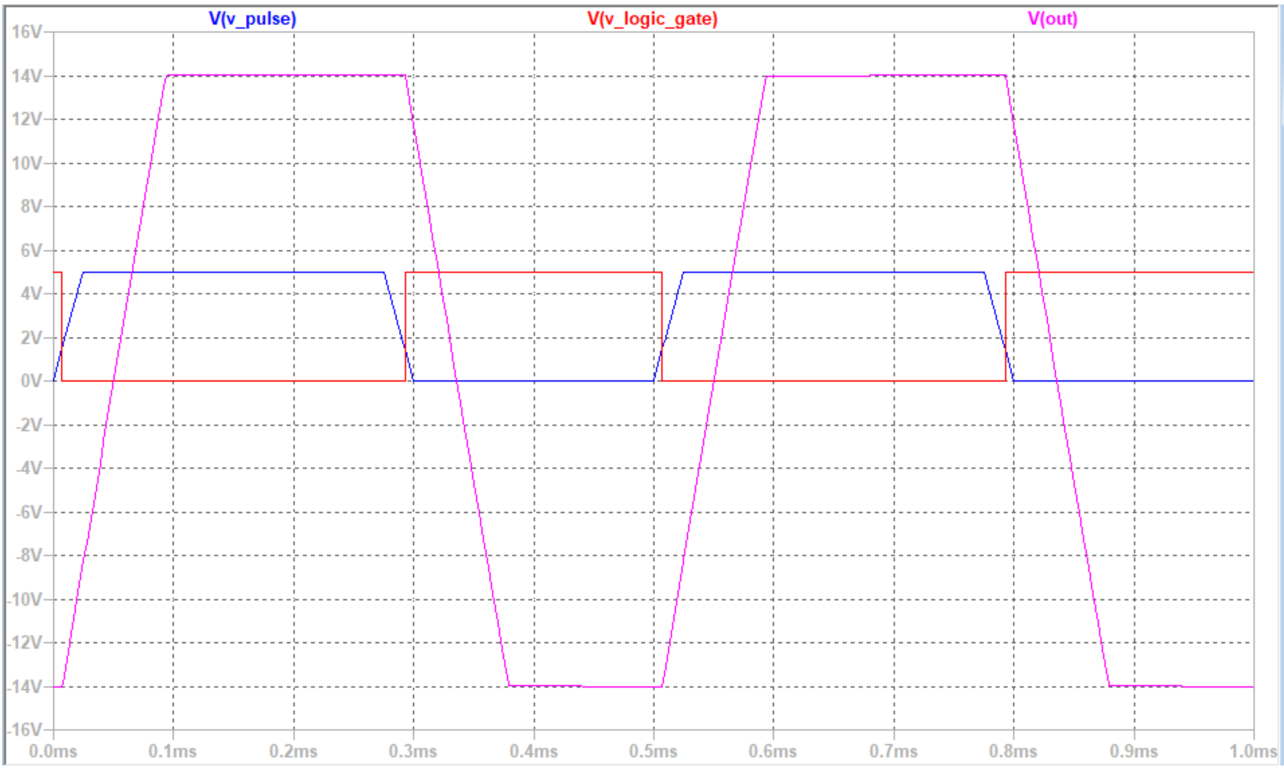
Observation: Vout has increased significantly. WIth 470 ohm resistor the Vout was around 4.4 V. 1k ohm resistor increased the amplification by 55.5%.

Task 3:

Implement the circuit below and check it's operation:



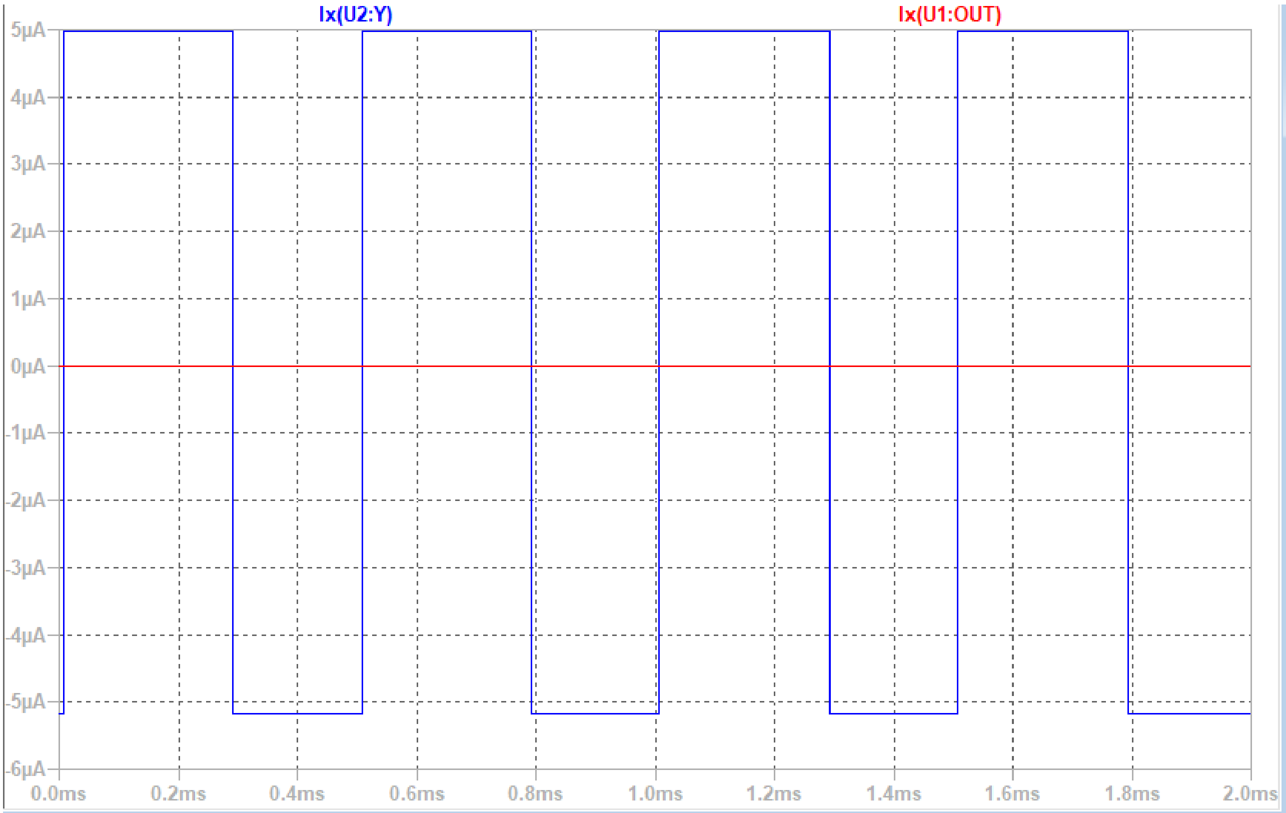
If you compare the output voltage of this circuit to output of a logic gate, what's the difference?:



Answer: Transient analysis indicates that the 74xx series component in the circuit functions as an inverter, correctly inverting the input signal. However, an abnormality is observed in the OUT node. The inversion from the 74xx series component seems to impact the output signal of the LM741 op-amp. When the input signal is inverted, the LM741 output also follows suit. Consequently, the voltage gain of the operational amplifier LM741 fluctuates between approximately +14V and -14V DC in response to the inverted input signal.

And, the rising pace and falling pace of OpAmp output signals is significantly smaller than inverters.

If you compare the output currents of 7400 and LM741 (look at the datasheets) how would you describe the difference?:



('LX(U2:Y)' is inverter output current and 'lx(U1:OUT)' is OpAmp output current.)

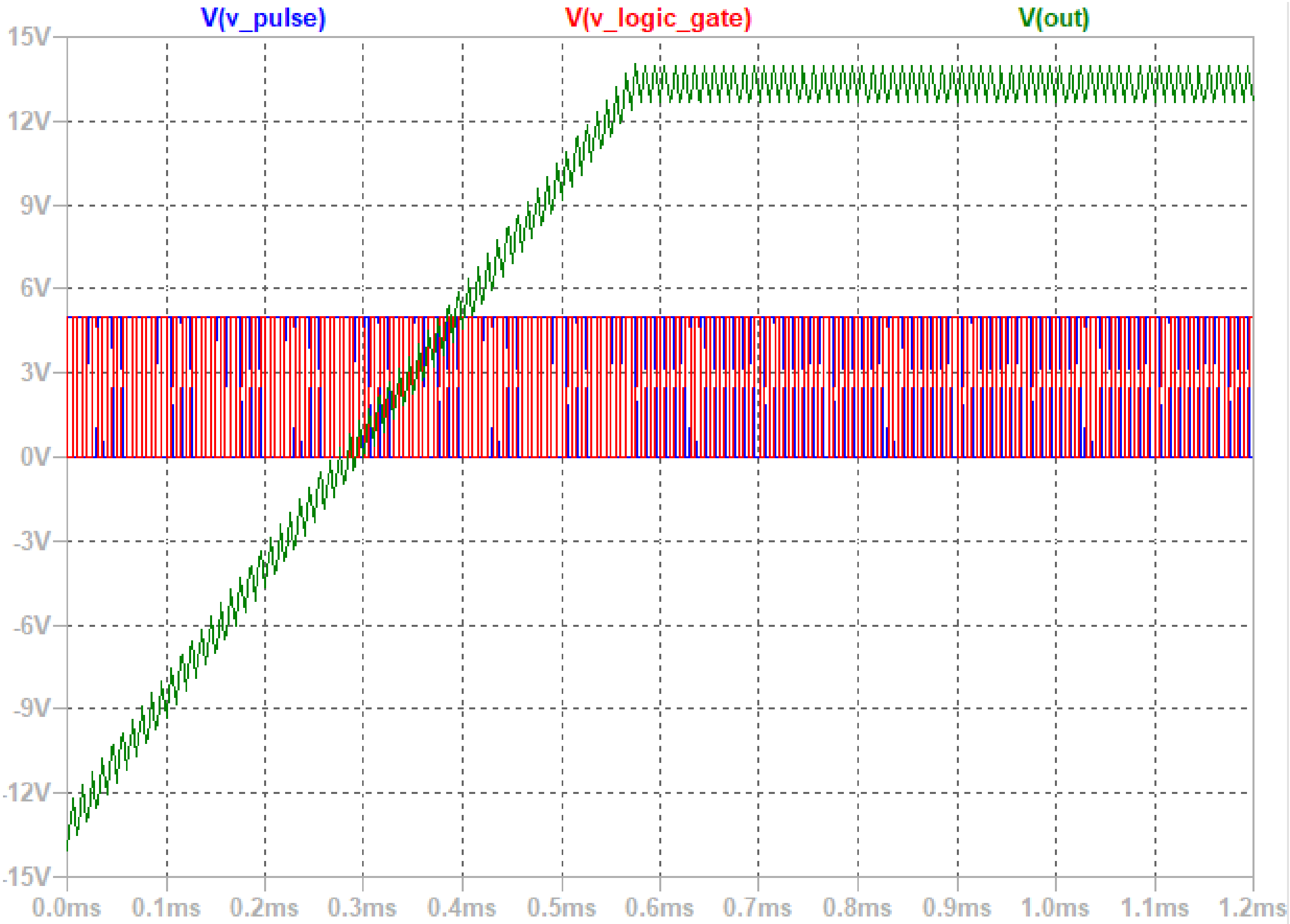
Answer: The 7400 inverter shows an output current of 5uA, which is typical for digital logic ICs and might reflect its internal current consumption during operation. The LM741 op-amp typically has a very low bias current, often in the range of tens of microamperes. However, measured 0 A at OpAmp output is abnormal. The LM741 can draw a small bias current, but without a load, this current might not manifest as an output current in this measurement setup. There's a lack of knowledge to make more precise observations at the moment.

Task 4:

Disconnect the logic switch and replace it with TTL generator:
Low logic usually works in 0.-0.8 range and high logic works in 2-5V range, therefore adjusting input voltage source (V3) to work either in low or high logic range is sufficient circuit adjustment.

Increase the frequency of TTL generator:
We can increase the frequency by adjusting the pulse period and Ton time. Previously we have used a 10k Hz input signal where the period is 100uS and Ton is 5uS. Now let's change the frequency to 100 KHz. Period is 10uS and Ton 0.5uS respectively.

measure what happens:



If you compare the speed of a logic gate and LM741 how would you describe the difference?:

Apparently due to the LM741 limitations and such a frequent change of input signal, the LM741 output signal variations become quite small. Meaning that LM741 can not possibly follow the inverting input signal at such a high frequency which will then result in amplified signal that increases to saturation in slew rate of LM741 operational amplifier.

Reduce the VC to +10V and VE to –10V:

We can accomplish this by adjusting the V1 and V2 voltage source in the required manner.

How does this change affect output voltage levels?:

Answer: Vc and Ve define the possible output voltage range and by adjusting them to +10 and -10, we limit the possible output voltage of the circuit. In other words, lowering Vc and Ve decreases the maximum output voltage swing capability of the LM741 op-amp.

How does it affect the rising time of LM741?:

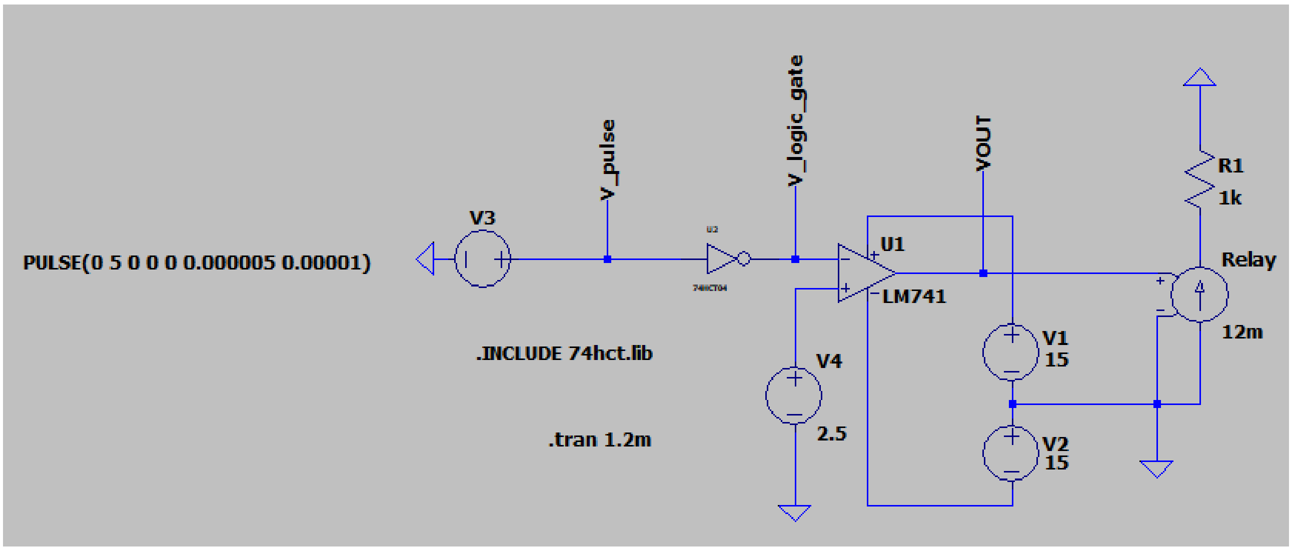
The rising time decreases as the op-amp reaches the saturation level faster due to smaller output voltage swing.

How does it affect the slew rate of LM741?:
It does not change the basic characteristics of the LM741 operational amplifier.

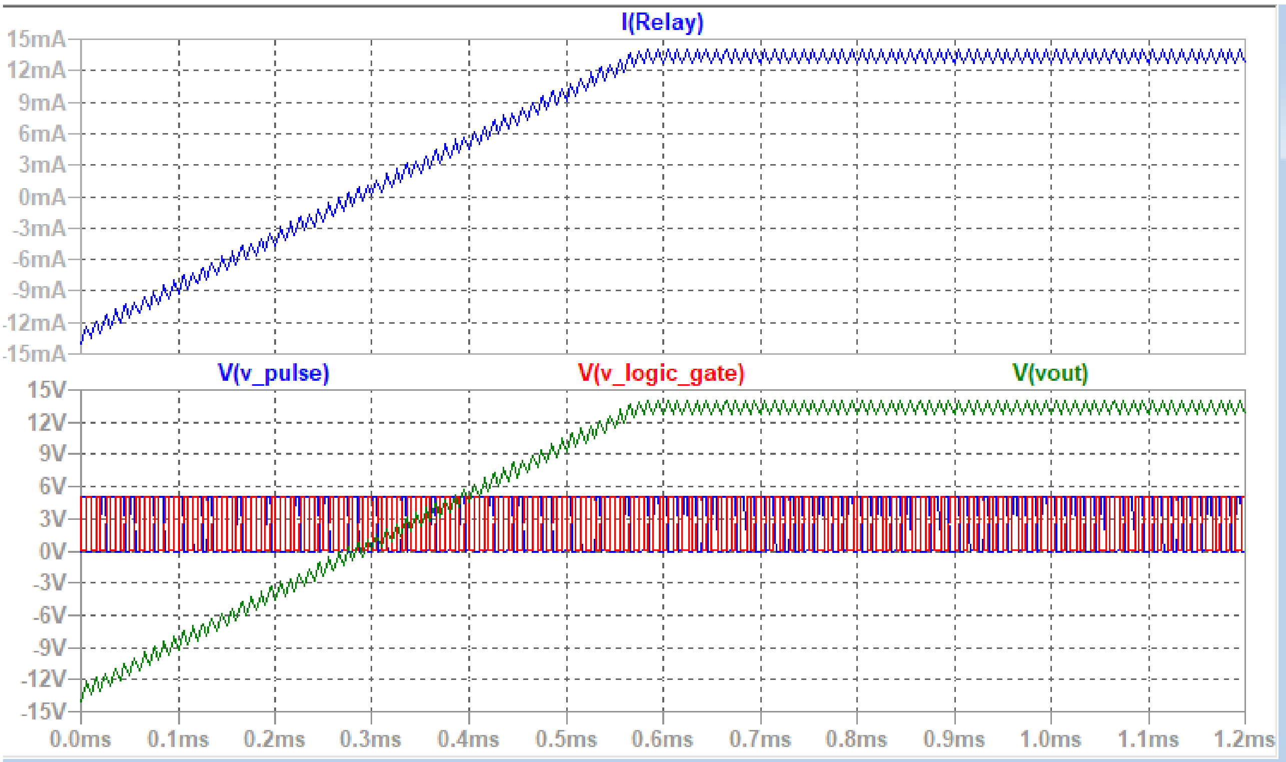
Task 6:

Try to implement a circuit, where a logic gate is controlling an operational amplifier and the amplifier is controlling a 12V relay:

Let’s use the previous circuit and modify it a bit. First we select a voltage dependent current source to work as our relay. Then we limit the output current of the relay to 12mA with 1k ohm resistor.
U: R*I
I = 12V : 1k ohm = 12mA



Measure the relay functionality:



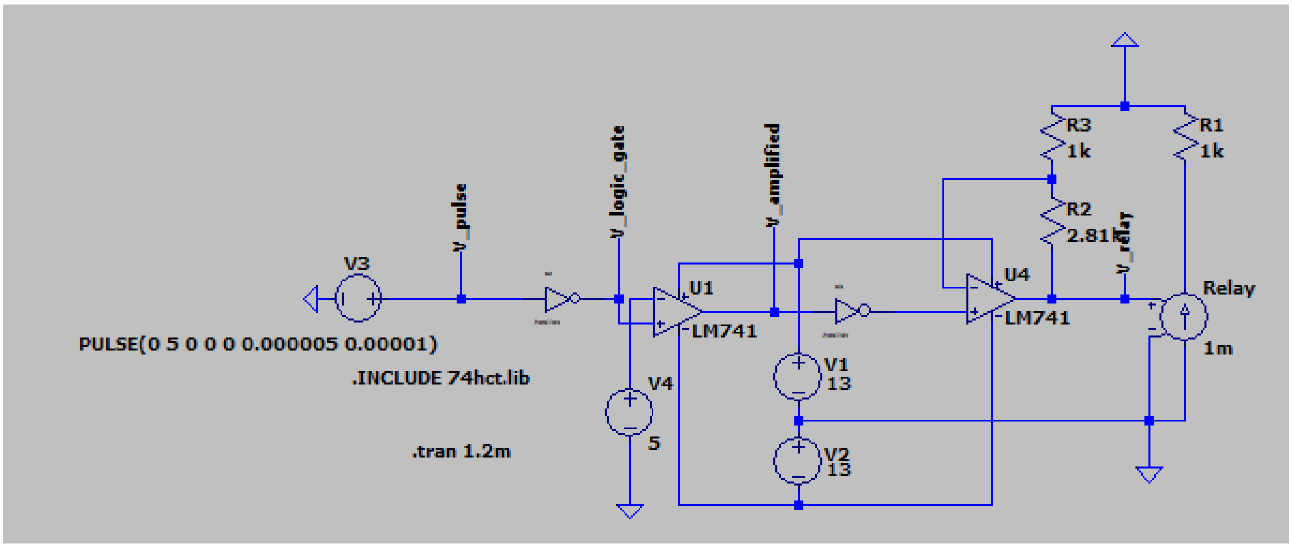
Answer: The relay functions as expected. Graph shows a current increase in the relay circuit at 12V point and the current reaching a around 12mA -ish level. Current seems to be getting level variation from LM741 and one fix for this could be to increase the input frequency to such a high level. This approach would take advantage of limits of LM741 but might introduce other problems that can happen in high frequency circuits. I do not recommend going around the problem with a given solution.

Operating the circuit at very high frequencies might introduce challenges such as signal distortion, phase shifts, increased noise, and limited bandwidth of the op-amp, which could affect the overall performance of the system.

Consider exploring other approaches like filtering, adjusting component values, or using different op-amps with better high-frequency characteristics might offer more effective solutions without the limitations associated with operating at extremely high frequencies. Also, you can configure the op-amp in a comparator mode: Select an op-amp suitable for use as a comparator. Some op-amps, like the LM311 or LM393, are designed for comparator applications.Connect the non-inverting (+) input of the op-amp to a reference voltage (could be a fixed voltage or from another circuit). The inverting (-) input of the op-amp receives the signal from the logic gate directly, bypassing the inverter. The logic gate output (0-5V pulse with 100 kHz frequency) directly connects to the inverting (-) input of the op-amp. The op-amp acts as a comparator, comparing the logic gate signal with the reference voltage. Its output will switch between high and low levels based on the comparison result.

One way to go about the variation problem:

- Adjusting reference voltage (V4) and connecting to the inverting pin.
- Connecting the control pulse to a non inverting pin.
- Adjusting output signal swing to +13 and -13.
- Adding 2.81 times amplification to 5.5 -ish V to meet +12V.



Now we have significantly less level variation:

I(Relay)
12mA
10mA
8mA
6mA
4mA
2mA
0mA
V(v_relay)
12V
-1V
-14V
V(v_pulse)
V(v_logic_gate)
V(v_amplified)
12V
-1V
-14V
0.0ms
0.1ms
0.2ms
0.3ms
0.4ms
0.5ms
0.6ms
0.7ms
0.8ms
0.9ms
1.0ms
1.1ms
1.2ms