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| Reg. No.: 2022-EE-134 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

github code address: https://github.com/2022ee134/Digital-system-lab/tree/main/lab2

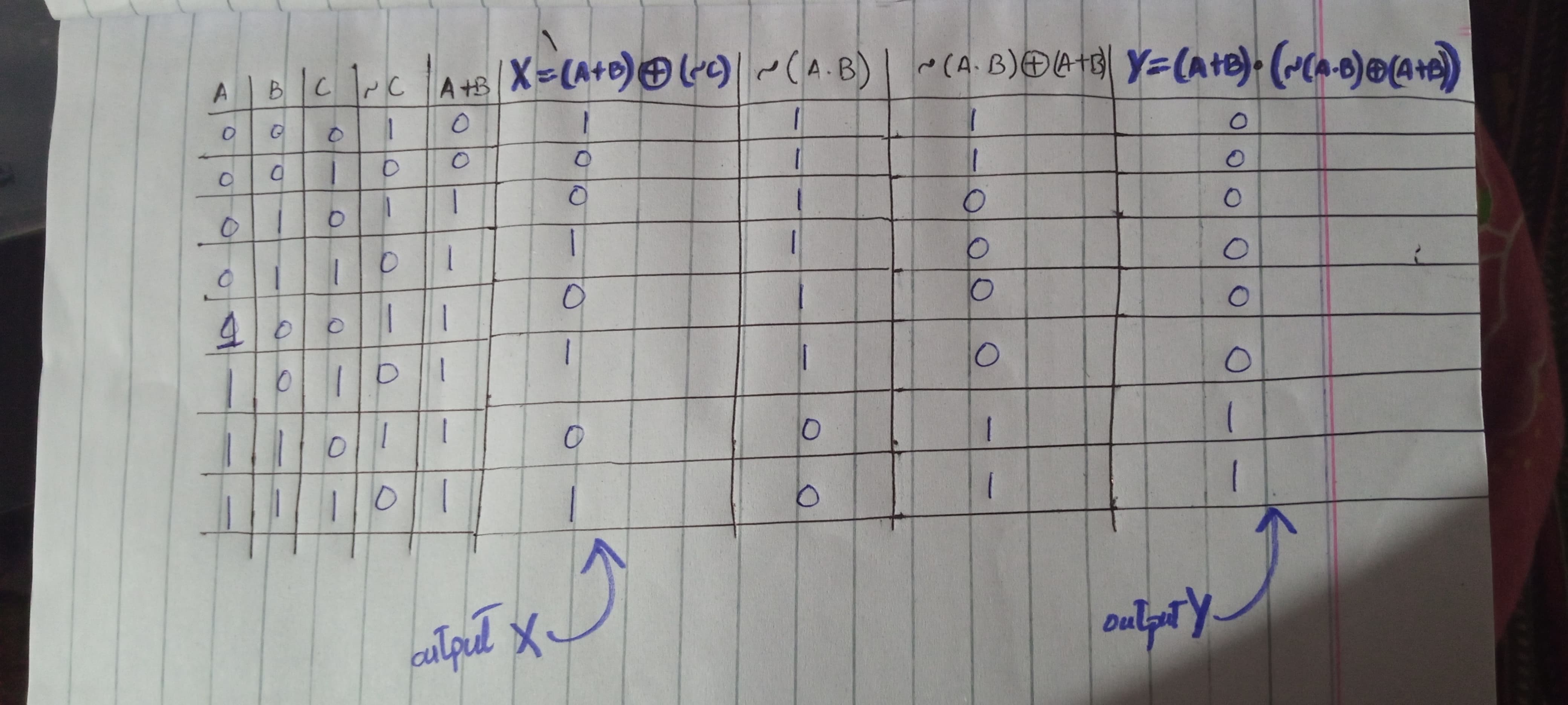
**Lab Manual**

**Lab 3**

**Combinational Circuits: Structural Modeling Simulation**

**Question No.1**

**(a) Truthtable of the circuit shown in Fig. 2.17**

**(b) Errors found in the codes (Listing 4 and 5).**

**Listing 4**

1. Unnecssary use of comma(,) in line no. 6.
2. Missing of word “assign” in line no. 9.
3. Missing symbole of “and gate (&)” in line no. 10.

**Listing 5**

1. Missing instance name in instantiation of module in line no. 7.
2. In line no.12 “carry1” is undefined.
3. In line no. 18 instead of using (a1,b1,c1),(a,b,c) are used.
4. In line no. 20 (c) is used instead of (c1).
5. In line no. 24 (b) is used intead of (b1).
6. In line no. 30 (a) is used insted of (a1).
7. In line no. 36 or 37 word “end” is missing.

**(c) Corrected codes**

**Listing 4**

module full\_adder(

input logic a,

input logic b,

input logic c,

output logic sum,

output logic carry

);

assign sum = (a ^ b) ^ c;

assign carry = (a & b) | (c&(a ^ b));

endmodule

**Listing 5**

module full\_adder\_tb();

logic a1;

logic b1;

logic c1;

logic sum1;

logic carry1;

full\_adder uut(

.a(a1),

.b(b1),

.c(c1),

.sum(sum1),

.carry(carry1)

);

initial

begin

// Provide different combinations of the inputs to check validity of code

a1 = 0; b1 = 0; c1 = 0;

#10;

a1 = 0; b1 = 0; c1 = 1;

#10;

a1 = 0; b1 = 1; c1 = 0;

#10;

a1 = 0; b1 = 1; c1 = 1;

#10;

a1 = 1; b1 = 0; c1 = 0;

#10;

a1 = 1; b1 = 0; c1 = 1;

#10;

a1 = 1; b1 = 1; c1 = 0;

#10

a1 = 1; b1 = 1; c1 = 1;

#10;

$stop;

end

endmodule