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| Name: Muhammad Boota | EE-272L Digital Systems Design |
| Reg. No.: 2022-EE-134 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

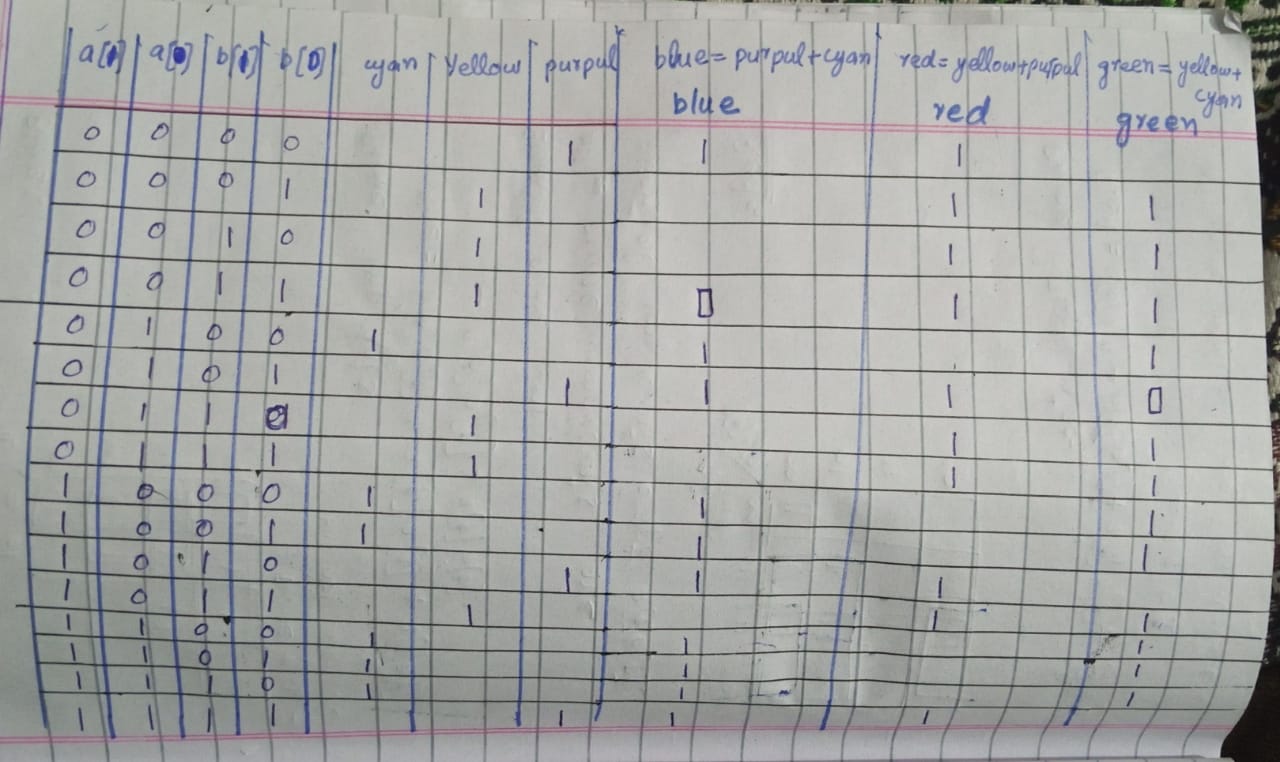
**Lab Manual**

**Lab 4**

**Combinational Circuit Design using K-Map**

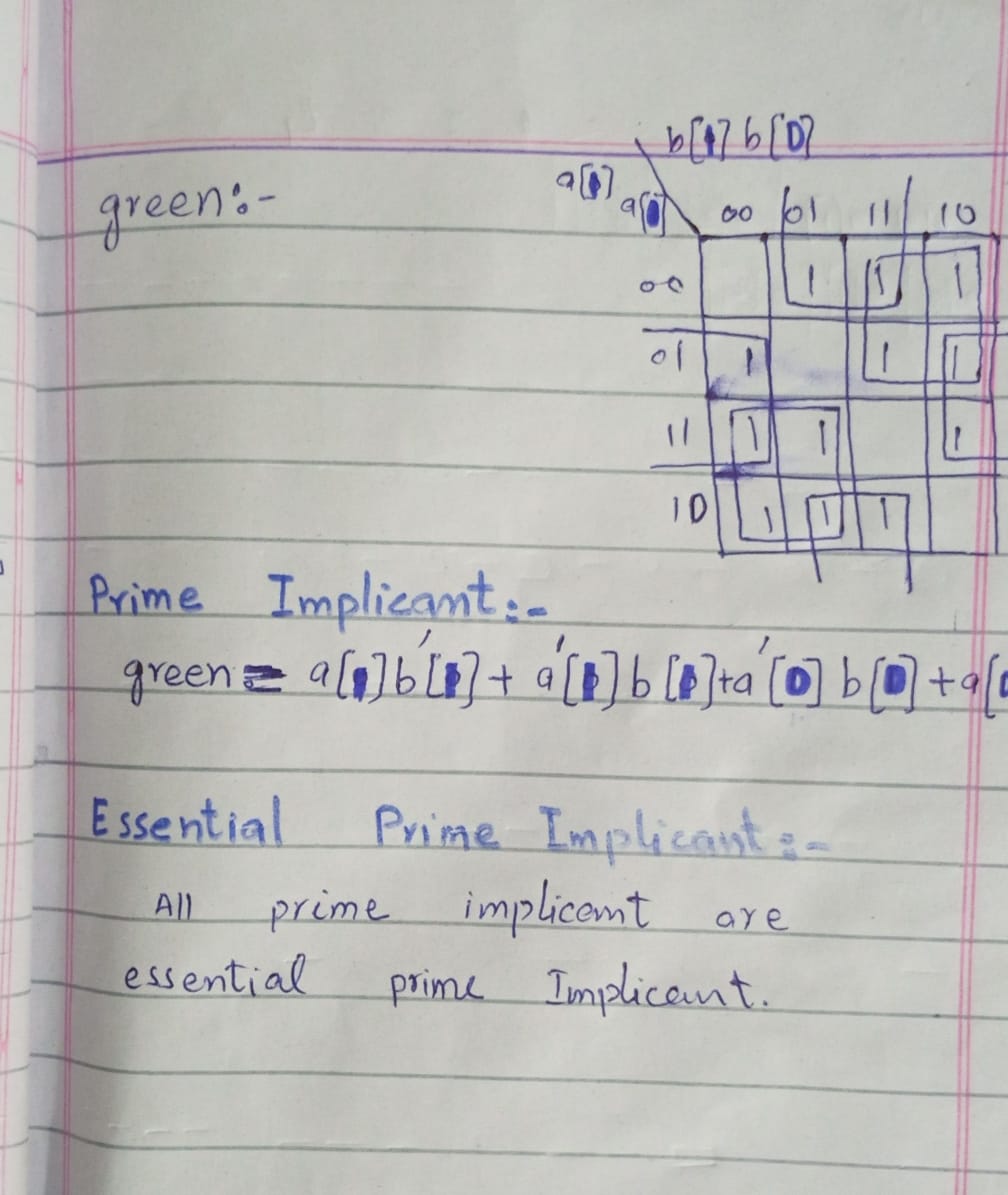
**Question No.1**

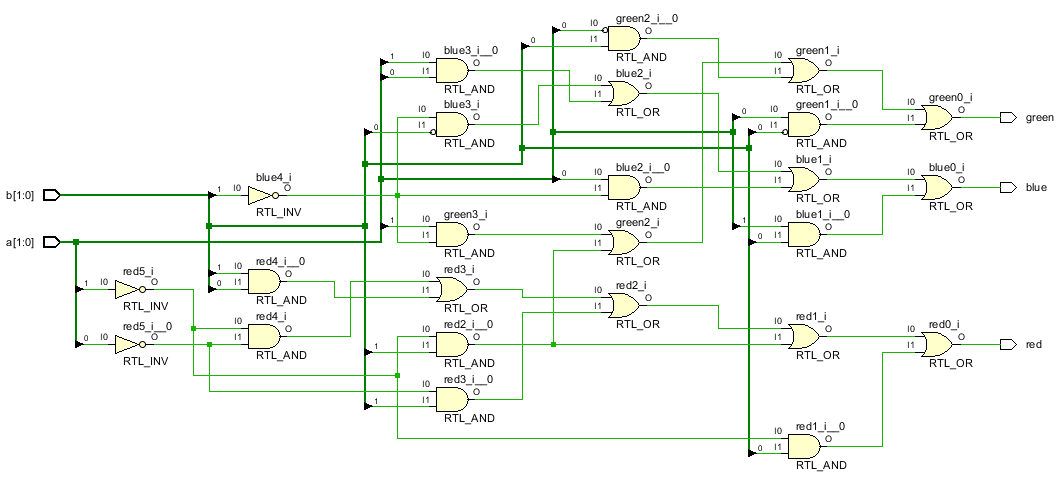
**(a) Truthtable of the circuit**



A notebook with writing on it

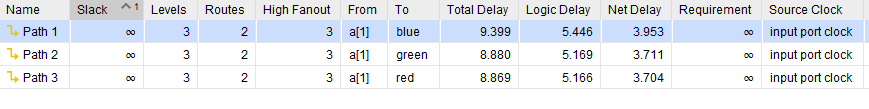
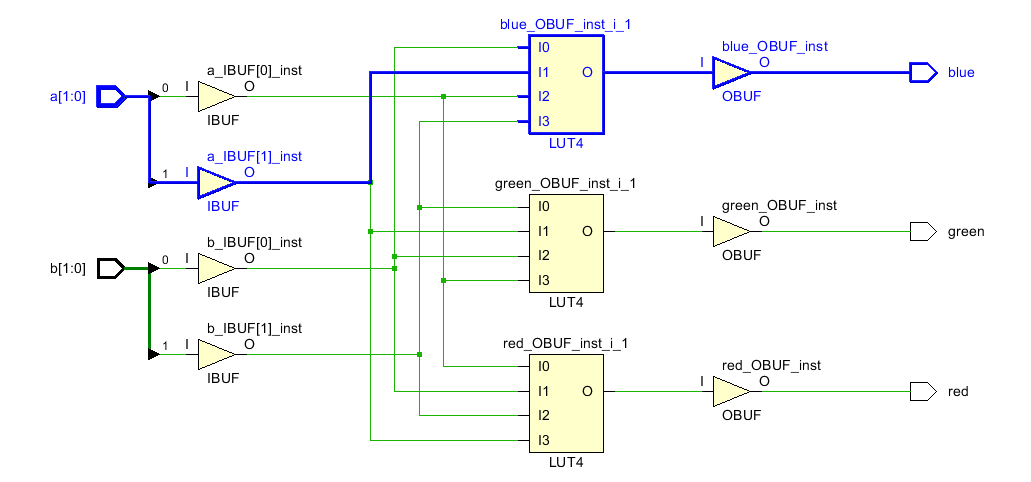
Description automatically generated**(****b)K-maps used to minimize the logic**



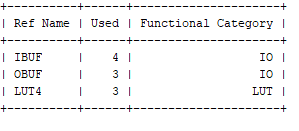
**(****d) Circuit diagram inferred by the Xilinx Vivado**

**(e)Maximum combinational delay in Synthesis:**

Maximum combinational delay is from a[1](input) to blue(output)

**(f) Resource Utilization**

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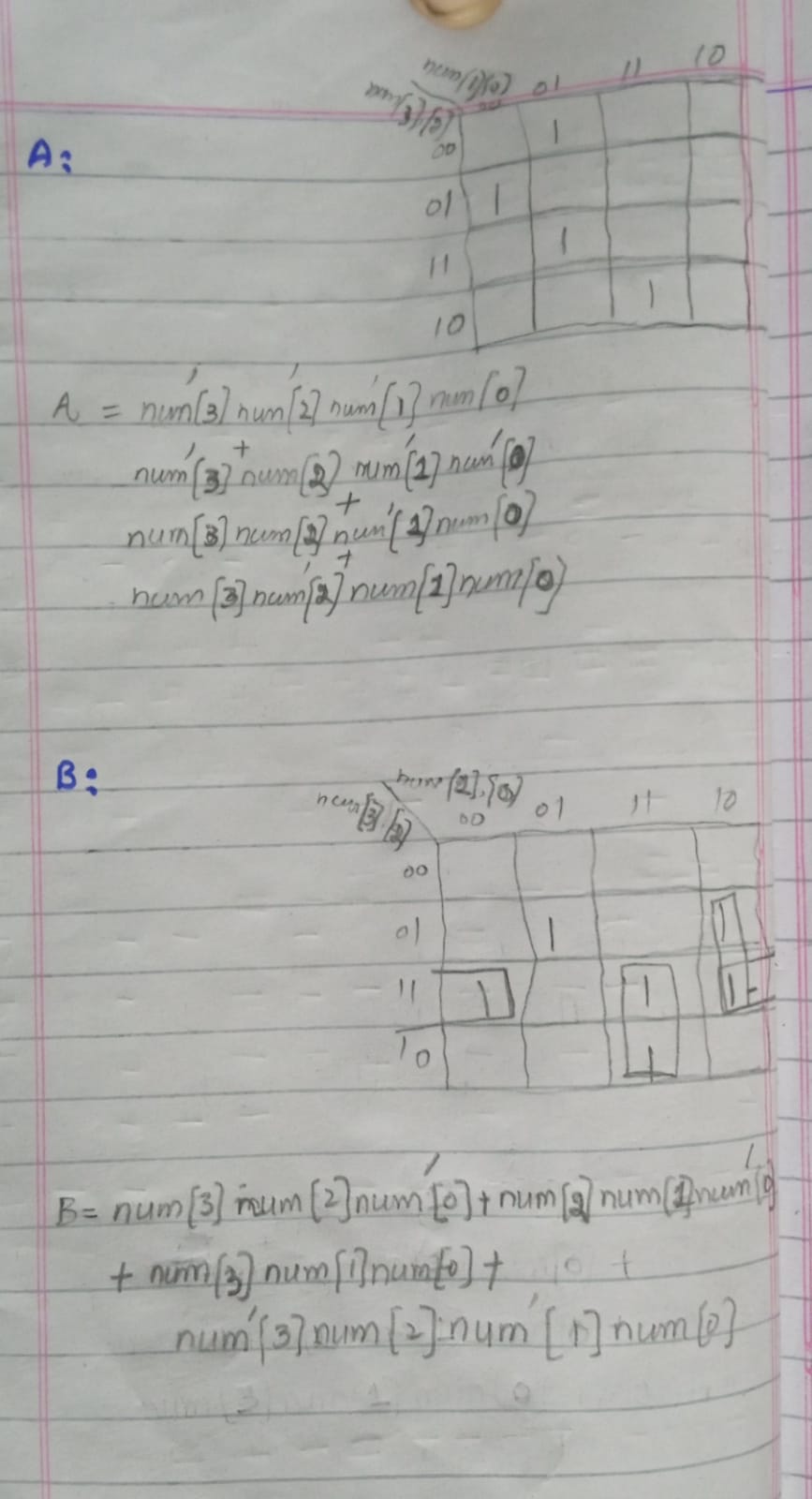
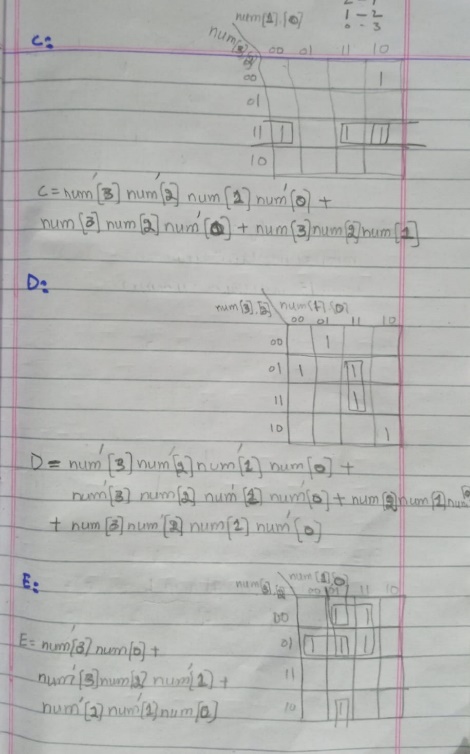
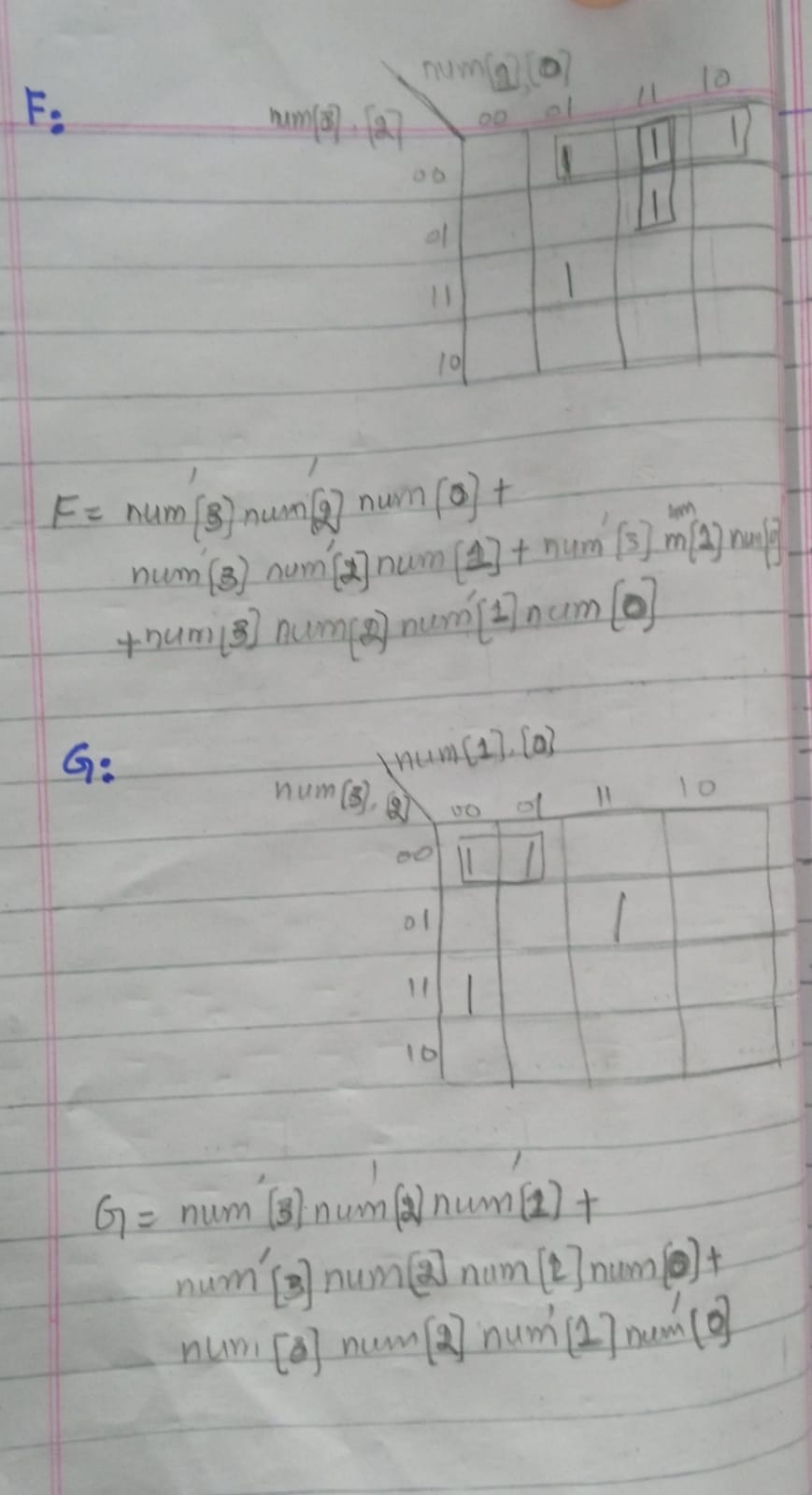
1. **No. of IOs=7**
2. **No. of LUTs=3**

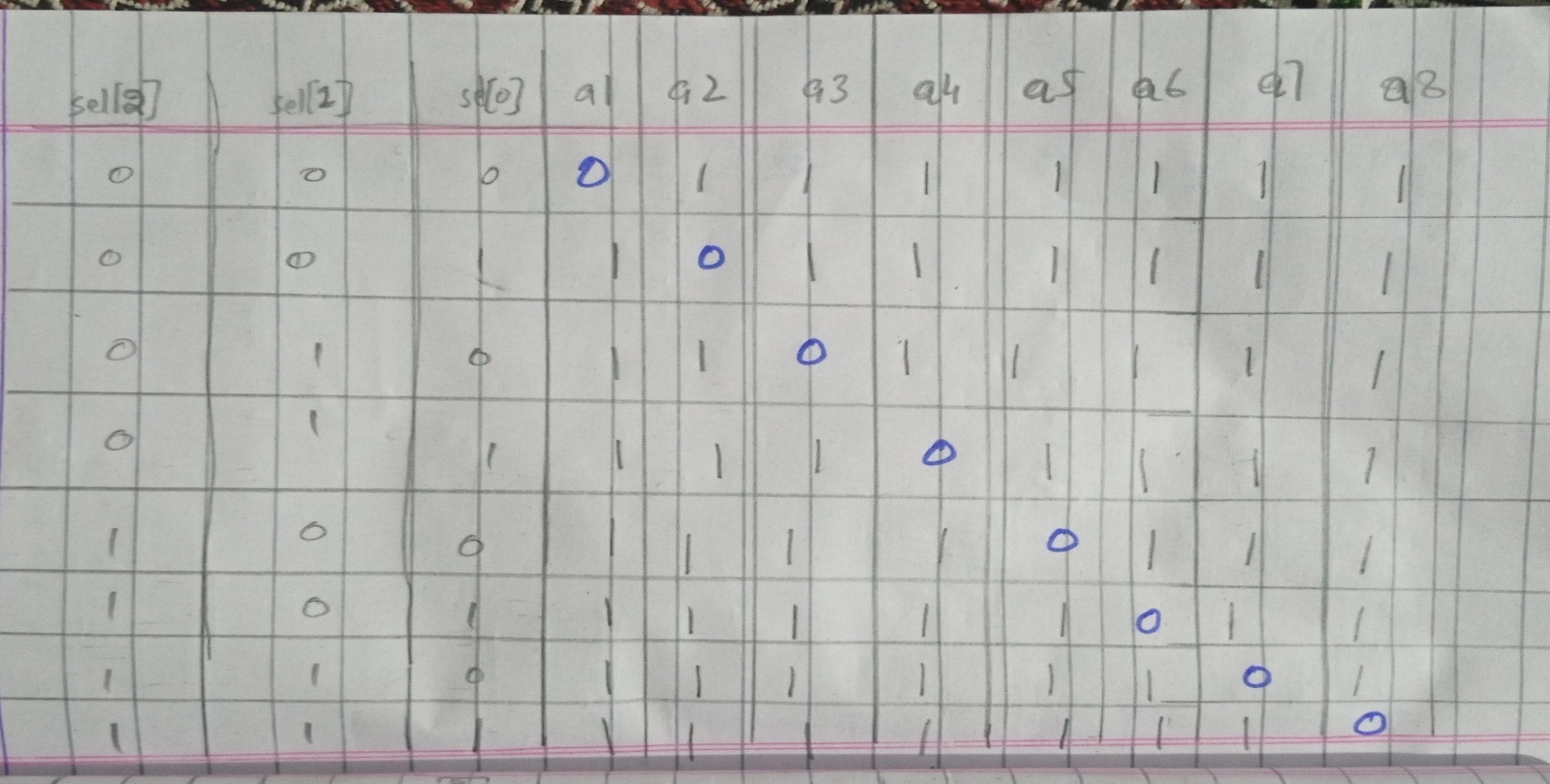
**Question No.2**

1. **Truthtable of the circuit**

A sheet of paper with writing on it

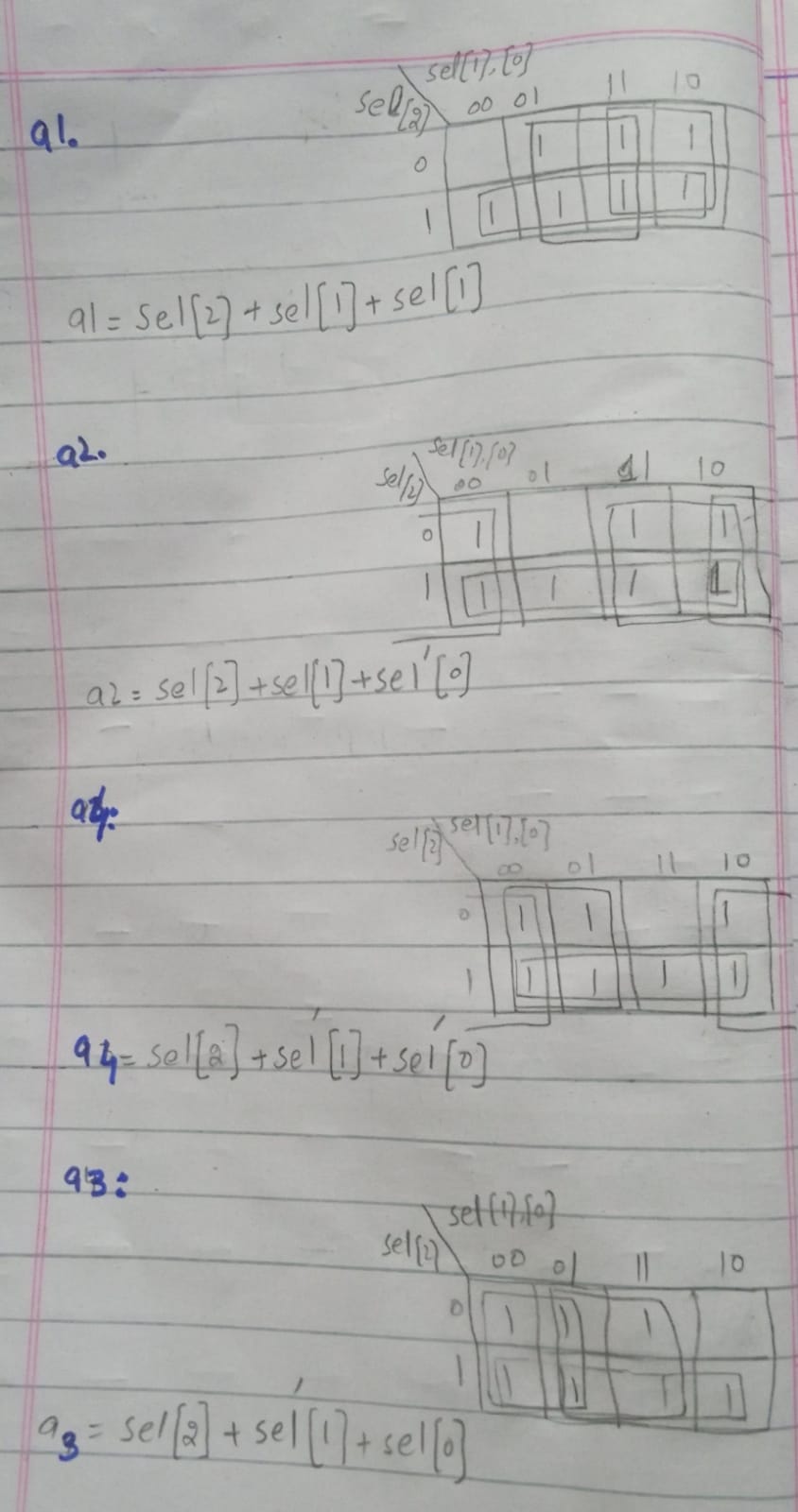
Description automatically generated**(i)**

**b)K-maps used to minimize the logic**

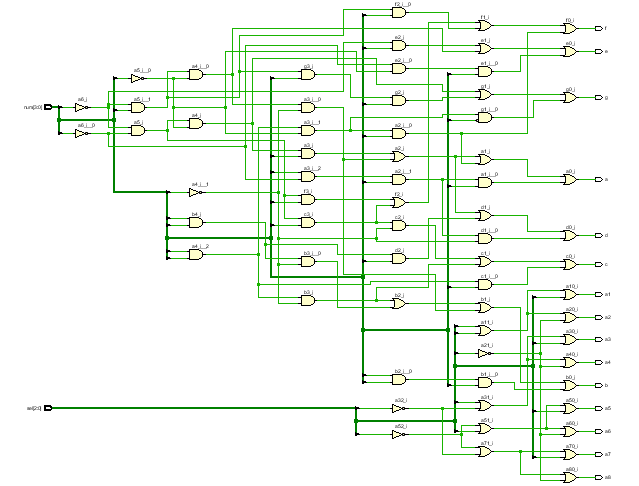
**(ii)**

**b) K-maps used to minimize the logic**

A notebook with writing on it

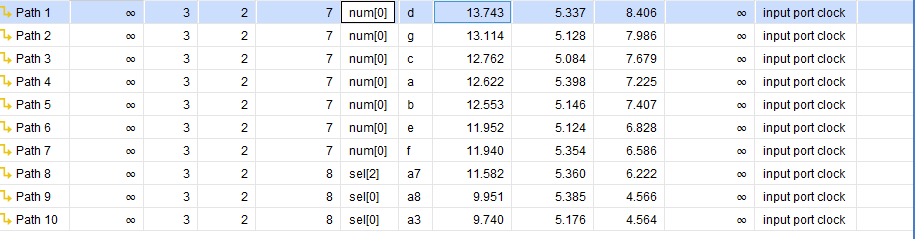
Description automatically generated

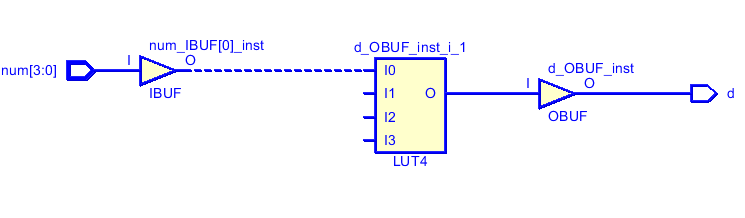
**d) Circuit diagram inferred by the Xilinx Vivado**

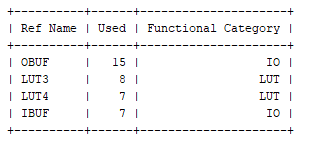
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**(e)Maximum combinational delay in Synthesis:**

Maximum combinational delay is from num[0](input) to d(output)



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**(f) Resource Utilization**

**No. of IOs=22**

**No. of LUTs=15**