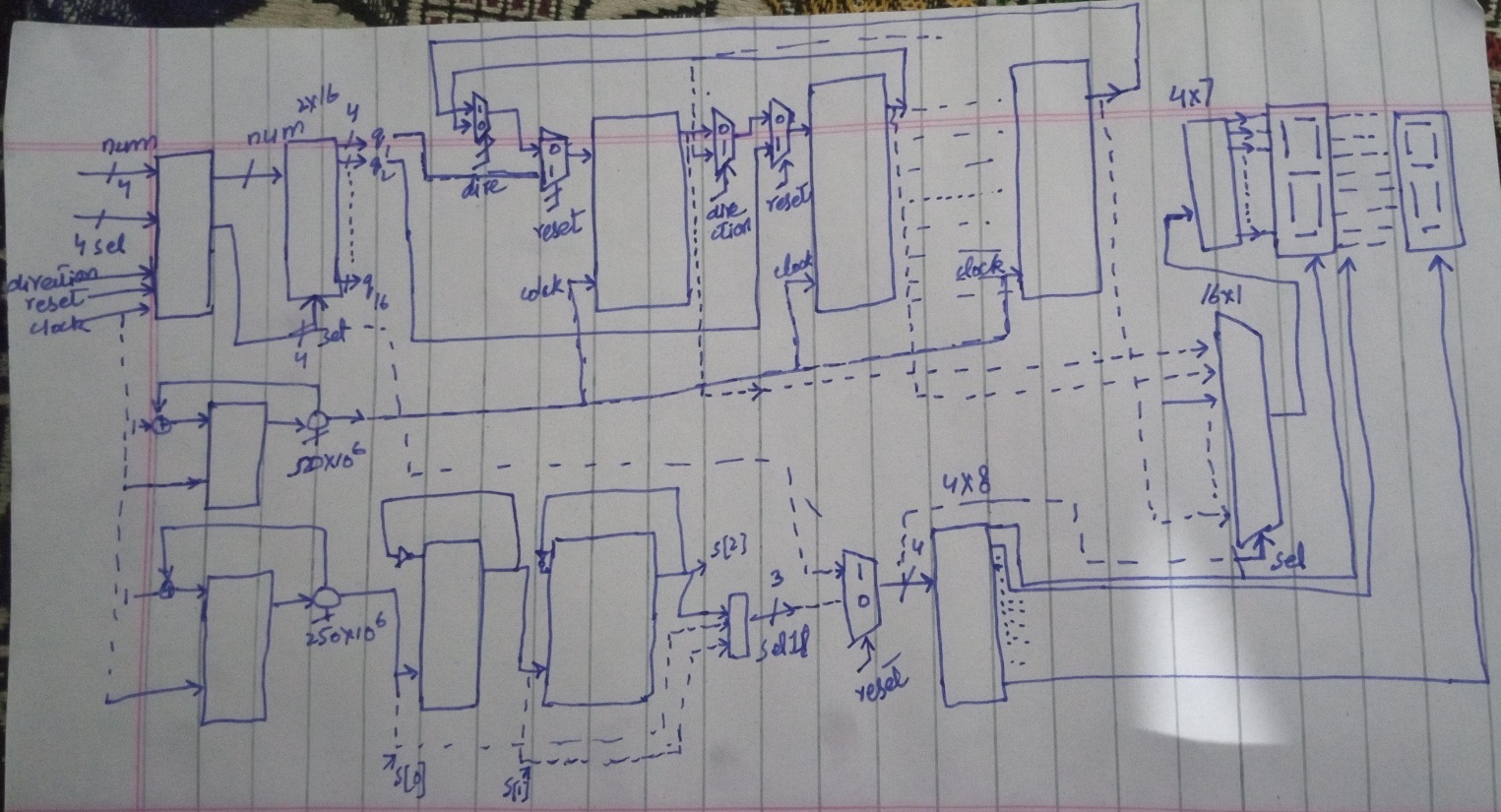
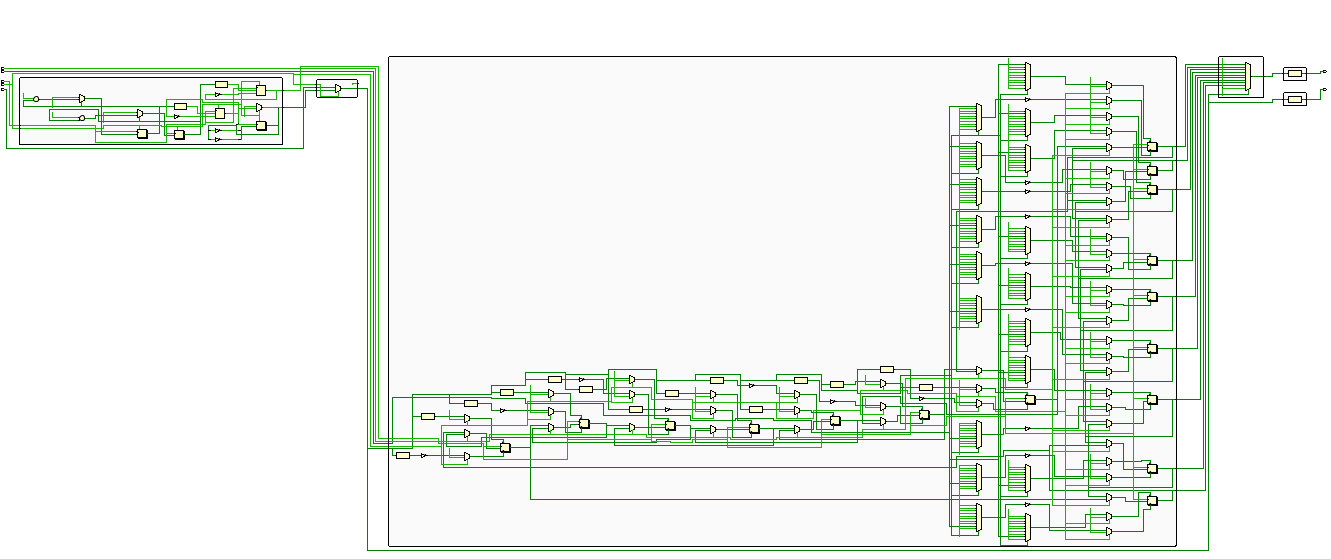
|  |  |
| --- | --- |
| Name: Muhammad Boota | EE-272L Digital Systems Design |
| Reg. No.: 2022-EE-134 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

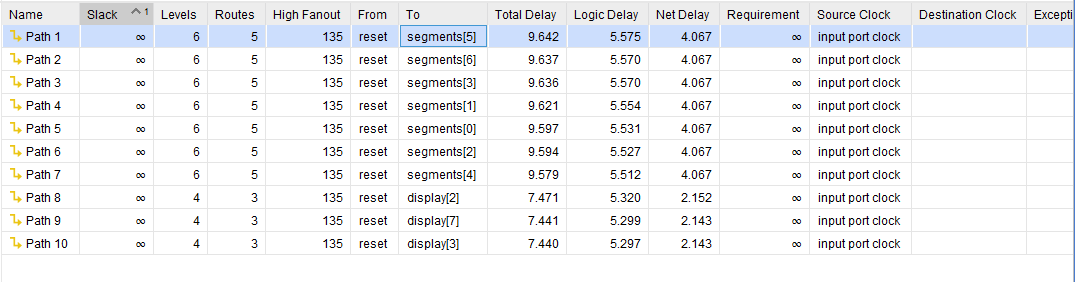
**Lab Report**

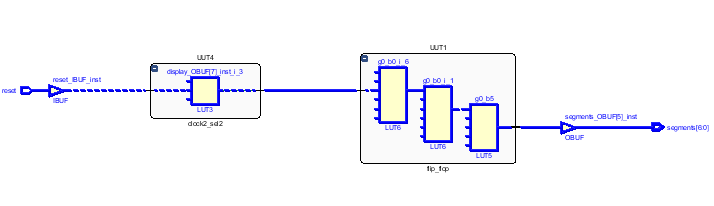
**Lab 8**

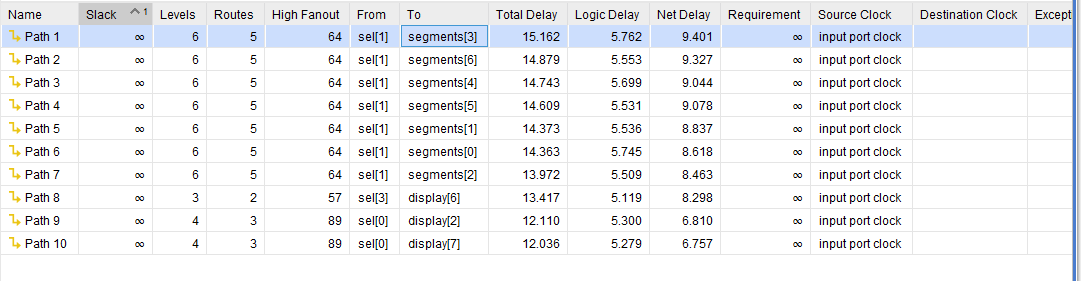
1. circuit design:
2. hand sketched.
3. A diagram of a circuit

   Description automatically generatedSchematic diagram



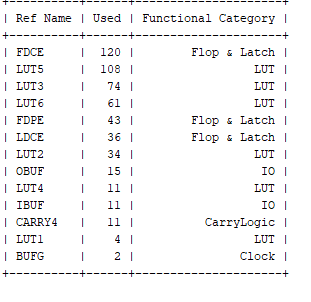
1. Synthesis maximum combinational delay.

Path (from reset to segment [5]) has the maximum synthesis combinational delay which is 9.642ns.

1. Implementation maximum combinational delay

Path (from sel[1] to segment [3]) has the maximum implementation combinational delay which is 15.162ns.

1. Resource Utilization Report.



No. of LUTs=292.

No. of IOs=26.

No. of Flip-flops =199