Solution 1

Question 1

Exercise 4.7

1. R-type : 30 + 250 + 150 + 25 + 200 + 25 + 20 = 700ps
2. ld : 30 + 250 + 150 + 25 + 200 + 250 + 25 + 20 = 950ps
3. sd : 30 + 250 + 150 + 25 + 200 + 250 = 905ps
4. beq : 30 + 250 + 150 + 25 + 200 + 5 + 25 + 25 + 20 = 730ps
5. I-type : 30 + 250 + 150 + 25 + 200 + 25 + 20 = 700ps

Question 2

Exercise 4.16

1. Pipelined: 350; non-pipelined: 1250
2. Pipelined: 1750; non-pipelined: 1250
3. Split the ID stage. This reduces the clock-cycle time to 300ps.
4. 35%
5. 65% or 85%

Question 3

Exercise 4.20

```
addi x11, x12, 5
NOP
NOP
add x13, x11, x12
addi x14, x11, 15
NOP
add x15, x13, x12
```

Question 4

Exercise 4.23

1. The clock period won't change because we aren't making any changes to the slowest stage.
2. Moving the MEM stage in parallel with the EX stage will eliminate the need for a cycle between loads and operations that use the result of the loads. This can

potentially reduce the number of stalls in a program.

3. Removing the offset from ld and sd may increase the total number of instructions because some ld and sd instructions will need to be replaced with a addi/ld or addi/sd pair.