HW1

Q1:

1. The latency of an R type instruction is (30+250+150+25+200+25+20) = 700ps
2. The latency of an ld is (30+250+150+25+200+250+25+20) = 950ps
3. The latency of an sd is (30+250+150+200+25+250) = 905ps
4. The latency of an beq is (30+250+150+25+200+5+25+20) = 705ps
5. The latency of an I type instruction is (30+250+150+25+200+25+20) = 700 ps
6. The minimum clock period if CPU is 950ps

Q2:

1. The clock cycle time in a pipelined is 350

   The clock cycle time in a non-pipelined is 1250

2. The total latency of an **ld** instruction in a pipelined is 1250

   The total latency of an **ld** instruction in a non-pipelined is 1250

3. we will split ID stage,This reduces the clock-cycle time to 300ps
4. The utilization of the data memory is 35%
5. The utilization of the write-register port of the "Registers" unit is 50%

Q3:

```
addi x11,x12,5
NOP
NOP
add x13,x11,x12
addi x14,x11,15
NOP
add x15,x13,x12
```

Q4:

1. The clock period don’t be changed ,because the slowest way don’t change.
2. Moving the MEM and EX stage will decrease the need for a cycle between loads and operations that use the result of the loads.
3. If we cancel the offset from ld and sd may increase the total number of instructions