Homework 4

答题版本 2021.07.15 00:44

试卷得分 12

1. 5.4 Say we have a memory consisting of 256 locations, and each location contains 16 bits.

   a. How many bits are required for the address?

   b. If we use the PC-relative addressing mode, and want to allow control transfer between instructions 20 locations away, how many bits of a branch instruction are needed to specify the PC-relative offset?

   c. If a control instruction is in location 3, what is the PC-relative offset of address 10? Assume that the control transfer instructions work the same way as in the LC-3.

简答题 (3 分) 0 分

a. 9 bits
b. 5 bits
c. 7

2. 5.9 We would like to have an instruction that does nothing. Many ISAs actually have an opcode devoted to doing nothing. It is usually called NOP, for NO OPERATION. The instruction is fetched, decoded, and executed. The execution phase is to do nothing! Which of the following three instructions could be used for NOP and have the program still work correctly?

   a. 0001001001100000
   b. 0000111000000001
   c. 0000 000 000000000

   What does the ADD instruction do that the others do not do?

简答题 (2 分) 1 分

(a) Add R1, R1, ~=0 differs from a NOP in that it sets the data.
(b) BR (n+z+p~=1) Unconditionally branches to one after the next address in the PC. There- fore no, this instruction is not the same as NOP.
(c) Branch that is never taken. Yes same as NOP.

教师评语:
ADD干了啥

3. 5.16 Which LC-3 addressing mode makes the most sense to use under the following conditions? (There may be more than one correct answer to each of these; therefore, justify your answers with some explanation.)

   a. You want to load one value from an address that is less than ±2^8 locations away.

   b. You want to load one value from an address that is more than 2^8 locations away.

   c. You want to load an array of sequential addresses.

简答题 (3 分)　3 分

a. Base + Offset mode explanation: because the range is [-2^8,+2^8],and the mode have 6 bits as a signed offset
b. Load Effective Addressing mode and Indirect Addressing Mode; explanation : it have 9bits signed offset
c. PC_relative mode ; explanation: we want to load an array , so we could use the mode.

4. 5.34 Using the overall data path in Figure 5.18, identify the elements that implement the NOT instruction of Figure 5.4.

   5.35 Using the overall data path in Figure 5.18, identify the elements that implement the ADD instruction of Figure 5.5.

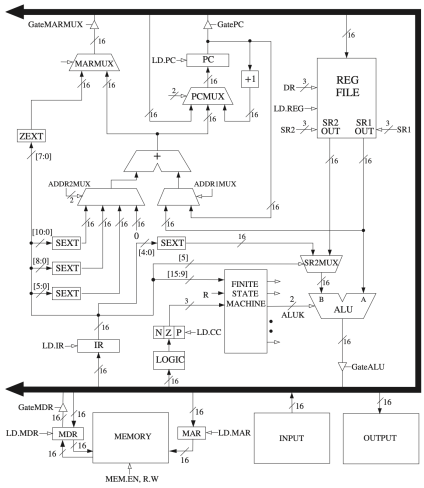
   5.36 Using the overall data path in Figure 5.18, identify the elements that implement the LD instruction of Figure 5.7.

   5.37 Using the overall data path in Figure 5.18, identify the elements that implement the LDI instruction of Figure 5.8.

   5.38 Using the overall data path in Figure 5.18, identify the elements that implement the LDR instruction of Figure 5.9.

   5.39 Using the overall data path in Figure 5.18, identify the elements that implement the LEA instruction of Figure 5.6.

   Hint: You can use 1 figure to solve these all questions. Copy or screenshot on Figure 5.18 and point out the structures used in different instructions.



简答题 (6 分)　6 分

NOT: figure1 ALU and REG but the LOGIC and finite state machine are also important
ADD: figure 2 ALU SR2MUX REG SEXT IR but the LOGIC and finite state machine are also important
LD : figure 3 IR SEXT REG ADD PC MAR MDR MEMORY but the LOGIC and finite state machine are also important
LDI: figure 4 IR SEXT REG ADD PC MAR MDR MEMORY but the LOGIC and finite state machine are also important
LDR: figure 5 IR SEXT ADD REG MAR MDR MEMORY and logic but the LOGIC and finite state machine are also important
LEA: figure 6 REG IR SEXT PC ADD but the finite state machine are also important

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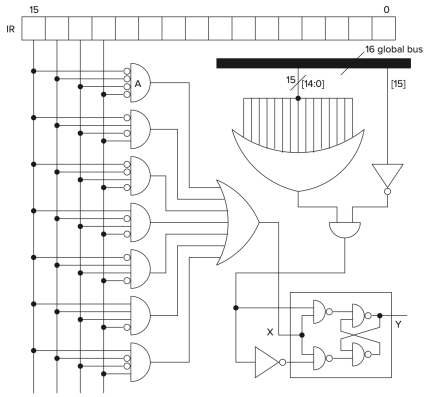
3.jpg

5. 5.41 A part of the implementation of the LC-3 architecture is shown in the following diagram.

a. What information does Y provide?

b. The signal X is the control signal that gates the gated D latch. Is there an error in the logic that produces X?

Hint: The error is gate marked 'A'. So do not be confused when answering the question a.



简答题 (2 分)　2 分

a: if the global bus data is positive ,then the input of the storage element is 1, so y is 1. But if the global bus data is zero or negative ,the input of the input of the storage element is 0.
SO the Y is the condition P code.
b: the input of X means the oldest input will be storage in storage element, so if a opcode can change the state, it will be connect will the gate.
But obviously opcode 0000(BR) shouldn't change the state. so the logic should not have the logic gate A