HW2

Q1

1. we write the code:

```
ld x11,0(x12);
add x3,x4,x5;
add x11,x12,x13;
we insert 1 nop instruction to make it run correctly
ld x11,0(x12);
add x3,x4,x5;
nop
add x11,x12,x13;
```

2.
```
ld  x11, 0(x5)
add x12, x6, x7
nop
nop
add x13, x11, x12
add x28, x29, x30
```

3. we get the stalls per instruction is 0.05* 2 + 0.2* 2 + 0.05 *1 + 0.1 *1 + 0.1 *2 = 0.85,so we get 0.85/1.85=46.7%
4. 20% of instructions will generate one stall for a CPI of 1.2. Th is means that 17% of the cycle are stalls.
5. If we forward from the EX/MEM register only，we get the average of 0.2*2+0.05 *1+0.1+0.1 =0.65 Thus the CPI is 1.65

   If we forward from the MEM/WB register only，we get the average of 0.2*1+0.05 *1+0.1=0.35 Thus the CPI is 1.35
6.

/	Nothing	EX/MEM	MEM/WB	FULL FORWARDING
SPEEDUP	/	1.12	1.37	1.42

Q2

1.
```
add x15, x12, x11
nop
nop
ld x13, 4(x15)
ld x12, 0(x2)
nop
or x13, x15, x13
nop
nop
sd x13, 0(x15)
```

2. If the processor has forwarding, but we forgot to implement the hazard detection unit , the code executes will correct,but if the instruction will a load use the result from load,the code will failed.
3. If there is forwarding , the cycle will be 8

Q3

1. The CPI will be 1.4125,
2. The CPI increases from 1 to 1.3375.
3. The CPI increases from 1 to 1.1125.
4. The speedup will be 1.0375/(1+0.125(1-0.85)) ≈ 1.018
5. The speedup will be 1.0375/(1+0.125*1.15) ≈ 0.907