# 实验 6: RV64 内核线程调度

姓名:	张云策	学号:	3200105787	学院:	计算机科学与技术学院	
课程名称:	计算机系统Ⅱ		同组学生姓名:		/	_
实验时间:	2021.	实验地点:	紫金港机房	指导老师	j: 申文博	

# 一、实验目的和要求

了解线程概念,并学习线程相关结构体,并实现线程的初始化功能。

了解如何使用时钟中断来实现线程的调度。

了解线程切换原理,并实现线程的切换。

掌握简单的线程调度算法,并完成两种简单调度算法的实现。

# 二、实验内容和原理

### 2.1 实验内容

添加 rand.c / rand.h, string.h/string.c, mm.h / mm.c 等函数文件,设计实现 proc.h, proc.c, 完善 entry.S 并且对 defs.h, head.S 以及 makefile 进行修改。

## 2.2 设计模块

● 修改 defs.h

将下列宏添加,发现可以继续运行

```
#define PHY_START 0x0000000080000000
#define PHY_SIZE 128 * 1024 * 1024 // 128MB, QEMU 默认内存大小
#define PHY_END (PHY_START + PHY_SIZE)

#define PGSIZE 0x1000 // 4KB
#define PGROUNDUP(addr) ((addr + PGSIZE - 1) & (~(PGSIZE - 1)))
#define PGROUNDDOWN(addr) (addr & (~(PGSIZE - 1)))
```

● 完成线程初始化

```
#define LAB_TEST_NUM 32;
void task_init() {
      current = (struct task_struct *)TASK_BASE;
      idle = (struct task_struct*)kalloc();
      idle -> state = TASK_RUNNING;
      idle -> counter = 0;
      idle -> priority = 0;
      idle -> pid = 0;
      current = idle;
      task[0] = idle;
      for (int i = 0; i <= LAB_TEST_NUM; i++) {</pre>
         unsigned long ret;
      ret = kalloc();
      task[i] = ret;
      task[i] -> state = TASK_RUNNING;
      task[i] -> counter = 0;
      task[i] -> priority = rand();
      task[i] -> pid = i;
      task[i] -> thread.ra = & dummy;
      task[i] -> thread.sp = ret + PGSIZE;
          if (i != 0) {
              puts("[PID = ");
              puti(task[i]->pid);
              puts("] Process Create Successfully! counter = ");
              puti(task[i]->counter);
              puts(" priority = ");
              puti(task[i]->priority);

√ #endif

              puts("\n");
      }
```

● 完善 entry.S,添加 dummy 和 dummy 部分,设置 spec

```
__dummy:
la t0, dummy
csrw sepc, t0
ecall
sret
```

● 利用\_\_switch\_to 在 entry.S 中实现线程切换,将当今的 ra/sp/S0~S11 寄存到结构中

```
_switch_to:
  li
        a4, 40
  add a3, a0, a4
  add a4, a1, a4
  sd ra,0(a3)
  sd sp,8(a3)
  sd s0,16(a3)
  sd s1,24(a3)
  sd s2,32(a3)
  sd s3,40(a3)
  sd s4,48(a3)
  sd s5,56(a3)
  sd s6,64(a3)
  sd s7,72(a3)
  sd s8,80(a3)
  sd s9,88(a3)
  sd s10,96(a3)
  sd s11,104(a3)
  ld ra,0(a4)
  ld sp,8(a4)
  ld s0,16(a4)
  ld s1,24(a4)
  ld s2,32(a4)
  ld s3,40(a4)
  ld s4,48(a4)
  ld s5,56(a4)
  ld s6,64(a4)
  ld s7,72(a4)
  ld s8,80(a4)
  ld s9,88(a4)
  ld s10,96(a4)
  ld s11,104(a4)
  la t0, current
  sd a1,0(t0)
  mv t0, a1
  addi t0, t0, 40
  ld ra, 0(t0)
  ld sp, 8(t0)
  addi t0, t0, 0x10
  ld s0, 0(t0)
  ld s1, 8(t0)
  ld s2, 16(t0)
  ld s3, 24(t0)
  ld s4, 32(t0)
  ld s5, 40(t0)
  ld s6, 48(t0)
  ld s7, 56(t0)
  ld s8, 64(t0)
  ld s9, 72(t0)
  ld s10, 80(t0)
  ld s11, 88(t0)
```

```
void do_timer() {
    puts("[PID = ");
    puti(current->pid);
    puts("] ");
    puts("Context Calculation: ");
    puts("counter = ");
    puti(current->counter);
    puts("\n");
    current->counter--;
    if (current->counter <= 0)</pre>
        schedule();
#else
    current->counter--;
    if (current->counter <= 0)</pre>
        current->counter = (current->pid == 0) ? 5 : 8 - current->pid;
    schedule();
#endif
}
```

#### ● 实现 sjf 调度

```
int i_min_cnt = LAB_TEST_NUM;
_Bool all_zeroes = 1;
for (int i = LAB_TEST_NUM; i > 0; i--)
int i_min_cnt
     if (task[i]->state == TASK_RUNNING) {
          if (task[i]->counter > 0 && task[i]->counter < task[i_min_cnt]->counter ||task[i_min_cnt]->counter == 0)
              all zeroes = 0:
if (all_zeroes) {
  for (int i = 1; i <= LAB_TEST_NUM; i++)
    if (task[i]->state == TASK_RUNNING)
               task[i]->counter = rand();
               puts("[PID = ");
               puti(task[i]->pid);
               puts("] Reset counter = ");
puti(task[i]->counter);
               puts("\n");
     schedule();
     puti(task[i_min_cnt]->pid);
     puti(task[i_min_cnt]->counter);
     puts("\n");
     switch_to(task[i_min_cnt]);
```

#### ● 实现优先级调度

```
int max_pri = __INT_MAX__, i_min_cnt = 1;
for (int i = 1; i <= LAB_TEST_NUM; i++)
    if (task[i]->state == TASK_RUNNING)
        if (task[i]->priority < max_pri) {</pre>
            i_min_cnt = i;
max_pri = task[i]->priority;
        } else if (task[i]->priority == max_pri &&
                   task[i]->counter < task[i_min_cnt]->counter && task[i]->counter > 0)
puti(current->pid);
puts(" to task ");
puti(task[i_min_cnt]->pid);
puts(", prio: ");
puti(task[i_min_cnt]->priority);
puts(", counter: ");
puti(task[i_min_cnt]->counter);
puts("\n");
for (int i = 1; i <= LAB_TEST_NUM; i++)</pre>
    if (task[i]->state == TASK_RUNNING)
        task[i]->priority = rand();
puts("tasks' priority changed\n");
for (int i = 1; i <= LAB_TEST_NUM; i++)
    if (task[i]->state == TASK_RUNNING) {
       puts("[PID = ");
        puti(task[i]->pid);
        puts("] ");
puts("counter = ");
        puts(" priority = ");
        puti(task[i]->priority);
        puts("\n");
switch_to(task[i_min_cnt]);
```

# 三、 主要仪器设备

Dockers in Lab3

## 四、 实验结果与分析

```
oslab@aecaba9cde0:-/lab3$ make run
qenu-system-riscv64: warning: No -blos option specified. Not loading a firmware.
qenu-system-riscv64: warning: This default will change in a future QEMU release. Please use the -
bios option to avoid breakages when this happens.
qenu-system-riscv64: warning: See QEMU's deprecation documentation for details.
ZJU-system lab6
[PID = 1] Process Create Successfully! counter = 7 priority = 5
[PID = 2] Process Create Successfully! counter = 6 priority = 5
[PID = 3] Process Create Successfully! counter = 5 priority = 5
[PID = 4] Process Create Successfully! counter = 5 priority = 5
[PID = 4] Process Create Successfully! counter = 4 priority = 5
[PID = 4] Process Create Successfully! counter = 4 priority = 5
[PID = 1] counter = 7 priority = 1
[PID = 2] counter = 6 priority = 1
[PID = 2] counter = 6 priority = 4
[PID = 3] counter = 6 priority = 4
[PID = 3] counter = 4 priority = 5
[PID = 4] counter = 7 priority = 5
[PID = 1] counter = 7 priority = 5
[PID = 2] counter = 6 priority = 5
[PID = 3] counter = 5 priority = 5
[PID = 3] counter = 6 priority = 5
[PID = 1] counter = 7 priority = 4
[PID = 1] counter = 5 priority = 4
[PID = 1] counter = 6 priority = 4
[PID = 1] counter = 6 priority = 4
[PID = 1] counter = 5 priority = 5
[PID = 1] counter = 6 priority = 5
[PID = 1] counter = 6 priority = 5
[PID = 1] counter = 6 priority = 4
[PID = 1] counter = 5 priority = 4
[PID = 1] counter = 5 priority = 4
[PID = 1] counter = 5 priority = 4
[PID = 1] counter = 5 priority = 4
[PID = 1] counter = 5 priority = 4
[PID = 1] counter = 5 priority = 5
[PID = 3] counter = 5 priority = 5
[PID = 3] counter = 5 priority = 5
[PID = 3] counter = 5 priority = 5
[PID = 3] counter = 5 priority = 5
[PID = 1] counter = 6 priority = 5
[PID = 2] counter = 6 priority = 5
[PID = 2] counter = 6 priority = 5
[PID = 3] counter = 5 priority = 6
[PID = 1] counter = 6 priority = 5
[PID = 2] counter = 6 priority = 5
[PID = 3] counter = 6 priority = 5
[PID = 3] counter = 6 priority = 5
[PID = 3] counter = 6 priority = 5
[PID =
```

```
PID = 1] Context Calculation: counter
       [PID = 1] Process Create Successfully! counter = 1
[PID = 2] Process Create Successfully! counter = 4
[PID = 3] Process Create Successfully! counter = 5
[PID = 4] Process Create Successfully! counter = 4
[PID = 2] Process Create Successfully! counter = 4
[PID = 3] Process Create Successfully! counter = 5
[PID = 4] Process Create Successfully! counter = 6
[PID = 4] Process Create Successfully! counter = 6
[1] Switch from task 0 [task struct: 0xffffffe000020000, sp: 0xffffffe000021000] to task 1 [task struct: 0xffffffe000021000], prio: 5, counter: 1
[PID = 1] Context Galculation: counter = 1
[1] Switch from task 1 [task struct: 0xffffffe000021000, sp: 0xffffffe000022000] to task 4 [task struct: 0xffffffe000021000], prio: 5, counter: 4
[PID = 4] Context Calculation: counter = 3
[PID = 4] Context Calculation: counter = 3
[PID = 4] Context Calculation: counter = 2
[PID = 4] Context Calculation: counter = 2
[PID = 4] Context Calculation: counter = 4
[PID = 2] Context Calculation: counter = 4
[PID = 2] Context Calculation: counter = 4
[PID = 2] Context Calculation: counter = 3
[PID = 2] Context Calculation: counter = 3
[PID = 2] Context Calculation: counter = 2
[PID = 2] Context Calculation: counter = 4
[PID = 3] Context Calculation: counter = 5
[PID = 3] Context Calculation: counter = 4
[PID = 3] Context Calculation: counter = 4
[PID = 3] Context Calculation: counter = 2
[PID = 4] Reset counter = 5
[PID = 3] Reset counter = 5
[PID = 4] Reset counter = 5
[PID = 4] Context Calculation: counter = 5
[PID = 4] Context Calculation: counter = 2
[PID = 4] Context Calculation: counter = 4
[PID = 4] Context Calculation: counter = 5
[PID = 4] Context Calculation: counter = 5
[PID = 4] Context Calculation: counter = 5
[PID = 3] Context Calculation: counter = 5
[PI
     [!] Switch from task 3 [task struct: 0xffffffe000023000, sp: 0xffffffe000023f00] to task 2 [task
```

#### 在 SJF 模式下:

```
[PID = 31] Process Create Successfully! counter = 4
[PID = 32] Process Create Successfully! counter = 2
[PID = 33] Process Create Successfully! counter = 2
[PID = 34] Process Create Successfully! counter = 2
[PID = 35] Process Create Successfully! counter = 5
[PID = 36] Process Create Successfully! counter = 5
[PID = 37] Process Create Successfully! counter = 5
[PID = 38] Process Create Successfully! counter = 5
[PID = 39] Process Create Successfully! counter = 5
[PID = 39] Process Create Successfully! counter = 5
[PID = 40] Process Create Successfully! counter = 5
[PID = 41] Process Create Successfully! counter = 2
[PID = 42] Process Create Successfully! counter = 3
[PID = 43] Process Create Successfully! counter = 3
[PID = 44] Process Create Successfully! counter = 2
[PID = 45] Process Create Successfully! counter = 5
[PID = 46] Process Create Successfully! counter = 2
[PID = 47] Process Create Successfully! counter = 5
[PID = 48] Process Create Successfully! counter = 5
[PID = 49] Process Create Successfully! counter = 5
[PID = 51] Process Create Successfully! counter = 5
[PID = 50] Process Create Successfully! counter = 5
[PID = 51] Process Create Successfully! counter = 5
[PID = 52] Process Create Successfully! counter = 2
[PID = 53] Process Create Successfully! counter = 3
[PID = 54] Process Create Successfully! counter = 3
[PID = 55] Process Create Successfully! counter = 2
[PID = 56] Process Create Successfully! counter = 1
[PID = 58] Process Create Successfully! counter = 1
[PID = 58] Process Create Successfully! counter = 1
[PID = 59] Process Create Successfully! counter = 1
[PID = 59] Process Create Successfully! counter = 1
[PID = 50] Process Create Successfully! counter = 1
[PID = 50] Process Create Successfully! counter = 3
[PID = 51] Process Create Successfully! counter = 3
[PID = 52] Process Create Successfully! counter = 3
[PID = 59] Process Create Successfully! counter = 1
[PID = 58] Process Create Successfully! counter = 3
[PID = 59] Process Create Successfully! counter = 3
[PID = 50] Proces
```

```
[PID = 59] Context Calculation: counter = 1
[!] Switch from task 59 to task 57, prio: 5, counter: 1
[PID = 57] Context Calculation: counter = 1
[!] Switch from task 57 to task 55, prio: 5, counter: 1
[PID = 55] Context Calculation: counter = 1
[!] Switch from task 57 to task 55, prio: 5, counter: 1
[PID = 55] Context Calculation: counter = 1
[!] Switch from task 43 to task 41, prio: 5, counter: 1
[PID = 43] Context Calculation: counter = 1
[!] Switch from task 43 to task 41, prio: 5, counter: 1
[PID = 41] Context Calculation: counter = 1
[!] Switch from task 41 to task 27, prio: 5, counter: 1
[PID = 27] Context Calculation: counter = 1
[!] Switch from task 27 to task 21, prio: 5, counter: 1
[PID = 21] Context Calculation: counter = 1
[!] Switch from task 21 to task 1, prio: 5, counter: 1
[PID = 1] Context Calculation: counter = 1
[!] Switch from task 1 to task 54, prio: 5, counter: 2
[PID = 54] Context Calculation: counter = 2
[PID = 54] Context Calculation: counter = 2
[PID = 50] Context Calculation: counter = 2
[PID = 45] Context Calculation: counter = 2
[PID = 45] Context Calculation: counter = 2
[PID = 46] Context Calculation: counter = 2
[PID = 47] Context Calculation: counter = 2
[PID = 48] Context Calculation: counter = 2
[PID = 34] Context Calculation: counter = 2
[PID = 34] Context Calculation: counter = 1
[!] Switch from task 45 to task 40, prio: 5, counter: 2
[PID = 34] Context Calculation: counter = 2
[PID = 33] Context Calculation: counter = 1
[!] Switch from task 34 to task 33, prio: 5, counter: 2
[PID = 33] Context Calculation: counter = 2
[PID = 36] Context Calculation: counter = 2
[PID = 38] Context Calculation: counter = 2
[PID = 38] Context Calculation: counter = 2
[PID = 8] Context Calcul
```

#### 在 Priority 模式下:

```
## Priority 快工 下:

File Edit View Search Terminal Help

[PID = 51] counter = 5 priority = 4

[PID = 52] counter = 5 priority = 4

[PID = 53] counter = 5 priority = 4

[PID = 53] counter = 5 priority = 3

[PID = 54] counter = 5 priority = 2

[PID = 56] counter = 5 priority = 1

[PID = 57] counter = 5 priority = 5

[PID = 58] counter = 5 priority = 5

[PID = 59] counter = 5 priority = 5

[PID = 60] counter = 5 priority = 1

[PID = 61] counter = 5 priority = 4

[PID = 62] counter = 5 priority = 4

[PID = 63] counter = 5 priority = 4

[PID = 63] counter = 7 priority = 4

[PID = 2] counter = 7 priority = 4

[PID = 2] counter = 6 priority = 3

[PID = 1] counter = 7 priority = 4

[PID = 3] counter = 5 priority = 2

[PID = 4] counter = 5 priority = 5

[PID = 6] counter = 5 priority = 5

[PID = 7] counter = 5 priority = 4

[PID = 9] counter = 5 priority = 4

[PID = 9] counter = 5 priority = 4

[PID = 1] counter = 5 priority = 5

[PID = 13] counter = 5 priority = 1

[PID = 14] counter = 5 priority = 2

[PID = 15] counter = 5 priority = 1

[PID = 16] counter = 5 priority = 1

[PID = 17] counter = 5 priority = 1

[PID = 18] counter = 5 priority = 1

[PID = 19] counter = 5 priority = 1

[PID = 19] counter = 5 priority = 1

[PID = 19] counter = 5 priority = 1

[PID = 20] counter = 5 priority = 1

[PID = 21] counter = 5 priority = 1

[PID = 22] counter = 5 priority = 1

[PID = 23] counter = 5 priority = 1

[PID = 24] counter = 5 priority = 1

[PID = 25] counter = 5 priority = 5

[PID = 27] counter = 5 priority = 1

[PID = 28] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[PID = 29] counter = 5 priority = 5

[
                   File Edit View Search Terminal Help
               [PID = 25] counter = 5 priority = 1
[PID = 26] counter = 5 priority = 1
[PID = 27] counter = 5 priority = 5
[PID = 28] counter = 5 priority = 5
[PID = 29] counter = 5 priority = 1
```

```
[PID = 47] counter = 5 priority = 2
[PID = 48] counter = 5 priority = 2
[PID = 49] counter = 5 priority = 2
[PID = 50] counter = 5 priority = 5
[PID = 51] counter = 5 priority = 5
[PID = 51] counter = 5 priority = 5
[PID = 52] counter = 5 priority = 4
[PID = 53] counter = 5 priority = 4
[PID = 54] counter = 5 priority = 2
[PID = 55] counter = 5 priority = 1
[PID = 55] counter = 5 priority = 1
[PID = 57] counter = 5 priority = 1
[PID = 57] counter = 5 priority = 1
[PID = 58] counter = 5 priority = 5
[PID = 68] counter = 5 priority = 5
[PID = 60] counter = 5 priority = 5
[PID = 61] counter = 5 priority = 5
[PID = 62] counter = 5 priority = 5
[PID = 63] counter = 5 priority = 5
[PI] Switch from task as to task 16, prio: 1, counter: 1
tasks' priority changed
[PID = 1] counter = 7 priority = 5
[PID = 2] counter = 6 priority = 3
[PID = 3] counter = 2 priority = 3
[PID = 4] counter = 4 priority = 4
[PID = 5] counter = 5 priority = 1
[PID = 7] counter = 5 priority = 1
[PID = 8] counter = 5 priority = 1
[PID = 10] counter = 5 priority = 1
[PID = 11] counter = 5 priority = 1
[PID = 12] counter = 5 priority = 3
[PID = 13] counter = 5 priority = 3
[PID = 14] counter = 5 priority = 3
[PID = 15] counter = 5 priority = 3
[PID = 16] counter = 5 priority = 3
[PID = 17] counter = 5 priority = 3
[PID = 18] counter = 5 priority = 3
[PID = 19] counter = 5 priority = 3
[PID = 19] counter = 5 priority = 3
[PID = 19] counter = 5 priority = 3
[PID = 19] counter = 5 priority = 3
[PID = 19] counter = 5 priority = 3
[PID = 19] counter = 5 priority = 3
[PID = 19] counter = 5 priority = 3
[PID = 20] counter = 5 priority = 5
[PID = 21] counter = 5 priority = 5
[PID = 22] counter = 5 priority = 5
[PID = 23] counter = 5 priority = 5
[PID = 24] counter = 5 priority = 5
[PID = 25] counter = 5 priority = 5
[PID = 26] counter = 5 priority = 5
[PID = 27] counter = 5 priority = 5
[PID = 28] counter = 5 priority = 5
[PID = 29] counter = 5 priority = 5
[PID = 29] counter = 5 priority = 5
[PID = 29] counter = 5 priority = 5
[PID = 29] counter = 5 prior
```

# 五、 讨论、心得

#### 思考题:

1. context\_switch 中一共存在着 ra、sp、s0~s11 这十四个寄存器,ra 和 sp 寄存器主要用来记录切换对象的栈位置以及程序下一步执行的目的代码,所以需要在进程切换中保存,然后才可以恢复进程的时候程序可以继续运行。

而寄存器 s0~s11 中,s0 是帧指针,s1 的作用是"保存寄存器",而寄存器 s2-s11,也是在程序运行中需要保存的寄存器,因此在上下文切换中需要保存。

而其他寄存器的值都是临时变量的值,没有必要保存。

2. 进入\_traps(1),随后进入 schedule 函数(2),进入 switch\_to 函数,可以得出结论: ra 的值就是 schedule 的地址(3),再次进入\_switch\_to 函数,ra 变成了调用\_switch\_to 的switch\_to 地址(4),完成上下文切换后,ra 变成了\_\_dummy 的地址(预设地址)(5),在切换完成后,返回地址写入前,ra 为 switch\_to 的地址(6),写入后,仍为 switch\_to 的地址(7),我们可以得出结论 ra 存储的返回地址和先前函数的调用者地址相同

```
0x80200000 <_stext>
                                      auipc
                                                 sp,0x5
    0x80200004 <_stext+4>
                                                 sp,sp
B+ 0x80200008 <_stext+8>
0x8020000c <_stext+12>
0x80200010 <_stext+16>
                                                 ra,0x80200450 <mm_init>
                                      jal
                                      auipc
                                                 t0,0x0
                                                 t0,t0,96
                                      addi
    0x80200014 <_stext+20>
                                                 stvec,t0
                                      csrw
    0x80200018 <_stext+24>
                                      csrr
                                                 t0,sie
    0x8020001c <_stext+28>
                                      ori
                                                 t0,t0,32
    0x80200020 <_stext+32>
                                      csrw
                                                 sie,t0
    0x80200024 <_stext+36>
0x80200028 <_stext+40>
0x8020002c <_stext+44>
0x80200030 <_stext+48>
                                      rdtime
                                                 t1
                                                 t0,0x989
t0,t0,1664
t1,t1,t0
                                      lui
                                      addiw
                                      add
    0x80200034 <_stext+52>
                                      li
                                                 a7,0
    0x80200038 <_stext+56>
                                      li
                                                 a6,0
    0x8020003c <_stext+60>
                                                 a0,t1
    0x80200040 <_stext+64>
0x80200044 <_stext+68>
0x80200048 <_stext+72>
                                                 a1,0
                                     li
                                     li
                                                 a2,0
                                                 a3,0
a4,0
                                      li
    0x8020004c <_stext+76>
                                     li
    0x80200050 <_stext+80>
                                                 a5,0
                                     li
    0x80200054 <_stext+84>
                                      ecall
    0x80200058 <_stext+88>
                                      csrr
                                                 t0,sstatus
    0x8020005c <_stext+92>
0x80200060 <_stext+96>
0x80200064 < stext+100
                                      ori
                                                 t0,t0,2
                                                 sstatus, t0
                                     csrw
```

(2)

```
0x80200744 <do_timer>
                                             addi
                                                       sp, sp, -16
   0x80200748 <do_timer+4>
0x8020074c <do_timer+8>
                                                       ra,8(sp)
                                             sd
                                             sd
                                                        s0,0(sp)
   0x80200750 <do_timer+12>
                                             addi
                                                       s0,sp,16
   0x80200754 <do_timer+16>
                                             auipc
                                                       a5,0x5
   0x80200758 <do_timer+20>
                                             addi
                                                       a5, a5, -1860
                                                       a4,0(a5)
B+>
                 <do_timer+24>
                                             ld
                 <do_timer+28>
                                             auipc
                                                       a5,0x5
   0x80200764 <do_timer+32>
0x80200768 <do_timer+36>
0x8020076c <do_timer+40>
                                             addi
                                                       a5,a5,-1880
                                             ld
                                                       a5,0(a5)
                                                       a4,a5,0x80200784 <do_timer+64>
                                             beq
   0x80200770 <do_timer+44>
                                             auipc
                                                       a5,0x5
   0x80200774 <do_timer+48>
                                             addi
                                                       a5, a5, -1888
   0x80200778 <do_timer+52>
                                             ld
                                                       a5,0(a5)
   0x8020077c <do_timer+56>
                                                       a5,16(a5)
                                             lα
   0x80200780 <do_timer+60>
0x80200784 <do_timer+64>
                                                       a5,0x80200788 <do_timer+68>
ra,0x80200554 <schedule>
                                             bnez
                                             jal
   0x80200788 <do_timer+68>
0x8020078c <do_timer+72>
                                                       a5,0x5
                                             auipc
                                             addi
                                                       a5, a5, -1912
                                                       a4,0(a5)
   0x80200790 <do_timer+76>
                                             ld
   0x80200794 <do_timer+80>
                                             auipc
                                                       a5,0x5
   0x80200798 <do_timer+84>
                                             addi
                                                       a5, a5, -1932
   0x8020079c <do_timer+88>
0x802007a0 <do_timer+92>
0x802007a4 <do_timer+96>
                                             ld
                                                       a5,0(a5)
                                                       a4,a5,0x802007d0 <do_timer+140>
                                             beq
                                             auipc
                                                       a5,0x5
   0x802007a8 <do_timer+100>
                                             addi
                                                       a5,a5,-1940
   0x802007ac <do_timer+104>
                                             ld
                                                       a5,0(a5)
   0x802007b0 <do_timer+108>
                                             ld
                                                       a5,16(a5)
   0x802007b4 <do_timer+112>
                                                        a5,0x802007d0 <do_timer+140>
                                             beqz
                                                       a5,0x5
   0x802007b8 <do_timer+116>
                                             auipc
   0x802007bc <do_timer+120>
0x802007c0 <do_timer+124>
0x802007c4 <do_timer+128>
                                                       a5,a5,-1960
a5,0(a5)
                                             addi
                                             ld
                                             ld
                                                       a4,16(a5)
```

```
0x802007e4 <switch_to>
0x802007e8 <switch_to+4>
0x802007ec <switch_to+8>
0x802007fc <switch_to+12>
0x802007f4 <switch_to+16>
0x802007f8 <switch_to+20>
0x802007fc <switch_to+24>
                                                                                                                             sp,sp,-32
ra,24(sp)
                                                                                                    addi
                                                                                                    sd
                                                                                                                             s0,16(sp)
                                                                                                    sd
                                                                                                                             s0,sp,32
a0,-24(s0)
                                                                                                    addi
                                                                                                    sd
                                                                                                                             a5,0x5
                                                                                                    auipc
                                                                                                    addi
                                                                                                                             a5, a5, -2024
                                                                                                                             a5,0(a5)
                                                             to+28>
                                                                                                    ld
                                                                                                                            a4,-24(s0)
a4,a5,0x80200848 <switch_to+100>
a5,-24(s0)
 0x80200804 <switch_to+32>
0x80200808 <switch_to+36>
0x8020080c <switch_to+40>
                                                                                                    ld
                                                                                                    beq
0x80200808 <switch_to+36>
0x80200810 <switch_to+40>
0x80200810 <switch_to+44>
0x80200814 <switch_to+48>
0x80200818 <switch_to+52>
0x80200812 <switch_to+56>
0x80200820 <switch_to+60>
0x80200824 <switch_to+64>
0x80200828 <switch_to+68>
0x80200820 <switch_to+72>
0x80200830 <switch_to+72>
0x80200830 <switch_to+76>
0x80200831 <switch_to+80>
0x80200832 <switch_to+80>
0x80200834 <switch_to+80>
0x80200834 <switch_to+80>
0x80200834 <switch_to+92>
0x80200844 <switch_to+92>
0x80200844 <switch_to+100>
0x80200850 <switch_to+100>
0x80200850 <switch_to+104>
0x80200850 <switch_to+112>
0x80200850 <task_init>
0x80200860 <task_init+8>
                                                                                                    ld
                                                                                                                             a4,32(a5)
                                                                                                    ld
                                                                                                                            a5,-24(s0)
a5,16(a5)
                                                                                                    ld
                                                                                                    ld
                                                                                                                             a2,a5
                                                                                                    mν
                                                                                                                             a1,a4
                                                                                                    mν
                                                                                                    auipc
                                                                                                                             a0,0x2
                                                                                                    addi
                                                                                                                             a0,a0,-1948
                                                                                                                             ra,0x80
a5,0x4
                                                                                                                                                 02010e0 <printk>
                                                                                                    jal
                                                                                                    auipc
                                                                                                                            a5,a5,2016
a5,0(a5)
                                                                                                    addi
                                                                                                    ld
                                                                                                    ld
                                                                                                                             a1,-24(s0)
                                                                                                                             a0,a5
                                                                                                    mν
                                                                                                                             ra,0x802001d4 <__switch_to>
                                                                                                    jal
                                                                                                    nop
                                                                                                                            ra,24(sp)
s0,16(sp)
                                                                                                    ld
                                                                                                    1.d
                                                                                                    addi
                                                                                                                             sp, sp, 32
                                                                                                    ret
                                                                                                                            sp,sp,-48
ra,40(sp)
s0,32(sp)
                                                                                                    addi
                                                                                                    sd
                                                                                                    sd
```

(3)

```
0x802001d4 <__switch_to>
                                                                                       t0,a0
0x802001d8 <__switch_to+4>
                                                                                        t0, t0, 40
                                                                      addi
                                                                                        ra,0(t0)
                                               to+8>
                                                                      sd
                                                                                       sp,8(t0)
t0,t0,16
s0,0(t0)
                        <__switch_to+12>
                                                                      sd
0x802001e4 <__switch_to+16>
0x802001e8 <__switch_to+20>
                                                                      addi
                                                                      sd
0x802001ec <__switch_to+24>
                                                                      sd
                                                                                        s1,8(t0)
0x802001f0 <__switch_to+28>
0x802001f4 <__switch_to+32>
0x802001f8 <__switch_to+36>
0x802001fc <_switch_to+40>
                                                                                       s2,16(t0)
                                                                      sd
                                                                                       s3,24(t0)
s4,32(t0)
                                                                      sd
                                                                      sd
                                                                                       s5,40(t0)
                                                                      sd
0x80200200 <__switch_to+40>
0x80200200 <__switch_to+44>
0x80200204 <__switch_to+48>
0x80200208 <__switch_to+56>
0x80200210 <__switch_to+60>
                                                                                       s6,48(t0)
                                                                      sd
                                                                                       s7,56(t0)
s8,64(t0)
s9,72(t0)
                                                                      sd
                                                                      sd
                                                                      sd
                                                                                        s10,80(t0)
                                                                      sd
0x80200210 <__switch_to+64>
0x80200218 <__switch_to+68>
0x8020021c <__switch_to+72>
0x80200220 <__switch_to+76>
                                                                      sd
                                                                                       s11,88(t0)
                                                                                       t0,0x5
t0,t0,-520
                                                                      auipc
                                                                      addi
                                                                                       a1,0(t0)
                                                                      sd
0x80200224 < _switch_to+80>
0x80200224 < _switch_to+84>
0x80200222 < _switch_to+88>
0x80200230 < _switch_to+96>
0x80200234 < _switch_to+96>
                                                                                       t0,a1
                                                                      mν
                                                                                       t0,t0,40
ra,0(t0)
sp,8(t0)
                                                                      addi
                                                                      ld
                                                                      ld
                                                                      addi
                                                                                        t0,t0,16
0x80200234 <__switch_to+100>
0x8020023c <__switch_to+104>
0x80200240 <__switch_to+108>
                                                                                       s0,0(t0)
s1,8(t0)
s2,16(t0)
                                                                      ld
                                                                      ld
                                                                      ld
0x80200244 <__switch_to+112>
0x80200244 <__switch_to+116>
0x8020024c <__switch_to+120>
0x80200250 <__switch_to+124>
                                                                                        s3,24(t0)
                                                                      ld
                                                                                        s4,32(t0)
                                                                      ld
                                                                                       s5,40(t0)
s6,48(t0)
s7,56(t0)
                                                                      ld
                                                                      ld
0x80200254 <__switch_to+128>
                                                                      ld
```

(4)

(5)

```
0x80200554 <schedule>
0x80200558 <schedule+4>
0x8020055c <schedule+8>
                                                         addi
                                                                       sp, sp, -48
                                                                       ra,40(sp)
s0,32(sp)
s1,24(sp)
                                                         sd
                                                         sd
0x80200560 <schedule+12>
                                                         sd
0x80200564 <schedule+16>
0x80200568 <schedule+20>
                                                         addi
                                                                       s0, sp, 48
                                                                       a5,1
                                                         li
 0x8020056c <schedule+24>
                                                         SW
                                                                       a5,-36(s0)
                                                                                           <schedule+108>
                    <schedule+28>
 0x80200574 <schedule+32>
                                                         auipc
                                                                       a4,0x5
0x80200578 <schedule+36>
0x8020057c <schedule+40>
                                                         addi
                                                                       a4,a4,-1364
                                                                       a5,-36(s0)
                                                         lw
 0x80200580 <schedule+44>
                                                         slli
                                                                       a5,a5,0x3
0x80200580 <schedule+44>
0x80200584 <schedule+48>
0x80200588 <schedule+56>
0x80200580 <schedule+66>
0x80200594 <schedule+64>
0x80200598 <schedule+68>
0x80200590 <schedule+72>
0x80200500 <schedule+78>
                                                                       a5,a4,a5
                                                         add
                                                                       a5,0(a5)
a5,16(a5)
                                                         ld
                                                         ld
                                                                       a5,0x802005b4 <schedule+96>
                                                         begz
                                                                       a4,0x5
                                                         auipc
                                                                       a4,a4,-1396
                                                         addi
                                                                       a5,-36(s0)
                                                         lw
                                                         slli
                                                                       a5, a5, 0x3
0x802005a0 <schedule+76>

0x802005a4 <schedule+80>

0x802005a8 <schedule+84>

0x802005ac <schedule+88>

0x802005b0 <schedule+92>

0x802005b4 <schedule+96>

0x802005b8 <schedule+100>
                                                                       a5,a4,a5
a5,0(a5)
                                                         add
                                                         ld
                                                                       a5,-48(s0)
                                                         sd
                                                                                          <schedule+124>
                                                         j
                                                                       a5,-36(s0)
a5,a5,1
                                                         1.w
                                                         addiw
0x802005bc <schedule+104>
0x802005c0 <schedule+108>
0x802005c4 <schedule+112>
                                                                       a5,-36(s0)
                                                         SW
                                                                       a5,-36(s0)
                                                         lw
                                                         sext.w
                                                                       a4,a5
 0x802005c8 <schedule+116>
                                                         li
                                                                       a5,31
                                                                       a5,a4,0x80200574 <schedule+32>
0x802005cc <schedule+120>
                                                         bge
0x802005d0 <schedule+124>
0x802005d4 <schedule+128>
                                                                       a5,-36(s0)
                                                         lw
                                                         sext.w a4,a5
```

```
0x802001d4 <__switch_to>
                                     mν
                                             t0,a0
   0x802001d8 <__switch_to+4>
                                             t0,t0,40
                                     addi
B+ 0x802001dc <__switch_to+8>
                                     sd
                                             ra,0(t0)
   0x802001e0 <__switch_to+12>
                                     sd
                                             sp,8(t0)
   0x802001e4 <__switch_to+16>
                                             t0,t0,16
                                     addi
   0x802001e8 <__switch_to+20>
                                             s0,0(t0)
                                     sd
      02001ec <__switch_to+24>
                                             s1,8(t0)
                                     sd
   0x802001f0 <__switch_to+28>
                                             s2,16(t0)
                                     sd
                                                24(+A)
```

```
0x802001d4 <__switch_to>
                                             t0,a0
                                    ΠV
   0x802001d8 <__switch_to+4>
                                             t0,t0,40
                                    addi
B+ 0x802001dc <__switch_to+8>
                                             ra,0(t0)
                                    sd
                                             sp,8(t0)
   0x802001e0 <__switch_to+12>
                                    sd
                                             t0,t0,16
   0x802001e4 <__switch_to+16>
                                    addi
    x802001e8 <__switch_to+20>
                                             s0,0(t0)
                                    sd
   0x802001ec <__switch_to+24>
                                             s1,8(t0)
                                    sd
      02001f0 <__switch_to+28>
                                             s2,16(t0)
                                    sd
   0x802001f4 <__switch_to+32>
                                             s3,24(t0)
                                    sd
   0x802001f8 <__switch_to+36>
                                             s4,32(t0)
                                    sd
   0x802001fc < __switch_to+40>
                                    sd
                                             s5,40(t0)
   0x80200200 <__switch_to+44>
                                    sd
                                             s6,48(t0)
   0x80200204 <__switch_to+48>
                                             s7,56(t0)
                                    sd
   0x80200208 <__switch_to+52>
                                             s8,64(t0)
                                    sd
   0x8020020c <__switch_to+56>
                                    sd
                                             s9,72(t0)
   0x80200210 <__switch_to+60>
                                             s10,80(t0)
                                    sd
   0x80200214 <__switch_to+64>
                                             s11,88(t0)
                                    sd
   0x80200218 <__switch_to+68>
                                             t0,0x5
                                    auipc
   0x8020021c <__switch_to+72>
                                    addi
                                             t0,t0,-520
   0x80200220 <__switch_to+76>
                                             a1,0(t0)
                                    sd
   0x80200224 <__switch_to+80>
                                             t0,a1
                                    mν
   0x80200228 <__switch_to+84>
                                    addi
                                             t0,t0,40
   0x8020022c <__switch_to+88>
                                    ld
                                             ra,0(t0)
                                             sp,8(t0)
   0x80200230 <__switch_to+92>
                                    ld
                                    addi
              <__switch_to+96>
                                             t0,t0,16
```

#### 心得:

本次实验的难度跟上几次感觉根本不是一个等级,中间多次出现 bug 和未知情况,并且需要参展 stackoverflow 和 github 上的资料进行修改,而且对于 entry.S 的修改也是很困难的,一开始根本没有修改思路,虽然这次仅仅需要编写两个文件,但是这两个文件需要的精力需要之前二十个的精力,对于 sp/ra/epc 等寄存器值的处理很麻烦。