DISPLAY SYNTHESIS REPORT

#---

Vivado v2024.1 (64-bit)

SW Build 5076996 on Wed May 22 18:37:14 MDT 2024

IP Build 5075265 on Wed May 22 21:45:21 MDT 2024

SharedData Build 5076995 on Wed May 22 18:29:18 MDT 2024

Start of session at: Fri Oct 25 21:44:10 2024

Process ID: 20272

Current directory: Z:/Vivado Projects/hw3/hw3.runs/synth_1

Command line: vivado.exe -log Display_unit.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source Display_unit.tcl

Log file: Z:/Vivado Projects/hw3/hw3.runs/synth_1/Display_unit.vds

Journal file: Z:/Vivado Projects/hw3/hw3.runs/synth_1\vivado.jou

Running On   :Ravi-Notebook

Platform   :Windows Server 2016 or Windows 10

Operating System :22631

Processor Detail :12th Gen Intel(R) Core(TM) i7-12700H

CPU Frequency   :2688 MHz

CPU Physical cores:14

CPU Logical cores :20

Host memory   :16781 MB

Swap memory   :2281 MB

Total Virtual   :19063 MB

Available Virtual :6842 MB

#---

source Display_unit.tcl -notrace

create_project: Time (s): cpu = 00:00:06 ; elapsed = 00:00:11 . Memory (MB): peak = 531.117 ; gain = 201.031

Command: synth_design -top Display_unit -part xc7a35tcpg236-1

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'

INFO: [Synth 8-7079] Multithreading enabled for synth_design using a maximum of 2 processes.

INFO: [Synth 8-7078] Launching helper process for spawning children vivado processes

INFO: [Synth 8-7075] Helper process launched with PID 21276

Starting Synthesize : Time (s): cpu = 00:00:03 ; elapsed = 00:00:08 . Memory (MB): peak = 987.570 ; gain = 453.461

INFO: [Synth 8-638] synthesizing module 'Display_unit' [Z:/Vivado Projects/hw3/hw3.srcs/sources_1/new/display.vhd:34]

INFO: [Synth 8-3491] module 'decoder' declared at 'Z:/Vivado Projects/hw3/hw3.srcs/sources_1/new/dec.vhd:25' bound to instance 'WUT' of component 'decoder' [Z:/Vivado Projects/hw3/hw3.srcs/sources_1/new/display.vhd:85]

INFO: [Synth 8-638] synthesizing module 'decoder' [Z:/Vivado Projects/hw3/hw3.srcs/sources_1/new/dec.vhd:33]

INFO: [Synth 8-226] default block is never used [Z:/Vivado Projects/hw3/hw3.srcs/sources_1/new/dec.vhd:40]

INFO: [Synth 8-256] done synthesizing module 'decoder' (0#1) [Z:/Vivado Projects/hw3/hw3.srcs/sources_1/new/dec.vhd:33]

INFO: [Synth 8-256] done synthesizing module 'Display_unit' (0#1) [Z:/Vivado Projects/hw3/hw3.srcs/sources_1/new/display.vhd:34]

Finished Synthesize : Time (s): cpu = 00:00:03 ; elapsed = 00:00:10 . Memory (MB): peak = 1099.113 ; gain = 565.004

Finished Constraint Validation : Time (s): cpu = 00:00:04 ; elapsed = 00:00:11 . Memory (MB): peak = 1099.113 ; gain = 565.004

Start Loading Part and Timing Information

Loading part: xc7a35tcpg236-1

INFO: [Device 21-403] Loading part xc7a35tcpg236-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:04 ; elapsed = 00:00:12 . Memory (MB): peak = 1099.113 ; gain = 565.004

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:04 ; elapsed = 00:00:12 . Memory (MB): peak = 1099.113 ; gain = 565.004

No constraint files found.

Start RTL Component Statistics

Detailed RTL Component Info :

+---Muxes :

2 Input 1 Bit Muxes := 14

4 Input 1 Bit Muxes := 1

Finished RTL Component Statistics

Start Part Resource Summary

INFO: [Device 21-9227] Part: xc7a35tcpg236-1 does not have CEAM library.

Part Resources:

DSPs: 90 (col length:60)

BRAMs: 100 (col length: RAMB18 60 RAMB36 30)

Finished Part Resource Summary

No constraint files found.

Start Cross Boundary and Area Optimization

WARNING: [Synth 8-7080] Parallel synthesis criteria is not met

---

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:08 ; elapsed = 00:00:35 . Memory (MB): peak = 1292.074 ; gain = 757.965

No constraint files found.

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:08 ; elapsed = 00:00:36 . Memory (MB): peak = 1292.074 ; gain = 757.965

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:08 ; elapsed = 00:00:36 . Memory (MB): peak = 1292.074 ; gain = 757.965

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1292.074 ; gain = 757.965

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1292.074 ; gain = 757.965

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1292.074 ; gain = 757.965

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1292.074 ; gain = 757.965

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1292.074 ; gain = 757.965

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1292.074 ; gain = 757.965

Start Writing Synthesis Report

Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----+------+

| |Cell |Count |

+------+-----+------+

|1 |LUT4 | 4|

|2 |LUT5 | 1|

|3 |LUT6 | 9|

|4 |IBUF | 8|

|5 |OBUF | 7|

+------+-----+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 29|

+------+---------+-------+------+

Finished Writing Synthesis Report : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1292.074 ; gain = 757.965

Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1292.074 ; gain = 757.965

Synthesis Optimization Complete : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1292.074 ; gain = 757.965

INFO: [Project 1-571] Translating synthesized netlist

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1295.980 ; gain = 0.000

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1394.051 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Synth Design complete | Checksum: de07eefb

INFO: [Common 17-83] Releasing license: Synthesis

17 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:13 ; elapsed = 00:00:44 . Memory (MB): peak = 1394.051 ; gain = 862.934

Write ShapeDB Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1394.051 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'Z:/Vivado Projects/hw3/hw3.runs/synth_1/Display_unit.dcp' has been generated.

INFO: [Vivado 12-24828] Executing command : report_utilization -file Display_unit_utilization_synth.rpt -pb Display_unit_utilization_synth.pb

INFO: [Common 17-206] Exiting Vivado at Fri Oct 25 21:45:09 2024...

DISPLAY UTILISATION REPORT

| Tool Version : Vivado v.2024.1 (win64) Build 5076996 Wed May 22 18:37:14 MDT 2024

| Date : Fri Oct 25 21:45:09 2024

| Host : Ravi-Notebook running 64-bit major release (build 9200)

| Command : report_utilization -file Display_unit_utilization_synth.rpt -pb Display_unit_utilization_synth.pb

| Design : Display_unit

| Device : xc7a35tcpg236-1

| Speed File : -1

| Design State : Synthesized

Utilization Design Information

Table of Contents

---

4. IO and GT Specific

5. Clocking

6. Specific Feature

7. Primitives

8. Black Boxes

9. Instantiated Netlists

1. Slice Logic

+-------------------------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+-------------------------+------+-------+------------+-----------+-------+

| Slice LUTs* | 12 | 0 | 0 | 20800 | 0.06 |

| LUT as Logic | 12 | 0 | 0 | 20800 | 0.06 |

| LUT as Memory | 0 | 0 | 0 | 9600 | 0.00 |

| Slice Registers | 0 | 0 | 0 | 41600 | 0.00 |

| Register as Flip Flop | 0 | 0 | 0 | 41600 | 0.00 |

| Register as Latch | 0 | 0 | 0 | 41600 | 0.00 |

| F7 Muxes | 0 | 0 | 0 | 16300 | 0.00 |

| F8 Muxes | 0 | 0 | 0 | 8150 | 0.00 |

+-------------------------+------+-------+------------+-----------+-------+

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

Warning! LUT value is adjusted to account for LUT combining.

Warning! For any ECO changes, please run place_design if there are unplaced instances

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00

+----------------+------+-------+------------+-----------+-------+

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

+-----------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+-----------+------+-------+------------+-----------+-------+

| DSPs | 0 | 0 | 0 | 90 | 0.00 |

+-----------+------+-------+------------+-----------+-------+

4. IO and GT Specific

+----------------------------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+----------------------------+------+-------+------------+-----------+-------+

| Bonded IOB | 15 | 0 | 0 | 106 | 14.15 |

| Bonded IPADs | 0 | 0 | 0 | 10 | 0.00 |

| Bonded OPADs | 0 | 0 | 0 | 4 | 0.00 |

| PHY_CONTROL | 0 | 0 | 0 | 5 | 0.00 |

| PHASER_REF | 0 | 0 | 0 | 5 | 0.00 |

| OUT_FIFO | 0 | 0 | 0 | 20 | 0.00 |

| IN_FIFO | 0 | 0 | 0 | 20 | 0.00 |

| IDELAYCTRL | 0 | 0 | 0 | 5 | 0.00 |

| IBUFDS | 0 | 0 | 0 | 104 | 0.00 |

| GTPE2_CHANNEL | 0 | 0 | 0 | 2 | 0.00 |

| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 0 | 20 | 0.00 |

| PHASER_IN/PHASER_IN_PHY | 0 | 0 | 0 | 20 | 0.00 |

| IDELAYE2/IDELAYE2_FINEDELAY | 0 | 0 | 0 | 250 | 0.00 |

| IBUFDS_GTE2 | 0 | 0 | 0 | 2 | 0.00 |

| ILOGIC | 0 | 0 | 0 | 106 | 0.00 |

| OLOGIC | 0 | 0 | 0 | 106 | 0.00 |

+----------+------+-------+------------+-----------+-------+

5. Clocking

+----------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+----------+------+-------+------------+-----------+-------+

| BUFGCTRL | 0 | 0 | 0 | 32 | 0.00 |

| BUFIO | 0 | 0 | 0 | 20 | 0.00 |

| MMCME2_ADV | 0 | 0 | 0 | 5 | 0.00 |

| PLLE2_ADV | 0 | 0 | 0 | 5 | 0.00 |

| BUFMRCE | 0 | 0 | 0 | 10 | 0.00 |

| BUFHCE | 0 | 0 | 0 | 72 | 0.00 |

| BUFR | 0 | 0 | 0 | 20 | 0.00 |

+----------+------+-------+------------+-----------+-------+

6. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
PCIE_2_1	0	0	0	1	0.00
STARTUPE2	0	0	0	1	0.00
XADC	0	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT6	9	LUT
IBUF	8	IO
OBUF	7	IO
LUT4	4	LUT

| LUT5 | 1 | LUT |

+----------+------+---------------------+

8. Black Boxes

+----------+------+

| Ref Name | Used |

+----------+------+

9. Instantiated Netlists

+----------+------+

| Ref Name | Used |

+----------+------+