INVERSE SUB BYTES SYNTHESIS REPORT

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#-----------------------------------------------------------
# Vivado v2022.1 (64-bit)
# SW Build 3526262 on Mon Apr 18 15:47:01 MDT 2022
# IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022
# Start of session at: Fri Oct 25 17:12:46 2024
# Process ID: 79168
# Current directory:
/home/btech/cs1230322/project_5/project_5.runs/synth_1
# Command line: vivado -log inv_subbytes_8bit.vds -product Vivado -mode
batch -messageDb vivado.pb -notrace -source inv_subbytes_8bit.tcl
# Log file:
/home/btech/cs1230322/project_5/project_5.runs/synth_1/inv_subbytes_8bi
t.vds
# Journal file:
/home/btech/cs1230322/project_5/project_5.runs/synth_1/vivado.jou
# Running On: dhd, OS: Linux, CPU Frequency: 2100.000 MHz, CPU Physical
cores: 12, Host memory: 33324 MB
#-----------------------------------------------------------
source inv_subbytes_8bit.tcl -notrace
Command: read_checkpoint -auto_incremental -incremental
/home/btech/cs1230322/project_5/project_5.srcs/utils_1/imports/synth_1/
aes_xor_8bit.dcp
INFO: [Vivado 12-5825] Read reference checkpoint from
/home/btech/cs1230322/project_5/project_5.srcs/utils_1/imports/synth_1/
aes_xor_8bit.dcp for incremental synthesis
INFO: [Vivado 12-7989] Please ensure there are no constraint changes
Command: synth_design -top inv_subbytes_8bit -part xc7a35tcpg236-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device
'xc7a35t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device
'xc7a35t'
INFO: [Vivado_Tcl 4-1810] synth_design options have changed between
reference and incremental; A full resynthesis will be run
INFO: [Device 21-403] Loading part xc7a35tcpg236-1
INFO: [Synth 8-7079] Multithreading enabled for synth_design using a
maximum of 4 processes.
INFO: [Synth 8-7078] Launching helper process for spawning children
vivado processes
INFO: [Synth 8-7075] Helper process launched with PID 79198
---------------------------------------------------------------------
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Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed =
00:00:04 . Memory (MB): peak = 2608.051 ; gain = 0.000 ; free physical
= 22485 ; free virtual = 41236
---------------------------------------------------------------------
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INFO: [Synth 8-638] synthesizing module 'inv_subbytes_8bit'
[/home/btech/cs1230322/project_5/project_5.srcs/sources_1/new/invsub.vh
d:37]
INFO: [Synth 8-3491] module 'bram_access' declared at
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'/home/btech/cs1230322/Downloads/bram.vhd:6' bound to instance
'sbox_rom' of component 'bram_access'
[/home/btech/cs1230322/project_5/project_5.srcs/sources_1/new/invsub.vh
d:57]
INFO: [Synth 8-638] synthesizing module 'bram_access'
[/home/btech/cs1230322/Downloads/bram.vhd:17]
INFO: [Synth 8-3491] module 'blk_mem_gen_0' declared at
'/home/btech/cs1230322/project_5/project_5.gen/sources_1/ip/blk_mem_gen
_0/synth/blk_mem_gen_0.vhd:59' bound to instance 'bram_inst' of
component 'blk_mem_gen_0' [/home/btech/cs1230322/Downloads/bram.vhd:34]
INFO: [Synth 8-638] synthesizing module 'blk_mem_gen_0'
[/home/btech/cs1230322/project_5/project_5.gen/sources_1/ip/blk_mem_gen
_0/synth/blk_mem_gen_0.vhd:68]
    Parameter C_FAMILY bound to: artix7 - type: string
    Parameter C_XDEVICEFAMILY bound to: artix7 - type: string
    Parameter C_ELABORATION_DIR bound to: ./ - type: string
    Parameter C_INTERFACE_TYPE bound to: 0 - type: integer
    Parameter C_AXI_TYPE bound to: 1 - type: integer
    Parameter C_AXI_SLAVE_TYPE bound to: 0 - type: integer
    Parameter C_USE_BRAM_BLOCK bound to: 0 - type: integer
    Parameter C_ENABLE_32BIT_ADDRESS bound to: 0 - type: integer
    Parameter C_CTRL_ECC_ALGO bound to: NONE - type: string
    Parameter C_HAS_AXI_ID bound to: 0 - type: integer
    Parameter C_AXI_ID_WIDTH bound to: 4 - type: integer
    Parameter C_MEM_TYPE bound to: 3 - type: integer
    Parameter C_BYTE_SIZE bound to: 9 - type: integer
    Parameter C_ALGORITHM bound to: 1 - type: integer
    Parameter C_PRIM_TYPE bound to: 1 - type: integer
    Parameter C_LOAD_INIT_FILE bound to: 1 - type: integer
    Parameter C_INIT_FILE_NAME bound to: blk_mem_gen_0.mif - type: stri
ng
    Parameter C_INIT_FILE bound to: blk_mem_gen_0.mem - type: string
    Parameter C_USE_DEFAULT_DATA bound to: 1 - type: integer
    Parameter C_DEFAULT_DATA bound to: 0 - type: string
    Parameter C_HAS_RSTA bound to: 0 - type: integer
    Parameter C_RST_PRIORITY_A bound to: CE - type: string
    Parameter C_RSTRAM_A bound to: 0 - type: integer
    Parameter C_INITA_VAL bound to: 0 - type: string
    Parameter C_HAS_ENA bound to: 1 - type: integer
    Parameter C_HAS_REGCEA bound to: 0 - type: integer
    Parameter C_USE_BYTE_WEA bound to: 0 - type: integer
    Parameter C_WEA_WIDTH bound to: 1 - type: integer
    Parameter C_WRITE_MODE_A bound to: WRITE_FIRST - type: string
    Parameter C_WRITE_WIDTH_A bound to: 8 - type: integer
    Parameter C_READ_WIDTH_A bound to: 8 - type: integer
    Parameter C_WRITE_DEPTH_A bound to: 256 - type: integer
    Parameter C_READ_DEPTH_A bound to: 256 - type: integer
    Parameter C_ADDRA_WIDTH bound to: 8 - type: integer
    Parameter C_HAS_RSTB bound to: 0 - type: integer
    Parameter C_RST_PRIORITY_B bound to: CE - type: string
    Parameter C_RSTRAM_B bound to: 0 - type: integer
    Parameter C_INITB_VAL bound to: 0 - type: string
    Parameter C_HAS_ENB bound to: 0 - type: integer
    Parameter C_HAS_REGCEB bound to: 0 - type: integer
    Parameter C_USE_BYTE_WEB bound to: 0 - type: integer
    Parameter C_WEB_WIDTH bound to: 1 - type: integer
    Parameter C_WRITE_MODE_B bound to: WRITE_FIRST - type: string
    Parameter C_WRITE_WIDTH_B bound to: 8 - type: integer
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    Parameter C_READ_WIDTH_B bound to: 8 - type: integer
    Parameter C_WRITE_DEPTH_B bound to: 256 - type: integer
    Parameter C_READ_DEPTH_B bound to: 256 - type: integer
    Parameter C_ADDRB_WIDTH bound to: 8 - type: integer
    Parameter C_HAS_MEM_OUTPUT_REGS_A bound to: 1 - type: integer
    Parameter C_HAS_MEM_OUTPUT_REGS_B bound to: 0 - type: integer
    Parameter C_HAS_MUX_OUTPUT_REGS_A bound to: 0 - type: integer
    Parameter C_HAS_MUX_OUTPUT_REGS_B bound to: 0 - type: integer
    Parameter C_MUX_PIPELINE_STAGES bound to: 0 - type: integer
    Parameter C_HAS_SOFTECC_INPUT_REGS_A bound to: 0 - type: integer
    Parameter C_HAS_SOFTECC_OUTPUT_REGS_B bound to: 0 - type: integer
    Parameter C_USE_SOFTECC bound to: 0 - type: integer
    Parameter C_USE_ECC bound to: 0 - type: integer
    Parameter C_EN_ECC_PIPE bound to: 0 - type: integer
    Parameter C_READ_LATENCY_A bound to: 1 - type: integer
    Parameter C_READ_LATENCY_B bound to: 1 - type: integer
    Parameter C_HAS_INJECTERR bound to: 0 - type: integer
    Parameter C_SIM_COLLISION_CHECK bound to: ALL - type: string
    Parameter C_COMMON_CLK bound to: 0 - type: integer
    Parameter C_DISABLE_WARN_BHV_COLL bound to: 0 - type: integer
    Parameter C_EN_SLEEP_PIN bound to: 0 - type: integer
    Parameter C_USE_URAM bound to: 0 - type: integer
    Parameter C_EN_RDADDRA_CHG bound to: 0 - type: integer
    Parameter C_EN_RDADDRB_CHG bound to: 0 - type: integer
    Parameter C_EN_DEEPSLEEP_PIN bound to: 0 - type: integer
    Parameter C_EN_SHUTDOWN_PIN bound to: 0 - type: integer
    Parameter C_EN_SAFETY_CKT bound to: 0 - type: integer
    Parameter C_DISABLE_WARN_BHV_RANGE bound to: 0 - type: integer
    Parameter C_COUNT_36K_BRAM bound to: 0 - type: string
    Parameter C_COUNT_18K_BRAM bound to: 1 - type: string
    Parameter C_EST_POWER_SUMMARY bound to: Estimated Power for
IP     :     2.3768 mW - type: string
INFO: [Synth 8-3491] module 'blk_mem_gen_v8_4_5' declared at
'/home/btech/cs1230322/project_5/project_5.gen/sources_1/ip/blk_mem_gen
_0/hdl/blk_mem_gen_v8_4_vhsyn_rfs.vhd:195321' bound to instance 'U0' of
component 'blk_mem_gen_v8_4_5'
[/home/btech/cs1230322/project_5/project_5.gen/sources_1/ip/blk_mem_gen
_0/synth/blk_mem_gen_0.vhd:232]
INFO: [Synth 8-256] done synthesizing module 'blk_mem_gen_0' (0#1)
[/home/btech/cs1230322/project_5/project_5.gen/sources_1/ip/blk_mem_gen
_0/synth/blk_mem_gen_0.vhd:68]
INFO: [Synth 8-256] done synthesizing module 'bram_access' (0#1)
[/home/btech/cs1230322/Downloads/bram.vhd:17]
INFO: [Synth 8-256] done synthesizing module 'inv_subbytes_8bit' (0#1)
[/home/btech/cs1230322/project_5/project_5.srcs/sources_1/new/invsub.vh
d:37]
WARNING: [Synth 8-7129] Port CLKB in module blk_mem_output_block is
either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB_I[7] in module blk_mem_output_block
is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB_I[6] in module blk_mem_output_block
is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB_I[5] in module blk_mem_output_block
is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB_I[4] in module blk_mem_output_block
is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB_I[3] in module blk_mem_output_block
is either unconnected or has no load
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WARNING: [Synth 8-7129] Port DOUTB_I[2] in module blk_mem_output_block
is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB_I[1] in module blk_mem_output_block
is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB_I[0] in module blk_mem_output_block
is either unconnected or has no load
WARNING: [Synth 8-7129] Port SBITERR_I in module blk_mem_output_block
is either unconnected or has no load
WARNING: [Synth 8-7129] Port DBITERR_I in module blk_mem_output_block
is either unconnected or has no load
WARNING: [Synth 8-7129] Port RDADDRECC_I[7] in module
blk_mem_output_block is either unconnected or has no load
WARNING: [Synth 8-7129] Port RDADDRECC_I[6] in module
blk_mem_output_block is either unconnected or has no load
WARNING: [Synth 8-7129] Port RDADDRECC_I[5] in module
blk_mem_output_block is either unconnected or has no load
WARNING: [Synth 8-7129] Port RDADDRECC_I[4] in module
blk_mem_output_block is either unconnected or has no load
WARNING: [Synth 8-7129] Port RDADDRECC_I[3] in module
blk_mem_output_block is either unconnected or has no load
WARNING: [Synth 8-7129] Port RDADDRECC_I[2] in module
blk_mem_output_block is either unconnected or has no load
WARNING: [Synth 8-7129] Port RDADDRECC_I[1] in module
blk_mem_output_block is either unconnected or has no load
WARNING: [Synth 8-7129] Port RDADDRECC_I[0] in module
blk_mem_output_block is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[35] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[34] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[33] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[32] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[31] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[30] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[29] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[28] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[27] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[26] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[25] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[24] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[23] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[22] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[21] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[20] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
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WARNING: [Synth 8-7129] Port DOUTB[19] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[18] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[17] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[16] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[15] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[14] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[13] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[12] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[11] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[10] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[9] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[8] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[7] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[6] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[5] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[4] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[3] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[2] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[1] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DOUTB[0] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port SBITERR in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DBITERR in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port SSRA in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port CLKB in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port SSRB in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port ENB in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port REGCEB in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port WEB[0] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port ADDRB[8] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
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WARNING: [Synth 8-7129] Port ADDRB[7] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port ADDRB[6] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port ADDRB[5] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port ADDRB[4] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port ADDRB[3] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port ADDRB[2] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port ADDRB[1] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port ADDRB[0] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[35] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[34] in module
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WARNING: [Synth 8-7129] Port DINB[29] in module
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WARNING: [Synth 8-7129] Port DINB[28] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[27] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[26] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[25] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[24] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[23] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[22] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[21] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[20] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[19] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[18] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[17] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[16] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[15] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
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WARNING: [Synth 8-7129] Port DINB[14] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[13] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[12] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[11] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[10] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[9] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
WARNING: [Synth 8-7129] Port DINB[8] in module
blk_mem_gen_prim_wrapper_init is either unconnected or has no load
INFO: [Common 17-14] Message 'Synth 8-7129' appears 100 times and
further instances of the messages will be disabled. Use the Tcl command
set_msg_config to change the current settings.
-------------------------------------------------------------------------
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Finished RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed =
00:00:09 . Memory (MB): peak = 2608.051 ; gain = 0.000 ; free physical
= 22538 ; free virtual = 41290
-------------------------------------------------------------------------
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-------------------------------------------------------------------------
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Start Handling Custom Attributes
-------------------------------------------------------------------------
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-------------------------------------------------------------------------
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Finished Handling Custom Attributes : Time (s): cpu = 00:00:07 ;
elapsed = 00:00:09 . Memory (MB): peak = 2608.051 ; gain = 0.000 ; free
physical = 22538 ; free virtual = 41290
-------------------------------------------------------------------------
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-------------------------------------------------------------------------
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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:07 ; elapsed
= 00:00:09 . Memory (MB): peak = 2608.051 ; gain = 0.000 ; free
physical = 22538 ; free virtual = 41290
-------------------------------------------------------------------------
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Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00
. Memory (MB): peak = 2608.051 ; gain = 0.000 ; free physical = 22529 ;
free virtual = 41281
INFO: [Netlist 29-17] Analyzing 1 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File
[/home/btech/cs1230322/project_5/project_5.runs/synth_1/dont_touch.xdc]
Finished Parsing XDC File
[/home/btech/cs1230322/project_5/project_5.runs/synth_1/dont_touch.xdc]
Completed Processing XDC Constraints
```

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Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00
. Memory (MB): peak = 2672.082 ; gain = 0.000 ; free physical = 22478 ;
free virtual = 41230
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00.01 ; elapsed =
00:00:00 . Memory (MB): peak = 2672.082 ; gain = 0.000 ; free physical
= 22478 ; free virtual = 41230
-----------------------------------------------------------------------
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Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed =
00:00:14 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free physical
= 22543 ; free virtual = 41296
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
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Start Loading Part and Timing Information
-----------------------------------------------------------------------
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Loading part: xc7a35tcpg236-1
-----------------------------------------------------------------------
----------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10
; elapsed = 00:00:14 . Memory (MB): peak = 2672.082 ; gain = 64.031 ;
free physical = 22543 ; free virtual = 41296
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start Applying 'set_property' XDC Constraints
-----------------------------------------------------------------------
----------
Applied set_property KEEP_HIERARCHY = SOFT for sbox_rom/bram_inst.
(constraint file  auto generated constraint).
-----------------------------------------------------------------------
----------
Finished applying 'set_property' XDC Constraints : Time (s): cpu =
00:00:10 ; elapsed = 00:00:14 . Memory (MB): peak = 2672.082 ; gain =
64.031 ; free physical = 22544 ; free virtual = 41296
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start Preparing Guide Design
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Finished Doing Graph Differ : Time (s): cpu = 00:00:10 ; elapsed =
00:00:15 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free physical
= 22538 ; free virtual = 41291
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Finished Preparing Guide Design : Time (s): cpu = 00:00:10 ; elapsed =
```

```
00:00:15 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free physical
= 22538 ; free virtual = 41291
---------------------------------------------------------------------
----------
---------------------------------------------------------------------
----------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed
= 00:00:15 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free
physical = 22541 ; free virtual = 41294
---------------------------------------------------------------------
----------


Incremental Synthesis Report Summary:

1. Incremental synthesis run: no

   Reason for not running incremental synthesis : synth_design options
have changed between reference and incremental


INFO: [Synth 8-7130] Flow is switching to default flow due to
incremental criteria not met. If you would like to alter this behaviour
and have the flow terminate instead, please set the following parameter
config_implementation {autoIncr.Synth.RejectBehavior Terminate}
---------------------------------------------------------------------
----------
Start RTL Component Statistics
---------------------------------------------------------------------
----------
Detailed RTL Component Info :
---------------------------------------------------------------------
----------
Finished RTL Component Statistics
---------------------------------------------------------------------
----------
---------------------------------------------------------------------
----------
Start Part Resource Summary
---------------------------------------------------------------------
----------
Part Resources:
DSPs: 90 (col length:60)
BRAMs: 100 (col length: RAMB18 60 RAMB36 30)
---------------------------------------------------------------------
----------
Finished Part Resource Summary
---------------------------------------------------------------------
----------
---------------------------------------------------------------------
----------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------
----------
WARNING: [Synth 8-7080] Parallel synthesis criteria is not met
---------------------------------------------------------------------
----------
Finished Cross Boundary and Area Optimization : Time (s): cpu =
```

```
00:00:10 ; elapsed = 00:00:16 . Memory (MB): peak = 2672.082 ; gain =
64.031 ; free physical = 22535 ; free virtual = 41296
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start Applying XDC Timing Constraints
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:13 ;
elapsed = 00:00:18 . Memory (MB): peak = 2672.082 ; gain = 64.031 ;
free physical = 22422 ; free virtual = 41183
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start Timing Optimization
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Finished Timing Optimization : Time (s): cpu = 00:00:13 ; elapsed =
00:00:18 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free physical
= 22422 ; free virtual = 41183
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start Technology Mapping
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Finished Technology Mapping : Time (s): cpu = 00:00:13 ; elapsed =
00:00:19 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free physical
= 22418 ; free virtual = 41179
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start IO Insertion
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start Flattening Before IO Insertion
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Finished Flattening Before IO Insertion
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start Final Netlist Cleanup
```

```
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Finished Final Netlist Cleanup
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Finished IO Insertion : Time (s): cpu = 00:00:14 ; elapsed = 00:00:20 .
Memory (MB): peak = 2672.082 ; gain = 64.031 ; free physical = 22419 ;
free virtual = 41179
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Start Renaming Generated Instances
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:14 ;
elapsed = 00:00:20 . Memory (MB): peak = 2672.082 ; gain = 64.031 ;
free physical = 22419 ; free virtual = 41179
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:14 ; elapsed
= 00:00:20 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free
physical = 22419 ; free virtual = 41179
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Start Renaming Generated Ports
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:14 ; elapsed
= 00:00:20 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free
physical = 22419 ; free virtual = 41179
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Start Handling Custom Attributes
---------------------------------------------------------------------------
----------
---------------------------------------------------------------------------
----------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:14 ;
```

```
elapsed = 00:00:20 . Memory (MB): peak = 2672.082 ; gain = 64.031 ;
free physical = 22419 ; free virtual = 41179
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start Renaming Generated Nets
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:14 ; elapsed =
00:00:20 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free physical
= 22419 ; free virtual = 41179
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Start Writing Synthesis Report
-----------------------------------------------------------------------
----------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+---------+------+
|      |Cell     |Count |
+------+---------+------+
|1     |BUFG     |     1|
|2     |RAMB18E1 |     1|
|3     |IBUF     |     9|
|4     |OBUF     |     8|
+------+---------+------+
-----------------------------------------------------------------------
----------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed
= 00:00:20 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free
physical = 22419 ; free virtual = 41179
-----------------------------------------------------------------------
----------
Synthesis finished with 0 errors, 0 critical warnings and 157 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:13 ; elapsed =
00:00:19 . Memory (MB): peak = 2672.082 ; gain = 0.000 ; free physical
= 22468 ; free virtual = 41229
Synthesis Optimization Complete : Time (s): cpu = 00:00:14 ; elapsed =
00:00:20 . Memory (MB): peak = 2672.082 ; gain = 64.031 ; free physical
= 22468 ; free virtual = 41229
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed =
00:00:00.01 . Memory (MB): peak = 2672.082 ; gain = 0.000 ; free
physical = 22465 ; free virtual = 41226
INFO: [Netlist 29-17] Analyzing 1 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
```

```
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00
. Memory (MB): peak = 2672.082 ; gain = 0.000 ; free physical = 22499 ;
free virtual = 41260
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synth Design complete, checksum: b4c0e4be
INFO: [Common 17-83] Releasing license: Synthesis
30 Infos, 101 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:19 ; elapsed = 00:00:23 . Memory
(MB): peak = 2672.082 ; gain = 64.031 ; free physical = 22701 ; free
virtual = 41462
INFO: [Common 17-1381] The checkpoint
'/home/btech/cs1230322/project_5/project_5.runs/synth_1/inv_subbytes_8b
it.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file
inv_subbytes_8bit_utilization_synth.rpt -pb
inv_subbytes_8bit_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Fri Oct 25 17:13:13 2024...
```

INVERSE SUB BYTES UTILISATION REPORT

```
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------------------------------------------------------------------------
------------------------------------------------------
| Tool Version : Vivado v.2022.1 (lin64) Build 3526262 Mon Apr 18
15:47:01 MDT 2022
| Date         : Fri Oct 25 17:13:13 2024
| Host         : dhd running 64-bit Ubuntu 20.04.3 LTS
| Command      : report_utilization -file
inv_subbytes_8bit_utilization_synth.rpt -pb
inv_subbytes_8bit_utilization_synth.pb
| Design       : inv_subbytes_8bit
| Device       : xc7a35tcpg236-1
| Speed File   : -1
| Design State : Synthesized
------------------------------------------------------------------------
------------------------------------------------------

Utilization Design Information

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```

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8. Black Boxes
9. Instantiated Netlists

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	0	0	0	20800	0.00
LUT as Logic	0	0	0	20800	0.00
LUT as Memory	0	0	0	9600	0.00
Slice Registers	0	0	0	41600	0.00
Register as Flip Flop	0	0	0	41600	0.00
Register as Latch	0	0	0	41600	0.00
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0.5	0	0	50	1.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	1	0	0	100	1.00
RAMB18E1 only	1				

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	90	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	17	0	0	106	16.04
Bonded IPADs	0	0	0	10	0.00
Bonded OPADs	0	0	0	4	0.00
PHY_CONTROL	0	0	0	5	0.00
PHASER_REF	0	0	0	5	0.00
OUT_FIFO	0	0	0	20	0.00
IN_FIFO	0	0	0	20	0.00
IDELAYCTRL	0	0	0	5	0.00
IBUFDS	0	0	0	104	0.00
GTPE2_CHANNEL	0	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	250	

| 0.00 |
IBUFDS_GTE2	0	0	0	2	0.00
ILOGIC	0	0	0	106	0.00
OLOGIC	0	0	0	106	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	1	0	0	32	3.13
BUFIO	0	0	0	20	0.00
MMCME2_ADV	0	0	0	5	0.00
PLLE2_ADV	0	0	0	5	0.00
BUFMRCE	0	0	0	10	0.00
BUFHCE	0	0	0	72	0.00
BUFR	0	0	0	20	0.00

6. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
PCIE_2_1	0	0	0	1	0.00
STARTUPE2	0	0	0	1	0.00
XADC	0	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
IBUF	9	IO
OBUF	8	IO
RAMB18E1	1	Block Memory
BUFG	1	Clock

8. Black Boxes

Ref Name	Used

9. Instantiated Netlists

Ref Name	Used