INVERSE SHIFT ROWS SYNTHESIS REPORT

```
#-----------------------------------------------------------
# Vivado v2022.1 (64-bit)
# SW Build 3526262 on Mon Apr 18 15:47:01 MDT 2022
# IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022
# Start of session at: Fri Oct 25 17:10:55 2024
# Process ID: 78443
# Current directory:
/home/btech/cs1230322/project_5/project_5.runs/synth_1
# Command line: vivado -log shift_rows.vds -product Vivado -mode batch
-messageDb vivado.pb -notrace -source shift_rows.tcl
# Log file:
/home/btech/cs1230322/project_5/project_5.runs/synth_1/shift_rows.vds
# Journal file:
/home/btech/cs1230322/project_5/project_5.runs/synth_1/vivado.jou
# Running On: dhd, OS: Linux, CPU Frequency: 2100.000 MHz, CPU Physical
cores: 12, Host memory: 33324 MB
#-----------------------------------------------------------
source shift_rows.tcl -notrace
Command: read_checkpoint -auto_incremental -incremental
/home/btech/cs1230322/project_5/project_5.srcs/utils_1/imports/synth_1/
aes_xor_8bit.dcp
INFO: [Vivado 12-5825] Read reference checkpoint from
/home/btech/cs1230322/project_5/project_5.srcs/utils_1/imports/synth_1/
aes_xor_8bit.dcp for incremental synthesis
INFO: [Vivado 12-7989] Please ensure there are no constraint changes
Command: synth_design -top shift_rows -part xc7a35tcpg236-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device
'xc7a35t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device
'xc7a35t'
INFO: [Vivado_Tcl 4-1810] synth_design options have changed between
reference and incremental; A full resynthesis will be run
INFO: [Synth 8-7079] Multithreading enabled for synth_design using a
maximum of 4 processes.
INFO: [Synth 8-7078] Launching helper process for spawning children
vivado processes
INFO: [Synth 8-7075] Helper process launched with PID 78469
---------------------------------------------------------------------
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Starting Synthesize : Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 .
Memory (MB): peak = 2608.047 ; gain = 0.000 ; free physical = 21562 ;
free virtual = 40505
---------------------------------------------------------------------
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INFO: [Synth 8-638] synthesizing module 'shift_rows'
[/home/btech/cs1230322/project_5/project_5.srcs/sources_1/new/invshiftr
ows.vhd:32]
INFO: [Synth 8-226] default block is never used
[/home/btech/cs1230322/project_5/project_5.srcs/sources_1/new/invshiftr
ows.vhd:37]
INFO: [Synth 8-256] done synthesizing module 'shift_rows' (0#1)
[/home/btech/cs1230322/project_5/project_5.srcs/sources_1/new/invshiftr
ows.vhd:32]
---------------------------------------------------------------------
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```

```
Finished Synthesize : Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 .
Memory (MB): peak = 2608.047 ; gain = 0.000 ; free physical = 22682 ;
free virtual = 41604
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Finished Constraint Validation : Time (s): cpu = 00:00:03 ; elapsed =
00:00:04 . Memory (MB): peak = 2608.047 ; gain = 0.000 ; free physical
= 22692 ; free virtual = 41604
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Start Loading Part and Timing Information
---------------------------------------------------------------------
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Loading part: xc7a35tcpg236-1
INFO: [Device 21-403] Loading part xc7a35tcpg236-1
---------------------------------------------------------------------
---------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:03
; elapsed = 00:00:04 . Memory (MB): peak = 2616.051 ; gain = 8.004 ;
free physical = 22691 ; free virtual = 41602
---------------------------------------------------------------------
---------
---------------------------------------------------------------------
---------
Start Preparing Guide Design
---------------------------------------------------------------------
---------
---------------------------------------------------------------------
---------
Finished Doing Graph Differ : Time (s): cpu = 00:00:03 ; elapsed =
00:00:04 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free physical
= 22625 ; free virtual = 41537
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Finished Preparing Guide Design : Time (s): cpu = 00:00:03 ; elapsed =
00:00:04 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free physical
= 22625 ; free virtual = 41537
---------------------------------------------------------------------
---------
---------------------------------------------------------------------
---------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:03 ; elapsed
= 00:00:04 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free
physical = 22621 ; free virtual = 41532
---------------------------------------------------------------------
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Incremental Synthesis Report Summary:

1. Incremental synthesis run: no
```

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   Reason for not running incremental synthesis : synth_design options
have changed between reference and incremental


INFO: [Synth 8-7130] Flow is switching to default flow due to
incremental criteria not met. If you would like to alter this behaviour
and have the flow terminate instead, please set the following parameter
config_implementation {autoIncr.Synth.RejectBehavior Terminate}
No constraint files found.
---------------------------------------------------------------------
---------
Start RTL Component Statistics
---------------------------------------------------------------------
---------
Detailed RTL Component Info :
+---Muxes :
       4 Input   32 Bit        Muxes := 1
---------------------------------------------------------------------
---------
Finished RTL Component Statistics
---------------------------------------------------------------------
---------
---------------------------------------------------------------------
---------
Start Part Resource Summary
---------------------------------------------------------------------
---------
Part Resources:
DSPs: 90 (col length:60)
BRAMs: 100 (col length: RAMB18 60 RAMB36 30)
---------------------------------------------------------------------
---------
Finished Part Resource Summary
---------------------------------------------------------------------
---------
No constraint files found.
---------------------------------------------------------------------
---------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------
---------
WARNING: [Synth 8-7080] Parallel synthesis criteria is not met
---------------------------------------------------------------------
---------
Finished Cross Boundary and Area Optimization : Time (s): cpu =
00:00:05 ; elapsed = 00:00:06 . Memory (MB): peak = 2616.051 ; gain =
8.004 ; free physical = 22409 ; free virtual = 41322
---------------------------------------------------------------------
---------
No constraint files found.
---------------------------------------------------------------------
---------
Start Timing Optimization
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Finished Timing Optimization : Time (s): cpu = 00:00:05 ; elapsed =
```

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00:00:07 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free physical
= 22404 ; free virtual = 41317
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
----------
Start Technology Mapping
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
----------
Finished Technology Mapping : Time (s): cpu = 00:00:05 ; elapsed =
00:00:07 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free physical
= 22403 ; free virtual = 41316
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
----------
Start IO Insertion
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
----------
Start Flattening Before IO Insertion
-----------------------------------------------------------------------
----------
-----------------------------------------------------------------------
----------
Finished Flattening Before IO Insertion
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
----------
Start Final Netlist Cleanup
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
----------
Finished Final Netlist Cleanup
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
----------
Finished IO Insertion : Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 .
Memory (MB): peak = 2616.051 ; gain = 8.004 ; free physical = 22400 ;
free virtual = 41313
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
----------
Start Renaming Generated Instances
-----------------------------------------------------------------------
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-----------------------------------------------------------------------
----------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:07 ;
elapsed = 00:00:08 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free
physical = 22400 ; free virtual = 41313
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---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------
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---------------------------------------------------------------------
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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:07 ; elapsed
= 00:00:08 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free
physical = 22400 ; free virtual = 41313
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Start Renaming Generated Ports
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:07 ; elapsed
= 00:00:08 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free
physical = 22400 ; free virtual = 41313
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Start Handling Custom Attributes
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:07 ;
elapsed = 00:00:08 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free
physical = 22400 ; free virtual = 41313
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Start Renaming Generated Nets
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:07 ; elapsed =
00:00:08 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free physical
= 22400 ; free virtual = 41313
---------------------------------------------------------------------
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---------------------------------------------------------------------
---------
Start Writing Synthesis Report
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Report BlackBoxes:
+-+--------------+----------+
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| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT6 |    32|
|2     |IBUF |    34|
|3     |OBUF |    32|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    98|
+------+---------+-------+------+
-------------------------------------------------------------------------
----------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:07 ; elapsed
= 00:00:08 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free
physical = 22400 ; free virtual = 41313
-------------------------------------------------------------------------
----------
Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:07 ; elapsed =
00:00:08 . Memory (MB): peak = 2616.051 ; gain = 8.004 ; free physical
= 22405 ; free virtual = 41319
Synthesis Optimization Complete : Time (s): cpu = 00:00:07 ; elapsed =
00:00:08 . Memory (MB): peak = 2616.059 ; gain = 8.004 ; free physical
= 22405 ; free virtual = 41319
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00
. Memory (MB): peak = 2616.059 ; gain = 0.000 ; free physical = 22491 ;
free virtual = 41404
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00
. Memory (MB): peak = 2616.059 ; gain = 0.000 ; free physical = 22408 ;
free virtual = 41322
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synth Design complete, checksum: 9b8da526
INFO: [Common 17-83] Releasing license: Synthesis
17 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:10 ; elapsed = 00:00:09 . Memory
(MB): peak = 2616.059 ; gain = 8.012 ; free physical = 22619 ; free
virtual = 41532
INFO: [Common 17-1381] The checkpoint
'/home/btech/cs1230322/project_5/project_5.runs/synth_1/shift_rows.dcp'
has been generated.
INFO: [runtcl-4] Executing : report_utilization -file
shift_rows_utilization_synth.rpt -pb shift_rows_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Fri Oct 25 17:11:08 2024...
```

INVERSE SHIFT ROWS UTILISATION REPORT


```
------------------------------------------------------------------------------------
| Tool Version : Vivado v.2022.1 (lin64) Build 3526262 Mon Apr 18 15:47:01 MDT 2022
| Date         : Fri Oct 25 17:11:08 2024
| Host         : dhd running 64-bit Ubuntu 20.04.3 LTS
| Command      : report_utilization -file shift_rows_utilization_synth.rpt -pb shift_rows_utilization_synth.pb
| Design       : shift_rows
| Device       : xc7a35tcpg236-1
| Speed File   : -1
| Design State : Synthesized
------------------------------------------------------------------------------------

Utilization Design Information

Table of Contents
-----------------
1. Slice Logic
1.1 Summary of Registers by Type
2. Memory
3. DSP
4. IO and GT Specific
5. Clocking
6. Specific Feature
7. Primitives
8. Black Boxes
9. Instantiated Netlists

1. Slice Logic
--------------

+-------------------------+------+-------+-----------+-----------+------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+-----------+-----------+------+
| Slice LUTs*             |   32 |     0 |          0 |     20800 |  0.15 |
|   LUT as Logic          |   32 |     0 |          0 |     20800 |  0.15 |
|   LUT as Memory         |    0 |     0 |          0 |      9600 |  0.00 |
| Slice Registers         |    0 |     0 |          0 |     41600 |  0.00 |
|   Register as Flip Flop |    0 |     0 |          0 |     41600 |  0.00 |
|   Register as Latch     |    0 |     0 |          0 |     41600 |  0.00 |
```

| F7 Muxes | 0 | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 0 | 8150 | 0.00 |

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	90	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	66	0	0	106	62.26
Bonded IPADs	0	0	0	10	0.00
Bonded OPADs	0	0	0	4	0.00
PHY_CONTROL	0	0	0	5	0.00
PHASER_REF	0	0	0	5	0.00
OUT_FIFO	0	0	0	20	0.00
IN_FIFO	0	0	0	20	0.00
IDELAYCTRL	0	0	0	5	0.00
IBUFDS	0	0	0	104	0.00
GTPE2_CHANNEL	0	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	250	0.00
IBUFDS_GTE2	0	0	0	2	0.00
ILOGIC	0	0	0	106	0.00
OLOGIC	0	0	0	106	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	0	0	0	32	0.00
BUFIO	0	0	0	20	0.00
MMCME2_ADV	0	0	0	5	0.00
PLLE2_ADV	0	0	0	5	0.00
BUFMRCE	0	0	0	10	0.00
BUFHCE	0	0	0	72	0.00
BUFR	0	0	0	20	0.00

6. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
PCIE_2_1	0	0	0	1	0.00
STARTUPE2	0	0	0	1	0.00
XADC	0	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
IBUF	34	IO
OBUF	32	IO
LUT6	32	LUT

8. Black Boxes

Ref Name	Used

9. Instantiated Netlists

Ref Name	Used