성균관대학교 | SAL

Week 3

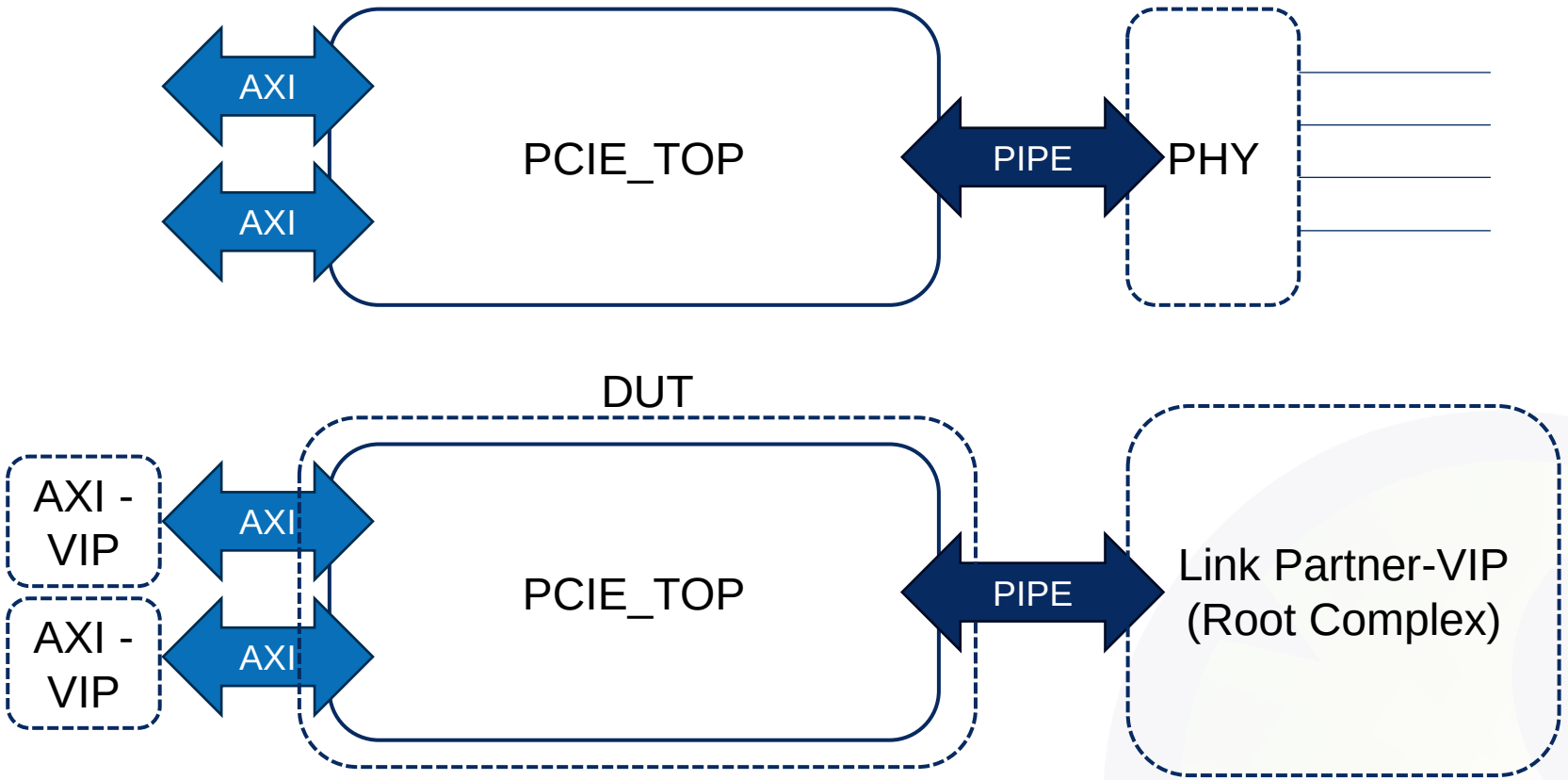
Please enter a sub-title here.

| **주관기관** | 성균관대학교

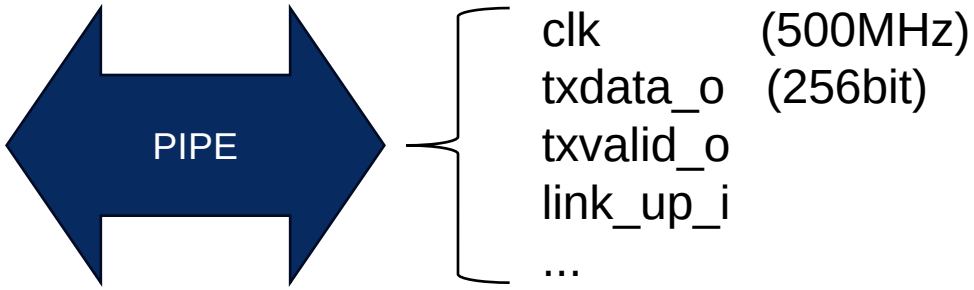
| **총괄책임자** | 박 상 현

2025.03.14

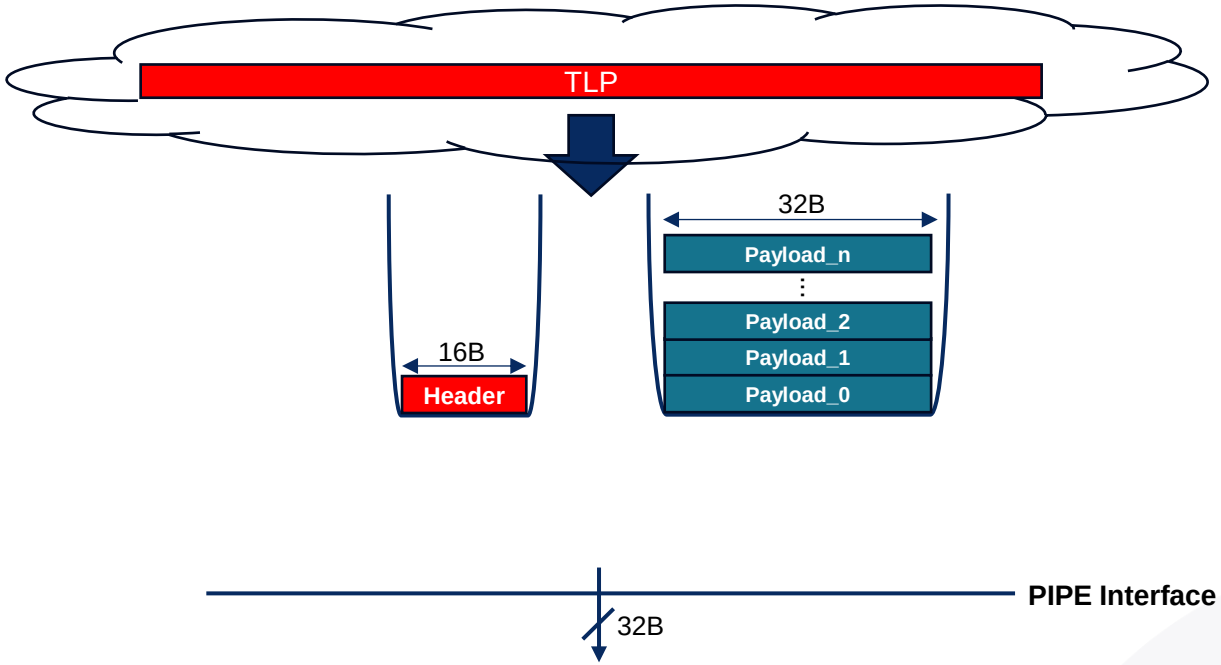
☑ PCIe Controller Architecture



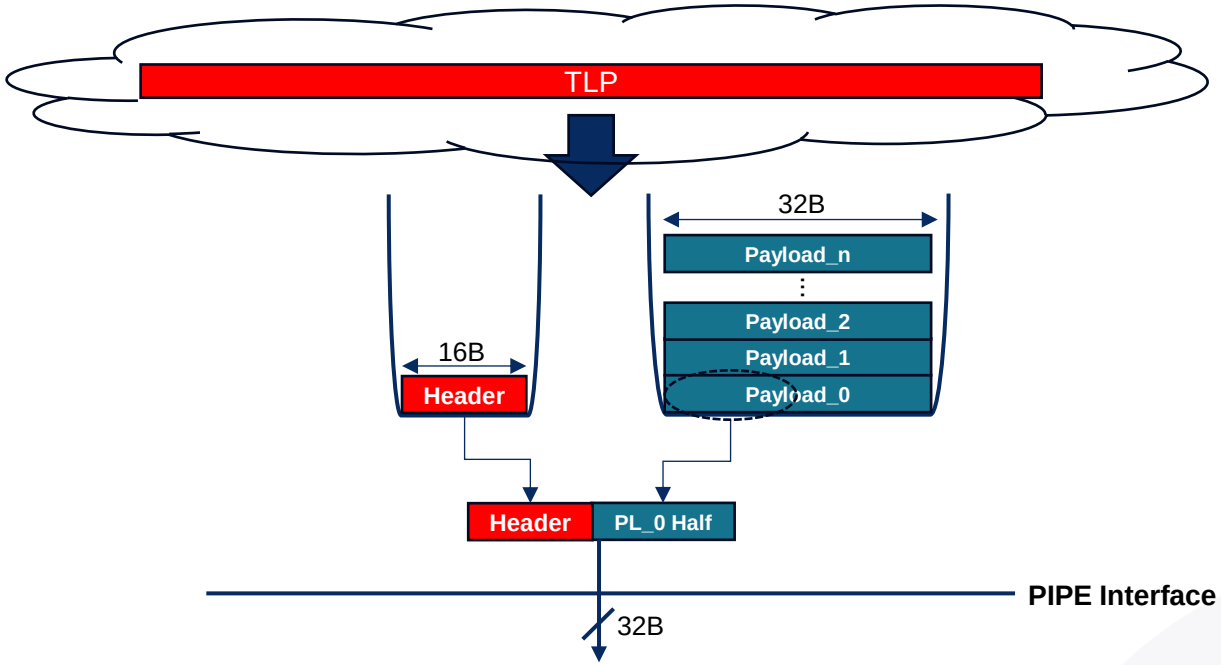
☑ PCIe Controller Architecture



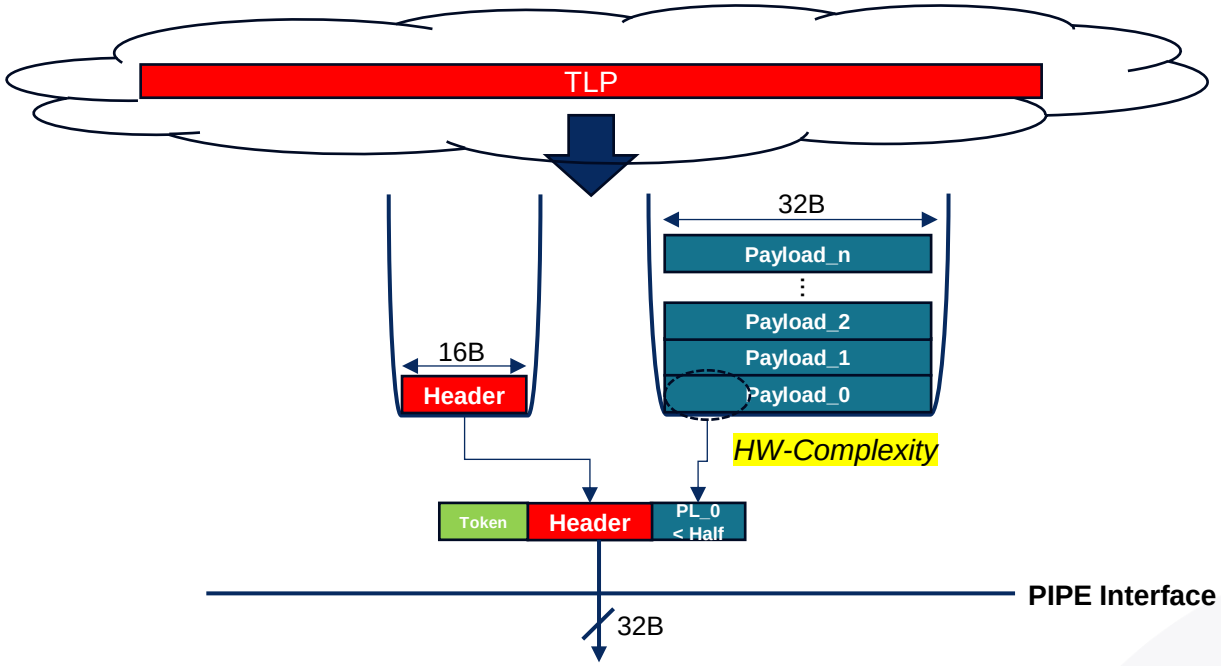
☑ PCIe Controller Architecture



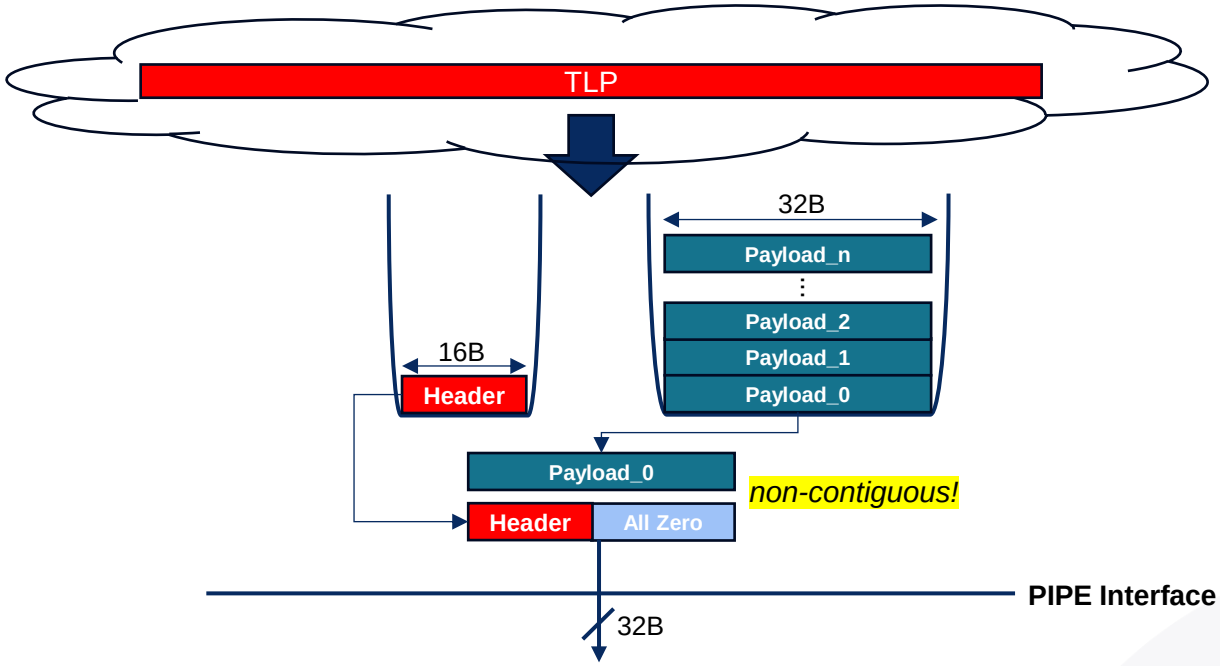
☑ PCIe Controller Architecture



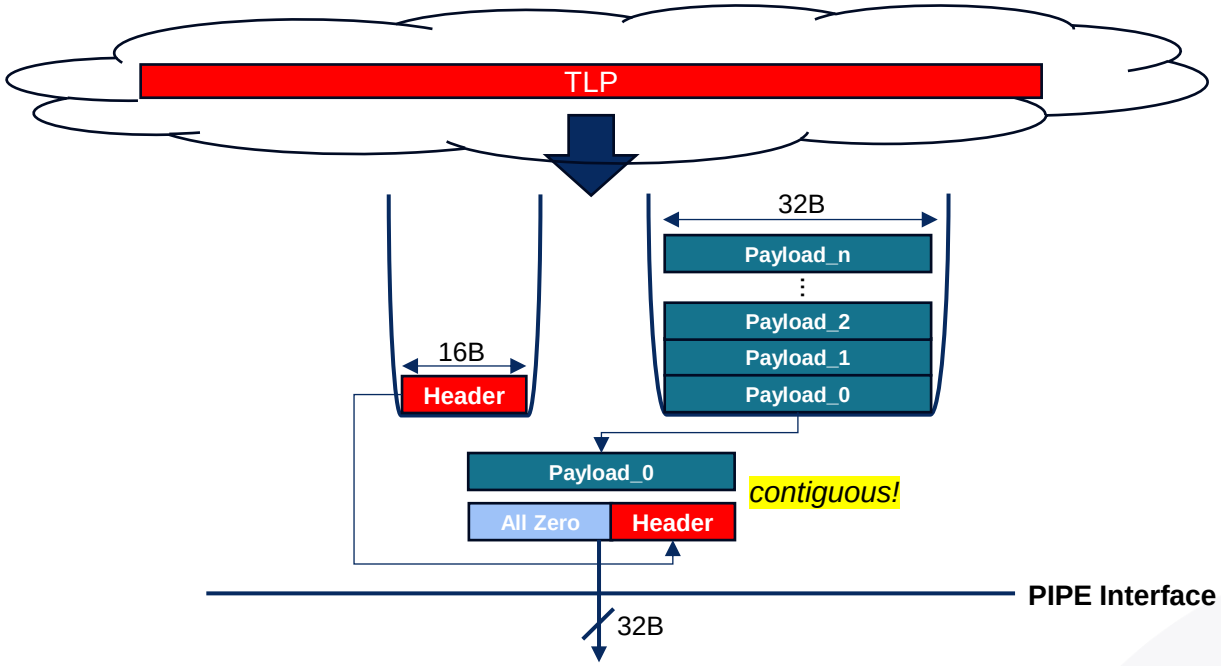
☑ PCIe Controller Architecture



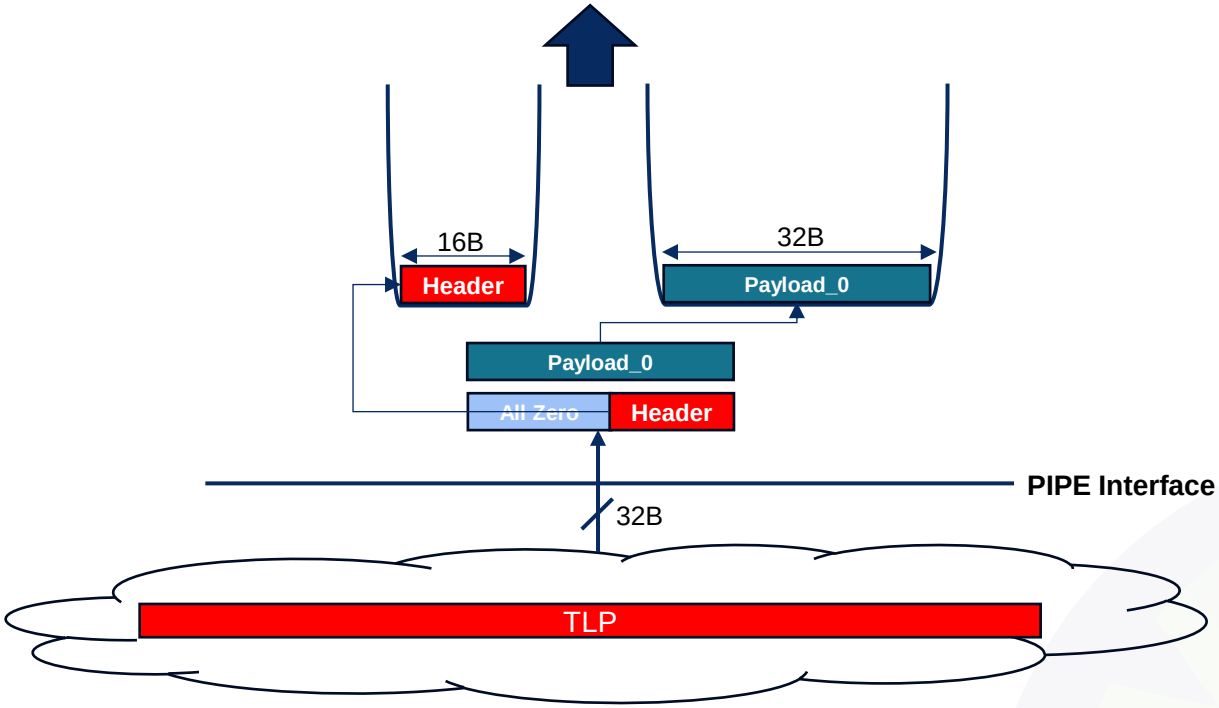
☑ PCIe Controller Architecture



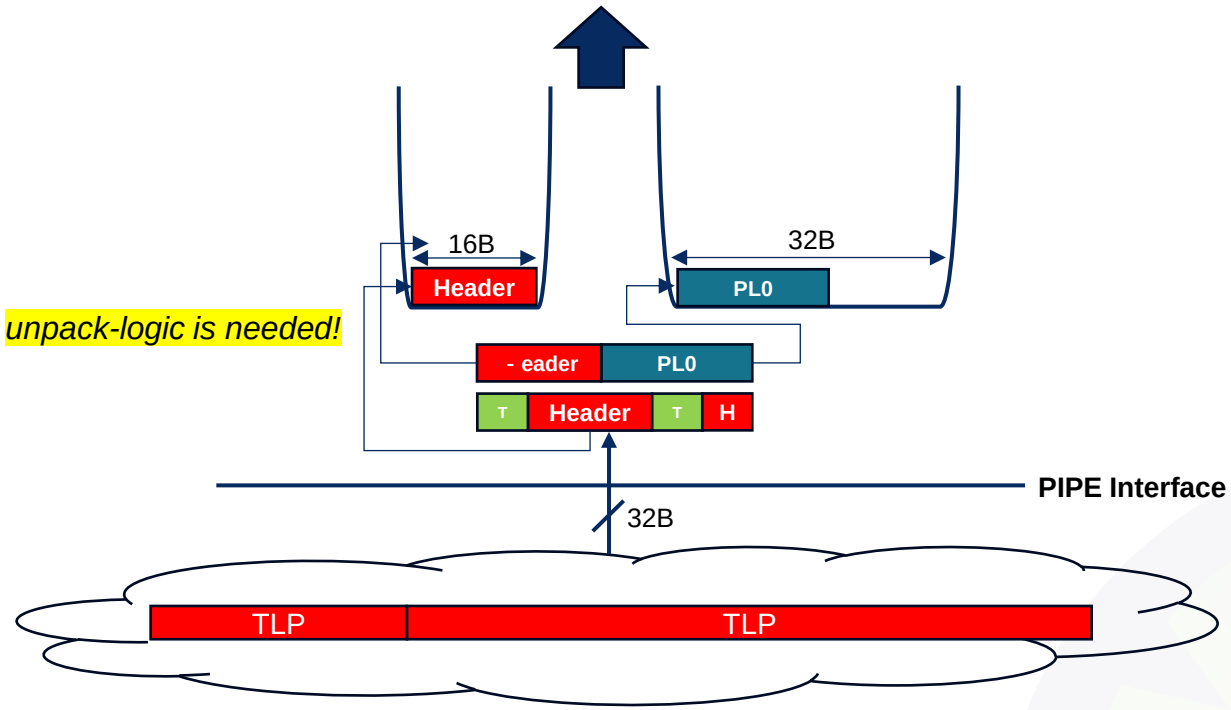
☑ PCIe Controller Architecture



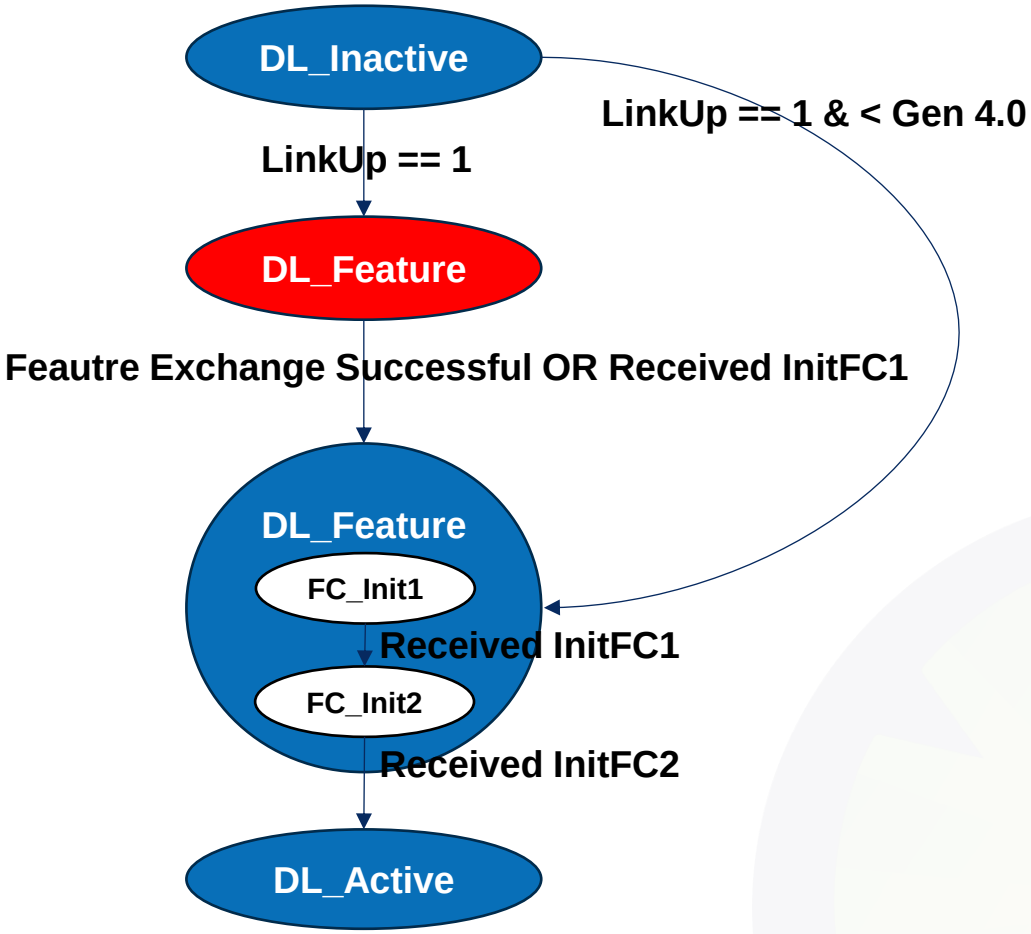
☑ PCIe Controller Architecture



☑ PCIe Controller Architecture



☑ Data Link Control & Management State Machine



☑ Credit

- Spec에서 정의하는 Credit의 단위
  - ex) 1 Credit Unit = 4DW(16B)
- Spec에서 정의하는 Minimum/Maximum Credit

☑ Issues

- 질문은 Github "Issues" Repo의 Issues란에 올려주세요.
  - https://github.com/2025-Spring-URP/Issues

☑ Git Ignore

- gitignore 설정
  - sim과 syn과정에서 발생하는 output은 ignore에 등록

☑ Synthesis

- Clock & Timing Margin
  - 500MHz? 300MHz
- Vivado
  - Target Board 설정

☑ Week_5

- **Seminar**
  - 담당 : Team 01
  - 주제

	내용	핵심	기타
1. Ack/Nak Protocol	Data Link Layer의 역할 중 Ack/Nak Protocol	• Ack/Nak Protocol 동작 • Ack/Nak Protocol에 대한 DLLP Format	참고 : PCI Express® Base Specification Revision 5.0 Version 1.0

감사합니다.

Q&A