

...

Week 3

Please enter a sub-title here.

| 주관기관 | 성균관대학교

| 총괄책임자 | 박 상 현

2025.03.14

✓ Directory Hierarchy

▪ /actions

- /README.md

▪ /design

- /sverilog

→ /PCIE_CONTROLLER_TOP.sv

→ /PCIE_PKG.svh

→ /AXI_IF.sv

→ ...

- /filelist.f

▪ /docs

- /README.md

▪ /sim

- /README.md

▪ /env.source

CXL_CACHE Private Watch

main 50 Branches 1 Tag Add file Code

dale40 Merge pull request #330 from scalable-arch/dale/decouple_mem_id_width e68915b · 2 weeks ago 1,300 Commits

.github/workflows	Update fpga_integration.yml	2 weeks ago
actions	update	2 weeks ago
design	Working	2 weeks ago
docs	docs: sync draw.io exported files	3 weeks ago
rtl-actions @ b8a9b70	migration to rtl-actions	2 years ago
sdc	test	5 months ago
sim	use single paramater for AXI data width	2 weeks ago

☑ Utils

▪ MemRd-Type TLP Header Format

```

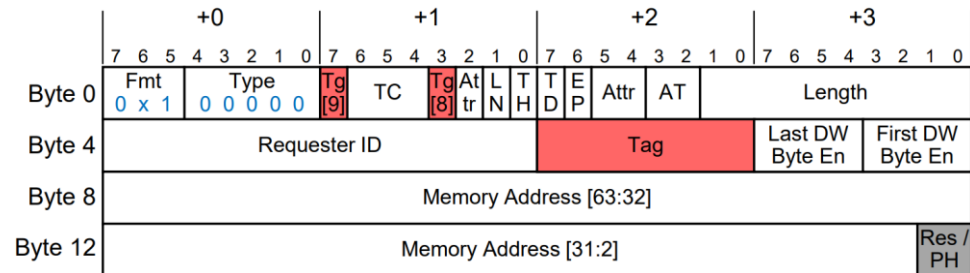
1  typedef struct packed {
2      // Header 16B
3      logic [5:0]      addr_l;
4      logic [1:0]      reserved;
5      logic [23:0]     addr_m;
6      logic [31:0]     addr_h;
7      logic [7:0]      byte_enable;
8      logic [7:0]      tag;
9      logic [15:0]     requester_id;
10
11     logic [7:0]      length_l;
12     logic            td;
13     logic            ep;
14     logic [1:0]      attr_l;
15     logic [1:0]      at;
16     logic [1:0]      length_h;
17     logic            tg_h;
18     logic [2:0]      tc;
19     logic            tg_m;
20     logic            attr_h;
21     logic            ln;
22     logic            th;
23     logic [2:0]      fmt;
24     logic [4:0]      tlp_type;
25 } tlp_memory_req_hdr_t;

```

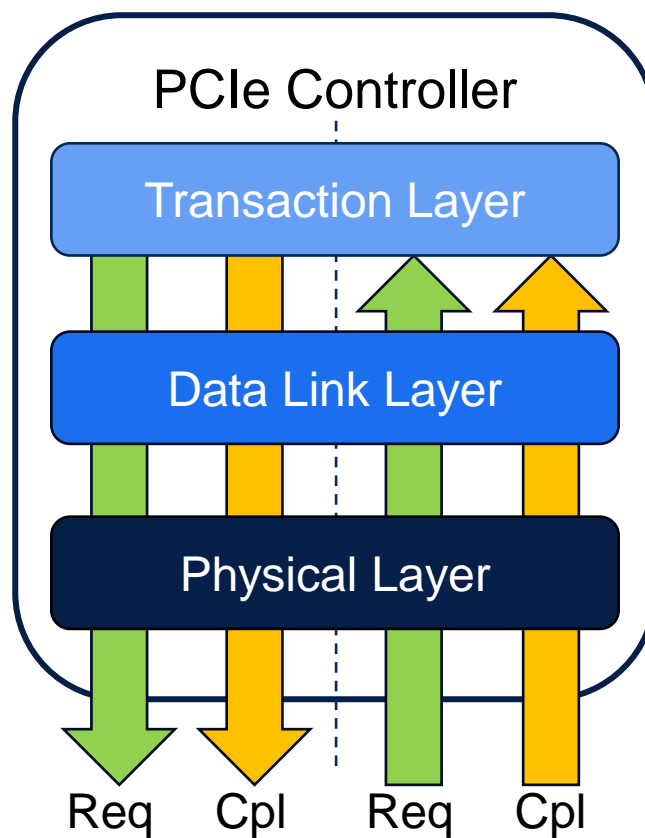
```

1  function automatic tlp_memory_req_hdr_t gen_tlp_memwr_hdr(
2      input logic [63:0] address
3  );
4      tlp_memory_req_hdr_t tlp_memwr_hdr;
5      tlp_memwr_hdr.addr_h = {address[39:32], address[47:40], address[55:48], address[63:56]};
6      /*
7       * TODO:
8       */
9  endfunction

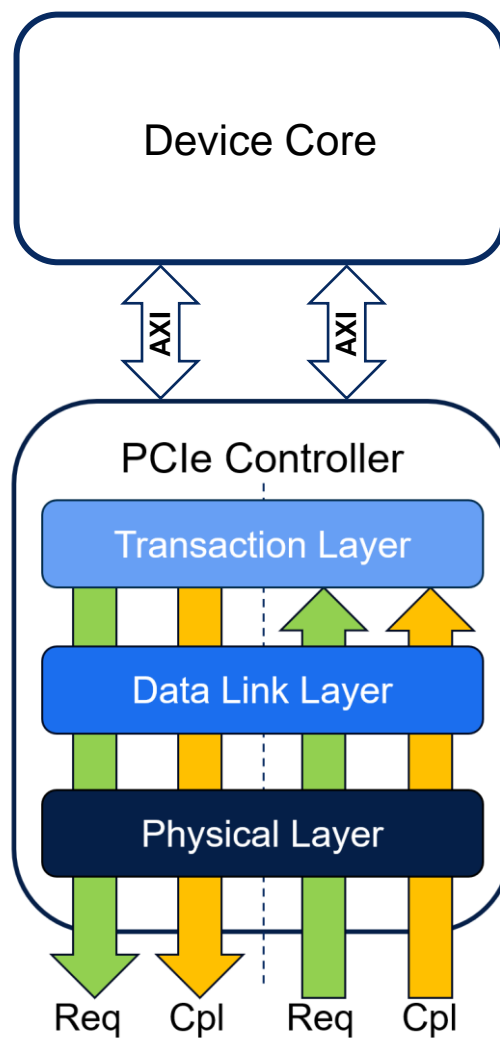
```



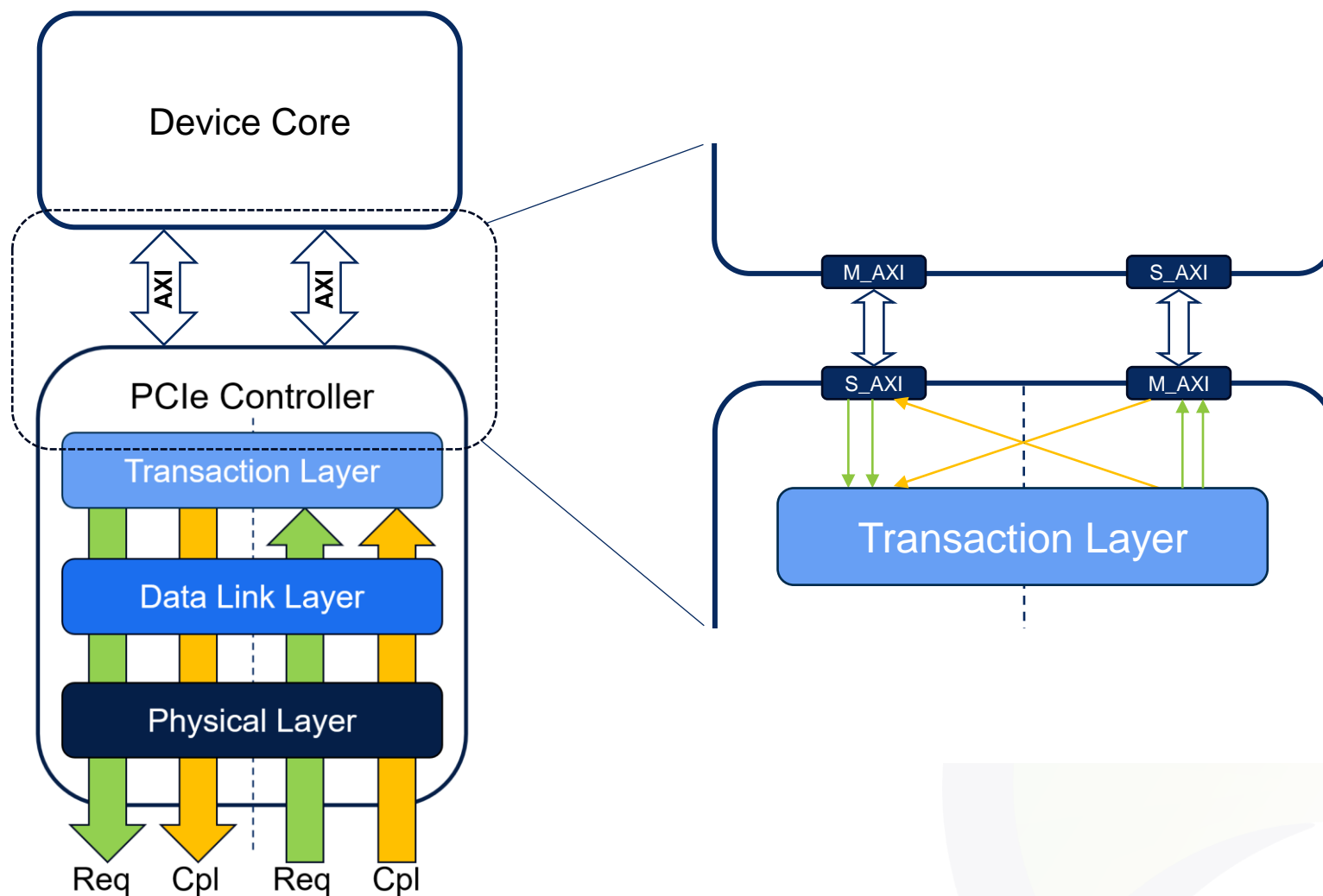
☑ MicroArchitecture



☑ MicroArchitecture

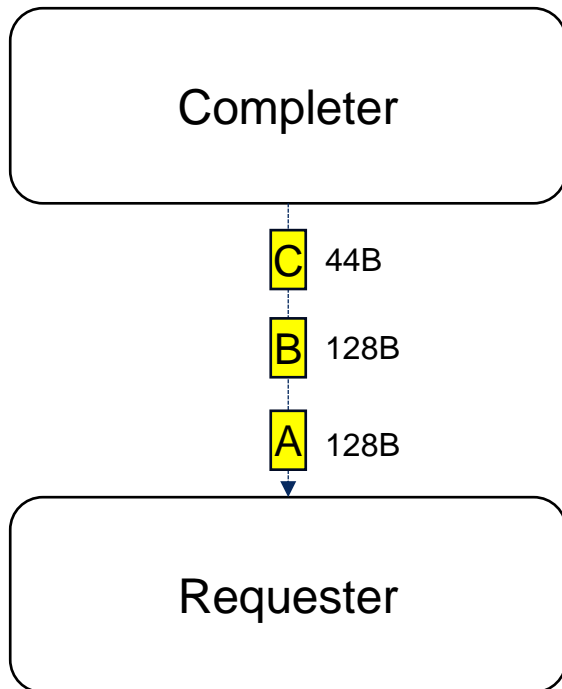


MicroArchitecture



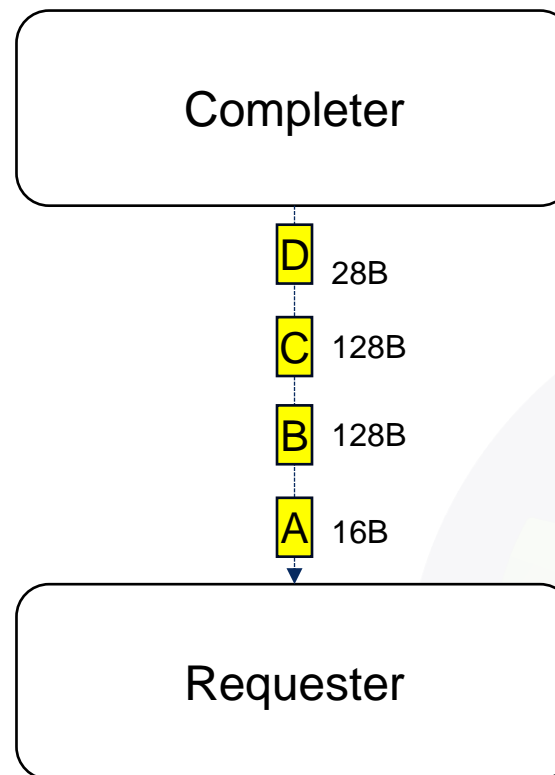
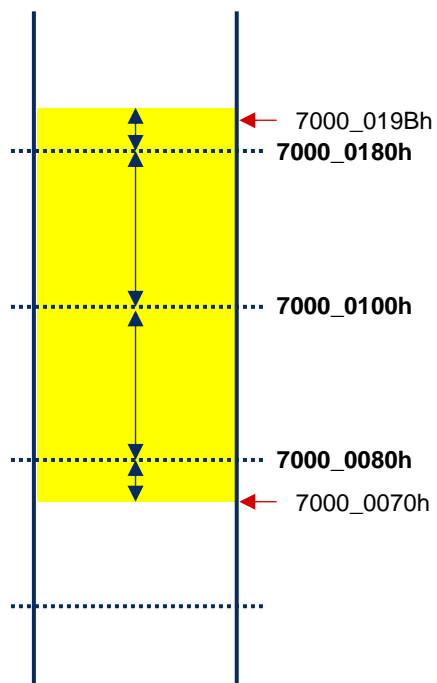
☑ Max_Read_Request_Size & Read Completion Boundary

- MemRd Header의 Length정보에는, Max_Payload_Size보다 큰 값이 담겨있을 수 있다.
 - Ex) Max_Read_Request_Size = 512B, Max_Payload_Size = 128B
 - Requester generates MRd
 - Addr : 7000_0070h
 - Length : 75DW (300bytes)



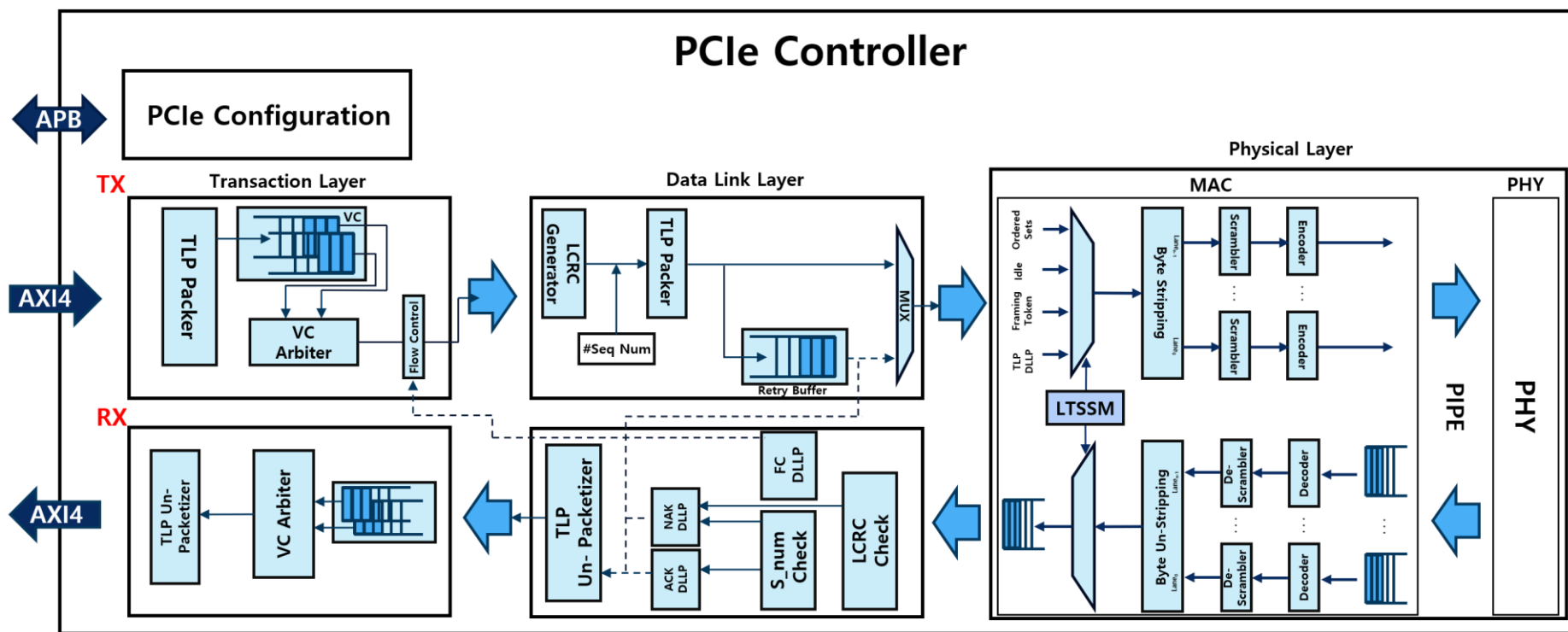
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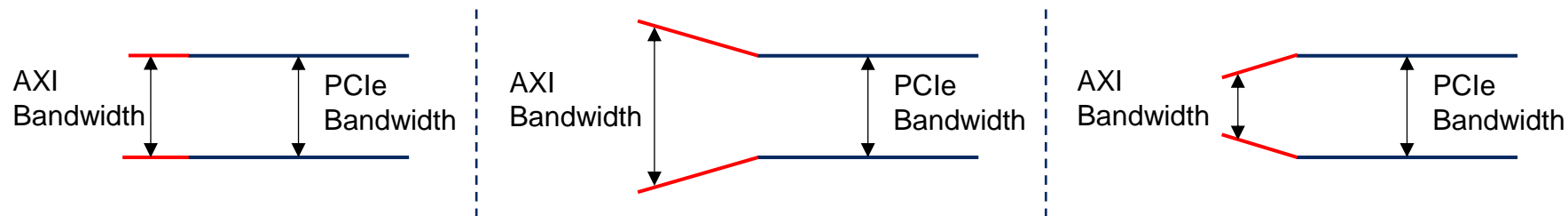
☑ PIPE & AXI Config

- PCIe Link Config = 32GT/s, x4 Lane
- PIPE Config = 500MHz, 32B



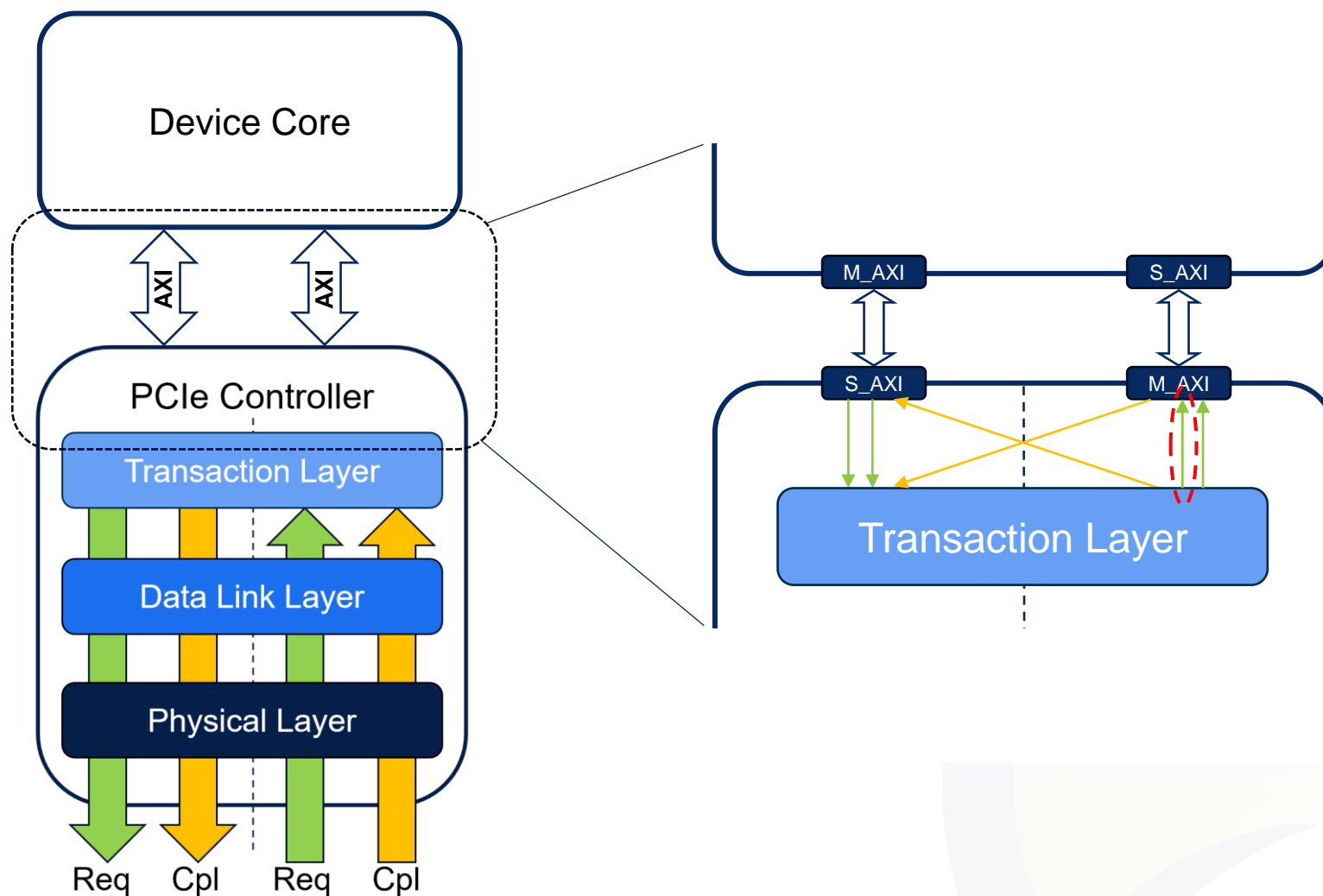
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- PCIe Link Config = 32GT/s, x4 Lane
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- AXI DATA WIDTH = 32B, ACLK = 500MHz(300MHz)

☑ MicroArchitecture



☑ 서버 할당

USER ID	PASSWORD	IP/PORT	주의사항
urp01	1234	IP : 115.145.211.102	<ul style="list-style-type: none">- 다른 사람 작업공간 접속x- Root 건드리지 마세요- Signal-Dump등 메모리 공간 많이 잡아먹는 Job은 지양- 비밀번호 변경 시 담당자에게 메일 하나 보내주세요. 990520kog2@gmail.com- 사용기한 : 6/23(학기 종강일)
urp02		PORT : 7777	
...			
urp12			

Team Num.	Num.	이름
1	1	김민수
	2	윤성빈
	3	김병훈
	4	김경빈
2	5	이승로
	6	임용성
	7	최원기
	8	김주성
3	9	정찬호
	10	조재우
	11	고보성
	12	김원규

☑ Issues

- 질문은 Github "Issues" Repo의 Issues란에 올려주세요.
 - <https://github.com/2025-Spring-URP/Issues>

☑ Week_4

▪ Seminar

- 담당 : Team 03
- 주제

	내용	핵심	기타
1. Flow Control	Data Link Layer의 역할 중 Flow Control	<ul style="list-style-type: none">• Flow Control 동작• Flow Control에 대한 DLLP Format	참고 : PCI Express® Base Specification Revision 5.0 Version 1.0

감사합니다. Q&A



성균관대학교



SAL

SUSTAINABLE ARCHITECTURE LIFE