성균관대학교 | SAL

[25'S URP] PCI-Express Core Design

From PCIe to CXL

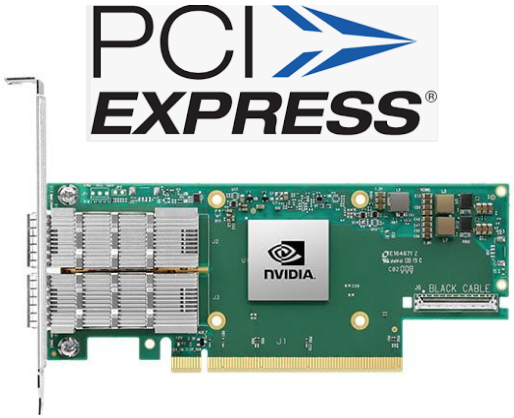
| **주관기관** | 성균관대학교

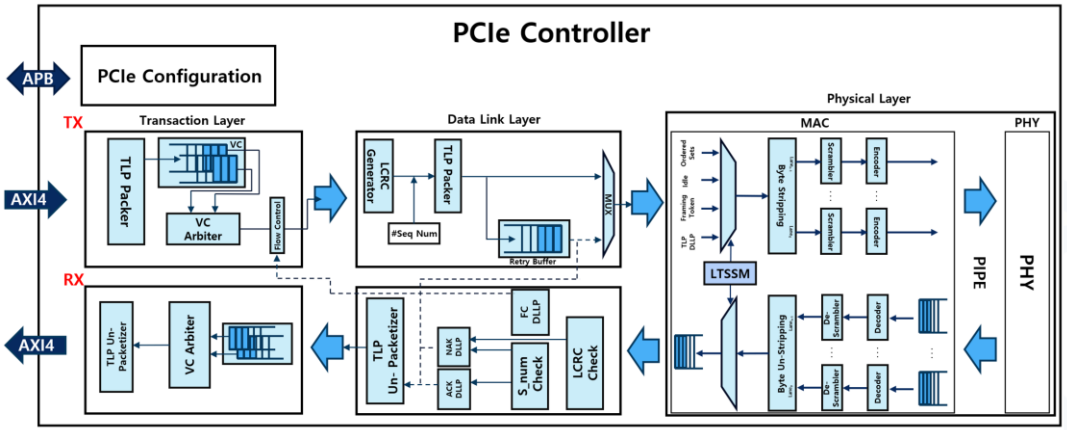
| **총괄책임자** | 박상현/최재혁

2025.03.04

☑ Theme

- PCIe Core(MAC)/Controller Design

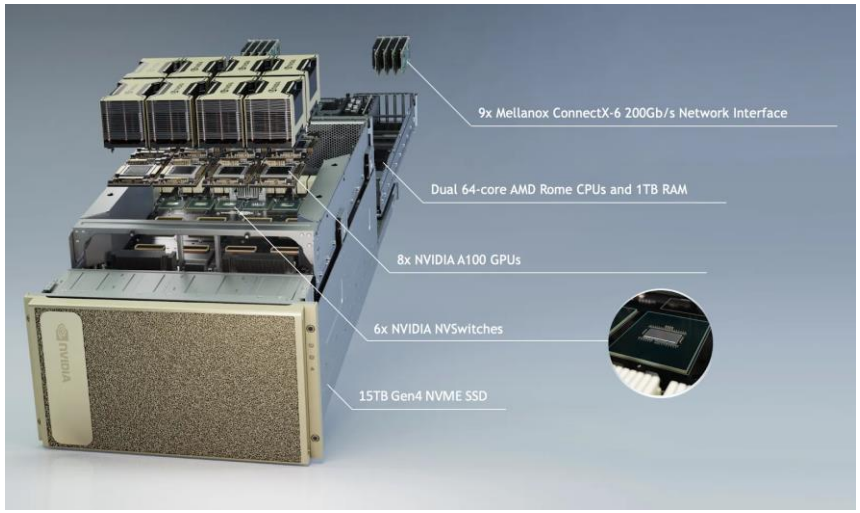


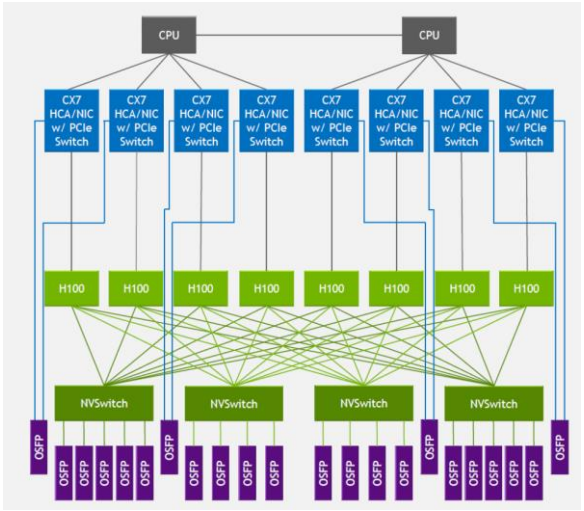


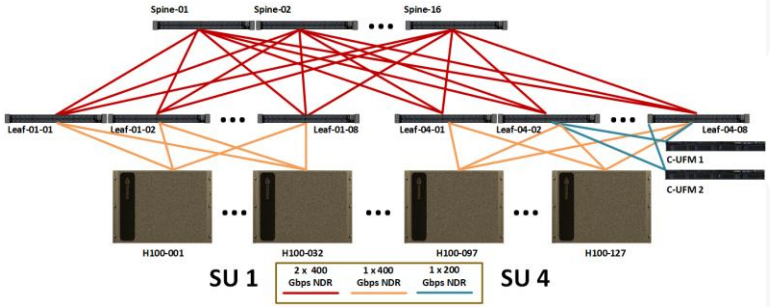
☑ Info

- 매주 화요일 15:00~17:45
- 반도체관 400502호 (변동가능)
- 조교
  - 박상현 / psh2018314072@gmail.com
  - 최재혁 / hyungyu66@naver.com

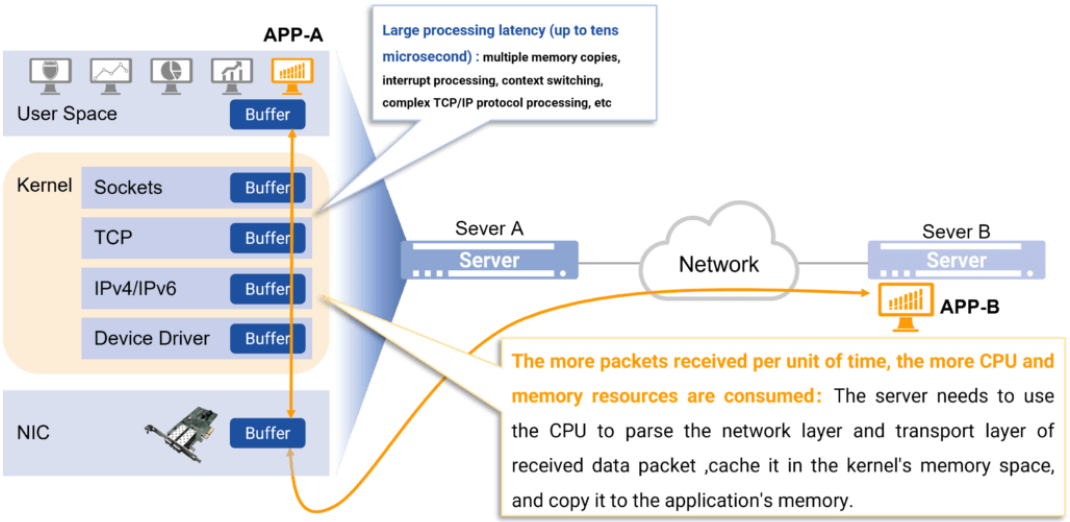
☑ Why NVIDIA?

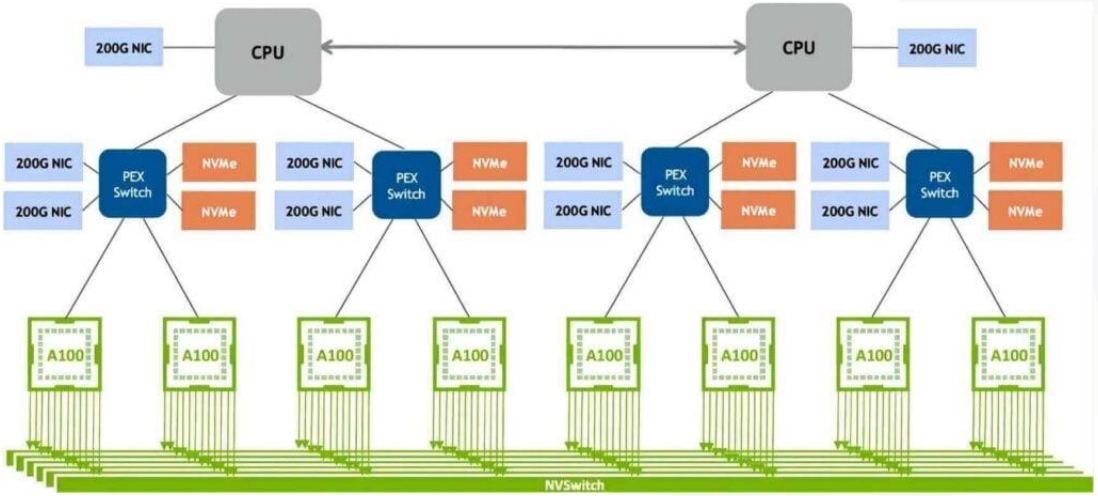






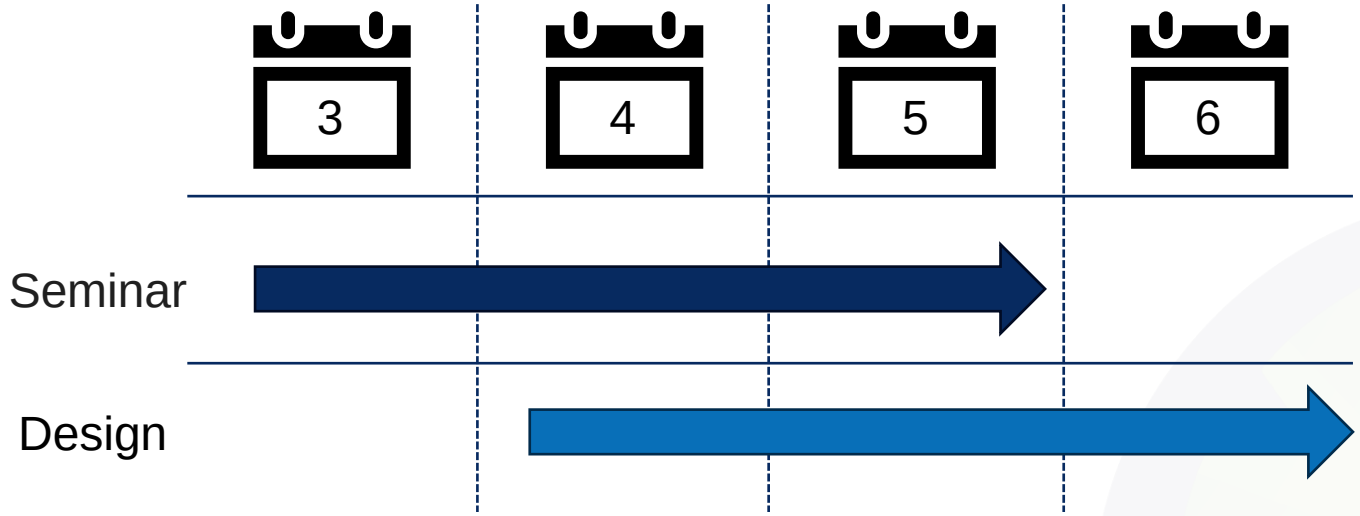
☑ Network & Interconnect





☑ Process

- **Seminar**
  - 주차별 PCIe Spec(gen5) 관련 발표 / 학생 주도 진행 / 조교 피드백 및 보완
    → *주의 : 단순번역(GPT) 금지
- **Design**
  - PCIe Core(MAC) IP 및 관련 VIP 개발



☑ Week_2

- **Seminar**
  - **담당 : Team 01**
  - **주제**

	내용	핵심	기타
1. Github	Github를 활용한 CI/CD	• 기본적인 Git/Github 사용법 • Github를 활용한 통합개발 환경 • 핵심용어 : Pull/Push, Commit, Branch, Merge, Pull-Request, Issue	
2. System Verilog	Scalability/Readability를 위한 다양한 Support	• Package, Interface, Task/Function, Structure	

- **과제**
  - **스프레드시트 : 이메일(github용) / 성균인ID & 핸드폰번호(vpn용)**
  - https://docs.google.com/spreadsheets/d/1mOEksYqqK9KbeBFrW9zuepl2RdivTUywoKiaoZ1ROMs/edit?usp=sharing

감사합니다.

Q&A