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Computer Systems / Rekenaarstelsels 245 - 2020

Lecture 19

Serial Communication – Transmission lines/
Seriële Kommunikasie - Transmissielyne

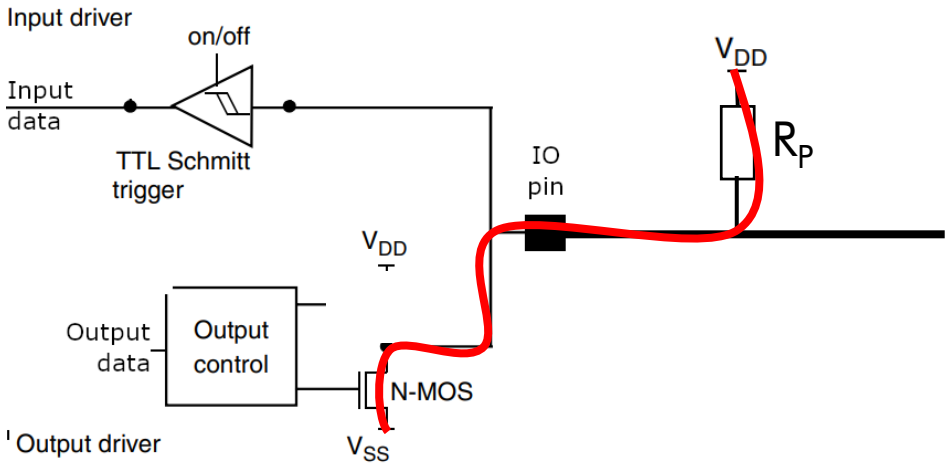
Dr Rensu Theart & Dr Lourens Visagie

Lecture Overview
Lesing oorsig

- I2C pull-up resistor values
- Differential signalling
- Impedance matching

I2C Pull-up resistor choice
I2C optrek weerstand keuse

- Can't use too **low** resistor value – then we have the same problem as with push-pull output (microcontroller cannot sink enough current, possibility of damaging port)



$$I = \frac{V_{DD}}{R_P}$$

I2C Pull-up resistor choice
I2C optrek weerstand keuse

- Can't use too **low** resistor value:
- With R_P too low, the IO port will not be able to drive the signal to 0V
- Minimum R_P value is determined by $V_{OL}(max)$ – the maximum voltage that the port can output that will still be recognised as a low (0) condition

$$R_P(min) = \frac{(V_{DD} - V_{OL}(max))}{I_{OL}}$$

For V_{DD} = 3.3V, V_{OL} = 0.4V, I_{OL}=8mA:
→R_P(min) = 360 ohm

For V_{DD} = 3.3V, V_{OL} = 1.3V, I_{OL} = 20mA
→R_P(min) = 100 ohm

From the STM32F411VE Datasheet:
Output driving current The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH})…

Table 54. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin	CMOS port(2)	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin	I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2)	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin	I_{IO} =+8 mA 2.7 V ≤V_{DD} ≤3.6 V	2.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	V
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DD}–1.3(4)	-	
V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	V
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DD}–0.4(4)	-	
V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6 V	-	0.4(5)	V
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DD}–0.4(5)	-	

I2C Pull-up resistor choice
I2C optrek weerstand keuse

- Can't use too **low** resistor value:
- Even if our microcontroller can work with R_P = 100ohm it does not mean other devices on the same bus will be able to recognise low voltage (their V_{IL} might be > microcontroller V_{OL})
- You have to perform this calculation for all the devices on the bus, and use $R_P(min) = max(R_{P1}(min), R_{P2}(min), \ldots)$

- Or design according to the I2C specification. All I2C devices should conform to this:
- NXP I2C-bus specification and user manual:

https://www.nxp.com/docs/en/user-guide/UM10204.pdf

Table 9. Characteristics of the SDA and SCL I/O stages
n/a = not applicable.

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
V_{IL}	LOW-level input voltage[1]		−0.5	$0.3V_{DD}$	−0.5	$0.3V_{DD}$	−0.5	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage[1]		$0.7V_{DD}$	[2]	$0.7V_{DD}$	[2]	$0.7V_{DD}$[1]	[2]	V
V_{hys}	hysteresis of Schmitt trigger inputs		-	-	$0.05V_{DD}$	-	$0.05V_{DD}$	-	V
V_{OL1}	LOW-level output voltage 1	(open-drain or open-collector) at 3 mA sink current; V_{DD} > 2 V	0	0.4	0	0.4	0	0.4	V
V_{OL2}	LOW-level output voltage 2	(open-drain or open-collector) at 2 mA sink current[3]; $V_{DD} \leq 2$ V	-	-	0	$0.2V_{DD}$	0	$0.2V_{DD}$	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	3	-	20	-	mA
		V_{OL} = 0.6 V[4]	-	-	6	-	-	-	mA
t_{of}	output fall time from V_{IHmin} to V_{ILmax}		-	250[5]	$20 \times (V_{DD} / 5.5\ V)$[6]	250[5]	$20 \times (V_{DD} / 5.5\ V)$[6]	120[7]	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	-	0	50[8]	0	50[8]	ns
I_i	input current each I/O pin	$0.1V_{DD} < V_I < 0.9V_{DDmax}$	−10	+10	−10[9]	+10[9]	−10[9]	+10[9]	µA
C_i	capacitance for each I/O pin[10]		-	10	-	10	-	10	pF

Standard mode : 100kHz
Fast-mode: 400kHz
Fast-mode Plus: 1MHz

I2C Pull-up resistor choice
I2C optrek weerstand keuse

- Can't use too **low** resistor value:

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
V_{OL1}	LOW-level output voltage 1	(open-drain or open-collector) at 3 mA sink current; V_{DD} > 2 V	0	0.4	0	0.4	0	0.4	V
V_{OL2}	LOW-level output voltage 2	(open-drain or open-collector) at 2 mA sink current[3]; $V_{DD} \leq 2$ V	-	-	0	$0.2V_{DD}$	0	$0.2V_{DD}$	V

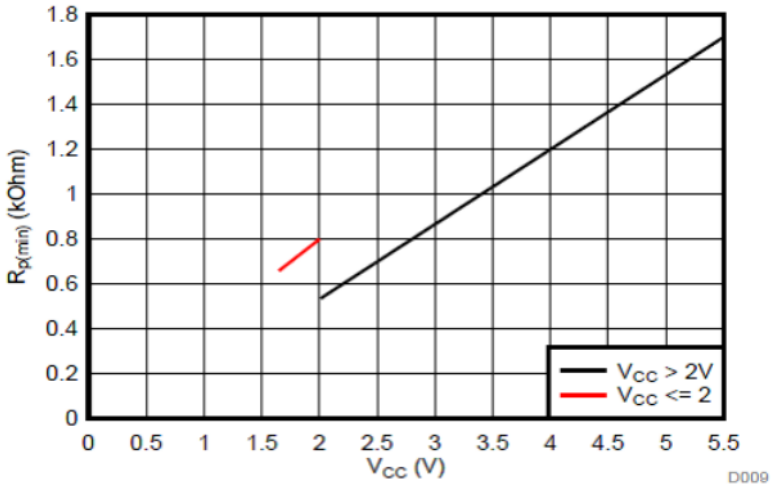


Figure 2. Minimum Pullup Resistance [R_P (min)] vs Pullup Reference Voltage (V_{CC})

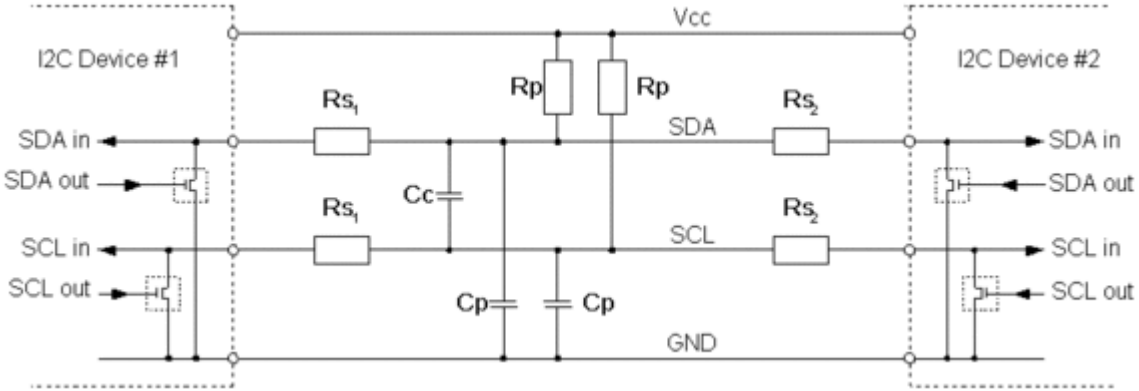
For V_{DD} = 3.3V, V_{OL} = 0.4V, I_{OL}=3mA:
→R_P(min) = 966 ohm

I2C Pull-up resistor choice
I2C optrek weerstand keuse

- Ok, so why don't we just always use a 1kΩ pull-up resistor (for a 3.3V bus)?
- I = V/R, and larger current = more power.
- Use a larger pull-up resistor value to decrease power consumption (especially if powering from batteries)

I2C Pull-up resistor choice
I2C optrek weerstand keuse

- Can't use too **high** resistor value: I2C wires and tracks are not perfect conductors



VCC	I2C supply voltage, typically ranging from 1.2 V to 5.5 V
GND	Common ground
SDA	Serial data (I2C data line)
SCL	Serial clock (I2C clock line)
Rp	Pull-up resistance (a.k.a. I2C termination)
Rs	Serial resistance
Cp	Wire capacitance
Cc	Cross channel capacitance

https://www.i2c-bus.org/i2c-primer/typical-i2c-bus-setup/

I2C Pull-up resistor choice
I2C optrek weerstand keuse

- Can't use too **high** resistor value:
- Bus capacitance causes non-zero rise time for I2C signals
- If the pull-up resistor value is too high the I2C line may not rise to a logical 1 in the allowed rise time

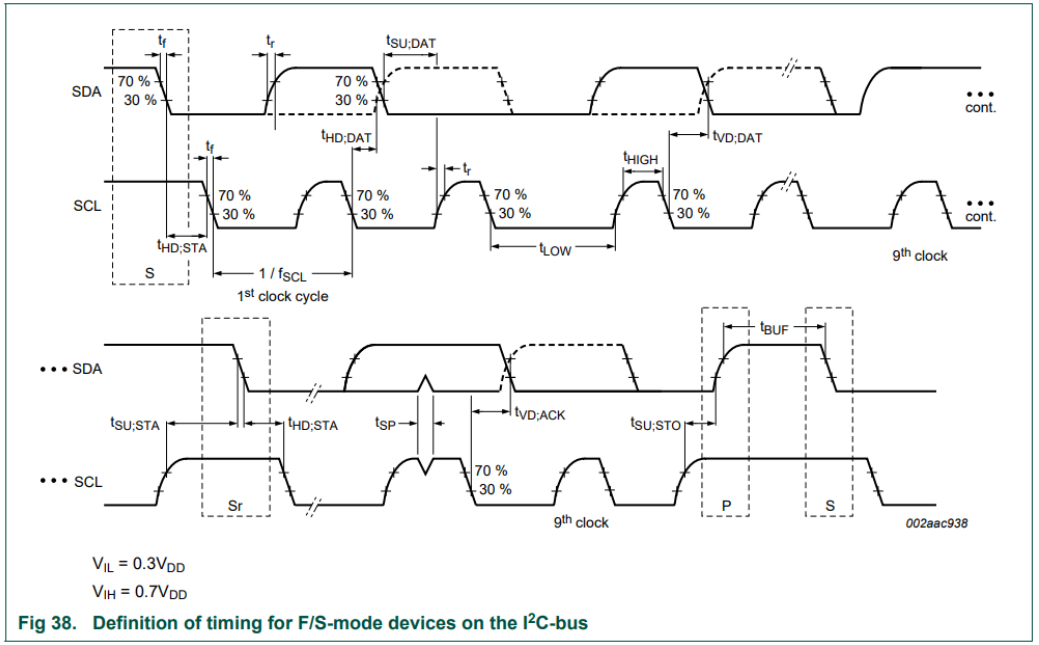


Fig 38. Definition of timing for F/S-mode devices on the I²C-bus

- Faster bus speeds require shorter rise times. R_P(min) is limited by IO port characteristics. R_P(max) is limited by I2C bus frequency and bus capacitance

I2C Pull-up resistor choice
I2C optrek weerstand keuse

- Can't use too **high** resistor value:
- Voltage waveform over time (during rise):
- $V(t) = V_{DD}\left(1 - e^{\frac{-t}{R_P C}}\right)$
- Voltage has to rise from V_{IL} to V_{IH} in allowed rise time, t_r
- I2C specification:
  - $V_{IL} = 0.3V_{DD}$
  - $V_{IH} = 0.7V_{DD}$
- $t_r = t_2 - t_1 = 0.8473R_PC_B$

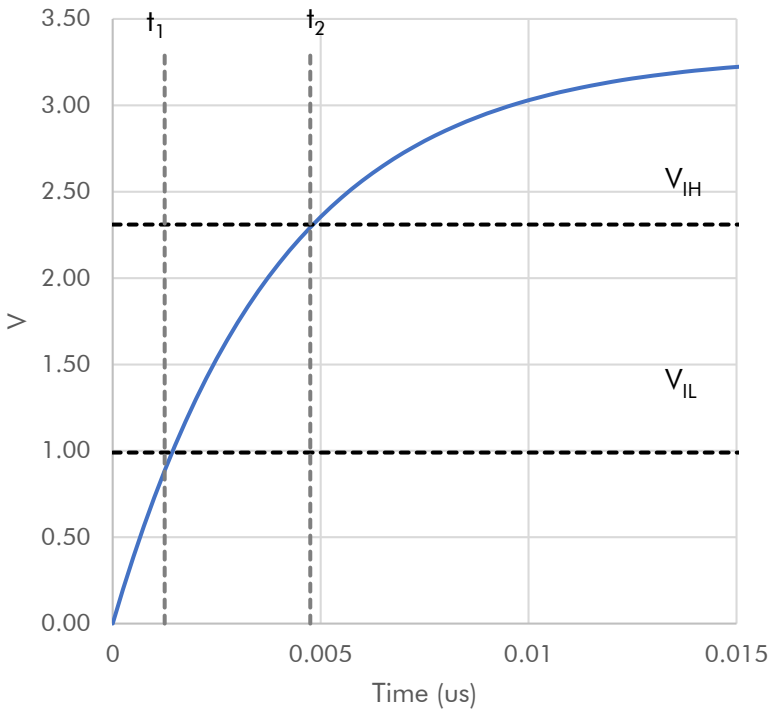


Table 1. Parametrics from I2C specifications

Parameter		Standard Mode (Max)	Fast Mode (Max)	Fast Mode Plus (Max)	Unit
t_r	Rise time of both SDA and SCL signals	1000	300	120	ns
C_b	Capacitive load for each bus line	400	400	550	pF

I2C Pull-up resistor choice
I2C optrek weerstand keuse

- Can't use too **high** resistor value:

$$R_P(max) = \frac{t_r}{0.8473 C_B}$$

- Example, for standard mode (100 kHz), C_B=200pF: $R_P(max) = 5k9$
- So how do we know what the bus capacitance, C_B, is?
- →Calculate:
  - Sum of all IO pin input capacitance (from datasheets)
  - PCB copper trace capacitance
  - Wire capacitance

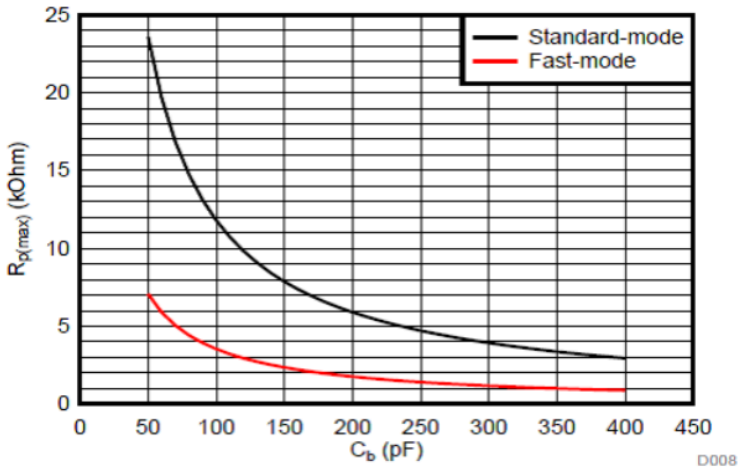
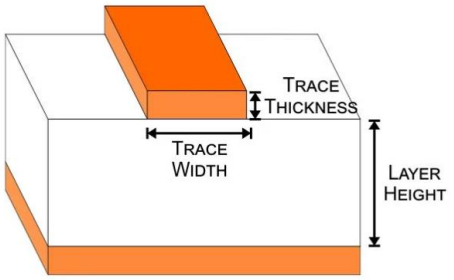


Figure 3. Maximum Pullup Resistance [R_P (max)] vs Bus Capacitance (C_b)

$$C[pf] \approx \frac{0.264 \frac{[pf]}{[mm]} (\epsilon_r + 1.41)}{Ln\left(\frac{0.598 \frac{1}{[mm]} \cdot \text{layer height}}{0.08 \frac{1}{[mm]} \cdot \text{trace width} + 0.1 \frac{1}{[mm]} \cdot \text{trace thickness}}\right)}$$



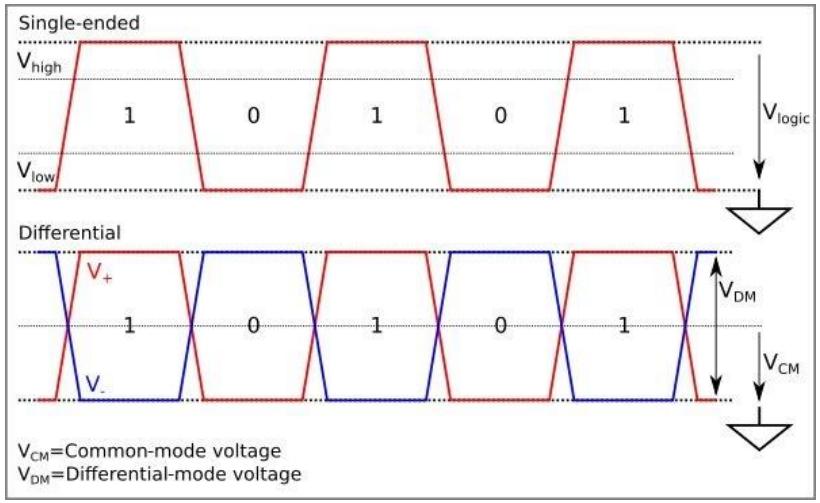
I2C Pull-up resistor choice
I2C optrek weerstand keuse

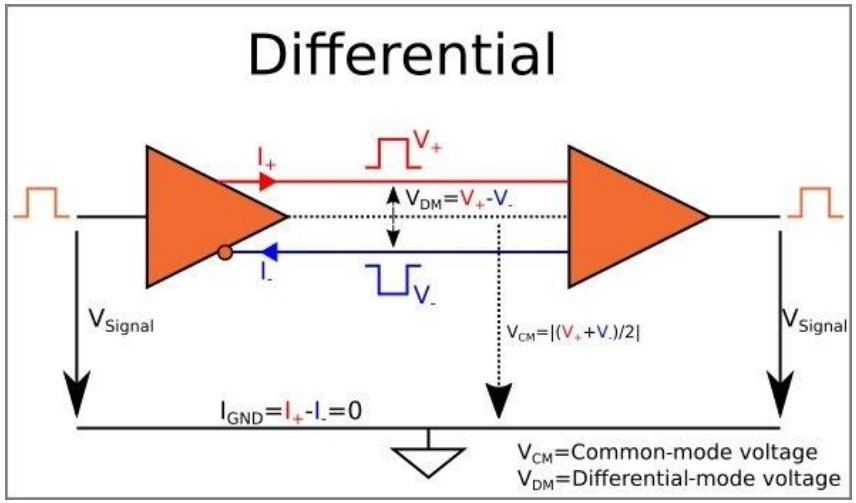
- In practise: trial-and-error approach (try different resistor values until signal is acceptable)
- Always use oscilloscope to check signal integrity
- Can also use multiple pull-up resistors, then calculate equivalent resistance for parallel pull-up resistors

- Further reading:
- https://www.allaboutcircuits.com/technical-articles/i2c-design-mathematics-capacitance-and-resistance/
- https://www.ti.com/lit/an/slva689/slva689.pdf

Differential Signalling
Differensiële Seine

- Differential signalling: In stead of having a single (ground referenced) signal, use two complementary signals: the original signal, and an inverted version of it
- Receiver detects potential difference between non-inverted and inverted signals



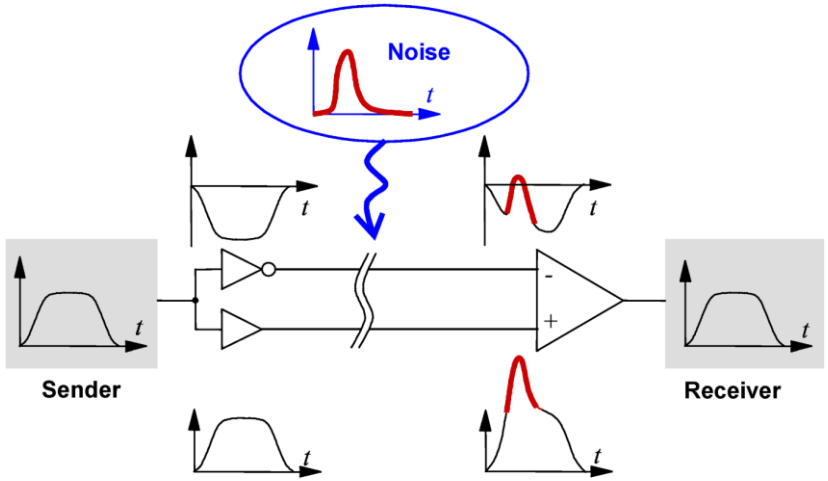


- The two signals are balanced → they are equal in magnitude but opposite polarity relative to common mode voltage.
- You need two conductors for one signal → more wires

https://www.allaboutcircuits.com/technical-articles/the-why-and-how-of-differential-signaling/

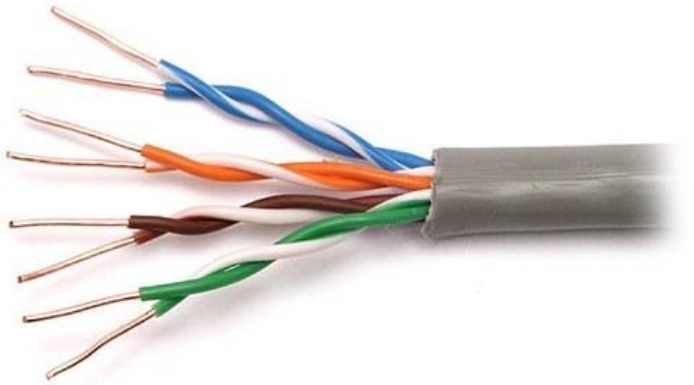
Differential Signalling
Differensiële Seine

- <u>Advantages</u> of differential signalling:
- Balanced signals imply there is ideally no return current – can possibly do away with a common ground connection
- Resistance to electromagnetic interference and "crosstalk"
  - EM noise affects both inverted and non-inverted signals.
  - The receiver only responds to the voltage difference between inverted and non-inverted signals, so noise is suppressed



Differential Signalling
Differensiële Seine

- Advantages of differential signalling:
- Differential signalling is less likely to cause EM interference:
  - Both inverted and non-inverted signals will cause EMI (changes in signal causes conductor to radiate EM waves – like an antenna)
  - But electromagnetic fields will be equal in magnitude but opposite in polarity, thus cancelling out (or at least greatly reducing the effect)
  - Need to keep both conductors close to each other (for instance twisted pairs in cables)



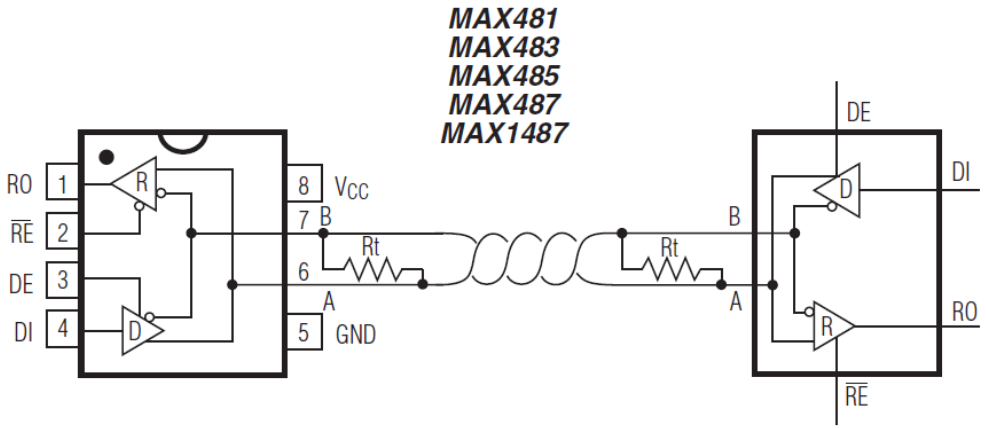
Differential Signalling
Differensiële Seine

- Advantages of differential signalling:
- Lower voltage levels can be used:
  - Signal-to-noise ratio (SNR) for differential signal is double that of single-ended signal with same common-mode voltage
  - Lower voltage implies lower radiated EMI, reduced power consumption and can transmit signals with higher frequencies

- There is one important implication:
  - Wires or traces carrying differential signals must have equal length, otherwise the one signal will arrive before the other – cross-over point will shift

Differential Signalling
Differensiële Seine

- Microcontrollers cannot interface with differential signals directly – need an external transceiver
- Examples of differential signalling:
- LVDS (Low Voltage Differential Signalling)
- RS-422: UART, but with differential signalling
- RS-485: Same as RS-422, but with tristate logic in transmitter – allows transmitter to turn off, thereby allowing for a communications bus – multiple devices using only two wires.



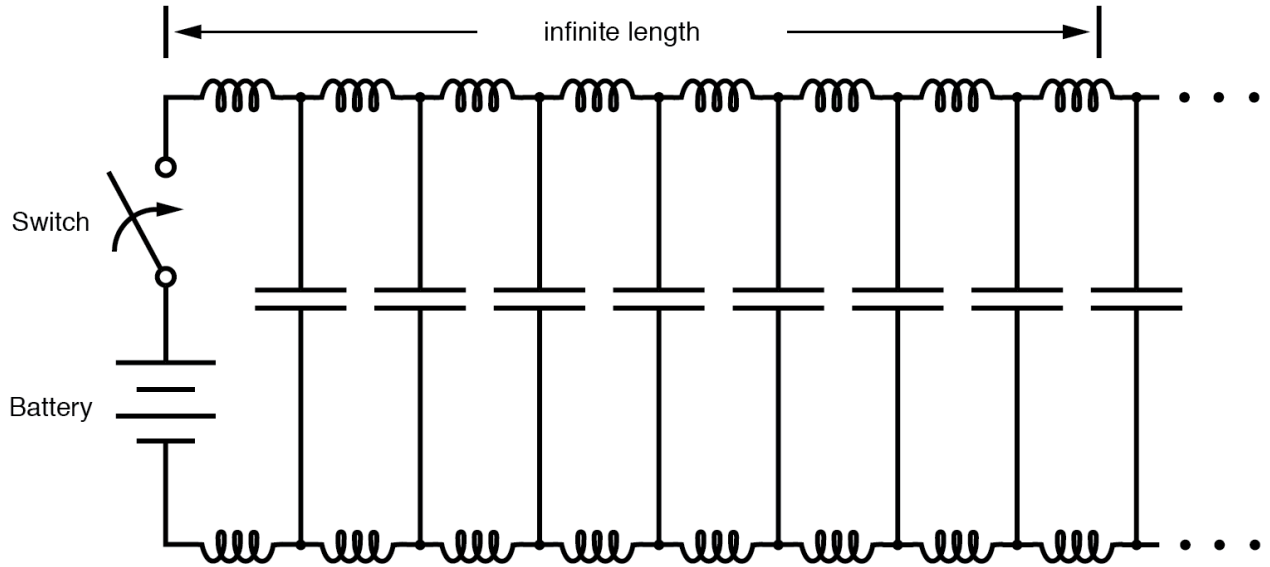
- Also: Ethernet, CAN, USB

Impedance Matching
Impedansie Aanpassing

- A theoretical ideal conductor is an equipotential connection – single voltage along entire conductor at any point in time
- Signals travel along conductors at the speed of light. If the signal changes fast or the cable is long, the conductor has to be modelled as a transmission line→ impedance matching at connections become important

Impedance Matching
Impedansie Aanpassing

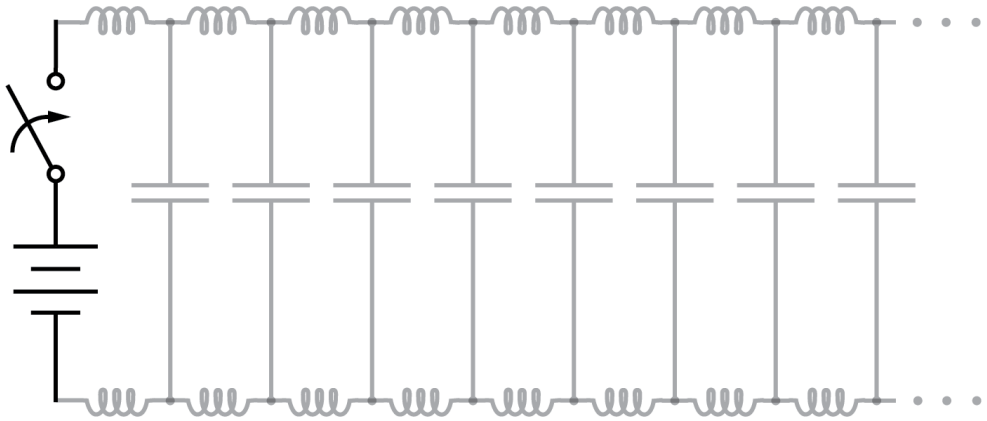
- Characteristic impedance:
- Consider two parallel wires with infinite length (assume zero resistance) and a voltage difference that is switched on at time t0
- The two conductors separated by insulating material will have capacitance between them
- Current drawn from charging up capacitors will be limited by wire inductance



https://www.allaboutcircuits.com/textbook/alternating-current/chpt-14/characteristic-impedance/

Impedance Matching
Impedansie Aanpassing

- Characteristic impedance:
- Electric charge carriers moves at nearly the speed of light, thus voltage and current "wave front" will also propagate down the lines at the same velocity
- As the wave propagates, distributed capacitance and inductance charges to full voltage and current



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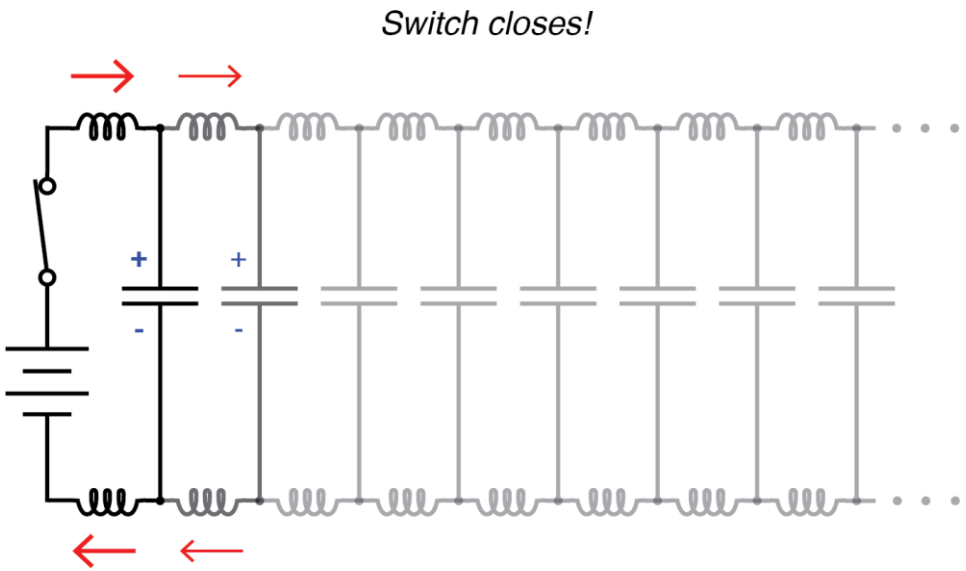

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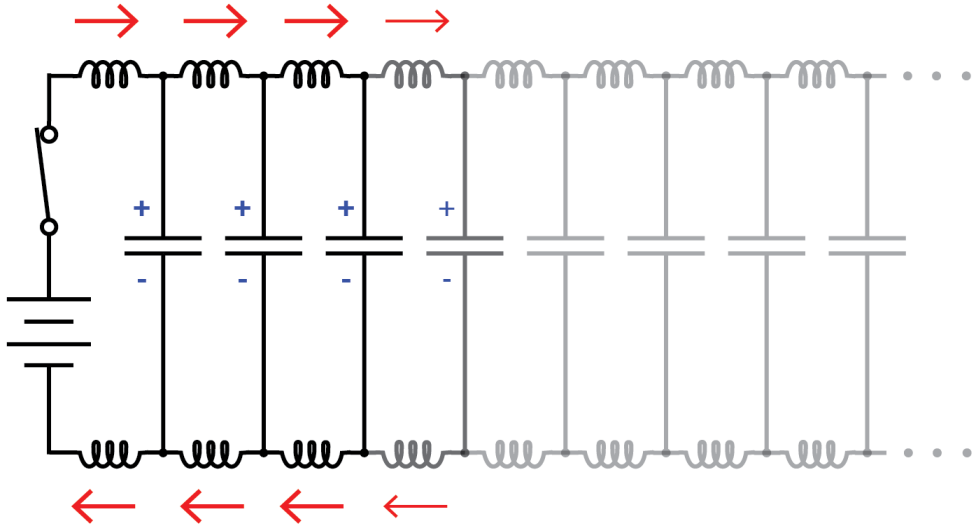

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Impedance Matching
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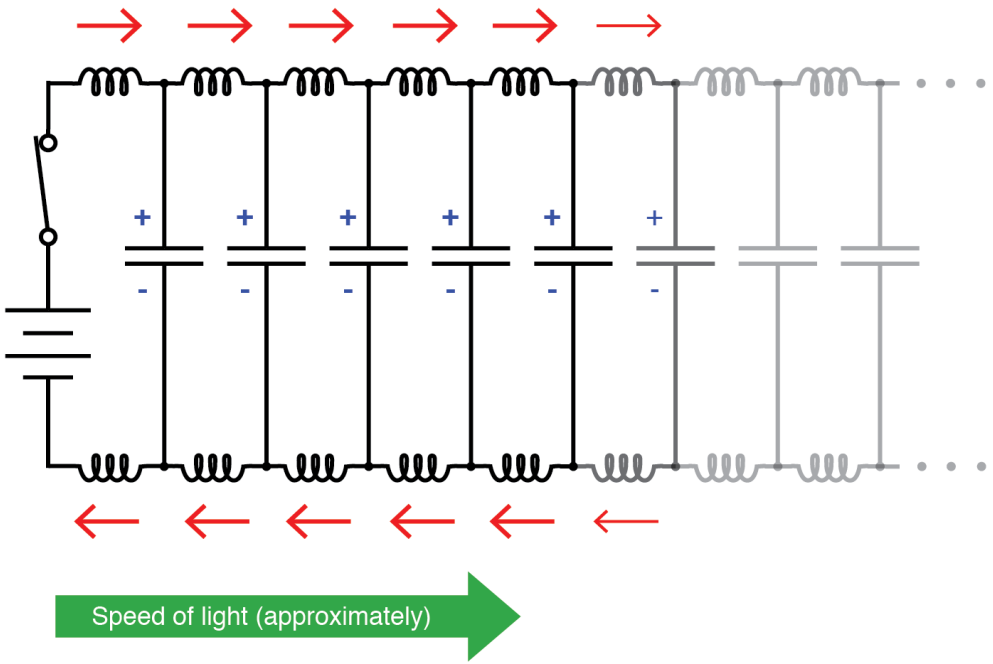


Impedance Matching
Impedansie Aanpassing

- Characteristic impedance:
- If the lines are infinitely long, there will be a constant current flowing, and the transmission line behaves like a constant load
- Characteristic impedance of a transmission line is the equivalent resistance if it were infinitely long (owing to the distributed capacitance and inductance and the voltage and current “waves” propagate at near the speed of light)
- Assuming no energy dissipation (zero conductor resistance) the characteristic impedance equals the square root of the ratio of inductance per unit length to capacitance per unit length
- $Z_0 = \sqrt{\frac{L}{C}}$

Impedance Matching
Impedansie Aanpassing

- Characteristic impedance:
- It is NOT the resistance of the wire (good transmission lines have near zero resistance)
- It is determined by the geometry of the two conductors
- Typical values: 50 or 75 ohm for coaxial cables. Twisted pair ~100 ohm
- On a PCB: thickness of traces, type of material, distance to ground plane

$$Z_0 = \frac{276}{\sqrt{k}} \log \frac{d}{r}$$

Where,

Z_0 = Characteristic impedance of line
d = Distance between conductor centers
r = Conductor radius
k = Relative permittivity of insulation between conductors

$$Z_0 = \frac{138}{\sqrt{k}} \log \frac{d_1}{d_2}$$

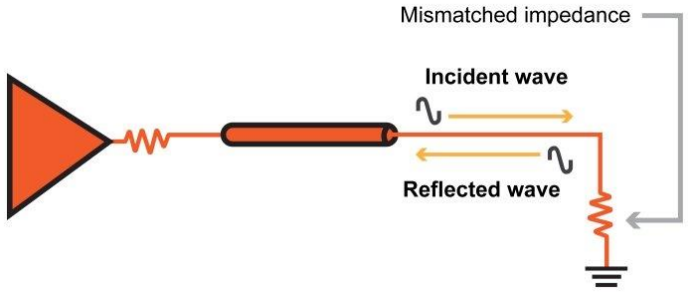
Where,

Z_0 = Characteristic impedance of line
d_1 = Inside diameter of outer conductor
d_2 = Outside diameter of inner conductor
k = Relative permittivity of insulation between conductors

https://www.allaboutcircuits.com/textbook/alternating-current/chpt-14/characteristic-impedance/

Impedance Matching
Impedansie Aanpassing

- Why does this matter?
- If there is a change to the characteristic impedance along the way, part of the signal will be reflected back



- If the propagation delay along the conductor is longer that a fraction (>20%) of the rise or fall time, reflections may distort the digital characteristics of the waveform→ incorrect logic
- Becomes a problem is the signal rise or fall time is short (fast signalling frequency) or if the propagation delay is long (longer conductor)

Impedance Matching
Impedansie Aanpassing

- Why does this matter?
- Velocity factor is the ratio of speed that wavefront propagates relative to speed of light in vacuum
- Can range from 50% to 75%

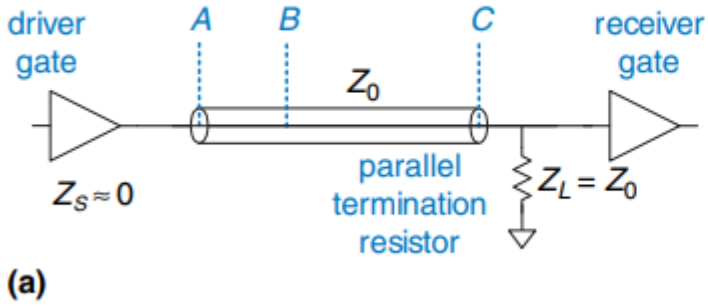
Minimum velocity factors for network cables

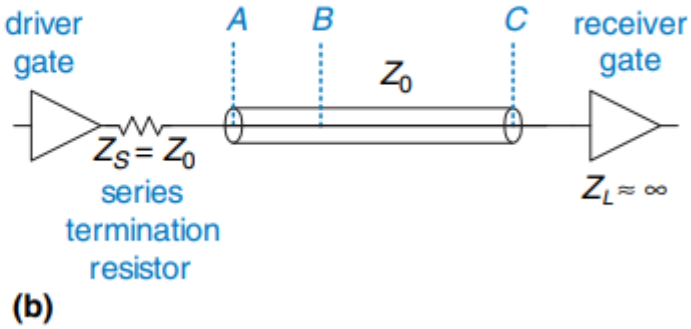
VF (%)	Cable	Ethernet physical layer
74–79	Cat-7 twisted pair	
77	RG-8/U	Minimum for 10BASE5[4]
67	Optical fiber	Minimum for 10BASE-FL,[5] 100BASE-FX, ...
65	RG-58A/U	Minimum for 10BASE2[6]
65	Cat-6A twisted pair	10GBASE-T
64	Cat-5e twisted pair	100BASE-TX, 1000BASE-T
58.5	Cat-3 twisted pair	Minimum for 10BASE-T[7]

- 1 MHz signal with 30ns rise time, 50% velocity factor → reflections will be a problem if conductor length exceed 0.9m

Impedance Matching
Impedansie Aanpassing

- What can you do about it?
- PCB traces laid our to match cable impedance
- Impedance matching with termination resistors
- Either series or parallel termination





- Continuous power dissipation when at high voltage

- No DC power dissipation
- Points near middle of transmission sees voltage of $V_{DD}/2$ until reflection returns -> illegal logical level

Summary
Opsomming

- Calculate R_P based on device characteristics and I2C specification
- Verify signals using an oscilloscope

- Use differential signalling to reduce EMI susceptibility and emissions

- Model conductors as transmission lines if the signalling frequency is high or for long conductors
- Use proper impedance matching and/or termination if needed