

Report for E-design 344

by

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E-Design final report (Assignment # 3)

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Declaration

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A handwritten signature in black ink, appearing to read "D.B. Wait". The signature is fluid and cursive, with a distinct flourish at the end.

Signature:
D.B. Wait

Date:

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Chapter 1

System design

1.1 System overview

This text deals with the design, simulation, and practical implementation of a power-meter. Power from the wall-socket is converted to an 18VAC input to the system which generates positive and negative rails. A load receives power from the transformer. The rails supply the components required to represent the load voltage, current, and phase-shift as an analogue DC voltage. The DC voltages are input to a micro-controller to calculate the inputs to the load. Should the current through the load be larger than 200mA, a switch controller by an SR-latch shall trip the power to the load. A graphical user interface, allows the user to observe the measured input values and to override the trip status if desired.

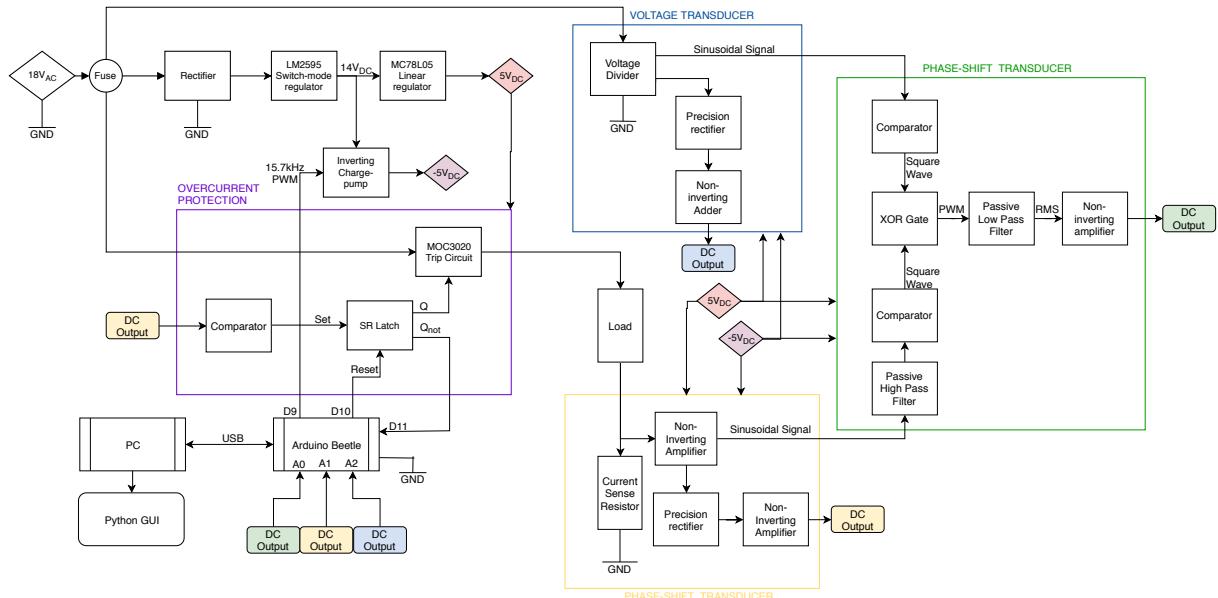


Figure 1.1: System diagram

Chapter 2

Power conversion

The power conversion circuit shown in Figure 2.1 is designed such that an AC signal from the wall-socket is converted to 5 VDC and -5 VDC rails. A transformer steps down the 240 VAC signal to a 18 VAC signal which is half-wave rectified with a small ripple. The rectified signal is input to a switch-mode regulator which produces a 14 VDC signal. This signal is fed to both a 5 VDC linear voltage regulator and an inverting charge-pump circuit.

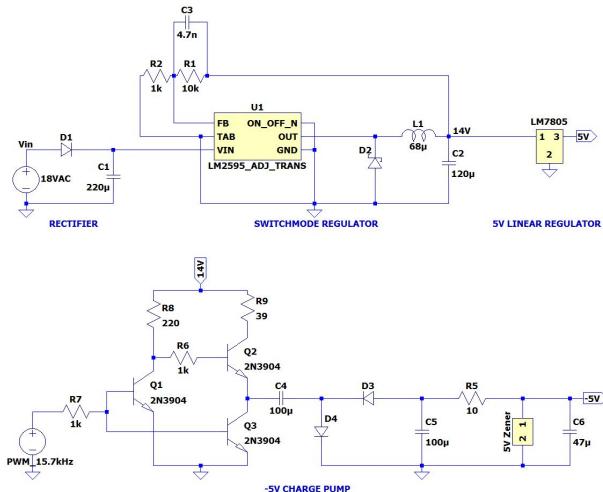


Figure 2.1: Power conversion circuit

2.1 Design

The half-wave rectifier was designed to meet the requirements of the switch-mode regulator. The input voltage to the rectifier is 18 VAC, an 1N4007 diode with a voltage drop of 1.1 VDC [1, p.2] rejects negative voltage. The capacitance was chosen to be $220\ \mu\text{F}$ as recommended [2, p.25]. The following calculation was used to check that, for a load that draws 100 mA, the capacitor is large enough to deliver current:

$$i = C \frac{\Delta V}{\Delta t} \quad (2.1)$$

Assuming a linear ripple voltage from the capacitor, one can solve for the rate of change of voltage with a straight line from the peak voltage to the minimum desired

voltage over the capacitor. The minimum voltage was selected to be 15 V based on the 12 V output condition [2, p.5].

$$\Delta V = (V_{peak} - V_{diode}) - V_{min} = (18\sqrt{2} - 1.1) - 15 = 9.36 \text{ V}$$

$$t_{period} = \frac{1}{f} = \frac{1}{50} = 20 \text{ ms}$$

$$t_{min} = \frac{\arccos \frac{V_{min}}{V_{peak} - V_{diode}}}{2\pi f} = 2.89 \text{ ms}$$

$$\Delta t = t_{period} - t_{min} = 17.10 \text{ ms}$$

$$i = 100 \text{ mA}$$

Solving for the minimum capacitance: $C = \frac{i\Delta t}{\Delta V} = 182.90 \mu\text{F}$ Therefore, 220 μF should meet the requirements - with a smaller ripple. A 50 V rated capacitor was chosen such that the rating be 1.25 times greater than the peak input voltage [2, p.15].

It was decided to use a switch mode regulator as an intermediate to step-down the rectified voltage for two reasons. Firstly, the transformer output regularly exceeds 30 V, which is the maximum input for the linear regulator [3, p.2], whereas the maximum input to the switch-mode regulator is 40 V [2, p.4]. Secondly, the elements in the inverting charge-pump result in a considerable voltage drop - so a larger DC input than 5 V is required to generate the -5 VDC rail. The switch-mode was connected in an adjustable output implementation so that possible design changes could be facilitated [2, p.26].

The Equation 2.2 allows one to select resistors for a desired voltage.

$$V_{out} = V_{ref}(1 + \frac{R_2}{R_1}) \quad (2.2)$$

An output of 13 V is needed to power the inverting charge-pump discussed later, therefore, for $V_{ref} = 1.23 \text{ V}$ and $R_1 = 1 \text{ k}\Omega$, the nearest E-12 resistor value for R_2 is 10 $\text{k}\Omega$. The feed-forward capacitor was chosen according to Equation 2.3 to be 4.7 nF [2, p.26].

$$C_{FF} = \frac{1}{31 \times 10^3 \times R_2} \quad (2.3)$$

The recommended inductor for L_1 is 100 μH [2, p.26]. However, the largest available inductor was 68 μH . The output capacitor was intuitively selected to be 100 μF .

The typical application of the MC78L05 linear regulator has been implemented [3, p.8]. However, the output capacitor of the switch-mode regulator, is sufficient as input to the linear regulator.

The inverting charge-pump's fundamental design was inspired by [4]. In order to increase the output current capability of the design, three NPN transistors are used in a push-pull configuration. By using a common-emitter configuration as a 'NOT gate', the 15.7 kHz pulse-train delivered to each BJT in the Class B amplifier is out of phase. Thus the push-pull behaviour of the amplifier is achieved. In order to keep the RMS current through the transistors below 200 mA [5, p.1], resistors were placed at the collectors of the common-emitter and the first transistor of the push-pull configuration. Due to the voltage drop across the diodes, there needs to be an oscillating 7.2 V output from the amplifier. Finally, a low impedance resistor and a zener diode are used to clamp the inverted voltage to -5 V - similar to the design at [6, p.85].

2.2 Simulation

The 5 V and -5 V outputs power operational amplifiers discussed in Chapter 3 - each op-amp may require 3 mA. To ensure that the project is not constrained by the output current capabilities of the rails, the output of each rail was simulated in LTSpice with a 100Ω load such that each rail should provide 50 mA.

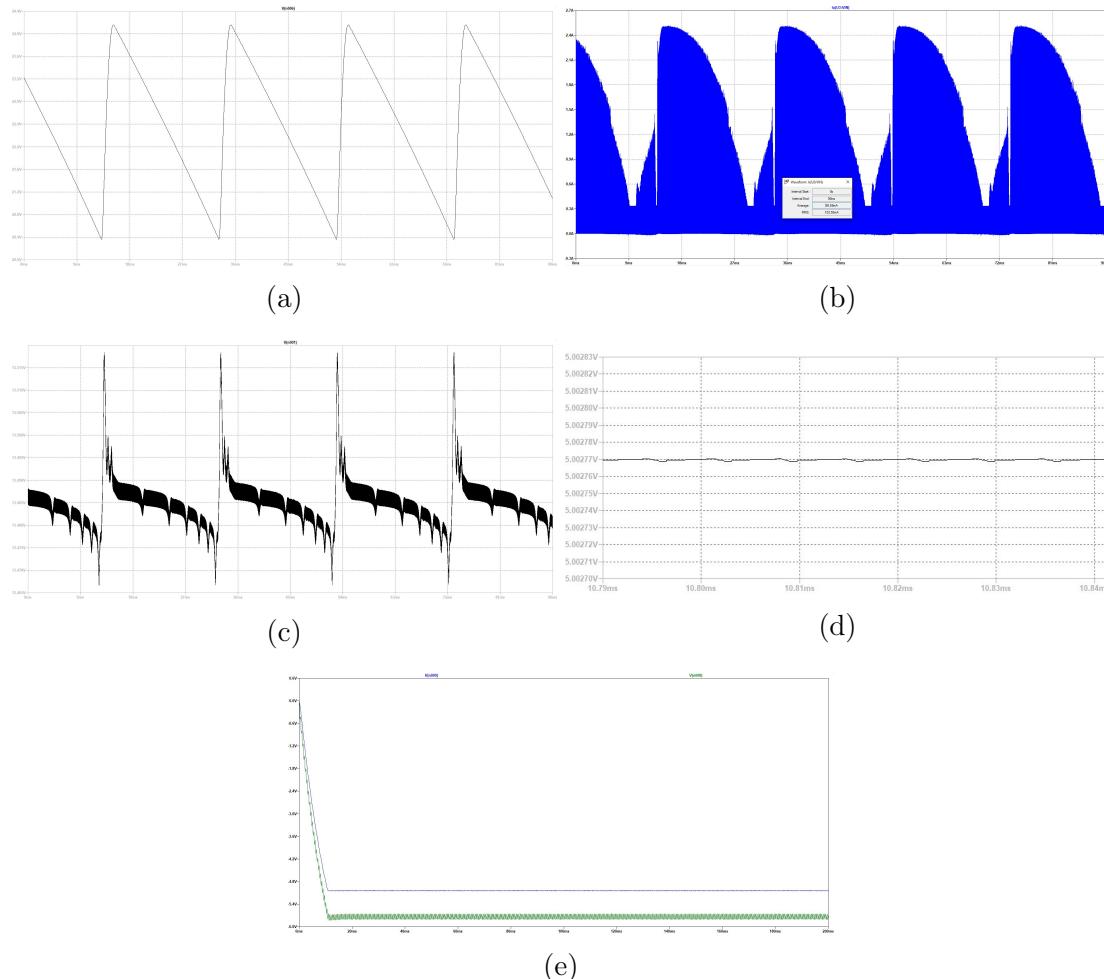


Figure 2.2: Power conditioning given 18 VAC input: (a) Half-wave rectified voltage. (b) Half-wave rectified current. (c) Switch-mode regulator. (d) Linear regulator output. (e) Charge-pump and zener clamp outputs

2.3 Measurements

Figure 2.3 shows the relevant rectifier, switch-mode regulator, linear regulator, and charge-pump outputs with the full design implemented and the mid-range load attached.

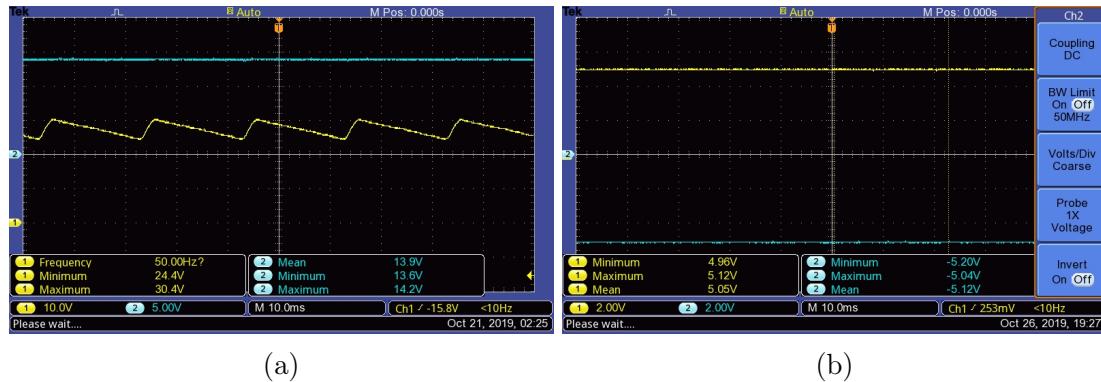


Figure 2.3: Oscilloscope measurements of power conversion: (a) Half-wave rectified voltage and switch-mode regulator output. (b) Positive and negative rails

2.4 Summary and implementation

The system is robust and performs within a 5% tolerance as desired. The input voltage from the transformer is considerably higher than expected, however, there are no adverse consequence owing to that.

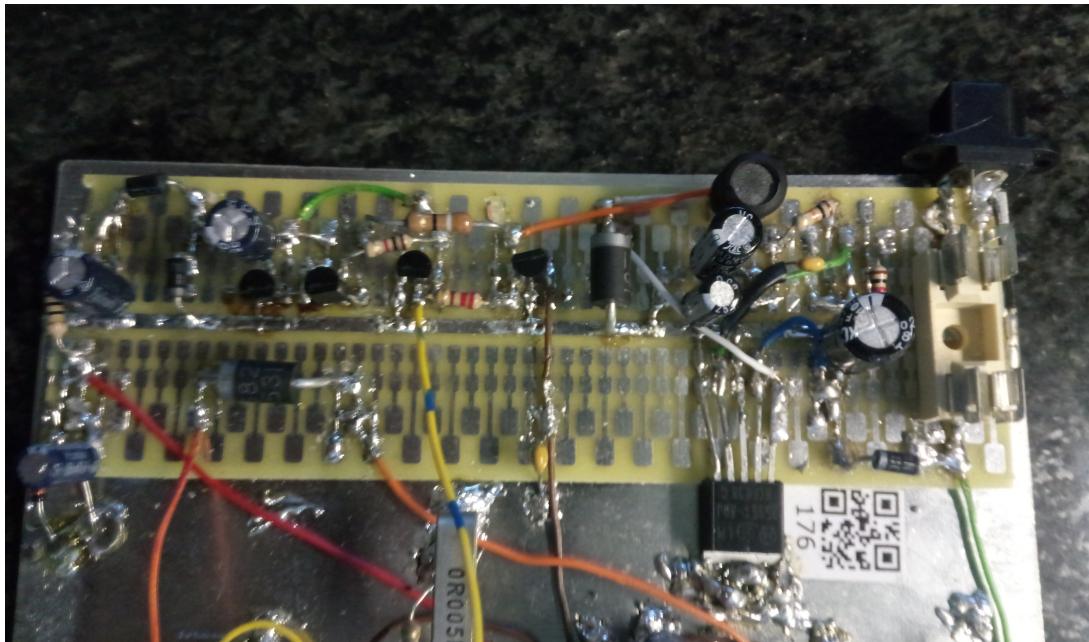


Figure 2.4: Power conversion build

Chapter 3

Signal conditioning

The design parameters were given to measure: an input voltage between 12 VAC to 20 VAC; a current through the load of 0 mA to 285 mA; and an absolute phase-shift of 0° to 45°. Each transducer's output shall be interpreted via a 0 V to 5 V, 10-bit ADC. The transformer voltage regularly exceeds 20 VAC, so the parameters were adjusted for a 23 VAC maximum input.

The 5 V and -5 V rails discussed in Chapter 2 are designed to output at least 50 mA. The system uses 7 TLC2272 op-amps and a TL081 op-amp. The maximum current consumption of the TLC2272 and TL081 is 3 mA and 2.8 mA according to [7, p.8] and [8, p.7]. The expected maximum current consumption is 23.8 mA - therefore the rails should be functional.

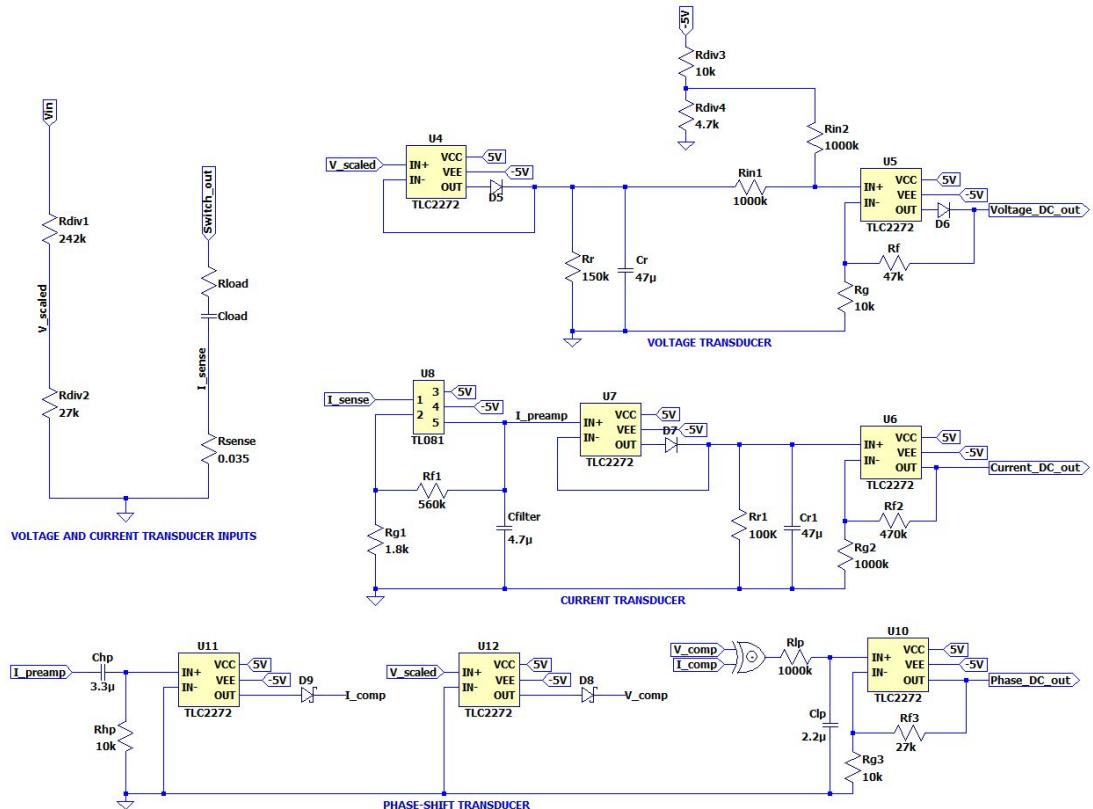


Figure 3.1: Signal conditioning circuit

3.1 Voltage transducer

3.1.1 Design

Firstly, the input AC voltage is divided with high-impedance resistors. This scaled voltage is input to the precision diode. To account for the maximum common-mode voltage of the TLC2272, the scaled voltage may be no more than 3.5 V. The transformer output may be as large as 31 Vpk, hence I chose to scale down the input voltage by a factor of 10 so that the common-mode limit will not be exceeded.

$$\frac{1}{10} = \frac{R_2}{R_1+R_2}$$

Choosing $R_2 = 27\text{k}\Omega$ to ensure a high series impedance, $R_1 = 243\text{k}\Omega$ which can be approximated with a series combination of $220\text{k}\Omega$ and $22\text{k}\Omega$ resistors.

Secondly, the scaled voltage is half-wave rectified. The rectified signal ripple must meet the 150 mV accuracy requirement while preserving the ability to detect a 1 V change at the input within one second.

$$V_L = V_M e^{-t/\tau} \quad (3.1)$$

Using Equation 3.1, the minimum value of τ can be determined such that a 23 VAC drops by 150 mV over a 20 ms period:

$$\tau_{min} = \frac{-0.02}{\ln(\frac{23\sqrt{2}-0.15}{23\sqrt{2}})} = 4.33$$

Similarly, for a minimum voltage of 16 VAC, to detect a 1 V decrease within 1 s, the maximum value of τ can be calculated:

$$\tau_{max} = \frac{-1}{\ln(\frac{16\sqrt{2}-1}{16\sqrt{2}})} = 22.12$$

Therefore, a resistor of $150\text{k}\Omega$ and a capacitor of $47\mu\text{F}$ results in an acceptable $\tau = RC = 7.05$.

Finally, the rectified signal is passed to a non-inverting summing amplifier which scales the voltage such that the original input of 12 VAC to 23 VAC lies within a range of 0 VDC to 5 VDC.

The amplifier takes the rectified signal and a DC offset as the inputs - both input resistances are $1\text{M}\Omega$ for simplicity. The negative rail is used to create an offset at the second input of the amplifier such that 12 VAC translates to 0 V. Thus, the negative rail divided with resistors (R_3 and R_4) to match an input of 12 VAC (divided and rectified to 1.7 V). The gain of the non-inverting adder is designed so that 23 VAC represents at most 4.85 V in compliance with the minimum high-level output voltage of the TLC2272 for low currents [7, p.7]. Therefore, a gain of 5.7 is chosen with $R_f = 47\text{k}\Omega$ and $R_g = 10\text{k}\Omega$

3.1.2 Simulation

Figure 3.2 is the result of the simulation of the voltage transducer. The graphic depicts the scaled voltage, decreasing input voltage, and DC output of the voltage transducer for an 18 VAC input.



Figure 3.2: Voltage Transducer LTSpice results

3.1.3 Measurement

The design was rigorously tested with emulated input voltages in order to determine the accuracy of the deduced input from the analogue output. The deduced input column is calculated from the circuit design to demonstrate the deviation from the expected output.

Emulated Input (Vpk)	Signal Generator Selected (Vpk-pk)	Signal generator Measured (Vpk)	Analogue output (Vdc)	Deduced input (Vpk)	Difference (mV)
16	1.577885693	1.6	-0.19	16.2635983	263.598304
21	2.070974972	2.12	1.25	21.30595278	305.952784
21.15	2.08576765	2.14	1.3	21.48103454	331.0345368
21.3	2.100560329	2.16	1.34	21.6210994	321.0999391
26	2.564064251	2.62	2.68	26.31329091	313.2909135

Figure 3.3: Emulated Voltage Transducer tests

Table 3.3 was used to generate an accurate linear model as shown in Figure 3.4. This model is to be used in the integrated test's calculation.

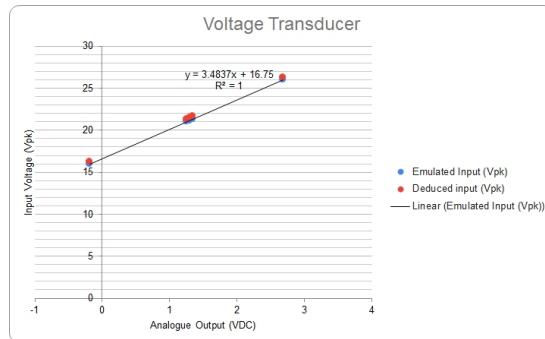


Figure 3.4: Voltage Transducer: Linear function of analogue output vs input voltage

The integrated test in Figure 3.5 verifies that inaccuracies in the output can be compensated for with the above linear equation.

Measurement	Load R	Scaled input (Vpk)	Input (Vpk)	Analogue output (Vdc)	Deduced input (Vpk)	Difference (mV)
No Load	open	3.08	31.23166667	4.17	31.277029	45.36233333
Full Load	100	2.96	30.01484848	3.79	29.953223	-61.62548485
Mid Range	1k	3.06	31.02886364	4.12	31.102844	73.98036364

Figure 3.5: Integrated test of the Voltage Transducer

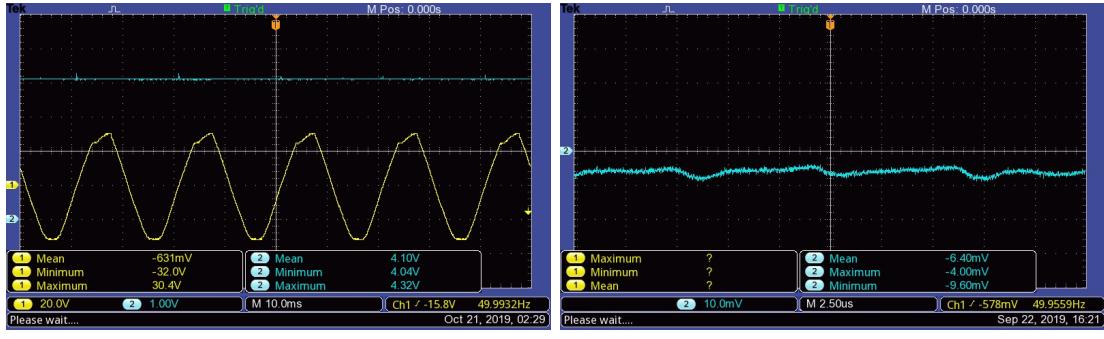


Figure 3.6: Oscilloscope measurement of analogue DC output and AC characteristics of the Voltage Transducer for the Mid-range load

3.2 Current transducer

3.2.1 Design

$30\text{ m}\Omega$ and $5\text{ m}\Omega$ current-sense resistors are connected in series to maximize the small voltage which is pre-amplified. TL081 op-amps have a better Common-Mode Rejection Ratio (CMRR) than that of a TLC2272 [8, p.7] [7, p.7]. Therefore, the TL081 makes for a better small-signal amplifier [9]. For a maximum current of 285 mA ($V_{Rsense} = 9.975\text{ mV}$), the voltage gain is required to comply with the TL081 minimum high-level output voltage of 3.5 V [8, p.9]. A gain of 312 is set by choosing $R_f1 = 560\text{ k}\Omega$ and $R_g1 = 560\text{ k}\Omega$.

The pre-amplified voltage is half-wave rectified. The precision diode ensures negligible voltage drop. The rectified signal ripple must meet the 1 mA accuracy requirement and be able to detect a 10 mA change in current for currents over 100 mA within one second.

The maximum value of τ can be determined such that a 285 mA drops by 1 mA over a 20 ms period:

$$\tau_{min} = \frac{-0.02}{\ln(\frac{285-1}{285})} = 5.69$$

Similarly, for a minimum current of 100 mA , to detect a 10 mA decrease within 1 s , the maximum value of τ can be calculated:

$$\tau_{max} = \frac{-1}{\ln(\frac{100-10}{100})} = 9.49$$

Therefore, a resistor of $270\text{ k}\Omega$ and a capacitor of $22\text{ }\mu\text{F}$ results in an acceptable $\tau = RC = 5.94$.

The rectified signal is post-amplified by a non-inverting amplifier such that 285 mA through the sensing resistor will output closer to the 5 V limit. Hence, for a configuration of $R_f2 = 470\text{ k}\Omega$ and $R_g2 = 1\text{ M}\Omega$, the gain is 1.47 and an input of 285 mA should be converted to 4.58 V .

3.2.2 Simualtion

An LTSpice simulation of the current transducer indicates that it satisfies the specifications. The input voltage is chosen to demonstrate that the chosen RC constant allows a 10 mA change to be detected for currents above 100 mA .

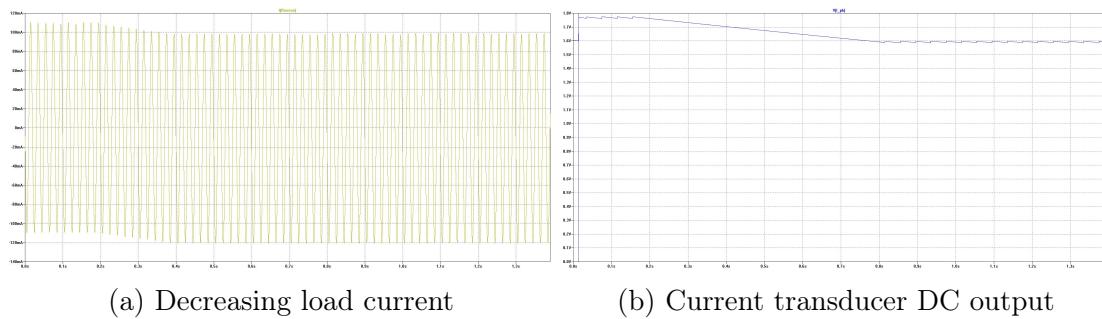


Figure 3.7: Current Transducer LTSpice results

3.2.3 Measurment

As with the voltage transducer, emulated tests were performed to determine the functionality of the design and compensate for inaccuracies. Resistors were used to divide the voltage applied to the system. The selected and measured function generator outputs differed considerably due to noise.

Emulated Input (mApk)	Signal Generator Selected (mVpk)	Signal Generator Selected (mVpk-pk)	Signal generator Measured (V+pk)	Analogue output (Vdc)	Deduced input (mApk)	Difference (mA)
0	0	0	0.264	-0.089	-5.507270835	-5.507270835
50	1.75	3.5	0.009	0.833	51.545579839	51.545579839
100	3.5	7	0.012	1.64	101.48229404	14.8229404
101	3.535	7.07	0.012	1.65	102.101088516	1.01088516
102	3.57	7.14	0.012	1.67	103.3386775	1.338677467
200	7	14	0.0152	3.2	198.0142323	-1.985767727
285	9.975	19.95	0.0184	4.56	282.170281	-2.829719011

Figure 3.8: Emulated Current Transducer tests

Due to the difficulties of emulating the load current, the linear function of the deduced input is more reliable for calculations. The linear function is given in Figure

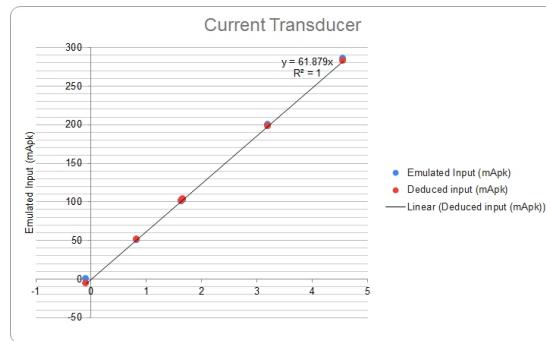
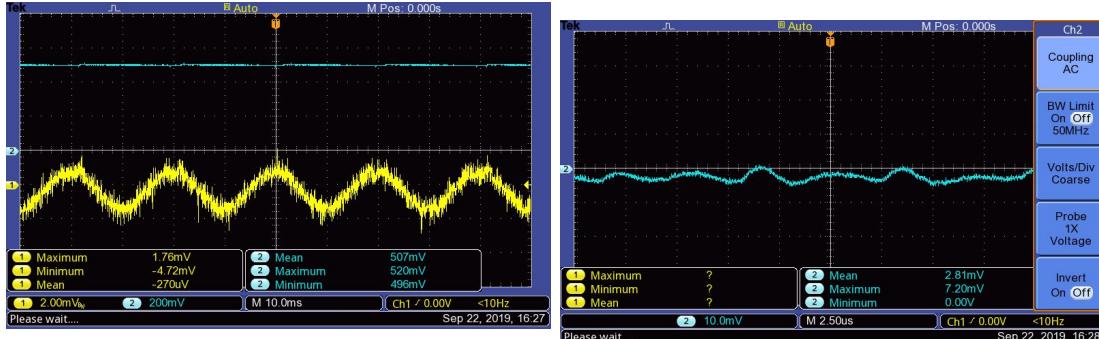


Figure 3.9: Current Transducer: Linear function of analogue output vs. load current

By applying the linear function in Figure 3.9 for the integrated tests, a marginally accurate calculation of the load current is achievable. The voltage drop over the sense resistors is indeterminate so the best I could do to determine the actual current in the system was to divide the measured input voltage by the load impedance.

Measurement	Load R1	Load R2	Measured input (Vpk)	Actual input (mApk)	Analogue output (Vdc)	Deduced input (mApk)	Difference (mA)
No Load	open	-	0.02	0	0.003	0.185637	0.185637
Full Load	100	-	0.011	281.9	4.57	282.78703	0.88703
Mid Range	1k	-	0.0013	31.2	0.506	31.310774	0.110774
Mid + δ	1k	24k	0.0016	32.3	0.519	32.115201	-0.184799
Mid + 2δ	1k	12k	0.0019	33.6	0.555	34.342845	0.742845

Figure 3.10: Integrated test of the Current Transducer



(a) AC coupled current Input and DC output

(b) Current transducer AC output

Figure 3.11: Oscilloscope measurement of analogue DC output and AC characteristics of the Current Transducer for the Mid-range load

3.3 Phase-shift transducer

3.3.1 Design

The transducer converts the voltage and amplified current sinusoidal signals into square waves using a comparator configuration referenced to ground such that it acts as a 'zero-crossing detector'. The TLC2272 op-amp was used for the comparators due to its high maximum common-mode voltage and large minimum high-level output voltage.

Due to intrinsic offsets in the amplified current signal, a high pass filter is used before the current comparator such that the corner frequency is much smaller than 50 Hz. Hence, for $R = 10 \text{ k}\Omega$ and $C = 3.3 \mu\text{F}$: $f_c = 4.8 \text{ Hz}$.

The comparator outputs are passed through an XOR gate to obtain a PWM which represents the phase shift between the voltage and current. due to the fact that XOR gate minimum input voltage is -0.5 V [10, p.4], the negative portion of the comparator outputs is blocked by diodes. Schottky diodes are used for the benefit of a low forward-voltage.

The PWM signal is filtered by the low-pass filter such that the lowest frequency components remain. For $R = 1 \text{ M}\Omega$ and $C = 2.2 \mu\text{F}$: $f_c = 0.07 \text{ Hz}$

For a PWM of 0 V to 5 V, the maximum phase shift of 45° results in a DC value of 1.25 V . For better resolution, a gain of 4 is desired. The DC voltage is amplified by a non-inverting TLC2272 amplifier. Selecting resistors $R_f3 = 27 \text{ k}\Omega$ and $R_g3 = 10 \text{ k}\Omega$, a gain of 3.7 is induced.

3.3.2 Simulation

LTS defense simulations of the designed circuit produce a satisfactory output, albeit noisy. The cause of the noise could not be determined and does not appear in the practical implementation.

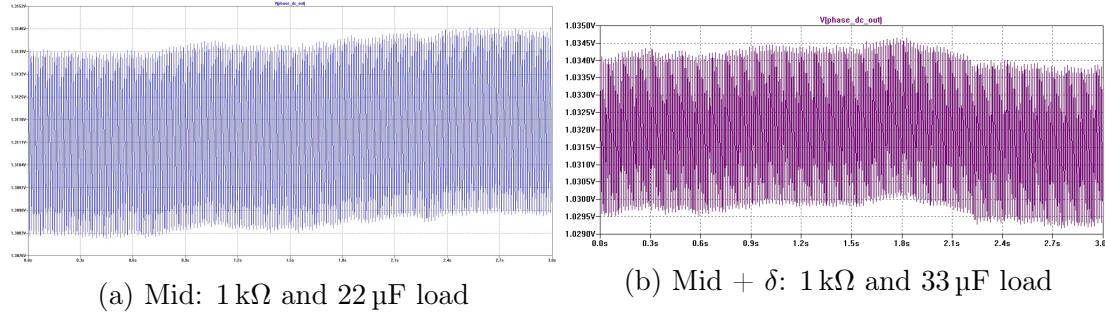


Figure 3.12: Phase Transducer LTS defense results

3.3.3 Measurement

The recommended integrated test was originally used to determine the phase difference. However, within the full system application, the accuracy was not satisfactory. The performance issues may be due to a mildly fluctuating reference voltage on the microcontroller as well as a noticeably lagging input voltage. Rather, adjusting the test to solve for a phase-shift in degrees and recording the reported ADC value, a more reliable and direct linear approximation was made.

Measurement	Load R	Load C	Phase (°)	ADC value	Deduced input (°)	Difference (°)
No Load	1k	-	0	149	-0.03	-0.03
Full Load	1k	3.3	43.96	710	43.728	-0.232
Mid Range	1k	22	8.23	255	8.238	0.008
Mid + δ	1k	33	5.51	218	5.352	-0.158
Mid + 2δ	1k	47	3.87	198	3.792	-0.078

Figure 3.13: Phase Transducer tests

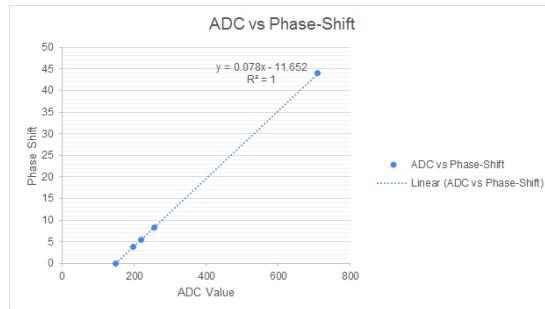


Figure 3.14: Phase Transducer: Linear function of ADC output vs phase-shift

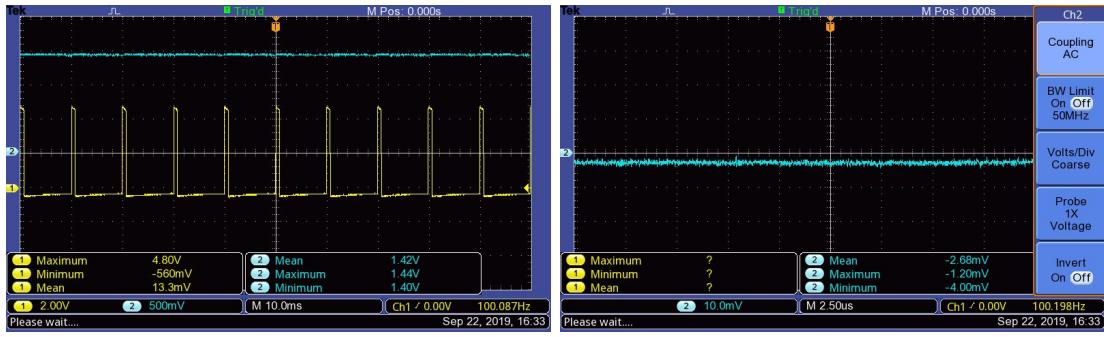


Figure 3.15: Oscilloscope measurement of analogue DC output and AC characteristics of the Phase Transducer for the Mid-range load

3.4 Summary and implementation

The transducers work reasonably well and inaccuracies can be simply adjusted.

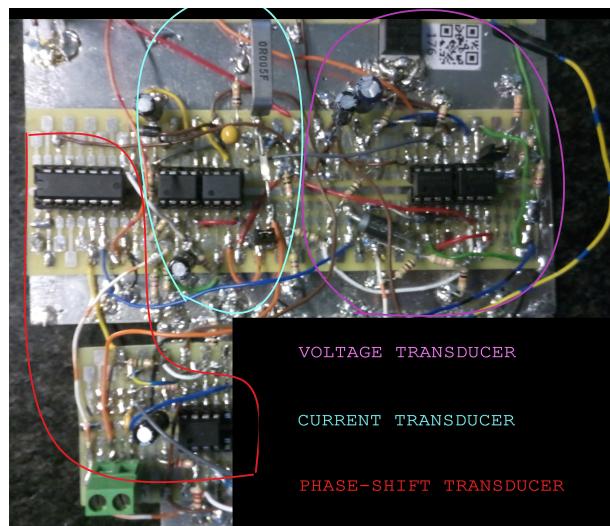


Figure 3.16: Signal conditioning build

Chapter 4

Over-current protection

Should the load current exceed 200 mA, an opto-coupled triac, which is controlled by an SR-latch, shall trip the input to the load. A trip override shall be implemented by using the micro-controller to input a reset condition to the SR-latch.

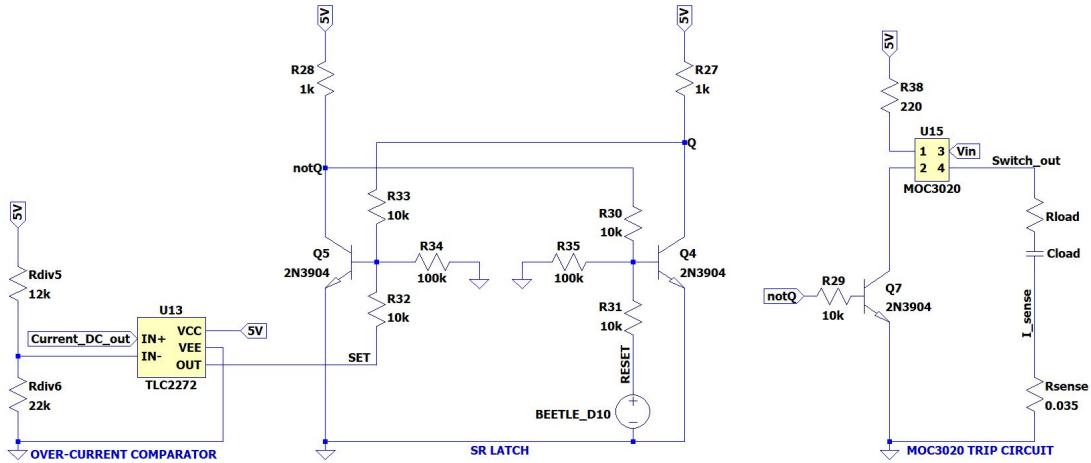


Figure 4.1: Over-current protection circuit

4.1 Design

200 mA translates to 3.23 V output from the current transducer. Therefore, a comparator has been designed that, should the current transducer exceed 3.23 V, a 5 V 'set' condition shall be input to the SR-latch. For the reference voltage, a voltage divider is implemented such that $V_{ref} = 5 \frac{R_{div6}}{R_{div5} + R_{div6}} = 3.23$ V. Therefore, the most ideal combination is $R_{div5} = 1.2\text{ k}\Omega$ and $R_{div6} = 2.2\text{ k}\Omega$.

The SR-latch design was taken from [11]. This latch uses BJTs rather than the traditional NOR gate design. The 'notQ' node is used as the input to the MOC3020 trip circuit.

The latch output current is insufficient to operate the switch, therefore the trip circuit was implemented as suggested by [12, p.2]. The maximum voltage required to turn on the MOC3020 is 1.5 V and the current required for internal LED is 15 mA to 30 mA [12, p.2]. Therefore, for a supply voltage of 5 V the requisite collector resistor is calculated to be 220 Ω . With this design, the voltage is supplied to the load when 'notQ' is high, and the supply is tripped when 'notQ' is low.

To protect the circuit from the transients associated with switching, a P6KE43CA transient voltage suppression diode is connected from the input voltage to ground.

4.2 Simulation

For all combinations of 'set' and 'reset' conditions, the SR-latch and trip perform as required.

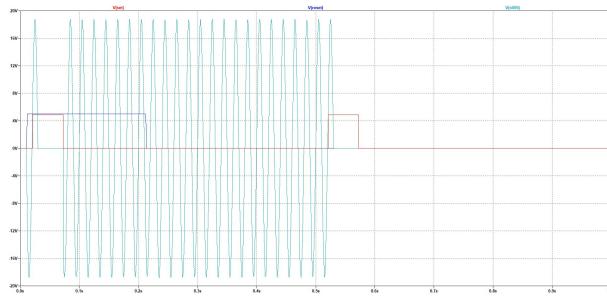
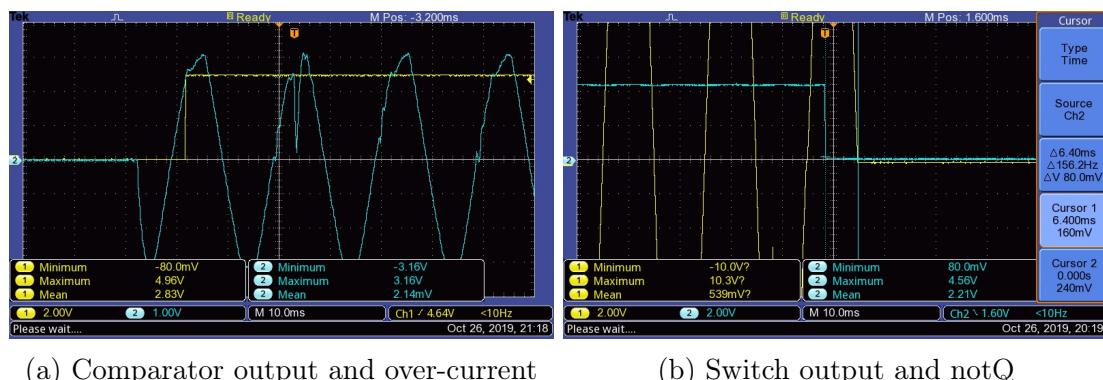


Figure 4.2: Integrated test of the current transducer

4.3 Measurements

The following measurements were used to test the response of the system. The first image shows the comparator response and the preamplified current. The 'set' signal would be triggered as soon as the current exceeds the limit. Please note that, for this test, the load is connected directly to the input. The second image shows the response of the switch to a change in 'notQ'. The input completes half a cycle before being tripped.



(a) Comparator output and over-current

(b) Switch output and notQ

Figure 4.3: Oscilloscope measurements of over-current response

Chapter 5

Reporting

The GUI was implemented with Python. The Python classes in 'gui.py' make use of 'connection.py' to connect to and communicate with the Arduino microcontroller. Figure 5.1 represents the operation of the software as a flow diagram.

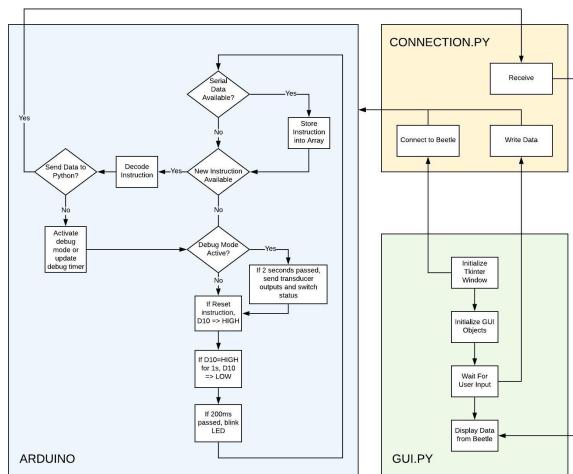


Figure 5.1: GUI Flow Diagram

5.1 Design

The transducers' outputs are connected to the analogue pins of the Arduino Beetle. Each analog pin of the Beetle is protected from over-voltage and under-voltage by two rectifying diodes which are connected from the pin to ground and the 5 V supply respectively.

The 'Reset Latch' button outputs a reset condition to the latch (via D10 on the beetle) which will override the tripped switch.

The 'Q' output, is the logical inverse of 'notQ' for all valid inputs to the latch. Therefore, D11 is configured as an input pin which reads the logical state of 'Q' to determine the trip status.

When the device is running in Debug-mode, the transducer outputs are read by the ADC and converted to the equivalent voltage, current, and phase inputs.

5.2 Results

The GUI output for the following sequence of events is shown in Figure 5.2

- $1\text{ k}\Omega$ and $3.3\text{ }\mu\text{F}$ load: normal operation
- $100\text{ }\Omega$ load: over-current and trip
- $1\text{ k}\Omega$ load: switch remains tripped
- Reset Latch: normal operation resumes

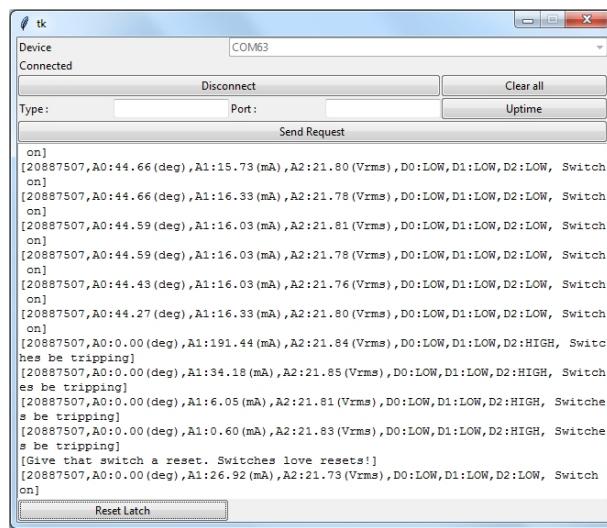


Figure 5.2: GUI output for changing loads

Chapter 6

System and conclusion

6.1 System

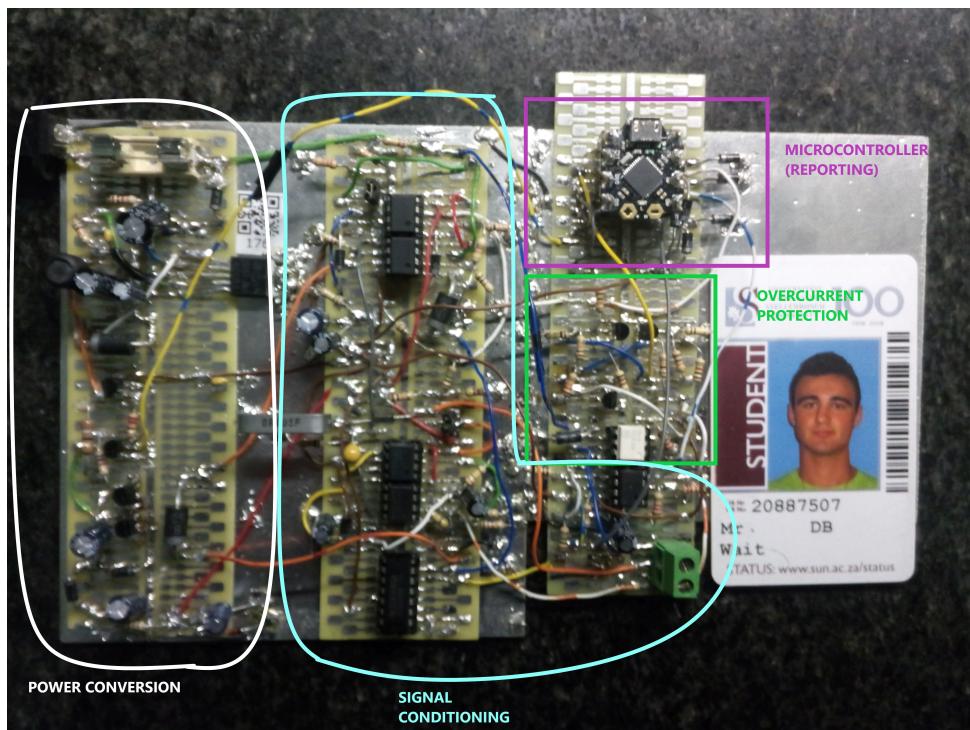


Figure 6.1: Complete PCB

6.2 Lessons learned

Some lessons which have either been reinforced or that I was ignorant of have been worth the uphill climb that was this semester

- It is best practice for filtering/bypass capacitors to be soldered close to IC pins in ascending order of capacitance.
- Rather build a circuit with ample space than a compact circuit which is difficult to debug.
- A fresh pair of eyes is commonly needed when debugging.

- Try explain the problem you're having to yourself before you seek help.
- Common-ground is very important.
- Never leave metal clippings on your desk.
- Switch off all power before moving probes to take another measurement.
- It's best to neglect redundant capacitors and other elements in SPICE so that the simulation finishes before the semester.
- Noise is a natural phenomenon and can be controlled - however - noise is kind of magic and one can only do so much...
- Capacitors are cheaper than fire-crackers and just as effective.

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Appendix A: GitHub Activity Heatmap

