**Lab 1 Report – UART**

**By Ryan Zaugg and Tom Prouty**

**Introduction**

The goal of the lab was to design a UART on our FPGA board that would convert lowercase letters input to it to uppercase letters, and vis versa. If a non-alphabetical symbol was inputted the UART will output an ‘E’ to symbolize the occurrence of an error. The UART should operate with 8 data-bits, 1 stop bit, 0 parity bits, no flow control, and use a 19,200 baud rate.

**Procedure**

**Results**

**Conclusion**