1. **Understand the VHDL code for D flip flop and observe the RTL netlist**

```
----------VHDL code for D flip flop -----------------
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

--ENTITY DECLARATION--
entity Dff_async_reset is
port(d,clk,rst:in std_logic;
                q:out std_logic
          );
end Dff_async_reset;
-------------------------------------------------


architecture Behavioral of Dff_async_reset is
begin
process(rst,clk)
begin
--SEQUENTIAL DECLARATION--
if(rst='1') then
--IF RESET IS 1 THEN SET OUTPUT TO 0
 q<='0';
elsif(clk'event and clk='1') then
--IF THERE IS CHANGE IN CLK AND CLK IS HIGH
--SET OUTPUT AS INPUT
 q<=d;
end if;
end process;

end Behavioral;
-------------------------------------------------------------
```

2. Design the universal shift resistor based on the given input description

S1	**S0**	**Operation**
0	0	Parallel loading
0	1	Left Shift
1	0	Right Shift
1	1	No Change

3. Write a VHDL program that synthesizes the above design and emulates the CPLD board as a 3-bit universal shift register. (Hint: Write VHDL code for D flip flop and MUX in behavioral modeling styles and top level design i.e shift register in structural modeling style)