Week 5: CSE BATCH

1. Design and implement a half subtractor circuit using a minimum number of 2 input NAND gates.

2. Familiarize 74LS83 IC and implement a controlled 3-bit adder/subtractor circuit which is controlled by signal CTRL using 74LS83 and minimum number of 2-input gates.

CTRL	OPERATION
0	Addition
1	Subtraction (either 1’s or 2’s complement)