UNIT-6
I/O Interface & Bus architecture

Bus interconnection
Bus structure
Basic parameters of Bus design
Peripheral component interconnect Bus
SCSI
USB

BUS INTERCONNECTION

- A bus is a communication pathway connecting two or more devices.
- A key characteristic of a bus is that it is a shared transmission medium.
- Multiple devices connect to the bus, and a signal transmitted by any one device is available for reception by all other devices attached to the bus (broadcast).
- Typically, a bus consists of multiple communication pathways, or lines. Each line is capable of transmitting signals representing binary 1 and binary 0.
- Taken together, several lines of a bus can be used to transmit binary digits simultaneously (in parallel). For example, an 8-bil unit of data can be transmitted over eight bus lines.
- Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy.
- A bus that connects major computer components (processor, memory, I/O) is called a **system bus**. The most common computer interconnection structures are based on the use of one or more system buses.

BUS STRUCTURE

A system bus consists, typically, of from about 50 to hundreds of separate lines. Each line is assigned a particular meaning or function. Although there are many different bus designs, on any bus the lines can be classified into three functional groups data, address, and control lines. In addition, there may he power distribution lines that supply power to the attached modules.

Data Bus

- Provide a path for moving, data between system modules. These lines, collectively, are called the data bus.

- The width of the data bus: The data bus may consist of from 32 to hundreds of separate lines, the number of lines being referred to as the width of the data bus. Because each line can carry only 1 bit at a time, the number of lines determines how many bits can be transferred at a lime. The width of the data bus is a key factor in determining overall system performance. For example, if the data bus is 8 bits wide and each instruction is 16 bits long, then the processor must access the memory module twice during each instruction cycle.

- As data bus carry information from and to the modules, so it is bidirectional in nature.

Address Bus

- Address lines are used to designate the source or destination of the data on the data bus. For example, if the processor wishes to read a word (8, 16. or 32 bits) of data from memory, it puts the address of the desired word on the address lines.

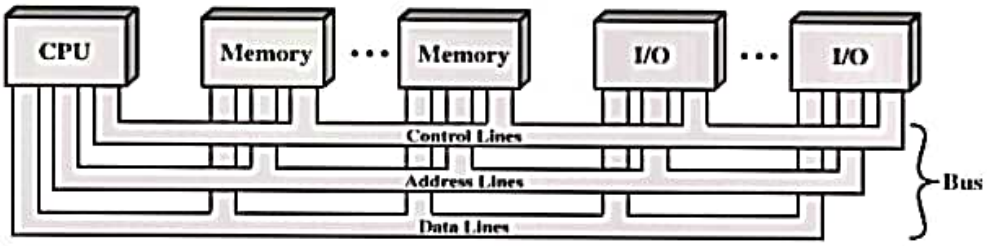
- The width of the address bus: determines the maximum possible memory capacity of the system. Furthermore, the address lines are generally also used to address I/O ports.

Control Bus

Control bus are used to control the access to and the use of the data and address lines. Because the data and address lines are shared by all components, there must be a means of controlling their use. Control signals transmit both command and timing information between system modules.

Typical control lines include the following:

- Memory write: Causes data on the bus to be written into the addressed location.
- Memory read: Causes data from the addressed location to be placed on the bus.
- I/O write: Causes data on the bus to be output to the addressed I/O port.
- I/O read: Causes data from the addressed I/O port to be placed on the bus.
- Transfer ACK: Indicates that data have been accepted from or placed on the bus.
- Bus request: Indicates that a module needs to gain control of the bus.
- Bus grant: Indicates that a requesting module has been granted control of the bus.
- Interrupt request: Indicates that an interrupt is pending.
- Interrupt ACK: Acknowledges that the pending interrupt has been recognized.
- Clock: Used to synchronize operations.
- Reset: Initializes all modules.



MULTIPLE-BUS ARCHITECTURE

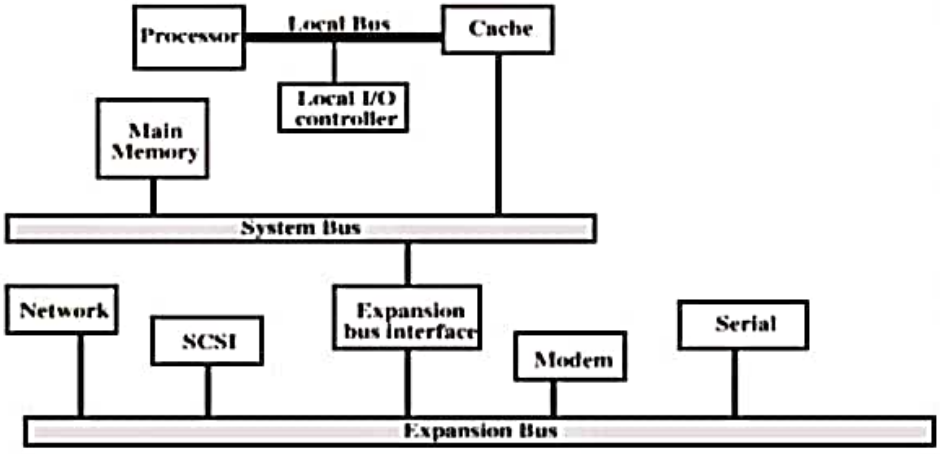
If a great number of devices are connected to the bus, performance will suffer. There are two main causes:

1. Propagation delay - the time it takes for devices to coordinate the use of the bus
2. The bus may become a bottleneck as the aggregate data transfer demand approaches the capacity of the bus (in available transfer cycles/second).

- Accordingly, most computer systems use multiple buses, generally laid out in a hierarchy.
- There are mainly two typical architecture like- 1)Traditonal Bus architecture 2)High performance Bus architecture\

Traditonal Bus architecture

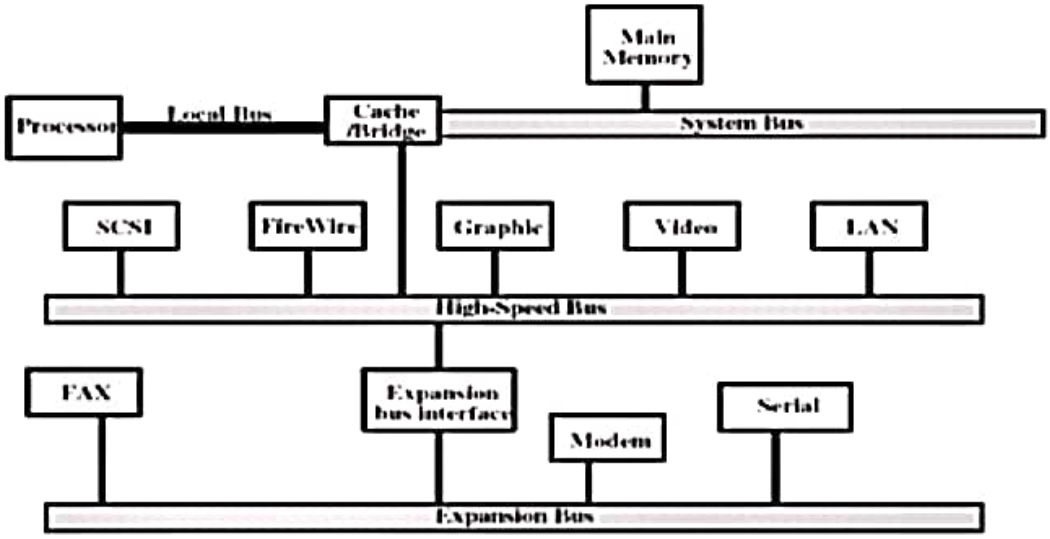
- This consists of three buses,like local bus,system bus and expansion bus
- There is a local bus that connects the processor to a cache memory and that may support one or more local devices.
- The cache memory controller connects the cache not only to this local bus, but to a system bus to which are attached all of the main memory modules.
- It is possible to connected I/O controllers directly onto the system bus. A more efficient solution is to make use of one or more expansion buses for this purpose.
- An expansion bus interface buffers data transfers between the system bus and the I/O controllers on the expansion bus.
- This arrangement allows the system to support a wide variety of I/O devices and at the same time insulate memory-to-processor traffic from I/O traffic.



High performance Bus architecture

- Due to the increasing need for adding more i/o devices the traditional architecture cannot support so, it is necessary to build a high performance bus.
- Similar to the traditional bus architecture, this too contains a local bus that connects the processor to a cache controller, which in turn is connected to the main memory through the system bus.
- The cache controller is integrated into a bridge or buffering device that connects to the high speed bus, which sometimes referred to as Mezzanine Architecture.
- This bus supports to high speed LANs, video and graphics work station controllers etc.
- The lower speed devices are still supported by the expansion bus with an interface buffering traffic between the expansion bus and high speed bus.

- This way the high speed devices are more closely integrated with the processor through the high speed bus and at the same time leaving processor independent.



BASIC PARAMETERS OF BUS DESIGN

Before designing a bus some of the following basic parameter are to be considered

1. Bus type
2. Width of the bus
3. Method of arbitration
4. Timing
5. Data transfer

Bus type

- Bus lines can be separated into two generic types: dedicated and multiplexed.
- A **dedicated bus** line is permanently assigned either to one function or to physical subset of computer components.
- Separate data & address lines are used.
- The use of the same lines for multiple purposes is known as **Multiplexing.** Shared lines
- Address valid or data valid control lines are used.

Width of the bus

- The width of the data bus has an impact on the system performance
- The wider the data bus, the greater the number of bits can be transferred at one time.
- The width of the address bus has an impact on the system capacity.
- The wider the address bus, the greater the range of locations that can be referenced.

Method of arbitration

It determining who can use the bus at a particular time

- ***Centralized*** - a single hardware device called the bus controller or arbiter allocates time on the bus

- ***Distributed*** - each module contains access control logic and the modules act together to share the bus
- Both methods designate one device (either CPU or an I/O module) as master, which may initiate a data transfer with some other device, which acts as a slave.

Timing

Synchronous Timing

- Bus includes a clock line upon which a clock transmits a regular sequence of alternating 1's and 0's of equal duration
- A single 1-0 transmission is referred to as a clock cycle or bus cycle
- All other devices on the bus can read the clock line, and all events start at the beginning of a clock cycle

Asynchronous Timing

- The occurrence of one event on a bus follows and depends on the occurrence of a previous event

Data transfer

A bus can support various type of data transfer such as-

- Read, Write, Read-modify-write, Read-after-write, Block
- All buses must support write (master to slave) and read (slave to master) transfers.
- ***Read-modify-write***: A read followed immediately by a write to the same address.
- Address is only broadcast once, at the beginning of the operation
- ***Read-after-write***: Indivisible operation consisting of a write followed immediately by a read from the same address (for error checking purposes) .
- ***Block:*** one address cycle followed by n data cycles
- first data item to or from specified address
- Remaining data items to or from subsequent addresses.

SCSI

The Small Computer System Interface (SCSI) is a set of parallel interface standards developed by the American National Standards Institute (ANSI) for attaching printers, disk drives, scanners and other peripherals to computers. SCSI (pronounced "skuzzy") is supported by all major operating systems.

It has some versions developed –

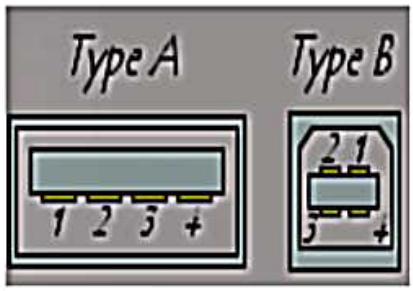
SCSI-1 is the original SCSI standard developed back in 1986 as ANSI X3.131-1986.

SCSI-1 is capable of transferring up to eight bits a second.

SCSI-2 was approved in 1990, added new features such as Fast and Wide SCSI, and support for additional devices.

SCSI-3 was approved in 1996 as ANSI X3.270-1996.

USB (Universal Serial Bus):



- Universal Serial Bus is a new connector that is introduced 1995 to replace Serial and Parallel ports.
- It is based on serial type architecture. However, it is much quicker than standard serial ports because Serial architecture gives the interface a much higher clock rate than a parallel interface and serial cables are much cheaper than parallel cables.
- So, from 1995, the USB standard has been developed for connecting a wide range of devices like scanners, keyboards, mice, joysticks, printers, modems and some CD-ROMs.
- USB is completely hot-swappable that means we can connect or disconnect any device when the computer is running.

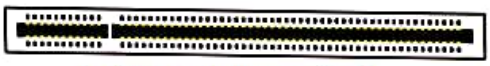
- Computer can recognize the device as soon as it plugged in, and the user can use of the device immediately.
- There are two types of USB connectors:

  Type A: This type of connectors is generally used for less bandwidth intensive devices like keyboard, mouse, webcam, etc. and shape is rectangular.

  Type B: This type of connectors is generally used for high speed devices like external hard disks, etc. and shape is square.

PCI :

- Stands for "Peripheral Component Interconnect." It is a hardware bus designed by Intel around 1992 and is used in both PCs and Macs.
- It is an intermediate bus located between the processor bus (Northbridge) and the I/O bus (Southbridge).
- Most add-on cards such as SCSI, Firewire, and USB controllers use a PCI connection. Some graphics cards use PCI, but most new graphics cards connect to the AGP slot.
- PCI slots are found in the back of the computer. The PCI interface exists in 32 bits with a 124-pin connector or in 64 bits with a 188-pin connector.
- There are also two signaling voltage levels i.e. 3.3V for laptop computers and 5V for desktop computers. The 64-bit PCI connectors offer additional pins and can accommodate 32-bit PCI cards.
- There are 2 types of 64-bit connectors. They are 64-bit PCI connector, 5V and 64-bit PCI connector, 3.3V.



32-bit PCI connector 3.3V

32-bit PCI connector 5V

64-bit PCI connector, 3.3V